5A, 30V, 500kHz Asynchronous Step-Down Converter

General Description

The RT6285 is a step-down regulator with an internal power MOSFET. It achieves 5A of continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization.

For protection, the RT6285 provides cycle-by-cycle current limiting and thermal shutdown protection. The soft-start reduces the stress on the input source at startup. In shutdown mode, the regulator draws only 25μA of supply current.

The RT6285 requires a minimum number of readily available external components, providing a compact solution. The RT6285 is available in the SOP-8 (Exposed Pad) package.

Ordering Information

RT6285 □□

- Package Type
  SP : SOP-8 (Exposed Pad-Option 1)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

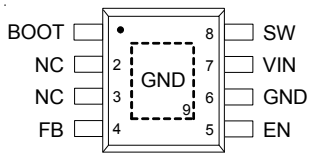
- **5A Output Current**
- **Internal Soft-Start**
- **110mΩ Internal Power MOSFET Switch**
- **Internal Compensation Minimizes External Parts Count**
- **High Efficiency up to 90%**
- **25μA Shutdown Mode**
- **Fixed 500kHz Frequency**
- **Thermal Shutdown**
- **Cycle-by-Cycle Over Current Protection**
- **Wide 5.5V to 30V Operating Input Range**
- **Adjustable Output Voltage from 1.222V to 24V**
- **Available In an SOP8 (Exposed Pad) Package**
- **Integrated Boot Recharge FET**
- **RoHS Compliant and Halogen Free**

Applications

- Distributive Power Systems
- Battery Charger
- DSL Modems
- Pre-regulator for Linear Regulators

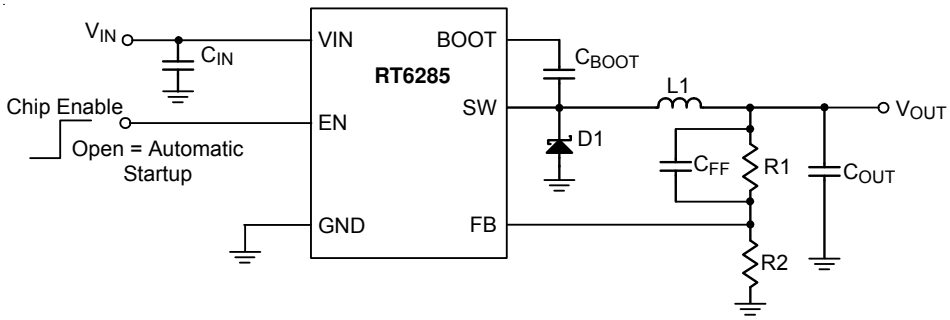
Pin Configuration

(TOP VIEW)

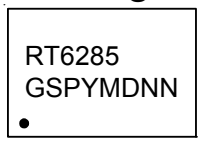


SOP-8 (Exposed Pad)

Simplified Application Circuit



Marking Information



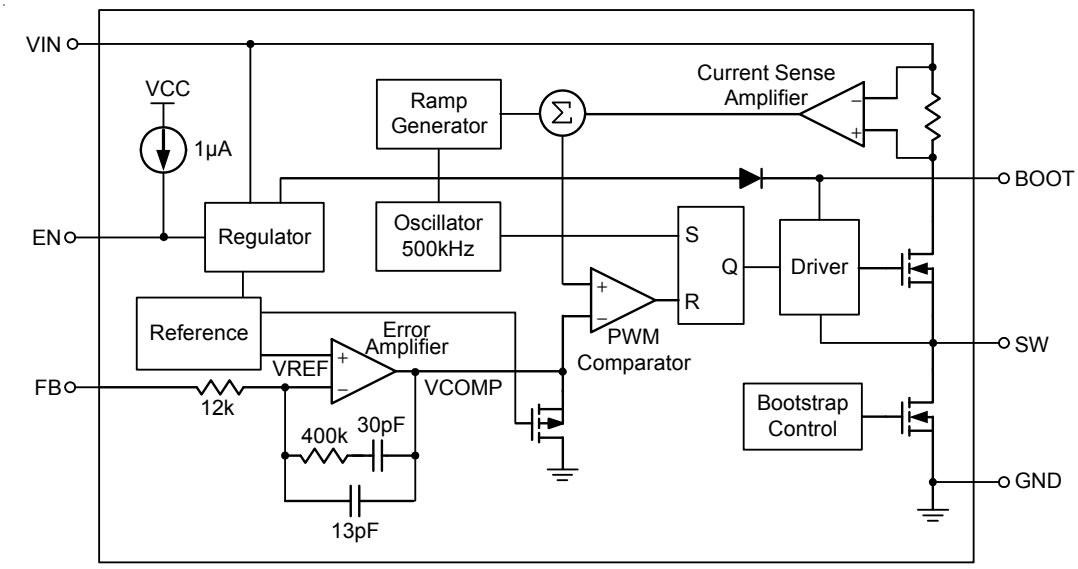
RT6285GSP : Product Number

YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	High side gate drive boost Input. BOOT supplies the drive for the high side N-MOSFET switch. Connect a 10nF or greater capacitor from SW to BOOT to power the high side switch.
2, 3	NC	No internal connection.
4	FB	Feedback input. The feedback threshold is 1.222V.
5	EN	Enable input. EN is a digital input that turns the regulator on or off. Drive EN higher than 1.4V to turn on the regulator, lower than 0.4V to turn it off. For automatic startup, leave EN unconnected.
6, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	VIN	Power input. A suitable large capacitor should be bypassed from VIN to GND to eliminate noise on the input to the IC.
8	SW	Power switching output. Note that a capacitor is required from SW to BOOT to power the high side switch.

Functional Block Diagram



Operation

Control Loop

The RT6285 is a high efficiency asynchronous step-down converter utilizes the peak current mode control. An internal oscillator initiates the turn-on of the high-side MOSFET. At the beginning of each clock cycle, the internal high-side MOSFET turns on, allowing current to ramp-up in the inductor. The inductor current is internally monitored during each switching cycle. The output voltage is sensed on the FB pin via the resistor divider, R1 and R2, and compared with the internal reference voltage (VREF) to generate a compensation signal (VCOMP) at the output of Error Amplifier. A control signal derived from the inductor current is compared to VCOMP. When the inductor current reaches its threshold, the high-side MOSFET is turned off and inductor current ramps down. While the high-side MOSFET is off, the inductor current is supplied through the external low-side diode, freewheel diode, connected between the SW pin and GND. This cycle repeats at the next clock cycle. In this way, duty-cycle and output voltage are controlled by regulating inductor current.

Enable Control

The RT6285 provides an EN pin, as an external chip enable control, to enable or disable the device. If VEN is held below the enable threshold voltage, switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold (VUVLOH). If VEN is held below 0.4V, the converter will enter into shutdown mode, that is, the converter is disabled. If the EN voltage rises above the enable threshold voltage while the VIN voltage is higher than VUVLOH, the device will be turned on, that is, switching being enabled and soft-start sequence being initiated. The EN pin has an internal pull-up current source IEN (1μA, typically) that enables operation of the RT6285 when the EN pin floats. The EN pin can be used to adjust the under-voltage lockout (UVLO) threshold and hysteresis by using two external resistors.

Input Under-Voltage Lockout

In addition to the EN pin, the RT6285 also provides enable control through the VIN pin. If VEN rises above VIH first, the switching will be inhibited until the VIN voltage rises above the UVLO rising threshold (VUVLOH). It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal high-side MOSFET can be prevented. After the device is powered up, if the input voltage VIN goes below the UVLO falling threshold(VUVLOH-VUVLO_HYS), this switching will be inhibited; if VIN rises above VUVLOH, the device will resume switching.

High-Side MOSFET Peak Current Limit Protection

The RT6285 includes a cycle-by-cycle high-side MOSFET peak current-limit protection against the condition that the inductor current increasing abnormally, even over the inductor saturation current rating. The inductor current through the high-side MOSFET will be measured after a certain amount of delay when the high-side MOSFET being turned on. If an over-current condition occurs, the converter will immediately turn off the high-side MOSFET to prevent the inductor current exceeding the high-side MOSFET peak current limit (I_{LIM}).

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{IN} ---------- –0.3V to 40V
- Switching Voltage, SW ---------- –1V to V_{IN} + 0.3V
- BOOT Voltage ---------- (V_{SW} – 0.3V) to (V_{SW} + 6V)
- The Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 1.333W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{IN} ---------- 5.5V to 30V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage		V_{REF}	5.5V ≤ V_{IN} ≤ 30V	1.202	1.222	1.239	V
High Side Switch-On Resistance		$R_{DS(ON)1}$		--	110	160	mΩ
Bootstrap Switch Ron		$R_{DS(ON)2}$		--	10	15	Ω
High Side Switch Leakage			V_{EN} = 0V, V_{SW} = 0V	--	--	10	μA
Current Limit		I_{LIM}	Duty = 90%, $V_{BOOT-SW}$ = 4.8V	6	7.5	9	A
Oscillator Frequency		f_{OSC}		425	500	575	kHz
Short Circuit Frequency			V_{FB} = 0V	--	150	--	kHz
Maximum Duty Cycle		D_{MAX}	V_{FB} = 0.8V	85	90	95	%
Minimum On-Time		t_{ON}		--	100	150	ns
Under Voltage Lockout Threshold Rising		V_{UVLOH}		3.8	4.2	4.5	V
Under Voltage Lockout Threshold Hysteresis		V_{UVLO_HYS}		--	315	--	mV
EN Threshold Voltage	Logic-High	V_{IH}	EN_hys = 350mV	1.4	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
Enable Pull Up Current				--	1	--	μA
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	25	45	μA
Quiescent Current		I_Q	V_{EN} = 2V, V_{FB} = 1.5V	--	0.6	1	mA
Soft-Start Period			C_{SS} = 0.1μF	3	5	8.2	ms
Thermal Shutdown		T_{SD}		--	150	--	°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

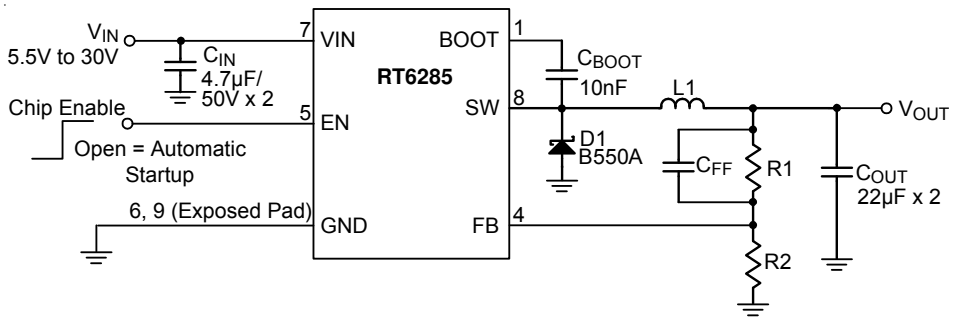


Table 1. Recommended Component Selection

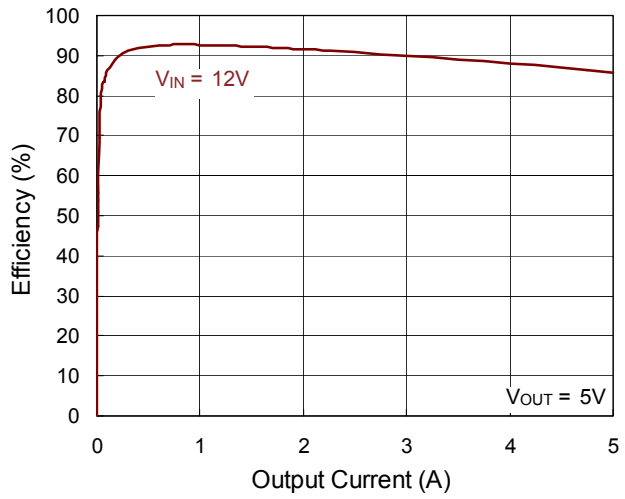
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{FF} (pF)	L (µH)	C_{OUT} (µF)
2.5	100	100	82	6.8	22 x 2
3.3	100	58.6	82	10	22 x 2
5	100	31.6	82	15	22 x 2
8	100	18	82	22	22 x 2

Note : R1 and CFF should be fixed (100kΩ and 82pF) to keep the optimized compensation point.

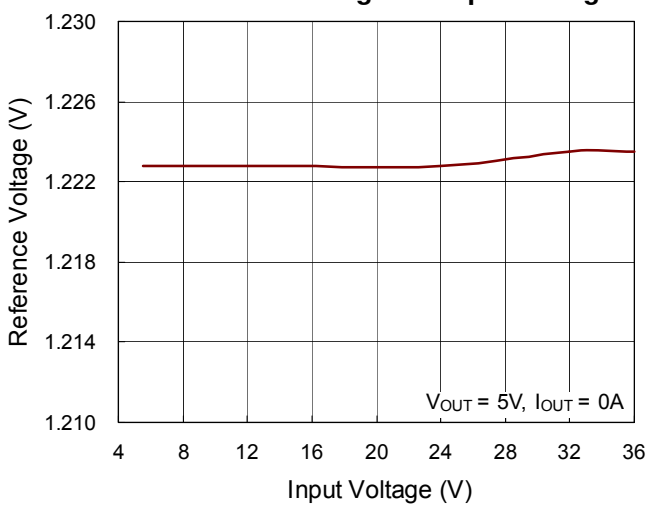
Considering the capacitance de-rating which is related to biased voltage level and size, the effective capacitance of C_{OUT} should meet 20µF

Typical Operating Characteristics

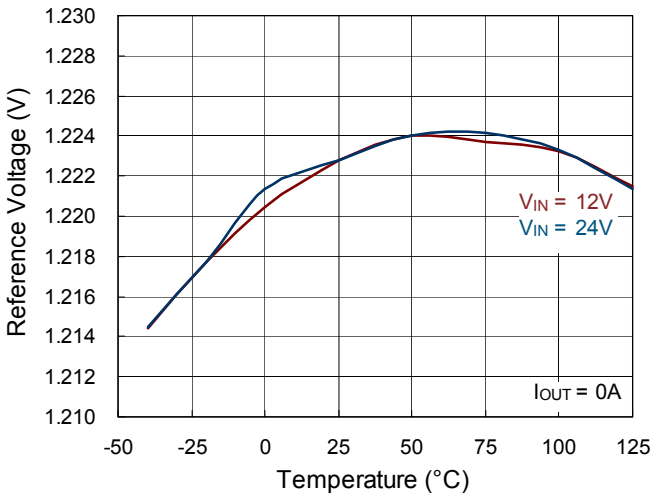
Efficiency vs. Output Current



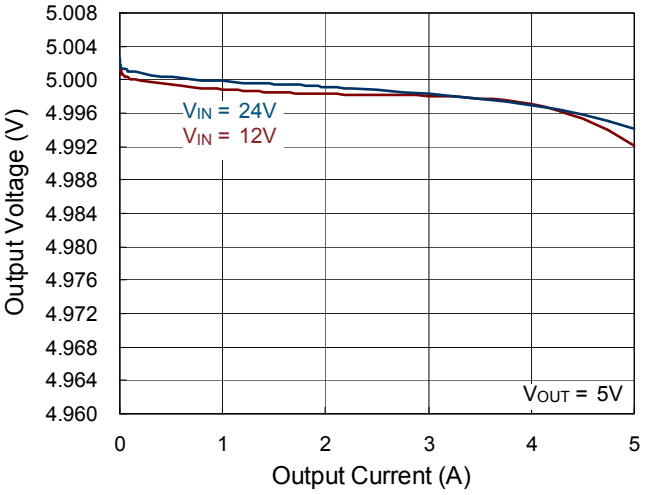
Reference Voltage vs. Input Voltage



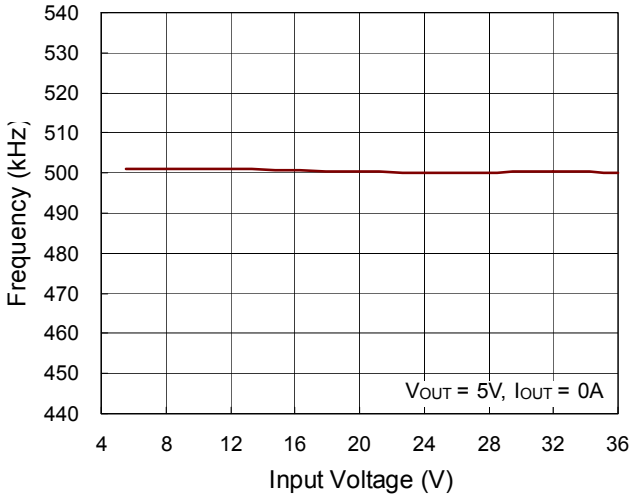
Reference Voltage vs. Temperature



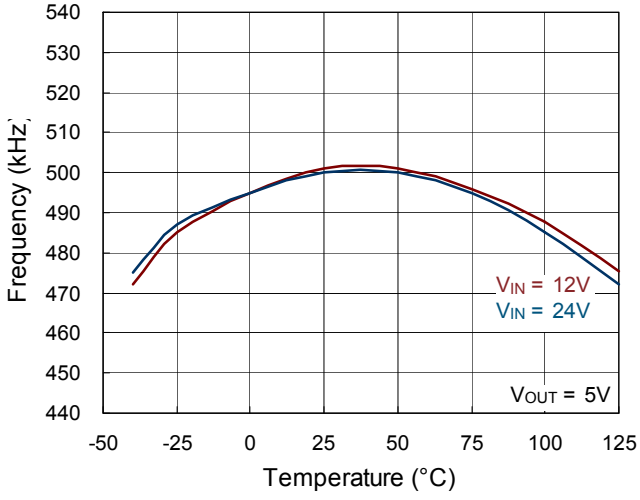
Output Voltage vs. Output Current



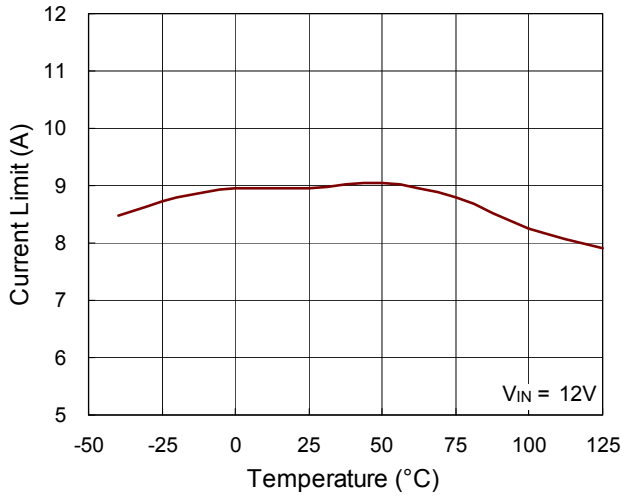
Frequency vs. Input Voltage



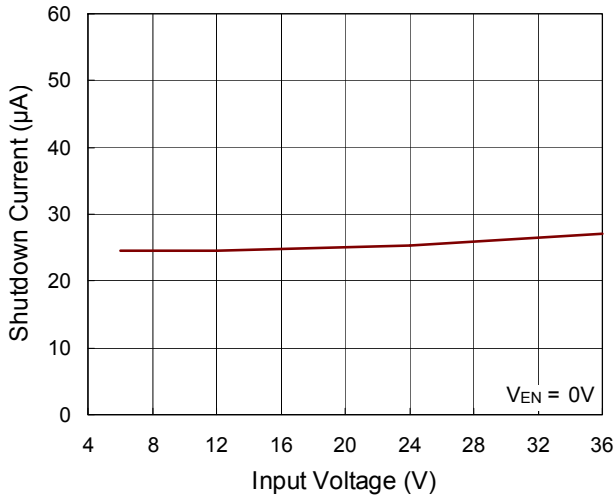
Frequency vs. Temperature



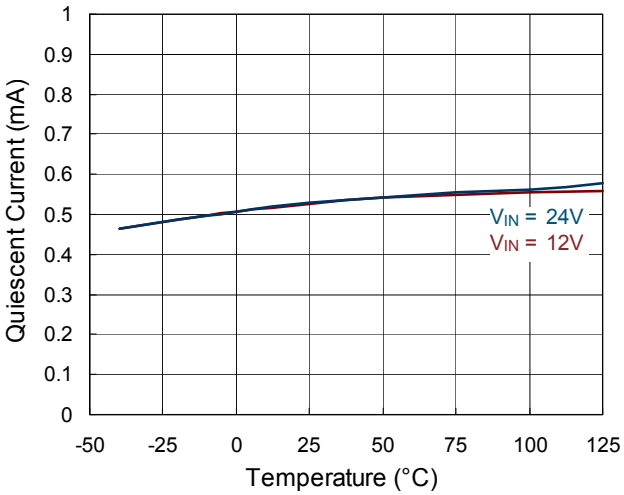
Current Limit vs. Temperature



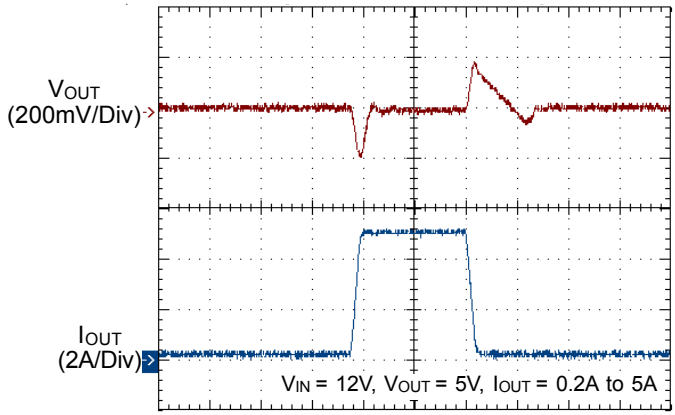
Shutdown Current vs. Input Voltage



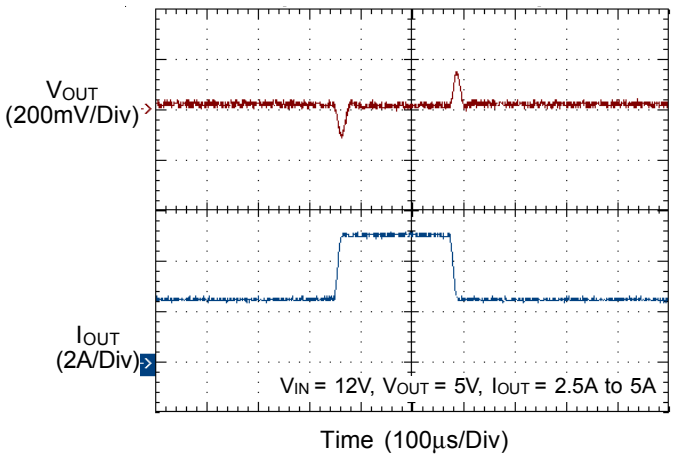
Quiescent Current vs. Temperature



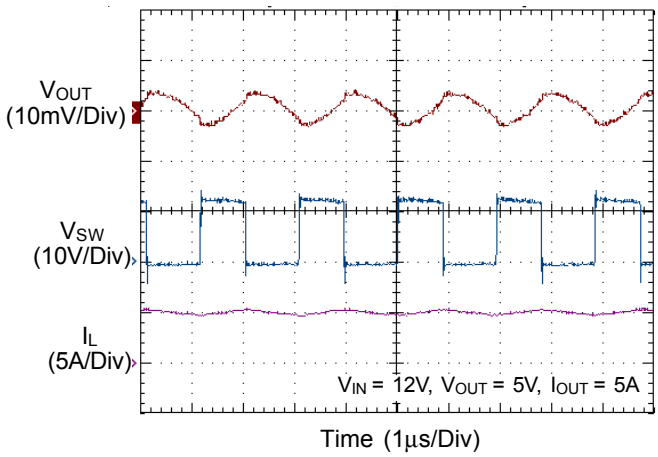
Load Transient Response



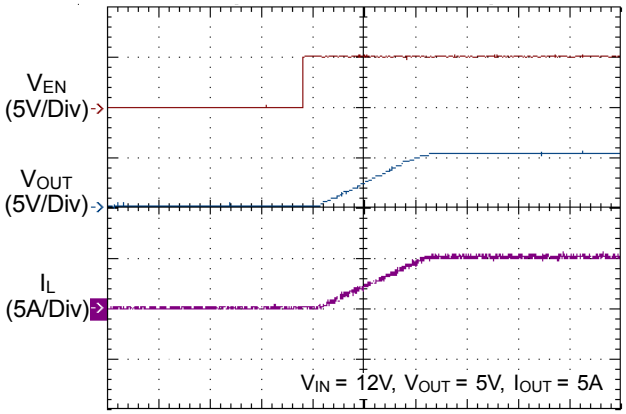
Load Transient Response



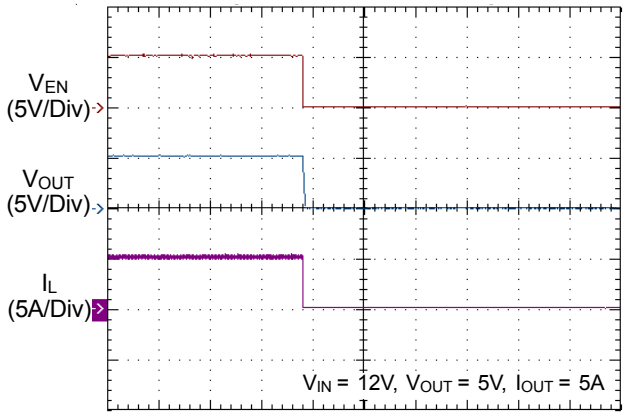
Switching



Power On from EN



Power Off from EN



Application Information

The RT6285 is an asynchronous high voltage buck converter that can support the input voltage range from 5.5V to 30V and the output current can be up to 5A.

Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

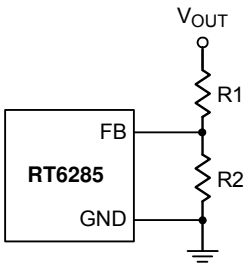


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right)$$

Where V_{REF} is the reference voltage (1.222V typ.).

Where R1 = 100kΩ.

External Bootstrap Diode

Connect a 10nF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT6285.

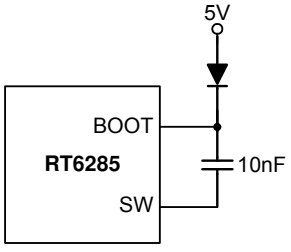


Figure 2. External Bootstrap Diode

Soft-Start

The RT6285 contains an internal soft-start clamp that gradually raises the output voltage. The typical soft-start time is 5ms.

Chip Enable Operation

The EN pin is the chip enable input. Pull the EN pin low (<0.4V) will shutdown the device. During shutdown mode, the RT6285 quiescent current drops to lower than 25μA. Drive the EN pin to high (>1.4V, <5.5V) will turn on the device again. If the EN pin is open, it will be pulled to high by internal circuit. For external timing control (e.g.RC), Figure 3 is the reference circuit, and the value of REN1 should be higher than 100kΩ to prevent high leakage current onto EN pin.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1-\frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.2(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1-\frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TAIYO YUDEN	NR10050	10 x 9.8 x 5
TDK	SLF12565	12.5 x 12.5 x 6.5

Freewheel Diode Selection

When the high-side MOSFET turns off, inductor current is supplied through the external low-side diode, freewheel diode, connected between the SW pin and GND.

The reverse voltage rating of freewheel diode should be equal to or greater than the V_{IN_MAX}. The maximum average forward rectified current of freewheel diode should be equal to or greater than the maximum load current. Considering the efficiency performance, the diode must have a minimum forward voltage and reverse recovery time. So Schottky Diodes are recommended to be freewheel diode.

The selected forward voltage of Schottky Diode must be less than the restriction of forward voltage in Figure 5 at operating temperature range to avoid the IC malfunction.

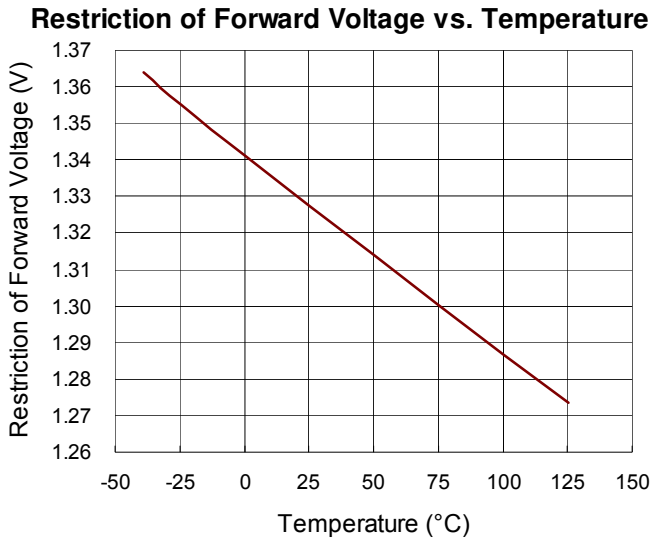


Figure 5. Restriction of Forward Voltage vs. Temperature

The losses of freewheel diode must be considered in order to ensure sufficient power rating for diode selection. The conduction loss in the diode is determined by the forward voltage of the diode, and the switching loss in the diode can be determined by the junction capacitor of the diode. The power dissipation of the diode can be calculated as following formula

$$P_D = P_{D\_CON} + P_{D\_SW} = I_{OUT} \times V_D \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + \frac{1}{2} \times C_J \times (V_{IN} + V_D)^2 \times f_{SW}$$

where C_J is the junction capacitance of the freewheel diode.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor, two 4.7μF low ESR ceramic capacitors are recommended. For the recommended capacitor, please refer to table 3 for more detail.

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8 f C_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR) also begins to charge or discharge C_{OUT} generating a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

EMI Consideration

Since parasitic inductance and capacitance effects in PCB circuitry would cause a spike voltage on SW pin when high side MOSFET is turned-on/off, this spike voltage on SW may impact on EMI performance in the system. In order to enhance EMI performance, there are two methods to suppress the spike voltage. One is to place an R-C snubber between SW and GND and make them as close as possible to the SW pin (see Figure 3). Another method is to add a resistor in series with the bootstrap capacitor, C_{BOOT}. But this method will decrease the driving capability to the high side MOSFET. It is strongly recommended to reserve the R-C snubber during PCB layout for EMI improvement. Moreover, reducing the SW trace area and keeping the main power in a small loop will be helpful on EMI performance. For detailed PCB layout guide, please refer to the section of Layout Consideration.

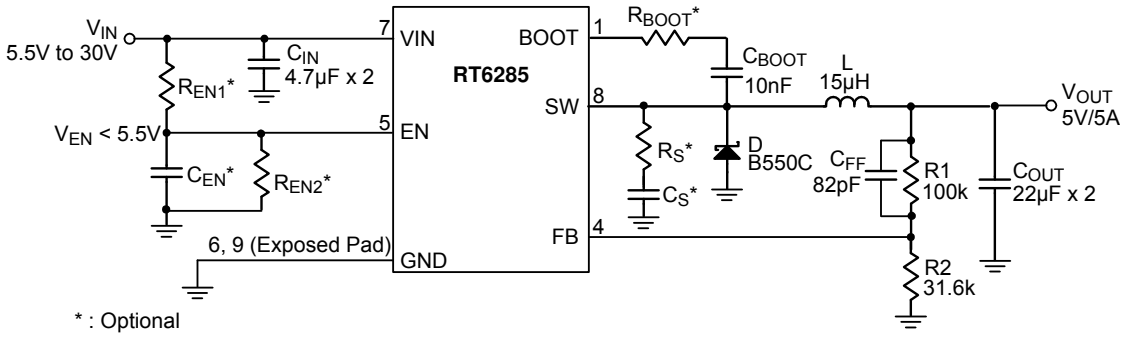


Figure 3. Reference Circuit with Snubber and Enable Timing Control

Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature , T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT6285, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For PSOP-8 package, the thermal resistance θ_{JA} is 75°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W (min.copper area PCB layout)

$P_{D(MAX)}$ = (125°C – 25°C) / (49°C/W) = 2.04W (70mm^2 copper area PCB layout)

The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package architecture design and the PCB layout design. However, the package architecture design had been designed. If possible, it's useful to increase thermal performance by the PCB layout copper design. The thermal resistance θ_{JA} can be decreased by adding copper area under the exposed pad of SOP-8 (Exposed Pad) package.

As shown in Figure 4, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 4a), θ_{JA} is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 4.b) reduces the θ_{JA} to 64°C/W. Even further, increasing the copper area of pad to 70mm^2 (Figure 4.e) reduces the θ_{JA} to 49°C/W.

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J\ (MAX)}$ and thermal resistance θ_{JA}. For the RT6285, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

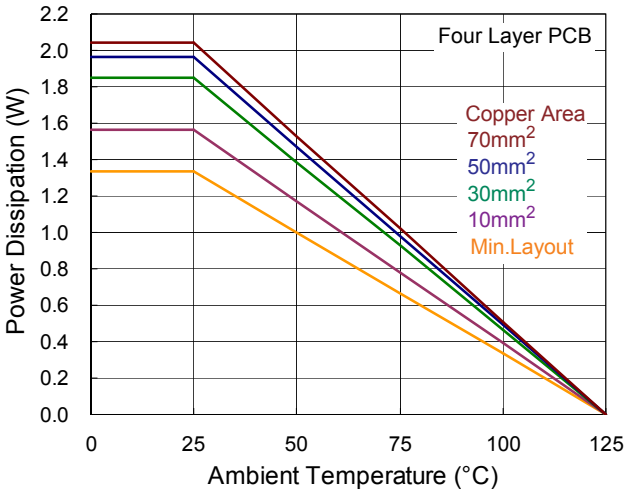
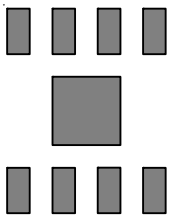
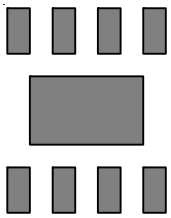


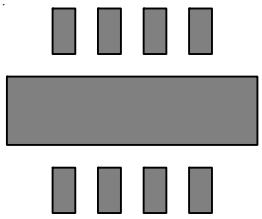
Figure 5. Derating Curves for RT6285 Package



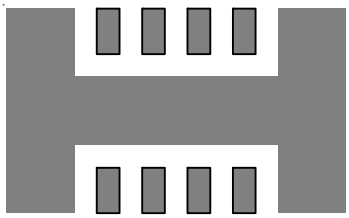
(a) Copper Area = (2.3 x 2.3) mm^2, θ_{JA} = 75°C/W



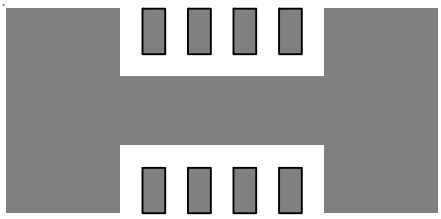
(b) Copper Area = 10mm^2, θ_{JA} = 64°C/W



(c) Copper Area = 30mm^2 , θ_{JA} = 54°C/W



(d) Copper Area = 50mm^2 , θ_{JA} = 51°C/W



(e) Copper Area = 70mm^2 , θ_{JA} = 49°C/W

Figure 4. Thermal Resistance vs. Copper Area Layout Design

Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT6285.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT6285.
- Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.
- An example of PCB layout guide is shown in Figure 6 for reference.

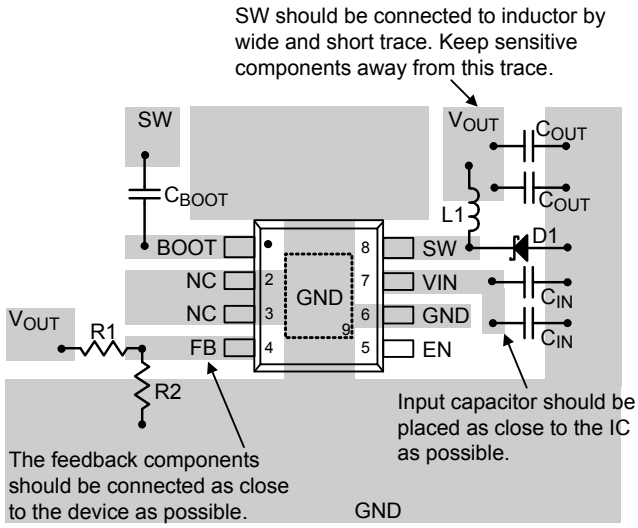


Figure 6. PCB Layout Guide

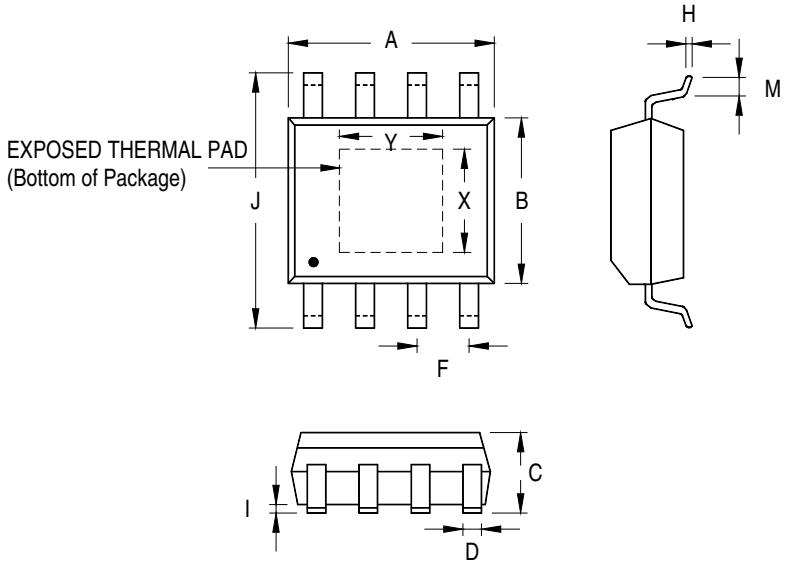
Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

Component	Description	Vendor P/N
CIN	4.7μF, 50V, X5R, 0805	GRM21BR61H475ME51 (MURATA) C2012X5R1H475M125AB (TDK)
COUT (VOUT = 5V)	22μF, 6.3V, X5R, 0603	GRM187R60J226ME15 (MURATA) C1608X5R0J226M080AC (TDK)

Table 4. Suggested Diode

Component Supplier	Series	V_{RRM} (V)	I_{OUT} (A)	Package
DIODES	B550C	50	5	SMC
PANJIT	SK55	50	5	SMC

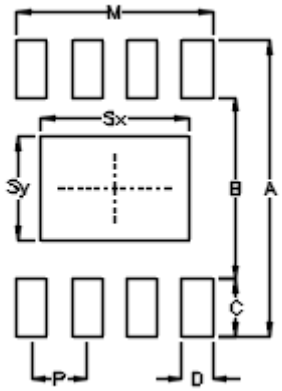
Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)							Tolerance
			P	A	B	C	D	Sx	Sy	M	
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

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