

✓ 54S/74S114 011004  
 ✓ 54LS/74LS114 011003

**DUAL JK NEGATIVE  
 EDGE-TRIGGERED FLIP-FLOP**  
 (With Common Clocks and Clears)

**DESCRIPTION** — The '114 features individual J, K and set inputs and common clock and common clear inputs. When the clock goes HIGH the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the Clock Pulse is HIGH and the bistable will perform according to the truth table as long as the minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

**TRUTH TABLE**

INPUTS		OUTPUT
J	K	Q
L	L	$Q_n$
L	H	L
H	L	H
H	H	$\bar{Q}_n$

Asynchronous Inputs:

- LOW input to  $\bar{S}_D$  sets Q to HIGH level
- LOW input to  $\bar{C}_D$  sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 $t_n$  = Bit time before clock pulse.  
 $t_{n+1}$  = Bit time after clock pulse.

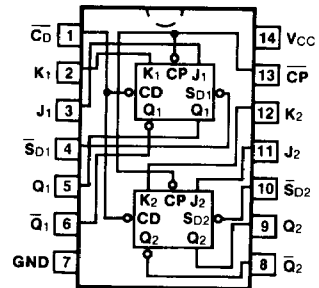
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 V \pm 5\%$ , $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = +5.0 V \pm 10\%$ , $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP (P)	A	74S114PC, 74LS114PC		9A
Ceramic DIP (D)	A	74S114DC, 74LS114DC	54S114DM, 54LS114DM	6A
Flatpak (F)	A	74S114FC, 74LS114FC	54S114FM, 54LS114FM	3I

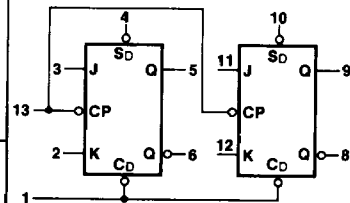
**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J <sub>1</sub> , J <sub>2</sub> , K <sub>1</sub> , K <sub>2</sub>	Data Inputs	1.25/1.0	0.5/0.25
$\bar{C}P$	Clock Pulse Input (Active Falling Edge)	5.0/5.0	2.0/0.5
$\bar{C}_D$	Direct Clear Input (Active LOW)	5.0/8.75	1.5/0.5
$\bar{S}_D1$ , $\bar{S}_D2$	Direct Set Inputs (Active LOW)	2.5/4.375	1.5/0.5
Q <sub>1</sub> , Q <sub>2</sub> , $\bar{Q}_1$ , $\bar{Q}_2$	Outputs	25/12.5	10/5.0 (2.5)

**CONNECTION DIAGRAM  
 PINOUT A**

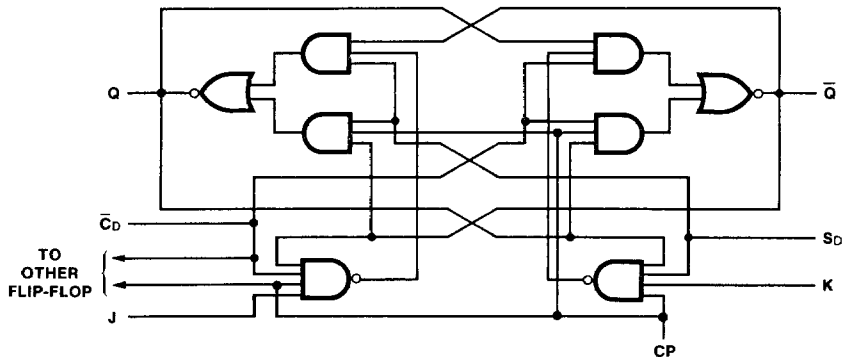


**LOGIC SYMBOL**



$V_{CC}$  = Pin 14  
 GND = Pin 7

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I <sub>CC</sub>	Power Supply Current	50		8.0		mA	V <sub>CC</sub> = Max, V <sub>CP</sub> = 0 V

AC CHARACTERISTICS: V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF R <sub>L</sub> = 280 Ω		C <sub>L</sub> = 15 pF			
		Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	80		30		MHz	Figs. 3-1, 3-9
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q or Q-bar	7.0		16 24		ns	Figs. 3-1, 3-9
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CD or SDn to Q or Q-bar	7.0		16 24		ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V<sub>C</sub> = +5.0 V, T<sub>A</sub> = +25° C

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time J <sub>n</sub> or K <sub>n</sub> to CP	7.0		20 15		ns	Fig. 3-7
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time J <sub>n</sub> or K <sub>n</sub> to CP	0		0 0		ns	Fig. 3-7
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse Width	6.0 6.5		20 15		ns	Fig. 3-9
t <sub>w</sub>	CD or SDn Pulse Width	8.0		15		ns	Fig. 3-10