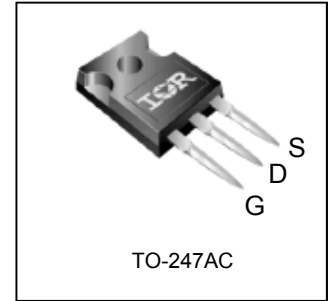
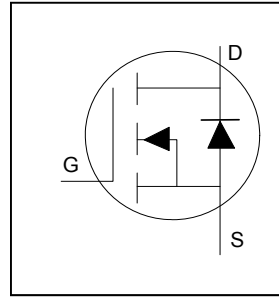


$V_{DSS}$	<b>60V</b>
$R_{DS(on)}$ <b>typ.</b>	<b>2.1m<math>\Omega</math></b>
<b>max.</b>	<b>2.5m<math>\Omega</math></b>
$I_D$ (Silicon Limited)	<b>270A<sup>①</sup></b>
$I_D$ (Package Limited)	<b>195A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

### Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

### Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP3006PbF	TO-247	Tube	25	IRFP3006PbF

### Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	270 <sup>①</sup>	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	190 <sup>①</sup>	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	195	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	1080	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	375	W
	Linear Derating Factor	2.5	W/ $^\circ\text{C}$
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
dv/dt	Peak Diode Recovery <sup>④</sup>	10	V/ns
$T_J$	Operating Junction and	-55 to + 175	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf.in (1.1N.m)	

### Avalanche Characteristics

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>③</sup>	320	mJ
$I_{AR}$	Avalanche Current <sup>②</sup>	See Fig. 14, 15, 22a, 22b	A
$E_{AR}$	Repetitive Avalanche Energy <sup>⑤</sup>		mJ

### Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case <sup>⑥</sup>	—	0.4	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

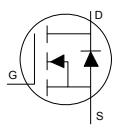
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.07	—	V/°C	Reference to 25°C, I <sub>D</sub> = 5mA <sup>②</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	2.1	2.5	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 170A <sup>⑤</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
R <sub>G</sub>	Internal Gate Resistance	—	2.0	—	Ω	

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

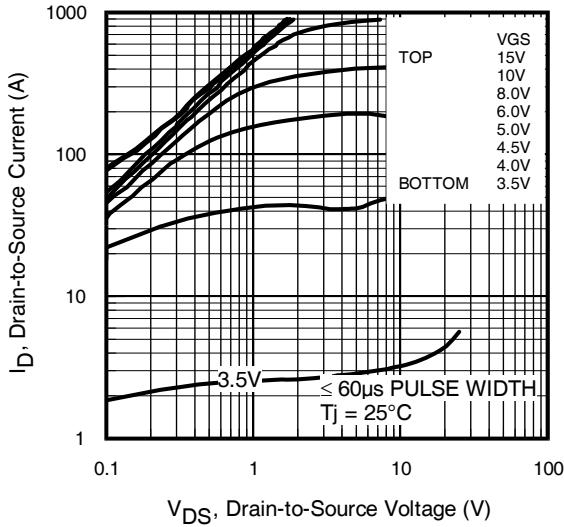
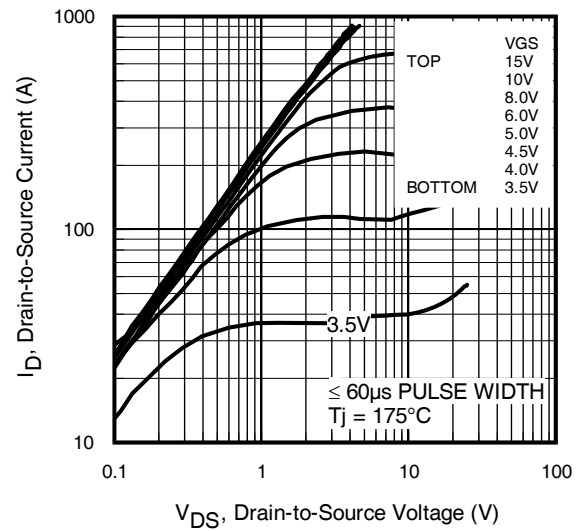
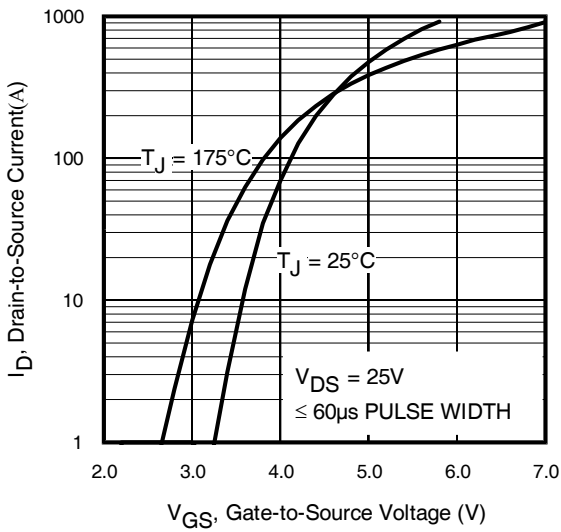
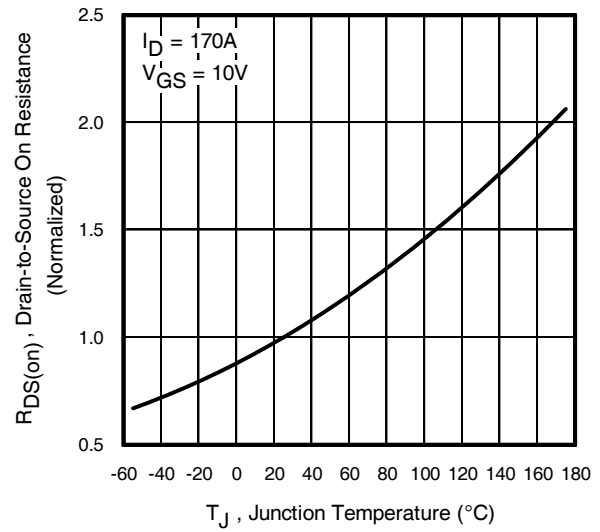
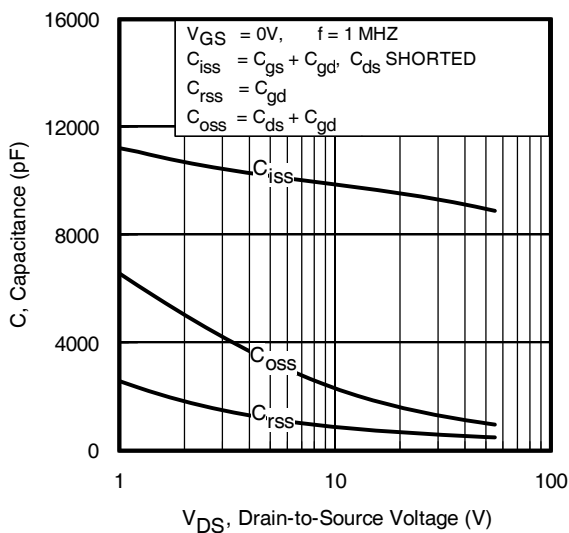
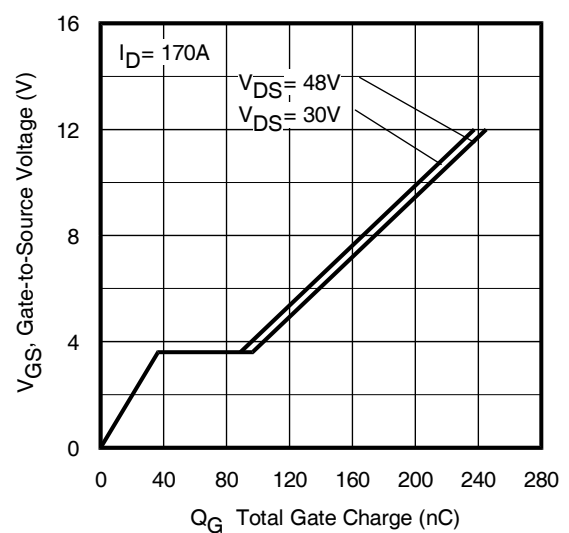
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	280	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 170A
Q <sub>g</sub>	Total Gate Charge	—	200	300		I <sub>D</sub> = 170A
Q <sub>gs</sub>	Gate-to-Source Charge	—	37	—	nC	V <sub>DS</sub> = 30V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	60	—		V <sub>GS</sub> = 10V <sup>⑤</sup>
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	140	—		I <sub>D</sub> = 170A, V <sub>DS</sub> = 0V, V <sub>GS</sub> = 10V
t <sub>d(on)</sub>	Turn-On Delay Time	—	16	—		V <sub>DD</sub> = 39V
t <sub>r</sub>	Rise Time	—	182	—	ns	I <sub>D</sub> = 170A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	118	—		R <sub>G</sub> = 2.7Ω
t <sub>f</sub>	Fall Time	—	189	—		V <sub>GS</sub> = 10V <sup>⑤</sup>
C <sub>iss</sub>	Input Capacitance	—	8970	—		V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	1020	—		V <sub>DS</sub> = 50V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	534	—	pF	f = 1.0 MHz, See Fig. 5
C <sub>oss</sub> eff. (ER)	Effective Output Capacitance (Energy Related)	—	1480	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 48V <sup>⑦</sup> See Fig. 11
C <sub>oss</sub> eff. (TR)	Effective Output Capacitance (Time Related)	—	1920	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 48V <sup>⑥</sup>

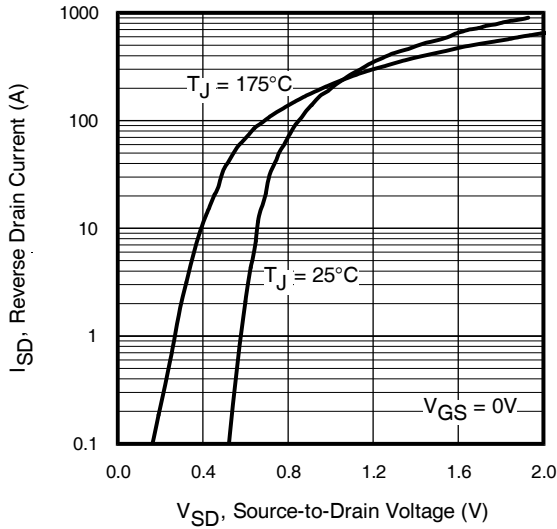
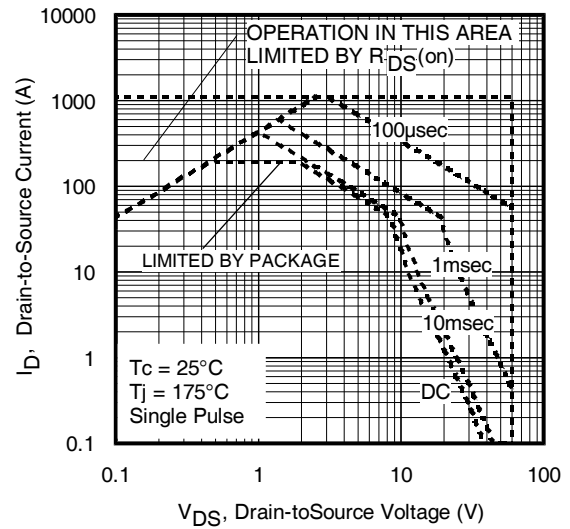
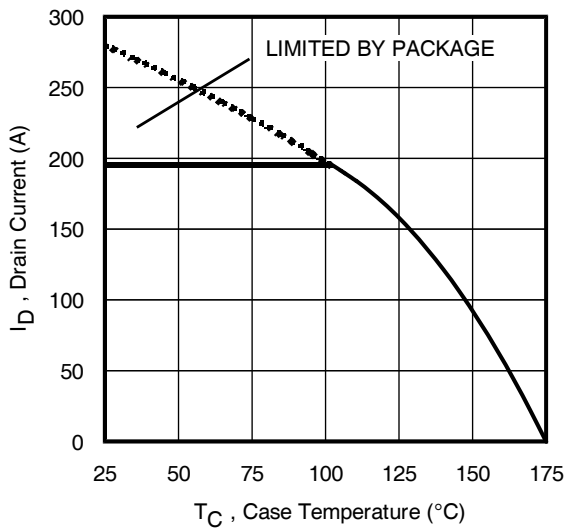
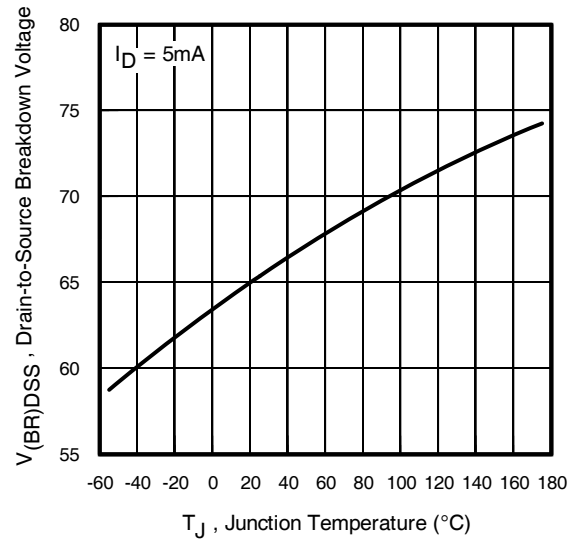
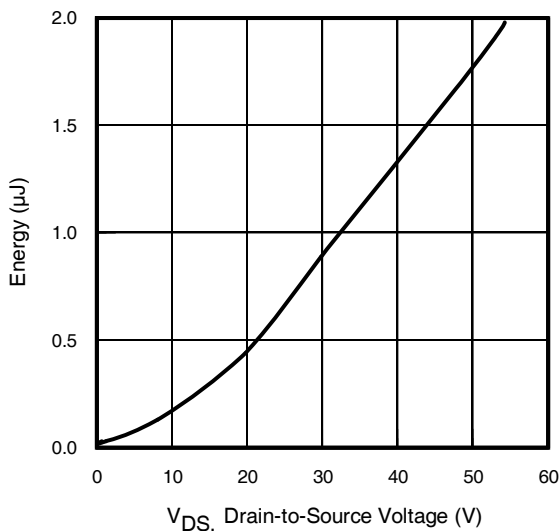
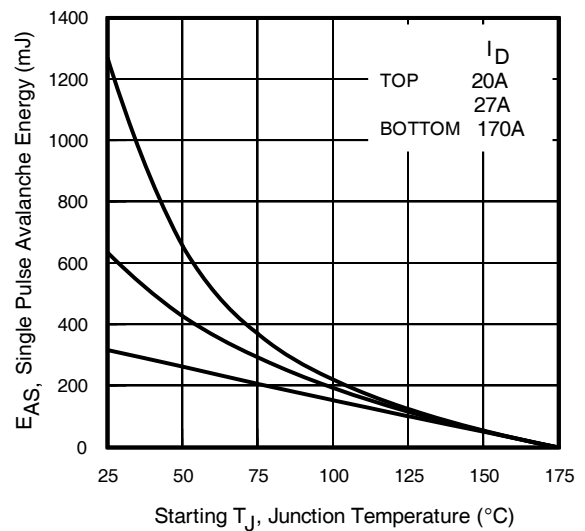
**Diode Characteristics**

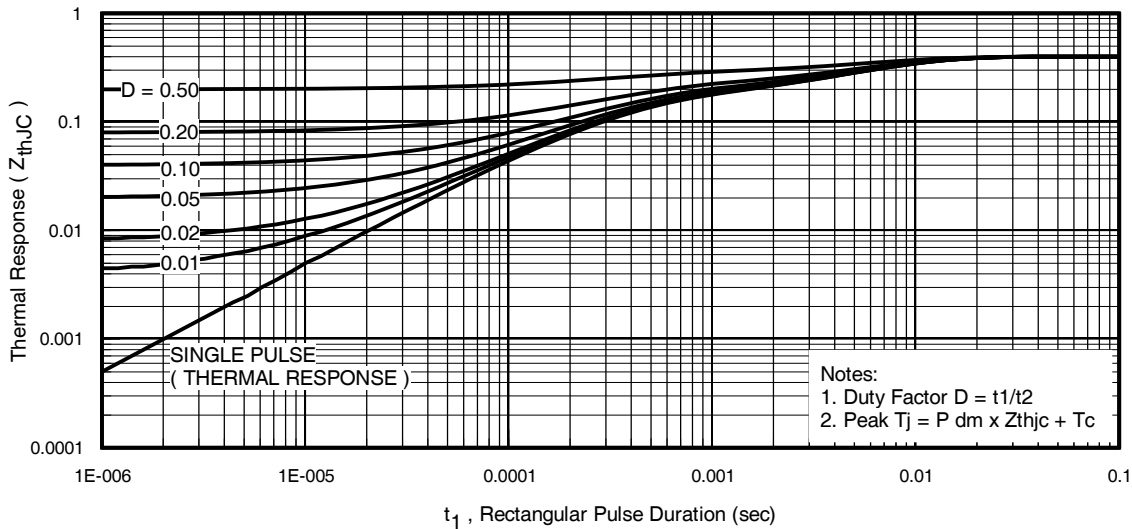
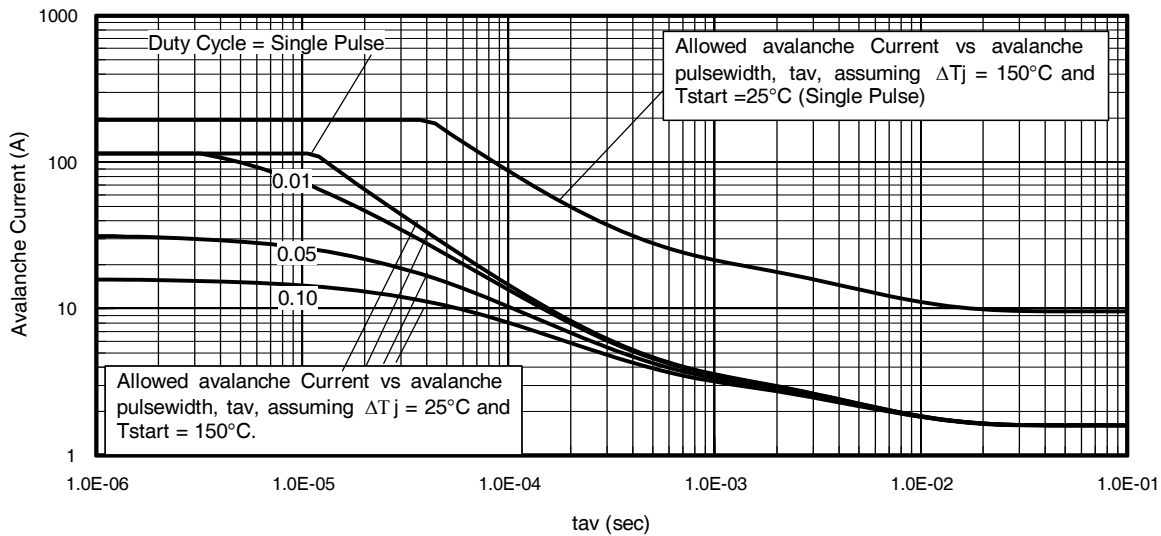
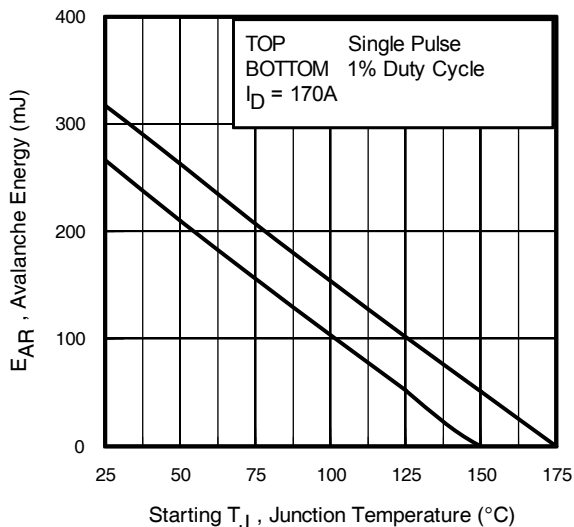
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	257 <sup>①</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>②</sup>	—	—	1028		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 170A, V <sub>GS</sub> = 0V <sup>④</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	44	—	ns	T <sub>J</sub> = 25°C
		—	48	—		T <sub>J</sub> = 125°C
Q <sub>rr</sub>	Reverse Recovery Charge	—	63	—	nC	T <sub>J</sub> = 25°C
		—	77	—		T <sub>J</sub> = 125°C
I <sub>RSM</sub>	Reverse Recovery Current	—	2.4	—	A	T <sub>J</sub> = 25°C V <sub>R</sub> = 51V, I <sub>F</sub> = 170A di/dt = 100A/μs <sup>⑤</sup>

**Notes:**

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
  - ② Repetitive rating; pulse width limited by max. Junction temperature.
  - ③ Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.022mH, R<sub>G</sub> = 50Ω, I<sub>AS</sub> = 170A, V<sub>GS</sub> = 10V. Part not Recommended for use above this value.
  - ④ I<sub>SD</sub> ≤ 170A, di/dt ≤ 1360A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
  - ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
  - ⑥ C<sub>oss</sub> eff. (TR) is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
  - ⑦ C<sub>oss</sub> eff. (ER) is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
  - ⑧ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.
- \* All spec data and curves based on (TO-220 Pak -IRFB3006PbF) Datasheet.


**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 7.** Typical Source-to-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Drain-to-Source Breakdown Voltage

**Fig 11.** Typical Coss Stored Energy

**Fig 12.** Maximum Avalanche Energy vs. Drain Current

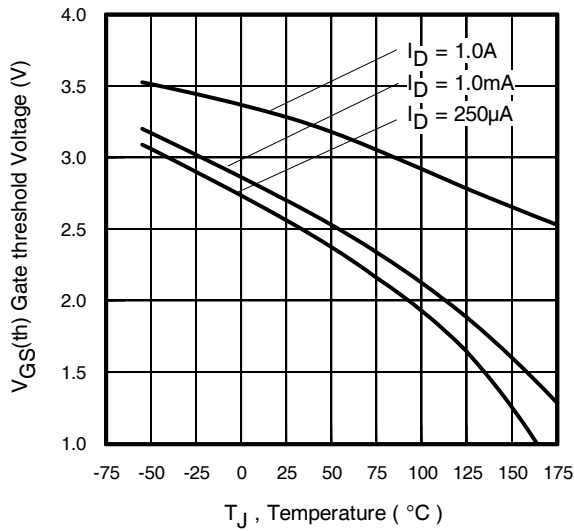
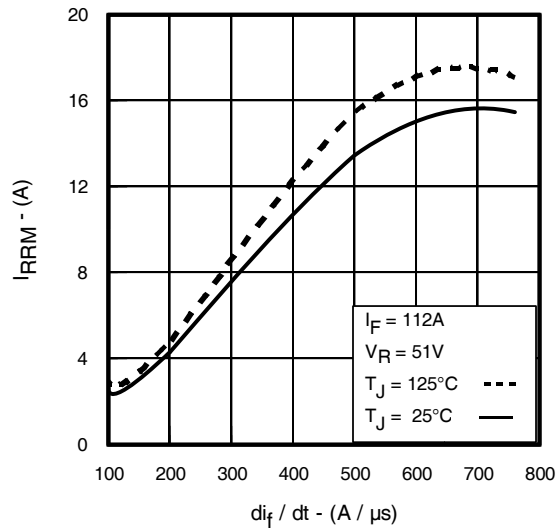
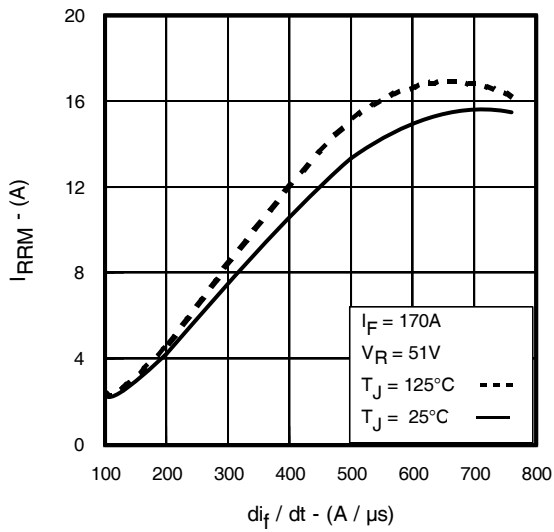
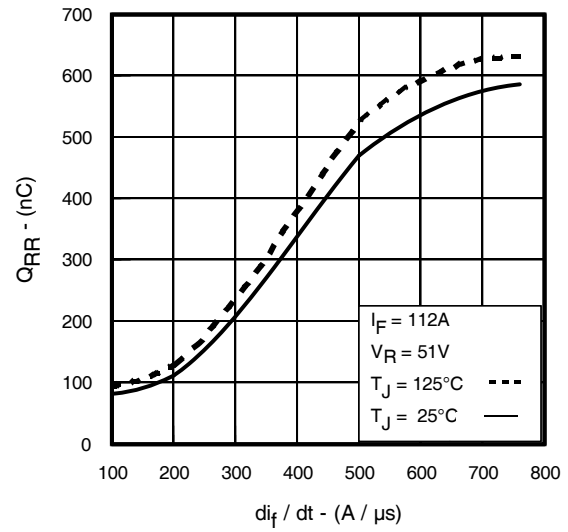
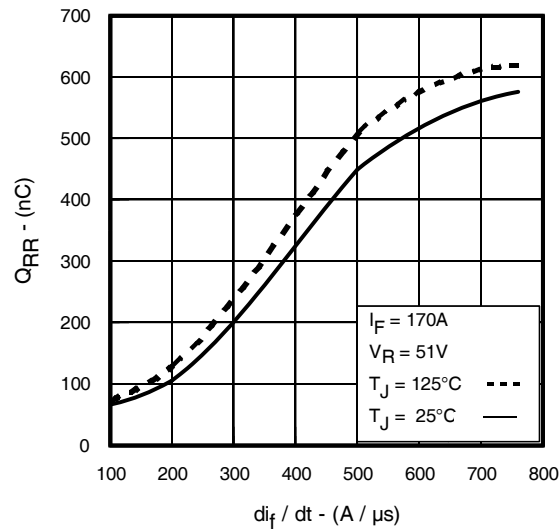

**Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 14. Typical Avalanche Current vs. Pulsewidth**

**Fig 15. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves, Figures 14, 15:  
(For further info, see AN-1005 at www.irf.com)**

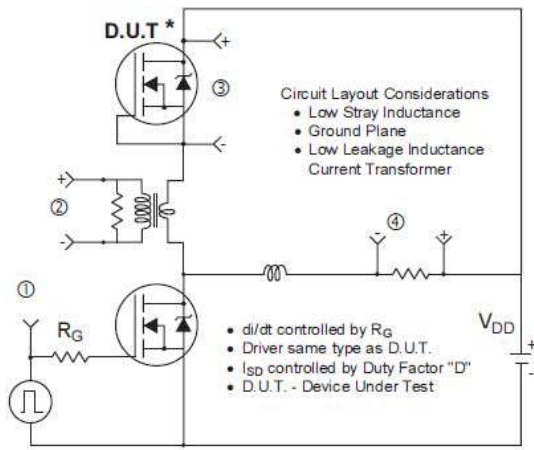
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as  $25^\circ C$  in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $tav \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

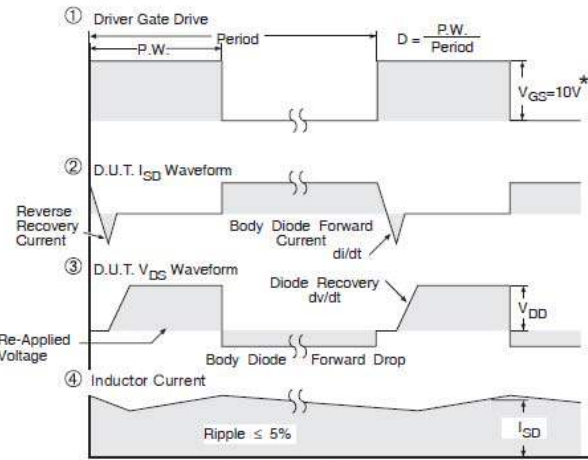
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


**Fig. 16** Threshold Voltage vs. Temperature

**Fig. 17** Typical Recovery Current vs.  $di_f/dt$ 

**Fig. 18.** Typical Recovery Current vs.  $di_f/dt$ 

**Fig. 19.** Typical Stored Charge vs.  $di_f/dt$ 

**Fig. 20.** Typical Stored Charge vs.  $di_f/dt$

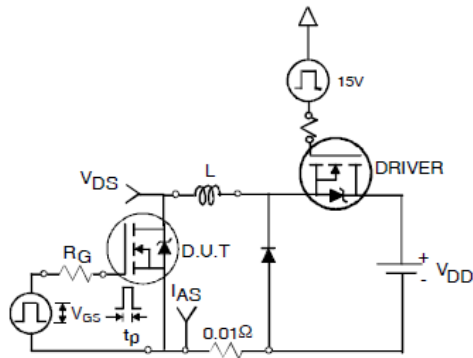


\* Reverse Polarity of D.U.T for P-Channel

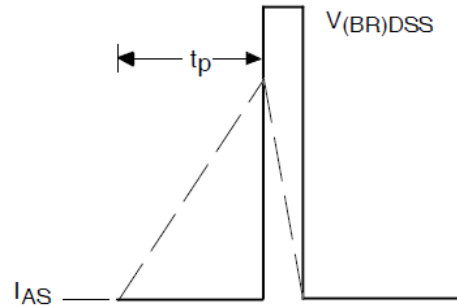


\* V<sub>GS</sub> = 5V for Logic Level Devices

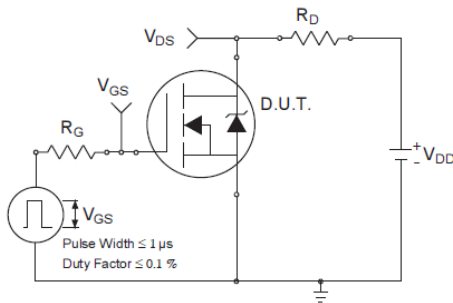
**Fig 21.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



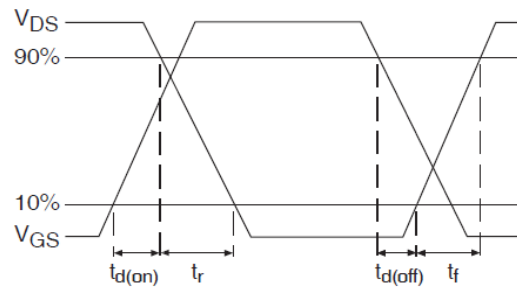
**Fig 22a.** Unclamped Inductive Test Circuit



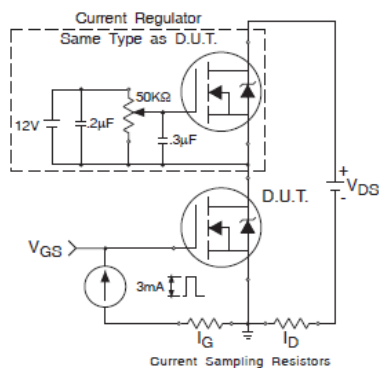
**Fig 22b.** Unclamped Inductive Waveforms



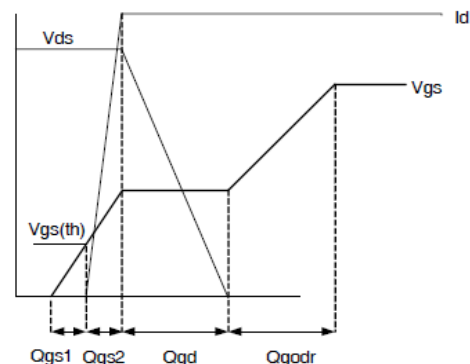
**Fig 23a.** Switching Time Test Circuit



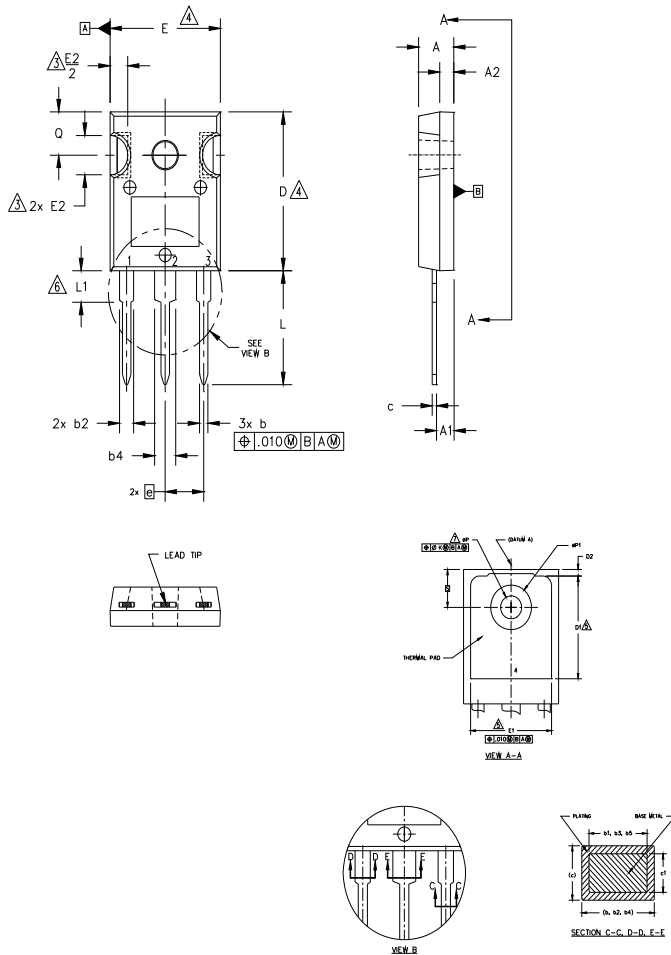
**Fig 23b.** Switching Time Waveforms



**Fig 24a.** Gate Charge Test Circuit



**Fig 24b.** Gate Charge Waveform

**TO-247AC Package Outline (Dimensions are shown in millimeters (inches))**


- NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
  2. DIMENSIONS ARE SHOWN IN INCHES.
  3. CONTOUR OF SLOT OPTIONAL.
  4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
  6. LEAD FINISH UNCONTROLLED IN L1.
  7.  $\phi P$  TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
  8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
$\phi k$	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
$\phi P$	.140	.144	3.56	3.66	
$\phi P1$	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

**LEAD ASSIGNMENTS**
**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

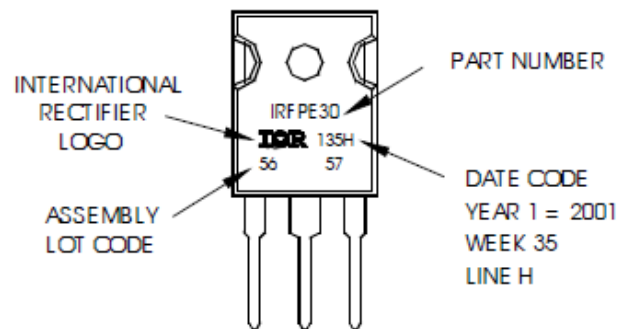
**DIODES**

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

**TO-247AC Part Marking Information**

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2001  
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



**Qualification information<sup>†</sup>**

Qualification level	Industrial (per JEDEC JESD47F ) <sup>††</sup>	
Moisture Sensitivity Level	TO-247AC	N/A
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

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