ADCxxDJxx00 Evaluation Module

User's Guide

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Introduction

The ADCxxDJxx00EVM is an evaluation board used to evaluate the ADCxxDJxx00 family (ADC08DJ3200, ADC12DJ2700 and ADC12DJ3200) of analog-to-digital converters (ADC) from Texas Instruments. The ADCxxDJxx00 devices are dual-channel, 8 or 12-bit ADCs, capable of operating at sampling rates up to 3.2 Giga-samples per second (GSPS) in dual channel mode or 6.4 GSPS in single channel mode. The ADCxxDJxx00EVM device output data is transmitted over a standard JESD204B high-speed serial interface. This evaluation board also includes the following important features:

- Transformer-coupled signal input network allowing a single-ended signal source from 500 kHz to 9 GHz
- The LMX2582 clock synthesizer generates the ADC sampling clock
- The LMK04828 and LMX2582 onboard system clock generator generates SYSREF and FPGA reference clocks for the high-speed serial interface
- Transformer-coupled clock input network to test the ADC performance with an external low-noise clock source
- LM95233 temperature sensor
- High-speed serial data output over a High Pin Count FMC+ interface connector

NOTE: To improve signal routing quality, serial lane polarity is inverted with respect to the standard FMC VITA-57 signal mapping. Signal mapping and polarity is shown in Table C-1).

- Device register programming through USB connector and FTDI USB-to-SPI bus translator

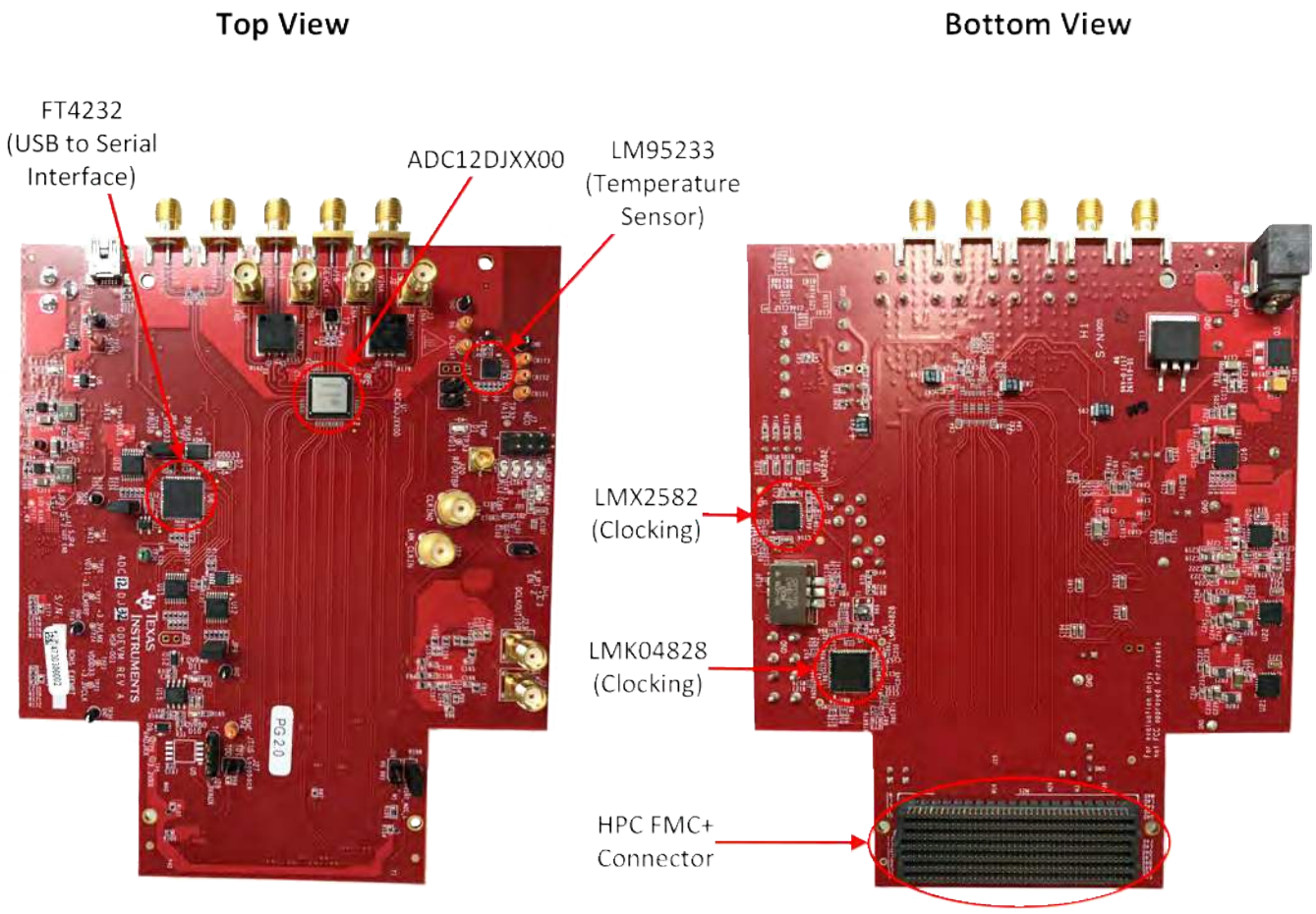

Figure 1-1. EVM Orientation

The digital data from the ADCxxDJxx00EVM board is quickly and easily captured with the TSW14J57EVM or TSW14J56EVM data capture boards.

NOTE: The TSW14J56EVM cannot be used for JMODES that use 16 data lanes, or serial rates above 12 Gbps.

The TSW14J57EVM captures the high-speed serial data, decodes the data, stores the data in memory, and then uploads it to a connected PC through a USB interface for analysis. The High-Speed Data Converter Pro (HSDC Pro) software on the PC communicates with the hardware and processes the data.

With proper hardware selection in the HSDC Pro software, the TSW14J57 device is automatically configured to support a wide range of operating speeds of the ADC12DJ3200EVM, but the device may not cover the full operating range of the ADC device. Serial data rates of 12.8 Gbps down to 1 Gbps are supported.

In the following sections of this document, the ADCxxDJxx00 evaluation board is referred to as the *EVM* and the ADCxxDJxx00 device is referred to as the *ADC* device.

Equipment

This section describes how to setup the EVM on the bench with the proper equipment to evaluate the full performance of the ADC device.

2.1 Evaluation Board Feature Identification Summary

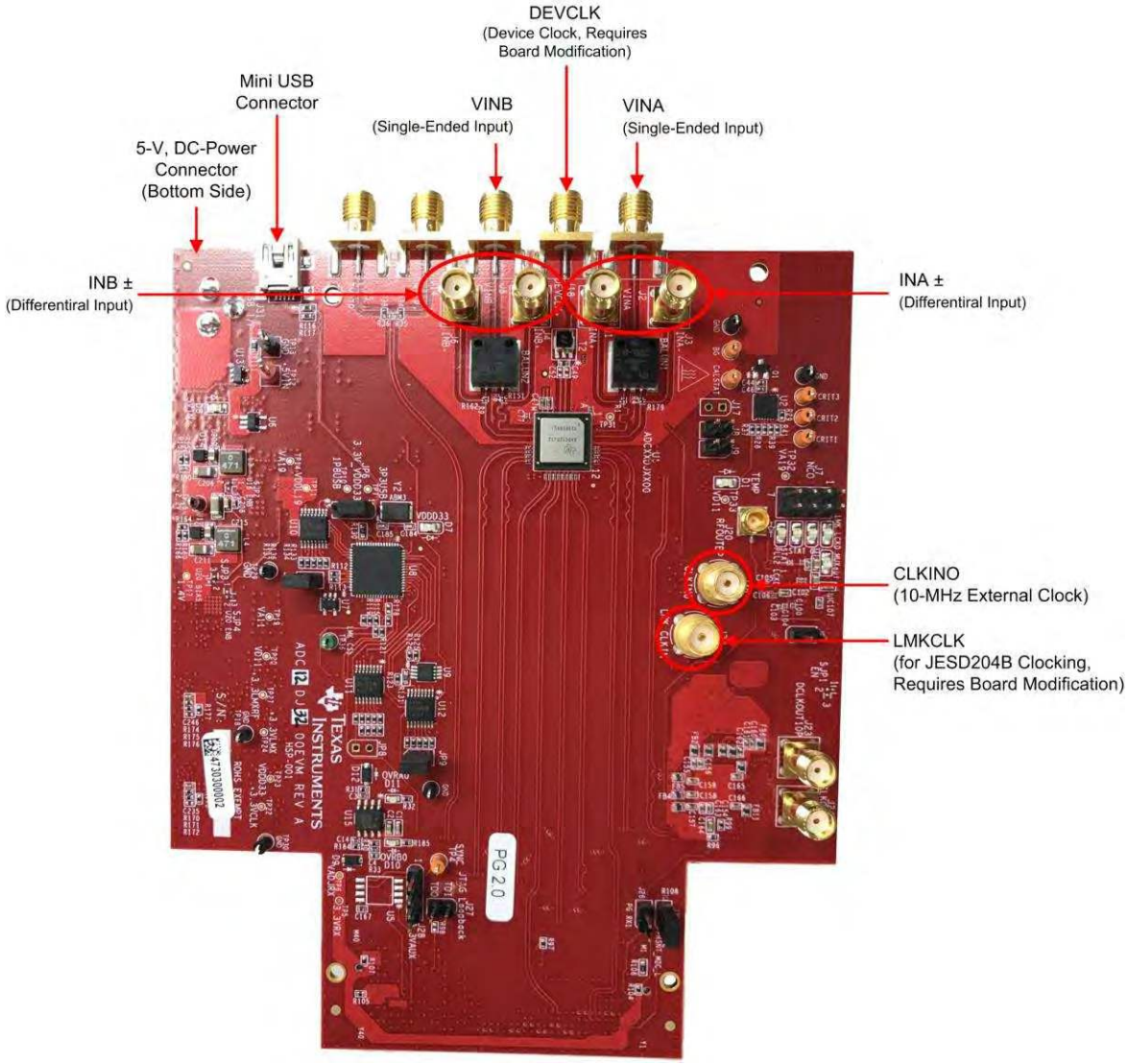

Figure 2-1. EVM Feature Locations

2.2 Required Equipment

The following equipment and documents are included in the EVM evaluation kit:

- Evaluation board (EVM)
- Mini-USB cable
- Power cable

The following equipment is **not** included in the EVM evaluation kit, but is required for evaluation of this product:

- TSW14J57EVM or TSW14J56EVM data capture board and related items
- High-Speed Data Converter Pro software
- PC computer running Microsoft® Windows® XP, 7, or 8
- One low-noise signal generator for analog input. TI recommends the following generators:
  - Keysight E8663D
  - Rohde & Schwarz® SMA100A
- Bandpass filter for analog input signal (1910 MHz or desired frequency). The following filters are recommended:
  - Bandpass filter, greater than or equal to 60-dB harmonic attenuation, less than or equal to 5% bandwidth, greater than 18-dBm power, less than 5-dB insertion loss
  - Trilithic™ 5VH-series tunable BPF
  - K&L Microwave™ BT-series tunable BPF
  - TTE KC6 or KC7-series fixed BPF
- Signal-path cables, SMA or BNC (or both SMA and BNC)

By default, the ADCxxDJxx00EVM has an onboard clocking solution. A few small board modifications enable external clocking. If external clocking is used, the following equipment is recommended.

- Two low-noise signal generators. TI recommends similar models to the analog input source.
- A bandpass filter for the DEVCLK input. TI recommends a filter similar to the analog-input path filter.

NOTE: The clock source used to drive the LMK04828 (labeled LMKCLK) must be equal in frequency to the ADC sampling clock (labeled DEVCLK). The clock generators must be frequency-locked using a common 10-MHz reference.

Setup Procedure

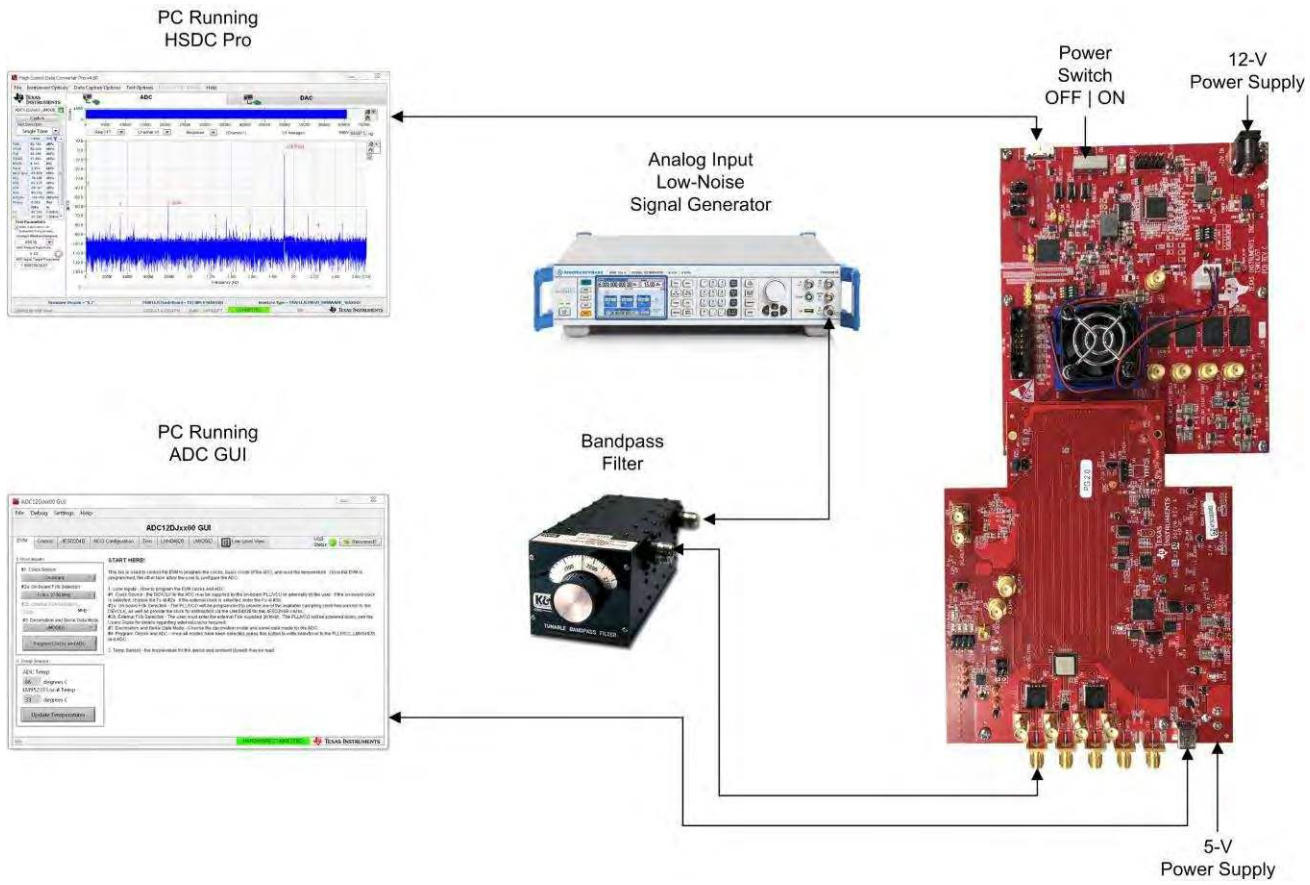

Figure 3-1. EVM Test Setup

NOTE: The HSDC Pro software must be installed before connecting the TSW14J57EVM to the PC for the first time.

3.1 Install the High Speed Data Converter (HSDC) Pro Software

Download the most recent version of the HSDC Pro software from www.ti.com/tool/dataconverterpro-sw. Follow the installation instructions to install the software.

3.2 Install the Configuration GUI Software

1. Download the Configuration GUI software from the EVM tool folder at ADC12DJxx00 GUI .
2. Extract files from the .zip file.
3. Run the executable file (setup.exe), and follow the instructions.

3.3 Connect the EVM and TSW14J57EVM

With the power off, connect the ADCxxDJxx00EVM to the TSW14J57EVM through the FMC connector as shown in Figure 3-1. Ensure that the standoffs provide the proper height for robust connector connections.

3.4 Connect the Power Supplies to the Boards (Power Off)

1. Confirm that the power switch on the TSW14J57EVM is in the off position. Connect the power cable to a 12-V DC (minimum 2 A) power supply. Ensure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 12 V. Connect the power cable to the EVM power connector.
2. Confirm that the power switch on the ADCxxDJxx00EVM is in the off position. Connect the power cable to a 5-V DC (minimum 3 A) power supply. Ensure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 5 V. Connect the power cable to the EVM power connector.

CAUTION

Ensure the power connections to the EVMs are the correct polarity. Failure to do so may result in immediate damage

Ensure the 12-V power supply is connected to the TSW14J57EVM and not the ADCxxDJxx00EVM. Providing the ADCxxDJxx00EVM with 12 V may result in immediate damage

Leave the power switches in the off position until directed later.

3.5 Connect the Signal Generators to the EVM (*RF Outputs Disabled Until Directed)

1. Connect a signal generator to the VIN input of the ADCxxDJxx00EVM through a bandpass filter and attenuator at the SMA connector. This must be a low-noise signal generator. TI recommends a Trilithic-tunable bandpass filter to filter the signal from the generator. Configure the signal generator for 1910 MHz, 0 dBm.

   If External Clocking is Used (Optional)

   a. Connect a signal generator to the DEVCLK input of the EVM through a bandpass filter. This signal generator must be a low-noise signal generator. TI recommends a Trilithic-tunable bandpass filter to filter the signal coming from the generator. Configure the signal generator for the desired clock frequency in the range of 0.8 to 3.2 GHz. For best performance when using an RF signal generator, the power input to the CLK SMA connector must be 9 dBm (2.2 Vpp into 50 Ω). The signal generator must increase above 9 dB by an amount equal to any additional attenuation in the clock signal path, such as the insertion loss of the bandpass filter. For example, if the filter insertion loss is 2 dB, the signal generator must be set to 9 dBm + 2 dB = 11 dBm.

   b. Connect a signal generator to the LMKCLK input of the EVM through a bandpass filter. Configure the signal generator for the desired clock frequency in the range of 0.8 to 3.2 GHz. Set the output power to approximately 6–9 dBm.

NOTE: 1. The LMKCLK frequency must be equal to the frequency of the DEVCLK.
2. Ensure that the DEVCLK and LMKCLK sources are frequency-locked using a common 10-MHz reference to ensure functionality. Frequency locking the input signal generator to the other generators can also be done if coherent sampling is desired.
3. Do not turn on the RF output of any signal generator at this time.
4. When using the ADC in single-input mode, the device uses both edges of DEVCLK for sampling.

3.6 Turn On the TSW14J57EVM Power and Connect to the PC

1. Turn on the power switch of the TSW14J57EVM.
2. Connect a mini-USB cable from the PC to the TSW14J57EVM.
3. If this is the first time connecting the TSW14J57EVM to the PC, follow the on-screen instructions to automatically install the device drivers. See the TSW14J57EVM user's guide (SLWU092) for specific instructions.

3.7 Turn On the ADCxxDJxx00EVM Power Supplies and Connect to the PC

1. Turn on the 5-V power supply to power up the EVM.
2. Connect the EVM to the PC with the mini-USB cable.

3.8 Turn On the Signal Generator RF Outputs

Turn on the RF signal output of the signal generator connected to VIN. If external clocking is used, turn on the RF signal outputs connected to DEVCLK and LMKCLK.

3.9 Open the ADCxxDJxx00EVM GUI and Program the ADC and Clocks

The Device Configuration GUI is installed separately from the HSDC Pro installation and is a stand-alone GUI.

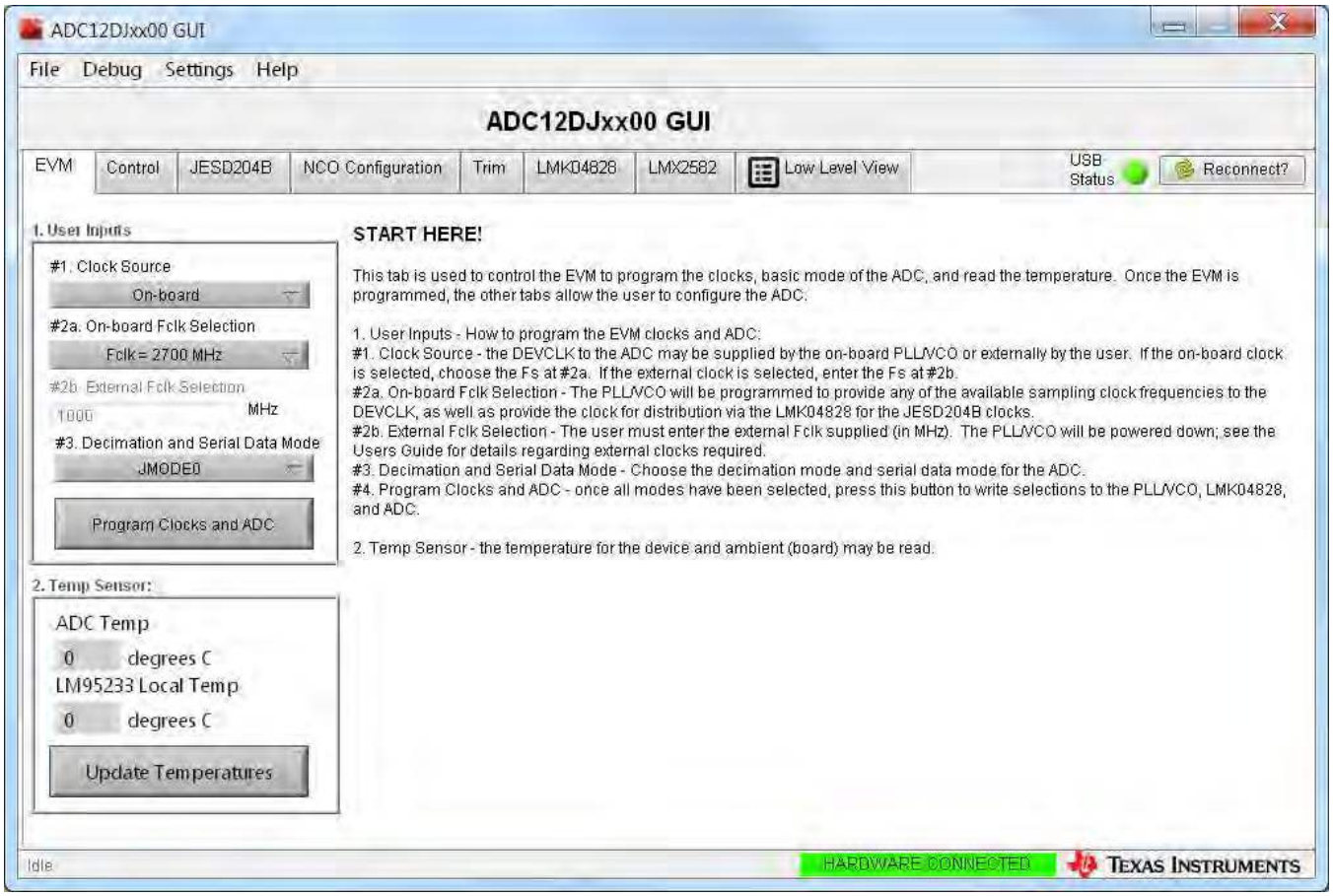

Figure 3-2. Configuration GUI EVM Tab

Figure 3-2 and Figure 3-3 show the GUI open to the *EVM* tab and *Control* tab respectively. Tabs at the top of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has three configurable devices, namely the ADCxxDJxx00, LMK04828, and LMX2582. The register map for each device is provided in the device data sheet (SLVSD97, SNAS605, and SNAS680, respectively).

1. Open the ADC12DJxx00EVM GUI.
2. Select the onboard clock as the clock source.
3. Select Fs = 2700 MHz MSPS as the onboard Fs selection.
4. If using the ADC12DJ2700EVM or ADC12DJ3200EVM, select JMODE0 for the decimation and serial data mode. If using the ADC08DJ3200EVM, select JMODE5 for the decimation and serial data mode.
5. Click *Program Clocks and ADC* (Note: This action will overwrite any previous device register settings.)

3.10 Calibrate the ADC Device on the EVM

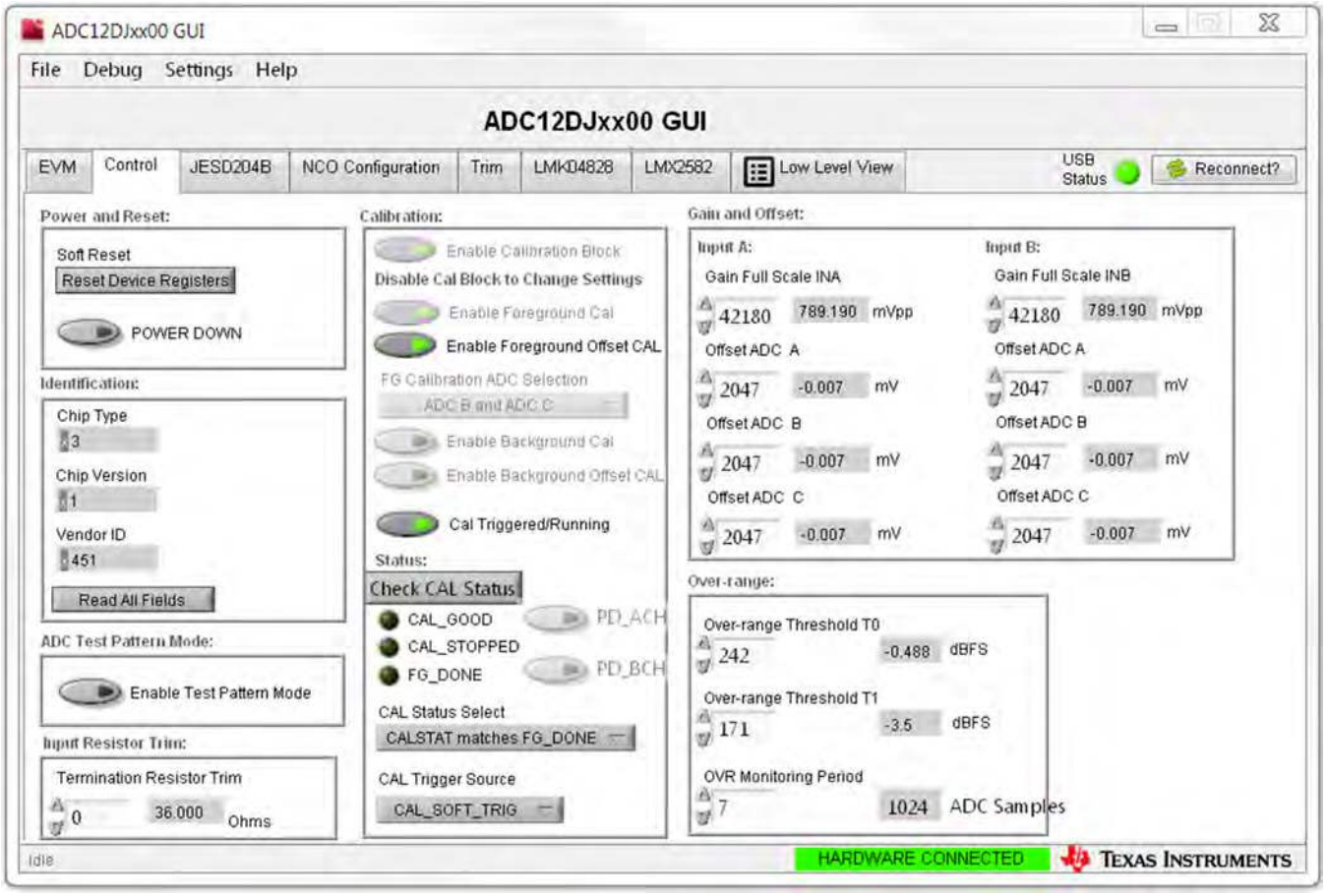

Figure 3-3. Configuration GUI ADC Control

1. With the EVM GUI open on the PC, navigate to the *Control* tab.
2. To calibrate the ADC, click *Call Triggered/Running* once, then click it again. This will stop and re-start the Calibration engine.

NOTE: This calibrate button executes a calibration sequence that is required for full performance. This calibration is performed automatically during the Section 3.9 step but must be performed again, any time the sampling rate changes, after significant temperature change of the ADC, or after exiting the power-down mode. See the ADCxxDJxx00 device data sheet, (SLVSD97) , for details regarding the necessary calibration sequence.

3. To enable background calibration, use the following steps:
   - Navigate to the *JESD204B* tab and click on *JESD Block Enable* to stop the JESD204B block.
   - Navigate back to the *Control* tab and click on *Enable Calibration Block* to disable calibration and allow setting changes.
   - Click on *Enable Background Cal*.
   - If background offset calibration is desired also, click on *Enable Background Offset Cal*.
   - Click on *Enable Calibration Block* to re-enable the calibration subsystem
   - Navigate to the *JESD204B* tab and click on *JESD Block Enable* to re-start the JESD204B block.
   - Navigate back to the *Control* tab and click the *Cal Triggered/Running* button once, then click it again. This restarts the Calibration engine.

4. To disable background calibration, use the following steps:
   - Navigate to the *JESD204B* tab and click on *JESD Block Enable* to stop the JESD204B block.
   - Navigate back to the *Control* tab and click on *Enable Calibration Block* to disable calibration and allow setting changes.
   - If background offset calibration was enabled, click on *Enable Background Offset Cal* to disable the feature.
   - Click on *Enable Background Cal* to disable the feature.
   - Click on *Enable Calibration Block* to re-enable the calibration subsystem.
   - Navigate to the *JESD204B* tab and click on *JESD Block Enable* to re-start the JESD204B block.
   - Navigate back to the *Control* tab and click the *Cal Triggered/Running* button once, then click it again. This restarts the Calibration engine.

3.11 Open the HSDC Software and Load the FPGA Image to the TSW14J57EVM

1. Open the HSDC Pro software.
2. Click *OK* to confirm the serial number of the TSW14J57EVM device. If multiple TSWxxxxx boards are connected, select the model and serial number for the one connected to the ADCxxDJxx00EVM.
3. If using the ADC12DJ2700EVM or the ADC12DJ3200EVM, select the ADC12DJxx00_JMODE0 device from the ADC select drop-down in the top left corner. If using the ADC08DJ3200EVM, select ADC12DJxx_JMODE5.
4. When prompted, click *Yes* to update the firmware.

NOTE: If the user configures the EVM with options other than the default register values, different instructions may be required for selecting the device in HSDC Pro. See Appendix B for more details.

5. Enter the ADC Output Data Rate ($f_{(SAMPLE)}$) as "5400M" or the desired output sample rate. This number must be equal to the actual sampling rate of the device and must be updated if the sampling rate changes.

3.12 Capture Data Using the HSDC Pro Software

The following steps show how to capture data using the HSDC Pro software (see Figure 3-4):

1. Select the test to perform.
2. Select the data view.
3. Select the channel to view.
4. Click the capture button to capture new data.

Additional tips:

- Use the *Notch Frequency Bins* from the *Test Options* file menu to remove bins around DC (eliminate DC noise and offset) or the fundamental (eliminate phase noise from signal generators).
- Open the *Capture Option* dialog from the *Data Capture Options* file menu to change the capture depth or to enable Continuous Capture or FFT averaging.
- For analyzing only a portion of the spectrum, use the *Single Tone* test with the *Bandwidth Integration Markers* from the *Test Options* file menu. The *Channel Power* test is also useful.
- For analyzing only a subset of the captured data, set the *Analysis Window (samples)* setting to a value less than the number of total samples captured and move the green or red markers in the small transient data window at the top of the screen to select the data subset of interest.

Figure 3-4. High Speed Data Converter Pro (HSDC) GUI

When using decimation and NCO features, click the gear symbol to access the *Additional Device Parameters* dialog box to enter the following details:

1. ADC Sampling Rate
2. ADC Input Signal Frequency
3. NCO Frequency
4. Decimation Factor

The HSDC Pro GUI will calculate the *ADC Output Data Rate* based on these inputs. The *Fundamental and Harmonic* frequency locations will also be calculated and identified in the FFT display.

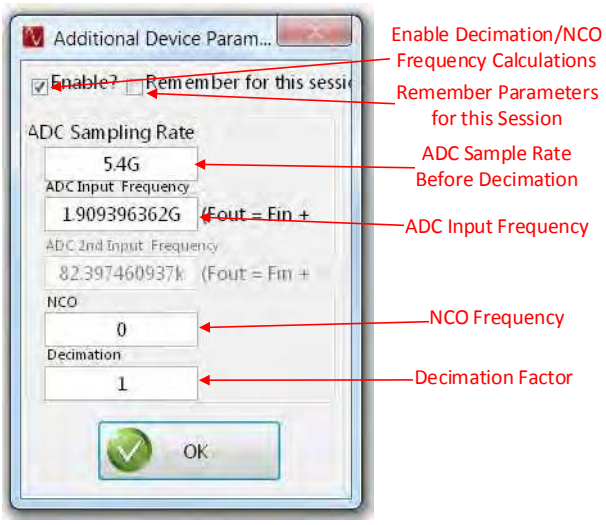

Figure 3-5. Additional Device Parameters Dialog Box

Device Configuration

The ADC device is programmable through the serial programming interface (SPI) bus accessible through the FTDI USB-to-SPI converter located on the EVM. A GUI is provided to write instructions on the bus and program the registers of the ADC device.

For more information about the registers in the ADC device, see the ADCxxDJxx00 device data sheet (SLVSD97).

4.1 Supported JESD204B Device Features

The ADC device supports some configuration of the JESD204B interface. Due to limitations in the TSW14J57EVM firmware, all JESD204B link features of the ADC device are not supported. Table 4-1 lists the supported and non-supported features.

Table 4-1. Supported and Non-Supported Features of the JESD204B Device

JESD204B Feature	Supported by ADC Device	Supported by TSW14J57EVM	Supported by TSW14J56EVM
Number of lanes per link (L)	L = 1, 2, 4, 8 (1)	L = 1, 2, 4, 8 supported	L = 1, 2, 4, 8 supported
Total number of lanes active	1, 2, 4, 8, 16	1, 2, 4, 8, 16	1, 2, 4, 8
Number of frames per multiframe (K)	K_{min} = 3–18, (1) K_{max} = 32, K_{step} = 1 or 2	Most values of K supported, constrained by requirement that $K \times F = 4^n$	Most values of K supported, constrained by requirement that $K \times F = 4^n$
Scrambling	Supported	Supported	Supported
Test patterns	PBRS7, PBRS11, PBRS15, Ramp, D21.5, K28.5, Repeat ILA, Modified RPAT, Long/Short Transport, Serial Out 0, Serial Out 1, Bypass Lane ID, ADC Test Pattern (1)	ILA, Ramp, Long/Short Transport	ILA, Ramp, Long/Short Transport
Speed	Lane rates from 0.8 to 12.8 Gbps (1)	Lane rates from 2 to 15 Gbps $f_{(SAMPLE)}$ parameter must be properly set in HSDC Pro GUI.	Lane rates from 0.6 to 12.5 Gbps $f_{(SAMPLE)}$ parameter must be properly set in HSDC Pro GUI.

(1) Dependent on bypass or decimation mode and output rate selection. Always disable the JESD204 block before changing any of the JESD204B settings. Once the settings are changed, re-enable the JESD204 block.

4.2 Tab Organization

Control of the ADC device features are available in the EVM, Control, JESD204B, NCO Configuration tabs.

4.3 Low-Level Control

The *Low Level View* tab, illustrated in Figure 4-1, allows configuration of the devices at the bit-field level. At any time, the controls in Table 4-2 can be used to configure or read from the device.

Table 4-2. Low-Level Controls

Control	Description
Register map summary	Displays the devices on the EVM, registers for those devices, and the states of the registers • Clicking on a register field allows individual bit manipulation in the register data cluster • The value column shows the value of the register at the time the GUI was last updated • The LR column shows the value of the register at the time the register was last read
Write register button	Write to the register highlighted in the register map summary with the value in the *Write Data* field
Write all button	Update all registers shown in the register map summary with the values shown in the *Register Map* summary
Read register button	Read from the register highlighted in the *Register Map* summary and display the results in the *Read Data* field Can be used to re-synchronize the GUI with the state of the hardware
Read-all button	Read from all registers in the *Register Map* summary and display the current state of the hardware
Load Configuration button	Load a configuration file from disk and register address/data values in the file
Save Configuration button	Save a configuration file to disk that contains the current state of the configuration registers
Register Data cluster	Manipulate individual accessible bits of the register highlighted in the register map summary
Individual register cluster with read or write register buttons	Perform a generic read or write command to the device shown in the *Block* drop-down box using the address and write data information

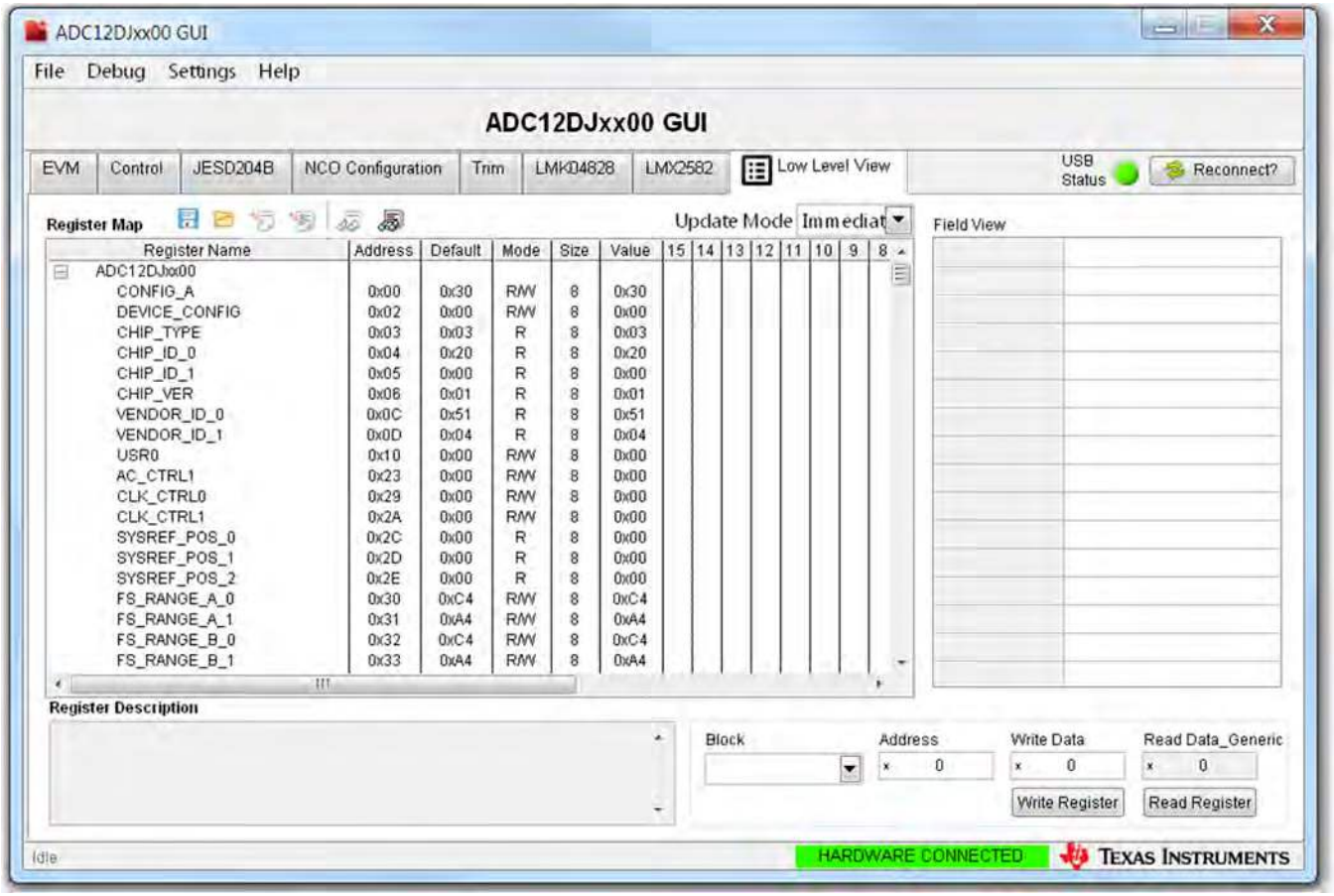

Figure 4-1. Low-Level Register Control Tab

Troubleshooting the ADCxxDJxx00EVM

Table 5-1 lists some troubleshooting procedures.

Table 5-1. Troubleshooting

Issue	Troubleshoot
General problems	• Verify the test setup shown in Figure 3-1, and repeat the setup procedure as described in this document. • Check power supply to EVM and TSW14J57EVM. Verify that the power switch is in the on position. • Check signal and clock connections to EVM. • Visually check the top and bottom sides of the board to verify that nothing looks discolored or damaged. • Ensure the board-to-board FMC+ connection is secure. • Try pressing the CPU_RESET button on the TSW14J57EVM. Also try clicking *Instrument Options → Reset Board* after changing the ADC configuration. • Try power-cycling the external power supply to the EVM, and reprogram the LMK and ADC devices.
TSW14J57 LEDs are not correct	• Verify the settings of the configuration switches on the TSW14J57EVM. • Verify that the clock going to the CLK input is connected and the appropriate LEDs are blinking. • Verify that the ADC device internal registers are configured properly. • If LEDs are not blinking, reprogram the ADC EVM devices. • Try pressing the CPU_RESET button on the TSW14J57EVM. • Try capturing data in HSDC Pro to force an LED status update
Configuration GUI is not working properly	• Verify that the USB cable is plugged into the EVM and the PC. • Check the computer device manager and verify that a *USB serial device* is recognized when the EVM is connected to the PC. • Verify that the green *USB Status* LED light in the top right corner of the GUI is lit. If it is not lit, click the *Reconnect FTDI* button. • Try restarting the configuration GUI.
Configuration GUI is not able to connect to the EVM	• Use the free FT_PROG software from FTDI chip and verify that the onboard FTDI chip is programmed with the product description *ADCxxDJxx00_A0* .
HSDC Pro software is not capturing good data or analysis results are incorrect.	• Verify that the TSW14J57EVM is properly connected to the PC with a mini-USB cable and that the board serial number is properly identified by the HSDC software. • Check that the proper ADC device mode is selected. The mode should match in HSDC Pro and the ADC GUI. • Check that the analysis parameters are properly configured.
HSDC Pro software gives a time-out error when capturing data	• Try to reprogram the LMK device and reset the JESD204 link. • Verify that the ADC sampling rate is correctly set in the HSDC software. • Try pressing the *CPU_RESET* button on the TSW14J57EVM. Also try clicking *Instrument Options → Reset Board* after changing the ADC configuration. Try to recapture again. • Select *Instrument Options → Download Firmware* and download 'TSW14J57REVD_FIRMWARE_10AX048.rbf'. Try to capture again.
Sub-optimal measured performance	• Try clicking *Cal Triggered/Running* button 2× to re-calibrate the ADC in the current operating conditions. It is located on the *Control* tab of the configuration GUI. • Check that the spectral analysis parameters are properly configured. • Verify that bandpass filters are used in the clock and input signal paths and that low-noise signal sources are used.

References

This section provides references to technical documents and user's guides.

A.1 Technical Reference Documents

- ADCxxDJxx00 device data sheet (SLVSD97)
- TSW14J57EVM user's guide (SLWU092)
- TSW14J56EVM user's guide (SLWU086)
- User's guide for the High Speed Data Converter Pro Software, also available in the help menu of the software (SLWU087)
- LMK04828 data sheet (SNAS605)
- LMX2582 data sheet (SNAS680)
- FTDI USB to Serial Driver Installation Manual (www.ftdichip.com/Support/Documents/InstallGuides.htm)

A.2 TSW14J57EVM Operation

Refer to the TSW14J57EVM user guide (SLWU092) for configuration and status information.

A.3 TSW14J56EVM Operation

Refer to the TSW14J56EVM user guide (SLWU086) for configuration and status information.

HSDC Pro Settings for Optional ADC Device Configuration

This appendix provides settings for optional ADC device configuration in HSDC Pro.

B.1 Changing the Number of Frames per Multi-Frame (K)

Changing the number of frames per multi-frame output by the JESD204 transmitter (ADC device) is configured using the K parameter on the *JESD204B* tab in the *Configuration* GUI. This parameter must be matched by the receiving device, and the SYSREF frequency must also be programmed to a compatible frequency. Ensure that the K value complies with the *K Min* and *Step* values for the selected JMODE. Refer to the ADCxxDJxx00 operating modes table in the ADCxxDJxx00 data sheet, (SLVSD97).

B.2 Customizing the EVM for Optional Clocking Support

Figure B-1 illustrates the ADCxxDJxx00EVM clocking system block diagram.

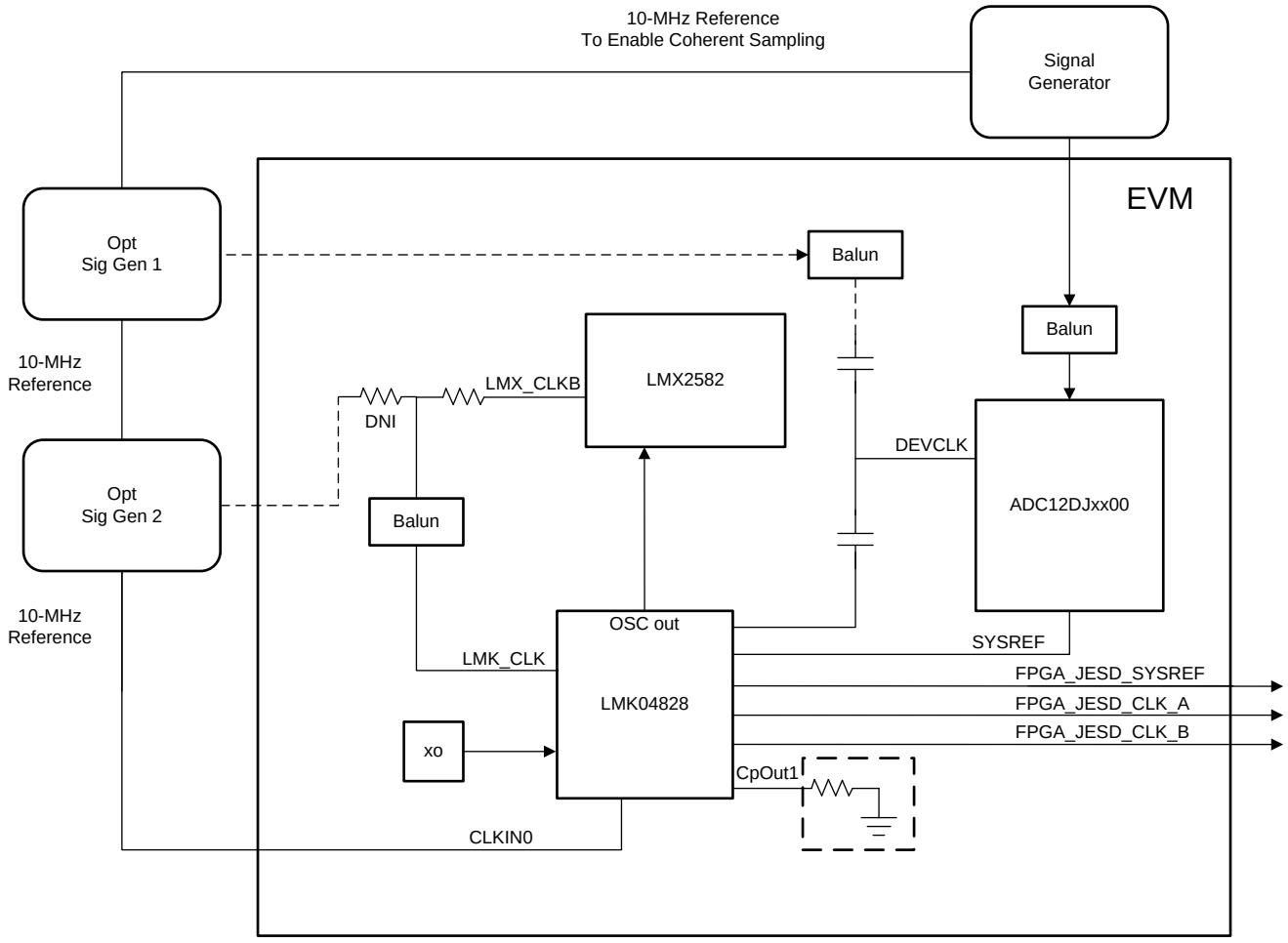

Figure B-1. ADC12DJxx00EVM Clocking System Block Diagram

The LMK04828 provides a buffered copy of the onboard crystal oscillator (OSCout) to the LMX2582. By default, the LMX2582 is configured to generate the ADC device clock using this 100-MHz reference and the LMK04828 is used in clock distribution mode and provides the SYSREF and device clocks for the FPGA. The EVM can be configured to use external clocks with the following steps (see Figure B-2):

1. Modify the hardware:
   a. Remove C50 and C51, populate C49 and C52.
   b. Remove R67, populate R70.
2. Connect the Signal Generators:
   a. Connect the 10-MHz reference from Sig Gen 1 to Sig Gen 2.
   b. Configure Sig Gen 2 to use the 10-MHz reference input from Sig Gen 1.
   c. Sig Gen 1 connects to DEVCLK (J18). Set to the generator frequency to the desired F_{DEVCLK}. Set output level to +9 dBm.
   d. Sig Gen 2 connects to LMKCLK (J22) with output level +6 dBm to +9 dBm. Set the generator frequency as follows:
   $F_{LMKCLK} = F_{DEVCLK}$
3. Program the GUI:
   a. In the EVM tab, set the Clock Source to *External*.
   b. Enter the *Sampling Frequency* (F_{DEVCLK}) in step 2(b).

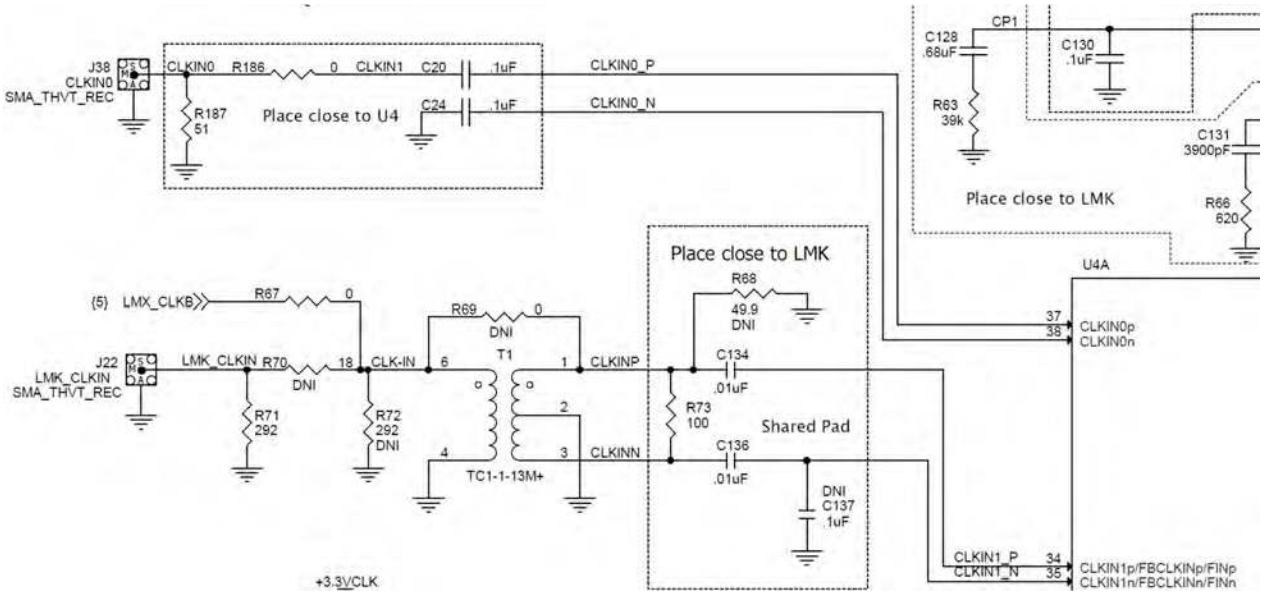

Figure B-2. External LMKCLK Configuration

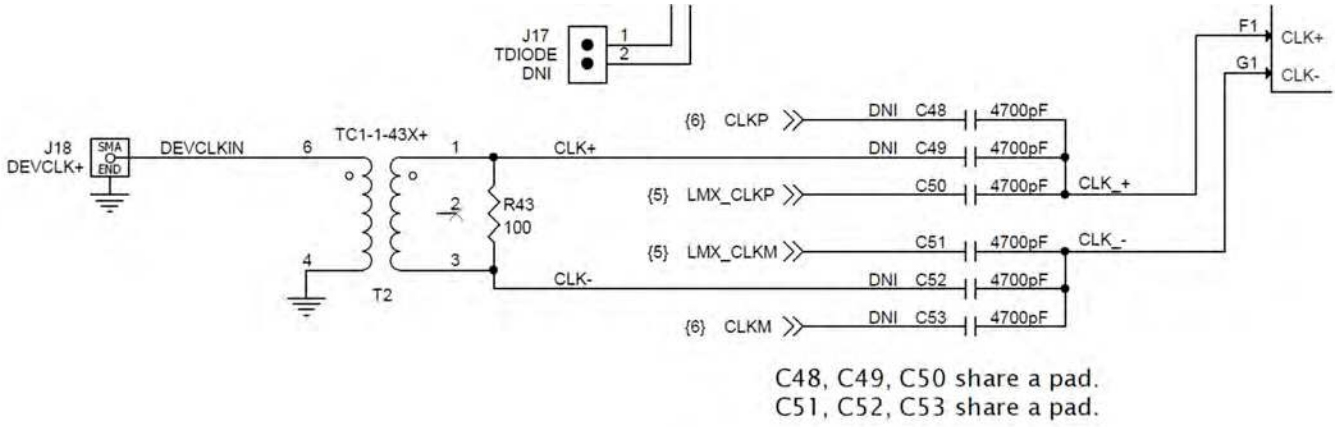

Figure B-3. External DevCLK EVM Configuration

The ADC12DJxx00EVM includes a reference clock input (CLKIN0) which allows the user to sync the LMK04828 to an external 10-MHz reference allowing for coherent sampling

The LMX2582 and LMK04828 may be reconfigured to exercise more features, but this EVM is not intended to be a full evaluation platform for these devices. For a full evaluation platform, see the LMK04828 tool folder and LMX2582 tool folder.

Signal Routing

Table C-1 provides the signal routing details for the ADCxxDJxx00EVM.

Table C-1. ADCxxDJxx00EVM Signal Routing

JESD204B Output	Link	LID	FMC(+) Pins	FMC(+) Signal Names[1]
DA0	A	0	A10,A11	DP3_M2C
DA1	A	1	C6,C7	DP0_M2C
DA2	A	2	A6,A7	DP2_M2C
DA3	A	3	A2,A3	DP1_M2C
DB0	B	0	B12,B13	DP7_M2C_INV
DB1	B	1	A14,A15	DP4_M2C_INV
DB2	B	2	B16,B17	DP6_M2C_INV
DB3	B	3	A18,A19	DP5_M2C_INV
DA4	A	4	Y14,Y15	DP12_M2C
DA5	A	5	Y10,Y11	DP10_M2C
DA6	A	6	B8,B9	DP8_M2C
DA7	A	7	B4,B5	DP9_M2C
DB4	B	4	Z12,Z13	DP11_M2C_INV
DB5	B	5	Z16,Z17	DP13_M2C_INV
DB6	B	6	Y18,Y19	DP14_M2C_INV
DB7	B	7	Y22,Y23	DP15_M2C_INV

(1) Red items with _INV in the signal name are inverted with respect to standard FMC polarity.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2017) to A Revision	Page
• Broadened scope of user guide from ADC12DJ3200 to include the ADC08DJ3200 and ADC12DJ2700 devices.	4

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      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

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      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

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(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Concernant les EVMs avec antennes détachables

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http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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