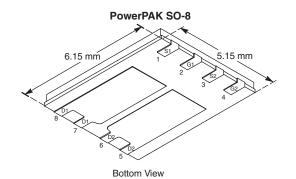


# **Dual N-Channel 150-V (D-S) MOSFET**

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A)		
150	0.150 at V <sub>GS</sub> = 10 V	3.3		
	0.168 at V <sub>GS</sub> = 6 V	3.1		



Ordering Information: Si7946DP-T1-E3 (Lead (Pb)-free)

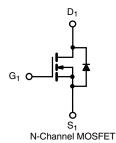
Si7946DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

#### **FEATURES**

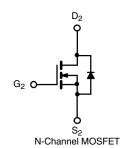
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET<sup>®</sup> Power MOSFETs
- New Low Thermal Resistance PowerPAK<sup>®</sup> Package
- Dual MOSFET for Space Savings
- · PWM Optimized for Fast Switching
- Avalanche Rated

#### **APPLICATIONS**

Primary Side Switch







<b>ABSOLUTE MAXIMUM RATINGS</b>	<b>T</b> <sub>A</sub> = 25 °C, unles	ss otherwise n	oted			
Parameter	Symbol	10 s	Steady State	Unit		
Drain-Source Voltage		$V_{DS}$	150		V	
Gate-Source Voltage		$V_{GS}$	± 20		V	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	l <sub>a</sub>	3.3	2.1		
Continuous Diain Current (1) = 150 °C)	T <sub>A</sub> = 70 °C	- I <sub>D</sub>	2.6	1.7		
Pulsed Drain Current		I <sub>DM</sub>	10		Α	
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	2.9	1.2		
Single Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	9			
Single Avalanche Energy		E <sub>AS</sub>	4		mJ	
Manipular Davier Disable ation 8	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.5	1.4	W	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C		2.2	0.9		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150			
Soldering Recommendations (Peak Temperature)b, c				260	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	t ≤ 10 s	R <sub>thJA</sub>	26	35	°C/W	
	Steady State		60	85		
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	3.2	4.2		

#### Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Solder Profile (<u>www.vishay.com/ppg?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

# Vishay Siliconix



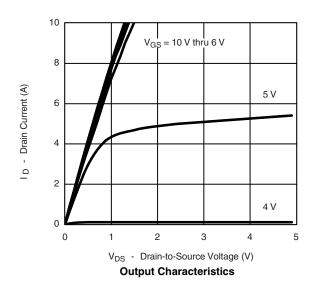
SPECIFICATIONS T <sub>,I</sub> = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Condition	Min.		Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2		4.0	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zava Cata Valtana Dvain Current	1	V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	5		μΑ		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	10			Α	
	В	$V_{GS} = 10 \text{ V}, I_D = 3.3 \text{ A}$		0.124	0.150	Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 6 \text{ V}, I_D = 3.1 \text{ A}$		0.137	0.137 0.168		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_D = 3.3 \text{ A}$		9		S	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>S</sub> = 2.9 A, V <sub>GS</sub> = 0 V		0.87	1.2	V	
Dynamic <sup>b</sup>							
Total Gate Charge	$Q_g$			12.6	20	nC	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 3.3 \text{ A}$		2.8			
Gate-Drain Charge	$Q_{gd}$			4.5			
Gate Resistance	$R_g$	f = 1 MHz		3.5		Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			11	20		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 75 V, $R_L$ = 75 $\Omega$		15	25	ns	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 1$ A, $V_{GEN}=10$ V, $R_g=6$ $\Omega$		30	45		
Fall Time	t <sub>f</sub>			20	30		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.9 A, dl/dt = 100 A/μs		62	100		

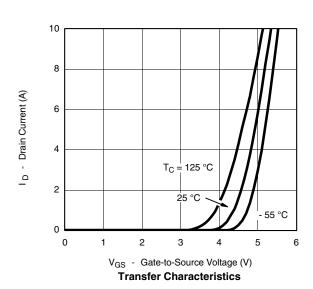
#### Notes:

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



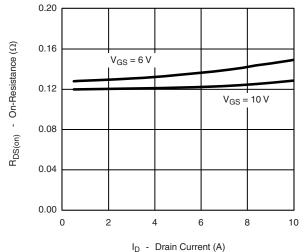


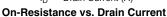


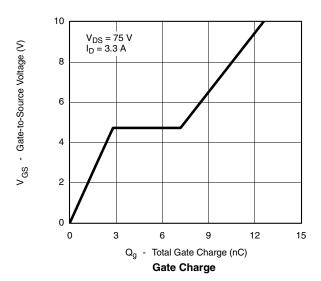


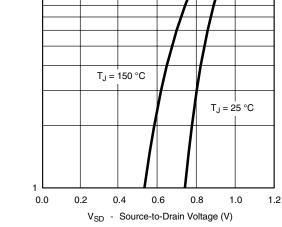


#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

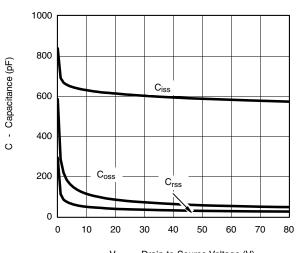






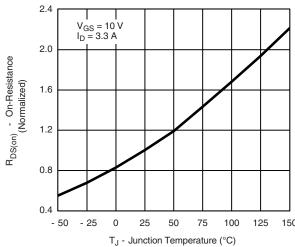


Source-Drain Diode Forward Voltage

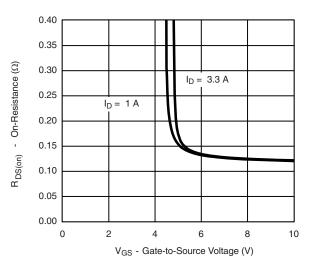


V<sub>DS</sub> - Drain-to-Source Voltage (V)





On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage

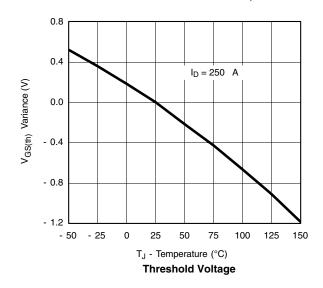
10

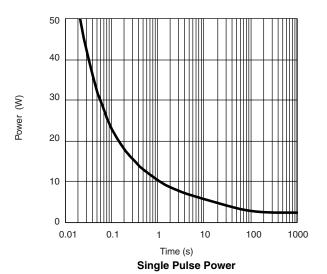
Is - Source Current (A)

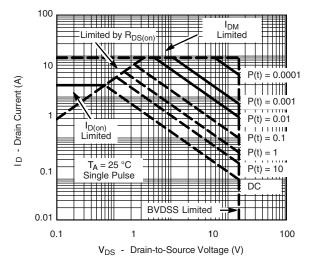
# Vishay Siliconix

# VISHAY

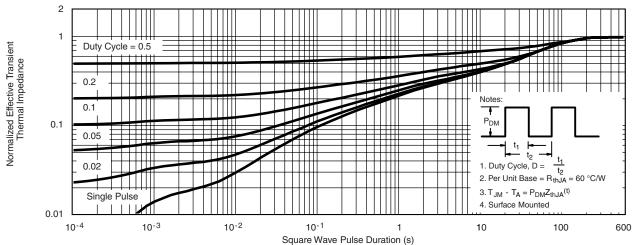
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





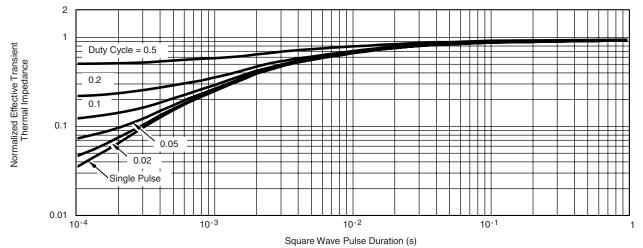


Safe Operating Area, Junction-to-Ambient





## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?72282">www.vishay.com/ppg?72282</a>.



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Vishay

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