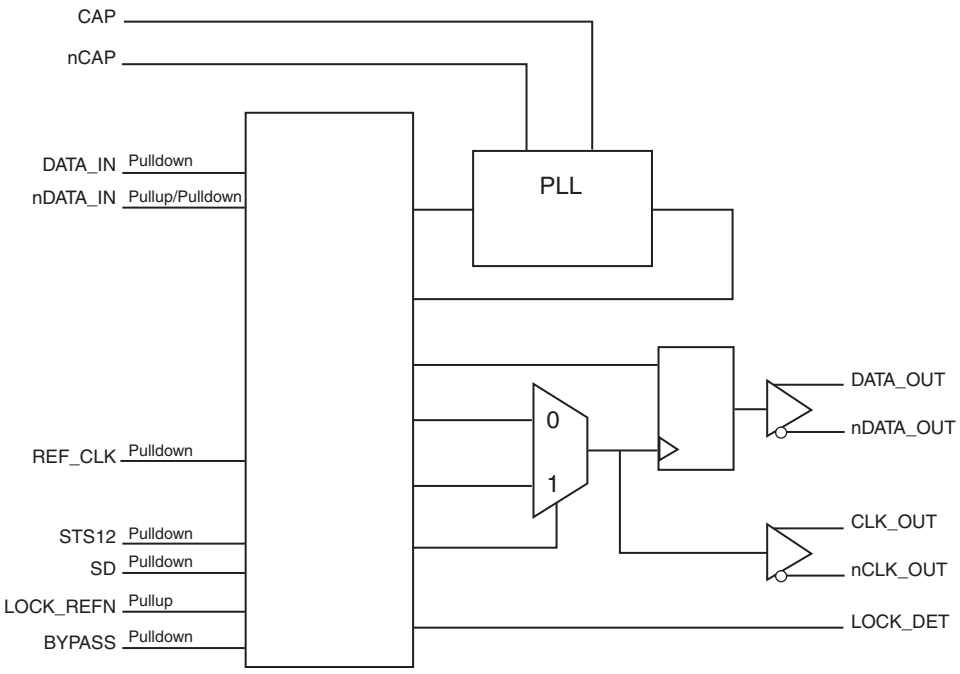
General Description

The 894D115I-04 is a clock and data recovery circuit. The device is designed to extract the clock signal from a NRZ-coded STM-4 (OC-12/STS-12) or STM-1 (OC-3/STS-3) input data signal. The output signals of the device are the recovered clock and retimed data signals. Input and output are differential signals for best signal integrity and to support high clock and data rates. All control inputs and outputs are single-ended signals. An internal PLL is used for clock generation and recovery. An external clock input is provided to establish an initial operating frequency of the clock recovery PLL and to provide a clock reference in the absence of serial input data. The device supports a signal detect input and a lock detect output. A bypass circuit is provided to facilitate factory tests.

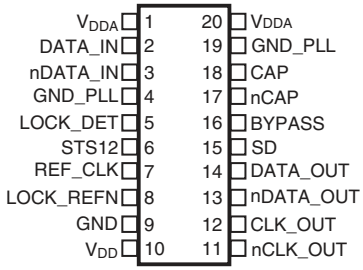
Features

- Clock recovery for STM-4 (OC-12/STS-12) and STM-1 (OC-3/STS-3)
- Input: NRZ data (622.08 or 155.52 Mbit/s)
- Output: clock signal (622.08MHz or 155.52MHz) and retimed data signal at 622.08 or 155.52 Mbit/s
- Internal PLL for clock generation and clock recovery
- Differential inputs can accept LVPECL levels
- Differential LVDS data and clock outputs
- Lock reference input and PLL lock output
- 19.44MHz reference clock input
- Full 3.3V supply mode
- -40°C to 85°C operating temperature
- Available in lead-free (RoHS 6) package
- See 894D115I for a clock/data recovery circuit with a TSSOP EPAD package and LVPECL outputs
- See 894D115I-01 for a clock/data recovery circuit with LVPECL outputs

Block Diagram



Pin Assignment



894D115I-04

20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm package body
G Package
Top View

Functional Description

The 894D115I-04 is designed to extract the clock from a NRZ-coded STM-4 (OC-12/STS-12) or STM-1 (OC-3/STS-3) input data signals. The output signals are the recovered clock and retimed data signals. The device contains an integrated PLL for clock generation and to lock the output clock to the input data stream. The PLL attempts to lock to the reference clock input (REF_CLK) in absence of the serial data stream or if it is forced to by the control inputs LOCK_REFN or SD. The output clock frequency is controlled by the STS12 input. The output frequency is 622.08MHz in STM-4/OC-12/STS-12 mode and 155.52MHz in STM-1/OC-3/STS-3 mode.

The 894D115I-04 will maintain an output (CLK_OUT/ nCLK_OUT) frequency deviation of less than ±500ppm with respect to the REF_CLK reference frequency in a loss of signal state (LOS). During the LOS state, the data outputs (DATA_OUT/ nDATA_OUT) are held at logic low state. An LOS state of the 894D115I-04 is given when BYPASS is set to the logic low state and either one of the SD or LOCK_REFN inputs are at a logic low state.

This will enable the use of the SD (signal detect) and the LOCK_REFN (lock-to-reference) inputs to accept loss of signal status information from electro-optical receivers. Please refer to *Figure 1, "Signal Detect/PLL Bypass Operation Control Diagram"*, for details.

The lock detect output (LOCK_DET) can be used to monitor the operating state of the clock/data recovery circuit. LOCK_DET is set to logic low level when the internal oscillator of the PLL and the reference clock (REF_CLK) deviate from each other by more than 500ppm, or when the CDR is forced to lock the REF_CLK input by the LOCK_REFN or SD control input. LOCK_DET is set to high when the PLL is locked to the input data stream and indicates valid clock and data output signals.

The BYPASS pin should be set to logic low state in all applications. BYPASS set to logic high state is used during factory test. In BYPASS mode (BYPASS and STS12 are at logic high state), the internal PLL is bypassed and the inverted REF_CLK input signal is output at CLK_OUT/nCLK_OUT.

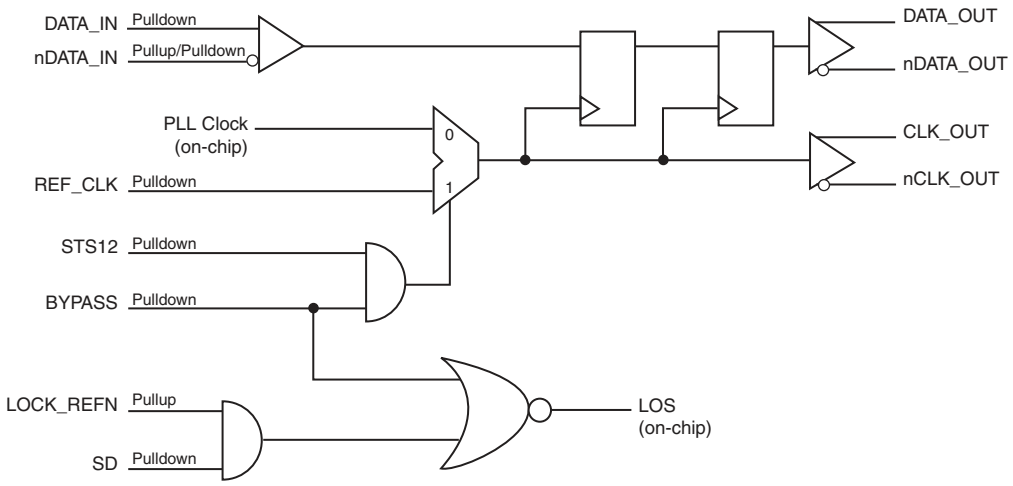


Figure 1. Signal Detect/PLL BYPASS Operation Control Diagram

Table 1. Signal Detect/PLL BYPASS Operation Control Table

Inputs				Outputs	
STS12	**BYPASS**	**LOCK_REFN**	**SD**	**DATA_OUT**	**CLK_OUT**
1	0	1	1	DATA_IN	PLL Clock
1	0	1	0	LOW	PLL Clock
1	0	0	1	LOW	PLL Clock
1	0	0	0	LOW	PLL Clock
1	1	X	X	DATA_IN	REF_CLK
0	0	1	1	DATA_IN	PLL Clock
0	0	1	0	LOW	PLL Clock
0	0	0	1	LOW	PLL Clock
0	0	0	0	LOW	PLL Clock
0	1	X	X	Not Allowed	Not Allowed

Table 2. Pin Descriptions

Number	Name	Type		Description
1, 20	V_{DDA}	Power		Analog supply pins.
2	DATA_IN	Input	Pulldown	Non-inverting differential signal input.
3	nDATA_IN	Input	Pullup/ Pulldown	Inverting differential signal input. $V_{DD}/2$ default when left floating.
4, 19	GND_PLL	Power		Power supply ground.
5	LOCK_DT	Output		Lock detect output. See Table 4A. Single-ended LVPECL interface levels.
6	STS12	Input	Pulldown	STM-4 (OC-12, STS-12) or STM-1 (OC-3, STS-3) selection mode. See Table 4B. LVCMOS/LVTTL interface levels.
7	REF_CLK	Input	Pulldown	Reference clock input of 19.44MHz. LVCMOS/LVTTL interface levels.
8	LOCK_REFN	Input	Pullup	Lock to REF_CLK input. See Table 4C. LVCMOS/LVTTL interface levels.
9	GND	Power		Power supply ground.
10	V_{DD}	Power		Core supply pin.
11, 12	nCLK_OUT, CLK_OUT	Output		Differential clock output pair. LVDS interface levels.
13, 14	nDATA_OUT, DATA_OUT	Output		Differential clock output pair. LVDS interface levels.
15	SD	Input	Pulldown	Signal detect input. Typically, SD is driven by the signal detect output of the electro-optical module. See Table 4D. Single-ended LVPECL interface levels.
16	BYPASS	Input	Pulldown	PLL bypass mode. See Table 4E. LVCMOS/LVTTL interface levels.
17, 18	nCAP, CAP	Input		External loop filter (1.0µF ±10%).

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 3, *Pin Characteristics,* for typical values.

Table 3. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 4A. LOCK_DET Operation Table

Operation	Output
	LOCK_DET
The PLL is not locked to the serial input data stream if any of these three conditions occur: A. Internal oscillator and REF_CLK input frequency are not within 500ppm of each other. B. SD input is at logic LOW state. C. LOCK_REFN is at logic LOW state.	LOW
When the PLL is locked to the serial input data stream, the CLK_OUT and DATA_OUT signals are valid.	HIGH

Table 4B. STS12 Mode Configuration Table

Input	
STS12	Operation
0	STM-1 (OC-3, STS-3) operation. The clock/data recovery circuit attempts to recover the clock from a 155.52 Mbit/s input data stream. The output clock frequency is 155.52MHz.
1	STM-4 (OC-12, STS-12) operation. The clock/data recovery circuit attempts to recover the clock from a 622.08 Mbit/s input data stream. The output clock frequency is 622.08MHz.

Table 4C. LOCK_REFN Mode Configuration Table

Input	
LOCK_REFN	Operation
0	Lock to reference clock. CLK_OUT/nCLK_OUT output frequency is within ±500ppm of the reference clock (REF_CLK). DATA_OUT is set to logic LOW state and nDATA_OUT is set to logic HIGH state. (DATA_OUT = L, nDATA_OUT = H).
1	Normal operation.

Table 4D. SD Mode Configuration Table

Input	
SD	Operation
0	Indicates a loss-of-signal (LOS) condition to the device. CLK_OUT/nCLK_OUT output frequency is within ±500ppm of the reference clock (REF_CLK). DATA_OUT is set to logic LOW state and nDATA_OUT is set to logic HIGH state. (DATA_OUT = L, nDATA_OUT = H).
1	Normal operation.

Table 4E. BYPASS Mode Configuration Table

Input	
BYPASS	**Operation**
0	Normal operation.
1	PLL bypassed (for factory test). The inverted REF_CLK input signal is output at CLK_OUT/nCLK_OUT.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuos Current Surge Current Outputs, I_O (LVPECL) Continuous Current Surge Current	 10mA 15mA 50mA 100mA
Package Thermal Impedance, θ_{JA}	81.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 5A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
I_{DD}	Power Supply Current				112	mA
I_{DDA}	Analog Supply Current				10	mA

Table 5B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	REF_CLK, STS12, BYPASS	$V_{DD} = V_{IN} = 3.465V$			150	µA
		LOCK_REFN	$V_{DD} = V_{IN} = 3.465V$			10	µA
I_{IL}	Input Low Current	REF_CLK, STS12, BYPASS	$V_{DD} = 3.465V, V_{IN} = 0V$	-10			µA
		LOCK_REFN	$V_{DD} = 3.465V, V_{IN} = 0V$	-150			µA

Table 5C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	DATA_IN/nDATA_IN	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	DATA_IN	$V_{DD} = 3.465V, V_{IN} = 0V$	-10			µA
		nDATA_IN	$V_{DD} = 3.465V, V_{IN} = 0V$	-150			µA
V_{IH}	Input High Voltage			$V_{DD} – 1.75$		$V_{DD} – 0.4$	V
V_{IL}	Input Low Voltage			$V_{DD} – 2.0$		$V_{DD} – 0.7$	V
ΔV_{IN}	Differential Input Voltage			250			mV

Table 5D. LVPECL DC Characteristics, V_{DD} = 3.3V ± 5%, T = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SD		$V_{DD} – 1.125$			V
V_{IL}	Input Low Voltage	SD				$V_{DD} – 1.5$	V
I_{IH}	Input High Current	SD	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	SD	$V_{DD} = 3.465V, V_{IN} = 0V$	-10			µA
V_{OH}	Output High Voltage; NOTE 1	LOCK_DT		$V_{DD} – 1.4$		$V_{DD} – 0.9$	V
V_{OL}	Output Low Voltage NOTE 1	LOCK_DT		$V_{DD} – 2.0$		$V_{DD} – 1.7$	V

NOTE 1: Outputs terminated with 50Ω to V_{DD} – 2V.

Table 5E. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	380	454	mV
ΔV_{OD}	V_{OD} Magnitude Change			5	50	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change			5	50	mV

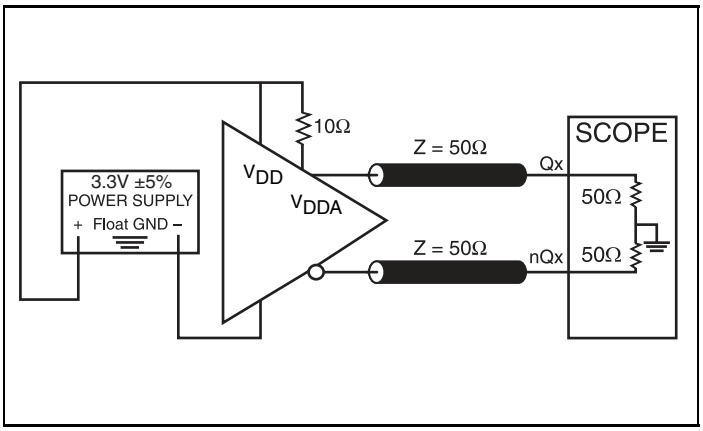
AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{EE} = 0V, T = -40°C to 85°C

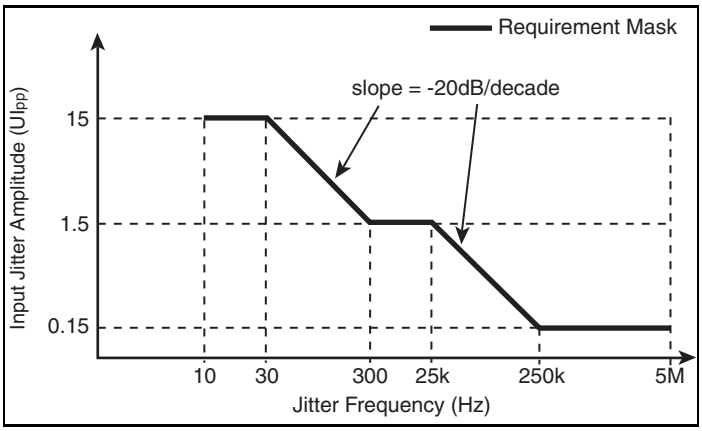
Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Center Frequency				622.08		MHz
f_{TOL}	CRU's Reference Clock Frequency Tolerance			-250		250	ppm
fT_{REF_CLK}	OC-12/STS-12 Capture Range		With respect to the fixed reference frequency		±500		ppm
t_{LOCK}	Acquisition Lock Time	OC-12/STS-12	Valid REF_CLK and device already powered-up			16	µs
J_{GEN_CLK}	Jitter Generation	CLK_OUT/ nCLK_OUT	14ps rms (max.) jitter on DATA_IN/nDATA_IN		0.005	0.01	UI
J_{TOL}	Jitter Tolerance	OC-12/STS-12; NOTE 1	Sinusoidal input jitter of DATA_IN/ nDATA_IN from 250kHz to 5MHz	0.45			UI
t_R / t_F	Output Rise/Fall Time; NOTE 1		20% to 80%			500	ps
odc	Output Duty Cycle; NOTE 1		20% minimum transition density	45		55	%
t_S	Setup Time; NOTE 1		STS-3	2000	3220		ps
			STS-12	450	800		ps
t_H	Hold Time; NOTE 1		STS-3	3000	3220		ps
			STS-12	650	800		ps

NOTE 1: See diagram in *Parameter Measurement Information* section.

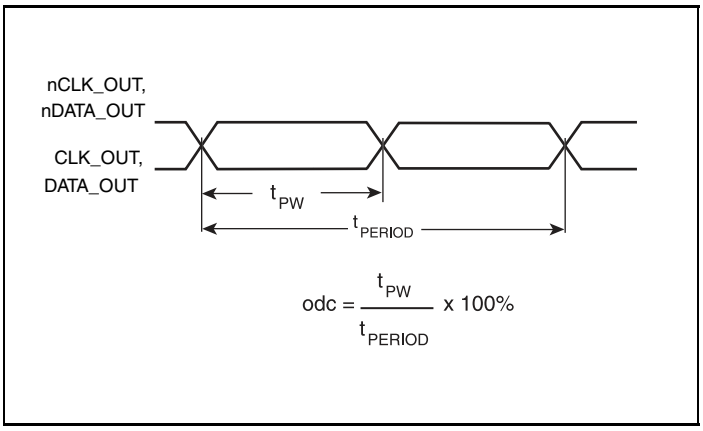
Parameter Measurement Information



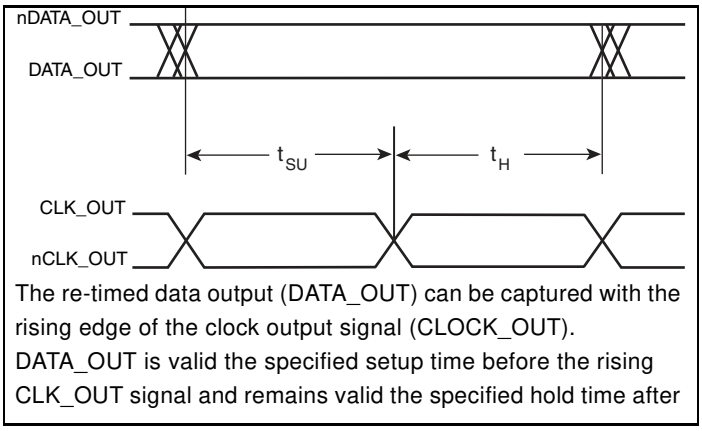
LVDS 3.3V Output Load AC Test Circuit



Jitter Tolerance Specification

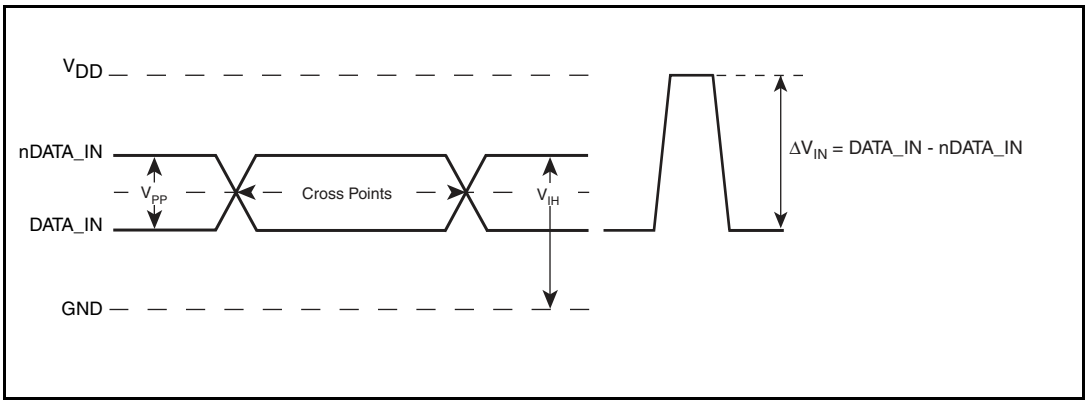


Output Duty Cycle/Pulse Width/Period



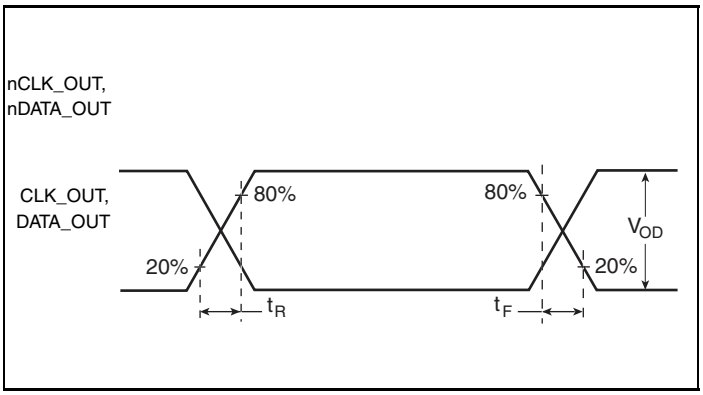
The re-timed data output (DATA_OUT) can be captured with the rising edge of the clock output signal (CLOCK_OUT). DATA_OUT is valid the specified setup time before the rising CLK_OUT signal and remains valid the specified hold time after

Setup/Hold Time

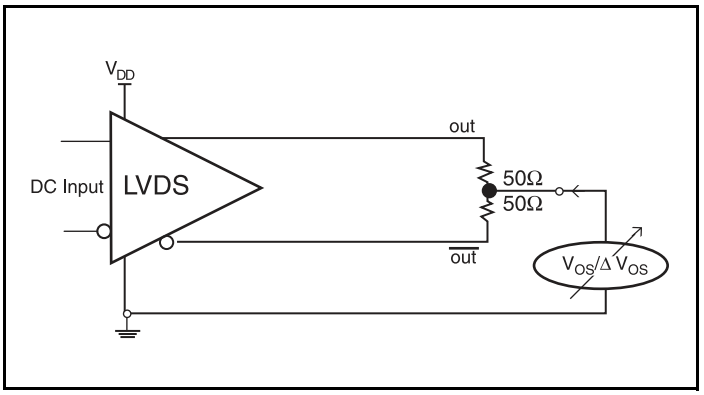


Differential Input Level

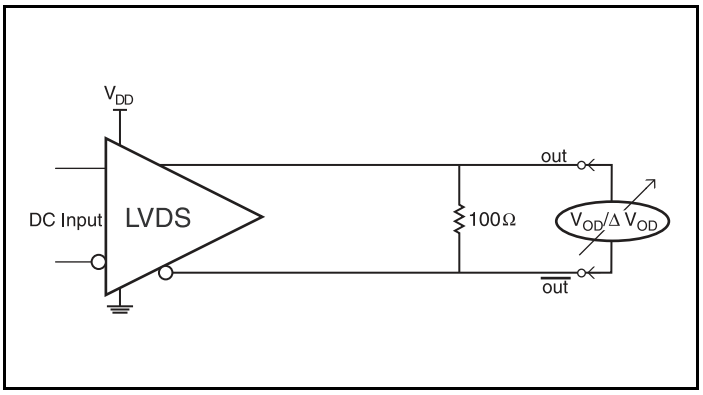
Parameter Measurement Information, continued



Output Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 894D115I-04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

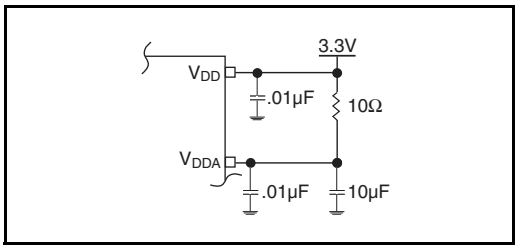


Figure 2. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

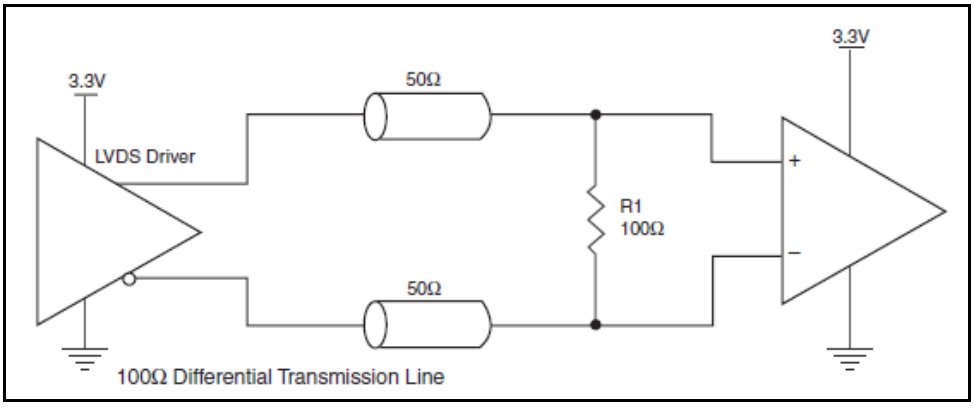


Figure 3. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 894D115I-04. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 894D115I-04 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

Core and LVDS Output Power Dissipation

- Power (core, LVDS)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.4655V * (92mA + 10mA) = **353.43mW**

Single-ended LVPECL Output Power Dissipation

- Power (LVPECL outputs)$_{MAX}$ = **19.8mW (for logic high)**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 353.43mW + 19.8mW = **373.23mW**

2. Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

Lower temperature refers to ambient temperature, maximum temperature refers to case temperature.

Table 7. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.3°C/W	76.9°C/W	74.8°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.3°C/W	76.9°C/W	74.8°C/W

Transistor Count

The transistor count for 894D115I-04 is: 10,557

Compatible with VSC8115

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

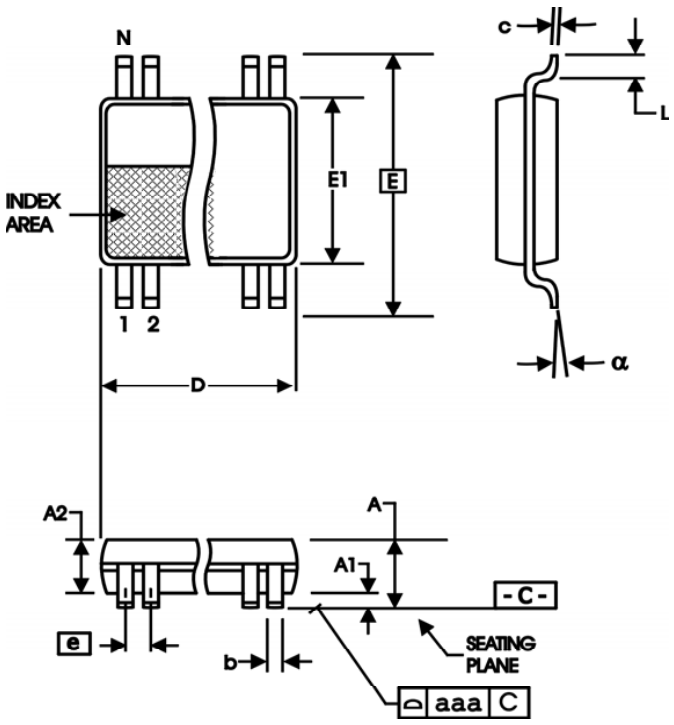


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
894D115AGI-04LF	ICSD115AI04L	“Lead-Free” 20 Lead TSSOP	Tube	-40°C to 85°C
894D115AGI-04LFT	ICSD115AI04L	“Lead-Free” 20 Lead TSSOP	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T6	7	AC Characteristics Table - corrected typo for Hold Time, STS-3 spec. from 300ps to 3000ps max.	6/24/08
C	T5C	6 8	Differential DC Characteristics Table - deleted V_{PP} and V_{CMR} specs and added V_{IH}, V_{IL}, ΔV_{IN} specs. Parameter Measurement Information Section - updated Differential Input Level diagram.	10/15/08
C	T10	1 13	Removed ICS from part numbers where needed. General Description - Deleted ICS chip. Ordering Information - Deleted quantity from tape and reel. Deleted LF note below table. Updated header and footer.	1/27/16

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