

TPA311 350-mW MONO AUDIO POWER AMPLIFIER

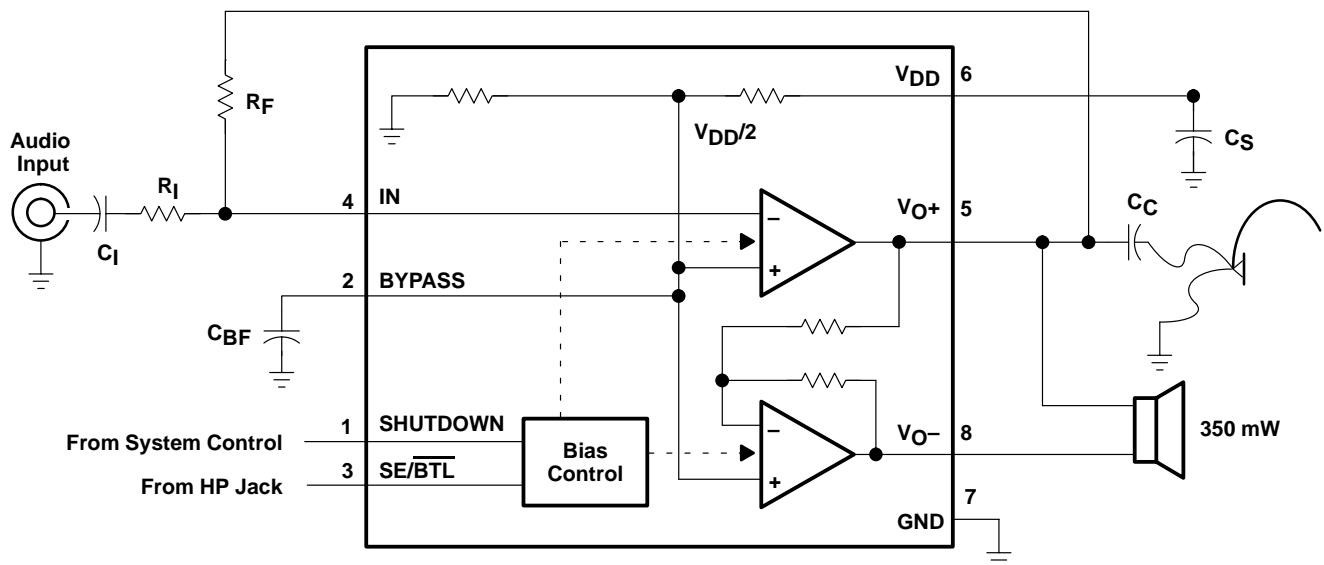
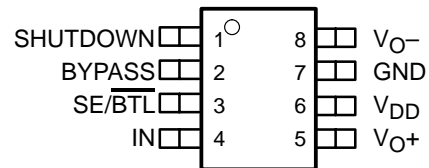
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- Fully Specified for 3.3-V and 5-V Operation
- Wide Power Supply Compatibility
2.5 V – 5.5 V
- Output Power for $R_L = 8 \Omega$
 - 350 mW at $V_{DD} = 5 \text{ V}$, BTL
 - 250 mW at $V_{DD} = 5 \text{ V}$, SE
 - 250 mW at $V_{DD} = 3.3 \text{ V}$, BTL
 - 75 mW at $V_{DD} = 3.3 \text{ V}$, SE
- Shutdown Control
 - $I_{DD} = 7 \mu\text{A}$ at 3.3 V
 - $I_{DD} = 60 \mu\text{A}$ at 5 V
- BTL to SE Mode Control
- Integrated Depop Circuitry
- Thermal and Short-Circuit Protection
- Surface Mount Packaging
 - SOIC
 - PowerPAD™ MSOP

description

The TPA311 is a bridge-tied load (BTL) or single-ended (SE) audio power amplifier developed especially for low-voltage applications where internal speakers and external earphone operation are required. Operating with a 3.3-V supply, the TPA311 can deliver 250-mW of continuous power into a BTL 8- Ω load at less than 1% THD+N throughout voice band frequencies. Although this device is characterized out to 20 kHz, its operation was optimized for narrower band applications such as cellular communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. A unique feature of the TPA311 is that it allows the amplifier to switch from BTL to SE *on the fly* when an earphone drive is required. This eliminates complicated mechanical switching or auxiliary devices just to drive the external load. This device features a shutdown mode for power-sensitive applications with special depop circuitry to virtually eliminate speaker noise when exiting shutdown mode and during power cycling. The TPA311 is available in an 8-pin SOIC surface-mount package and the surface-mount PowerPAD MSOP, which reduces board space by 50% and height by 40%.

D OR DGN PACKAGE
(TOP VIEW)



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PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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AVAILABLE OPTIONS

T _A	PACKAGED DEVICES		MSOP Symbolization
	SMALL OUTLINE† (D)	MSOPT (DGN)	
–40°C to 85°C	TPA311D	TPA311DGN	AAB

† The D and DGN packages are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA311DR).

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BYPASS	2	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-μF to 1-μF capacitor when used as an audio amplifier.
GND	7		GND is the ground connection.
IN	4	I	IN is the audio input terminal.
SE/BTL	3	I	When SE/BTL is held low, the TPA311 is in BTL mode. When SE/BTL is held high, the TPA311 is in SE mode.
SHUTDOWN	1	I	SHUTDOWN places the entire device in shutdown mode when held high (I _{DD} = 60 μA, V _{DD} = 5 V).
V _{DD}	6		V _{DD} is the supply voltage terminal.
V _{O+}	5	O	V _{O+} is the positive output for BTL and SE modes.
V _{O-}	8	O	V _{O-} is the negative output in BTL mode and a high-impedance output in SE mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{DD}	6 V
Input voltage, V _I	–0.3 V to V _{DD} + 0.3 V
Continuous total power dissipation	internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T _A (see Table 3)	–40°C to 85°C
Operating junction temperature range, T _J	–40°C to 150°C
Storage temperature range, T _{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C	DERATING FACTOR	T _A = 70°C	T _A = 85°C
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W§	17.1 mW/°C	1.37 W	1.11 W

§ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.



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recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2.5	5.5	V
High-level voltage, V_{IH}	SHUTDOWN	$0.9 V_{DD}$		V
	$\overline{SE/BTL}$	$0.9 V_{DD}$		
Low-level voltage, V_{IL}	SHUTDOWN	$0.1 V_{DD}$		V
	$\overline{SE/BTL}$	$0.1 V_{DD}$		
Operating free-air temperature, T_A (see Table 3)		-40	85	°C

electrical characteristics at specified free-air temperature, $V_{DD} = 3.3$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$ V_{OO} $	Output offset voltage (measured differentially)	SHUTDOWN = 0 V, $\overline{SE/BTL} = 0$ V, $R_L = 8 \Omega$, $R_F = 10$ k Ω			5	20	mV
PSRR	Power supply rejection ratio	$V_{DD} = 3.2$ V to 3.4 V	BTL mode		85		dB
			SE mode		83		
I_{DD}	Supply current (see Figure 6)	SHUTDOWN = 0 V, $\overline{SE/BTL} = 0.33$ V, $R_F = 10$ k Ω	BTL mode		0.7	1.5	mA
			SE mode		0.35	0.75	
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 7)	SHUTDOWN = V_{DD} , $\overline{SE/BTL} = 0$ V, $R_F = 10$ k Ω			7	50	μA
$ I_{IH} $	High-level input current	SHUTDOWN, $V_{DD} = 3.3$ V, $V_I = V_{DD}$				1	μA
		$\overline{SE/BTL}$, $V_{DD} = 3.3$ V, $V_I = V_{DD}$				1	
$ I_{IL} $	Low-level input current	SHUTDOWN, $V_{DD} = 3.3$ V, $V_I = 0$ V				1	μA
		$\overline{SE/BTL}$, $V_{DD} = 3.3$ V, $V_I = 0$ V				1	

operating characteristics, $V_{DD} = 3.3$ V, $T_A = 25^\circ\text{C}$, $R_L = 8 \Omega$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 0.5%,	BTL mode, See Figure 14		250		mW
		THD = 0.5%,	SE mode		110		
THD + N	Total harmonic distortion plus noise	$P_O = 250$ mW, $f = 20$ Hz to 4 kHz, $A_V = -2$ V/V, See Figure 12			1.3%		
B_{OM}	Maximum output power bandwidth	$A_V = -2$ V/V, THD = 3%, See Figure 12			10		kHz
B_1	Unity-gain bandwidth	Open loop, See Figure 36			1.4		MHz
	Supply ripple rejection ratio	$f = 1$ kHz, See Figure 5	$C_B = 1 \mu\text{F}$, BTL mode,		71		dB
		$f = 1$ kHz, See Figure 3	$C_B = 1 \mu\text{F}$, SE mode,		86		
V_n	Noise output voltage	$A_V = -1$ V/V, BTL,	$C_B = 0.1 \mu\text{F}$, See Figure 42	$R_L = 32 \Omega$,		15	$\mu\text{V(rms)}$

NOTE 1: Output power is measured at the output terminals of the device at $f = 1$ kHz.



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OO} $	Output offset voltage (measured differentially)	SHUTDOWN = 0 V, SE/BTL = 0 V, $R_L = 8\ \Omega$, $R_F = 10\ \text{k}\Omega$		5	20	mV
PSRR	Power supply rejection ratio	$V_{DD} = 4.9\text{ V to } 5.1\text{ V}$	BTL mode	78		dB
			SE mode	76		
I_{DD}	Supply current (see Figure 6)	SHUTDOWN = 0 V, SE/BTL = 0.5 V, $R_F = 10\ \text{k}\Omega$	BTL mode	0.7	1.5	mA
		SHUTDOWN = 0 V, SE/BTL = 4.5 V, $R_F = 10\ \Omega$	SE mode	0.35	0.75	
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 7)	SHUTDOWN = V_{DD} , SE/BTL = 0 V, $R_F = 10\ \text{k}\Omega$		60	100	μA
$ I_{IH} $	High-level input current	SHUTDOWN, $V_{DD} = 5.5\text{ V}$, $V_I = V_{DD}$			1	μA
		SE/BTL, $V_{DD} = 5.5\text{ V}$, $V_I = V_{DD}$			1	
$ I_{IL} $	Low-level input current	SHUTDOWN, $V_{DD} = 5.5\text{ V}$, $V_I = 0\text{ V}$			1	μA
		SE/BTL, $V_{DD} = 5.5\text{ V}$, $V_I = 0\text{ V}$			1	

operating characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 8\ \Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power, see Note 2	THD = 0.5%, BTL mode, See Figure 18		700		mW
		THD = 0.5%, SE mode		300		
THD + N	Total harmonic distortion plus noise	$P_O = 350\text{ mW}$, $f = 20\text{ Hz to } 4\text{ kHz}$, $A_V = -2\text{ V/V}$, See Figure 16		1%		
B _{OM}	Maximum output power bandwidth	$A_V = -2\text{ V/V}$, THD = 2%, See Figure 16		10		kHz
B ₁	Unity-gain bandwidth	Open loop, See Figure 37		1.4		MHz
	Supply ripple rejection ratio	$f = 1\text{ kHz}$, $C_B = 1\ \mu\text{F}$, BTL mode, See Figure 5		65		dB
		$f = 1\text{ kHz}$, $C_B = 1\ \mu\text{F}$, SE mode, See Figure 4		75		
V_n	Noise output voltage	$A_V = -1\text{ V/V}$, BTL, $C_B = 0.1\ \mu\text{F}$, See Figure 43, $R_L = 32\ \Omega$		15		$\mu\text{V(rms)}$

NOTE 2: Output power is measured at the output terminals of the device at $f = 1\text{ kHz}$.



PARAMETER MEASUREMENT INFORMATION

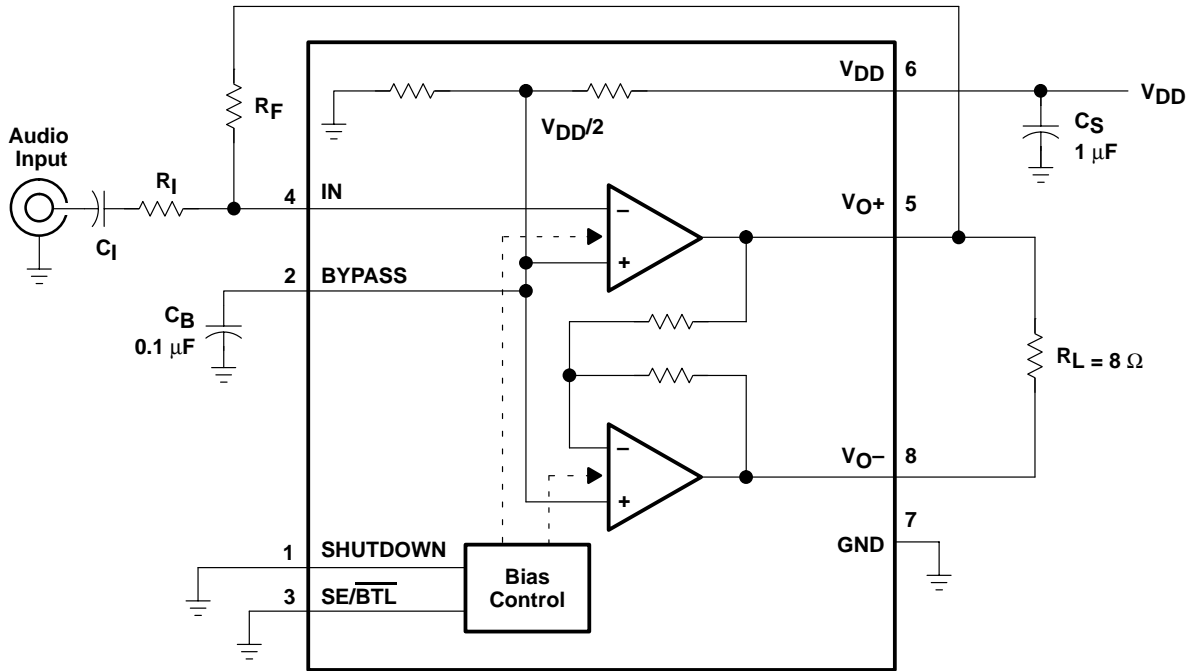


Figure 1. BTL Mode Test Circuit

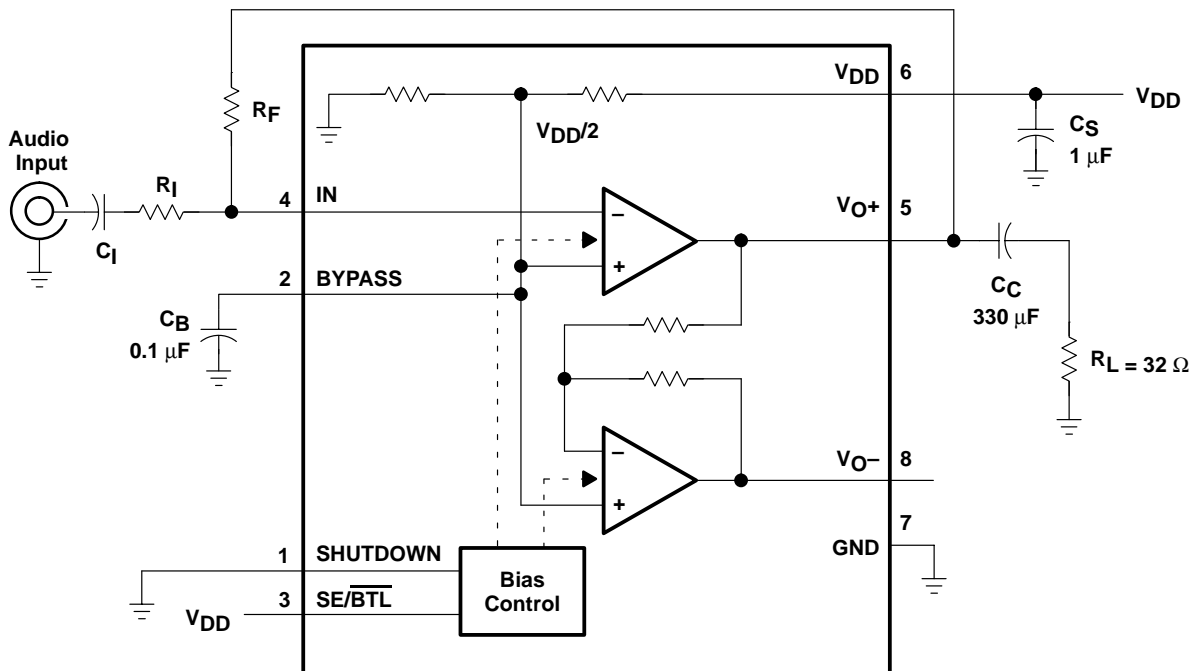


Figure 2. SE Mode Test Circuit

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TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Supply voltage rejection ratio	vs Frequency	3, 4, 5
I_{DD} Supply current	vs Supply voltage	6, 7
P_O Output power	vs Supply voltage	8, 9
	vs Load resistance	10, 11
THD+N Total harmonic distortion plus noise	vs Frequency	12, 13, 16, 17, 20, 21, 24, 25, 28, 29, 32, 33
	vs Output power	14, 15, 18, 19, 22, 23, 26, 27, 30, 31, 34, 35
Open loop gain and phase	vs Frequency	36, 37
Closed loop gain and phase	vs Frequency	38, 39, 40, 41
V_n Output noise voltage	vs Frequency	42, 43
P_D Power dissipation	vs Output power	44, 45, 46, 47

SUPPLY VOLTAGE REJECTION RATIO
VS
FREQUENCY

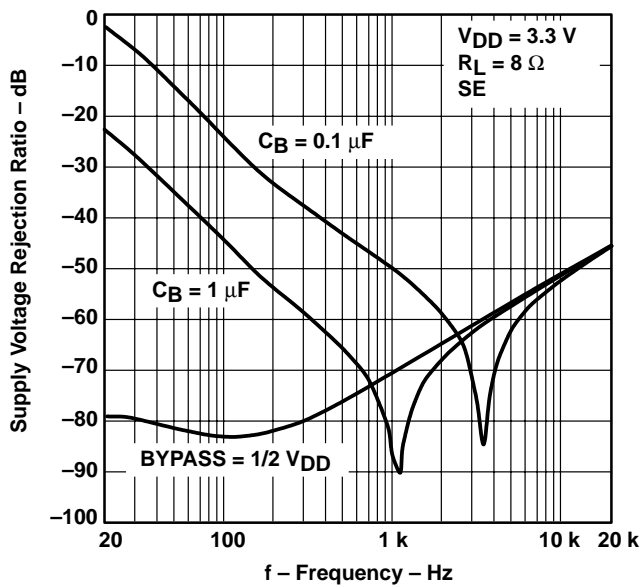


Figure 3

SUPPLY VOLTAGE REJECTION RATIO
VS
FREQUENCY

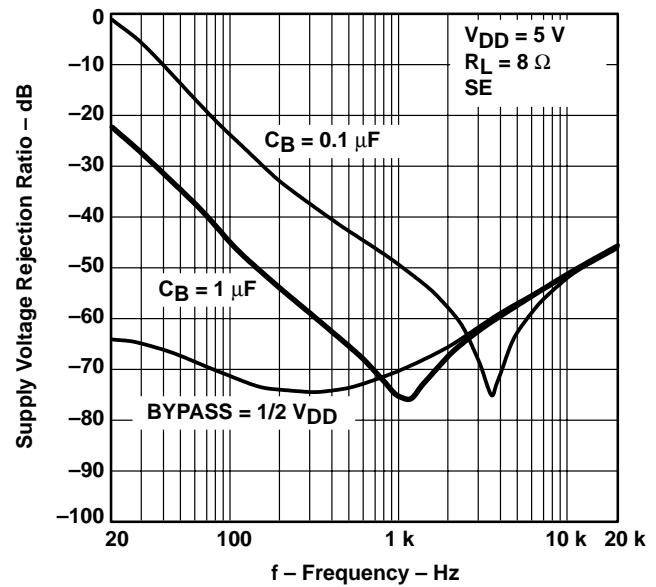


Figure 4



TYPICAL CHARACTERISTICS

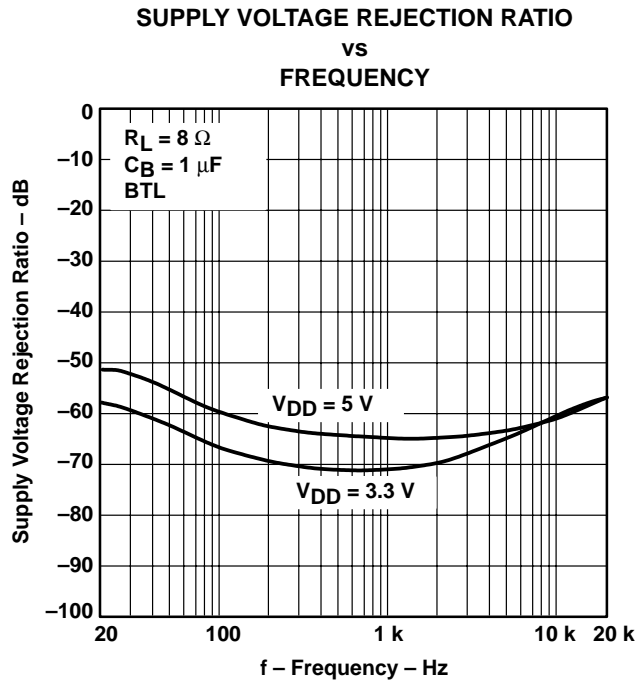


Figure 5

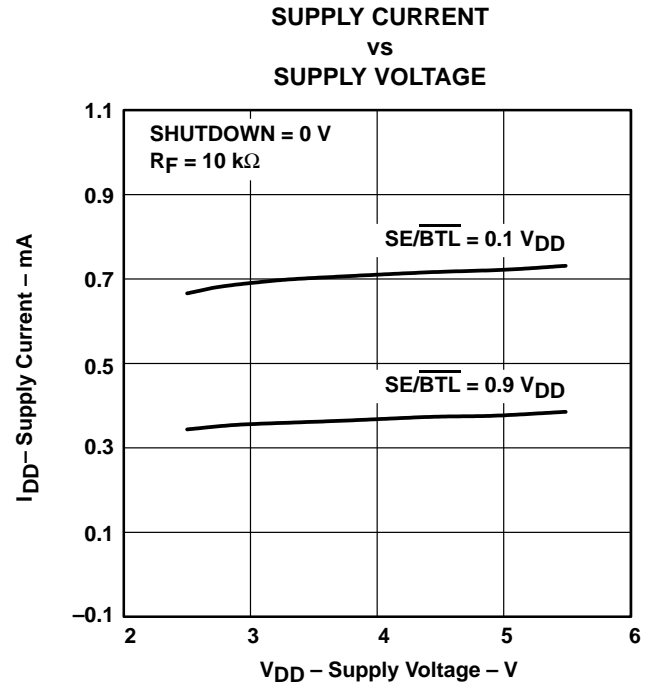


Figure 6

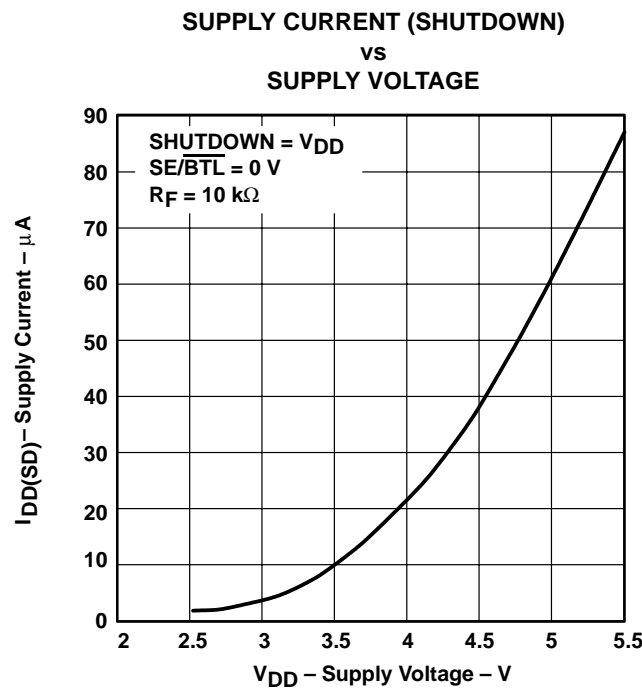


Figure 7

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TYPICAL CHARACTERISTICS

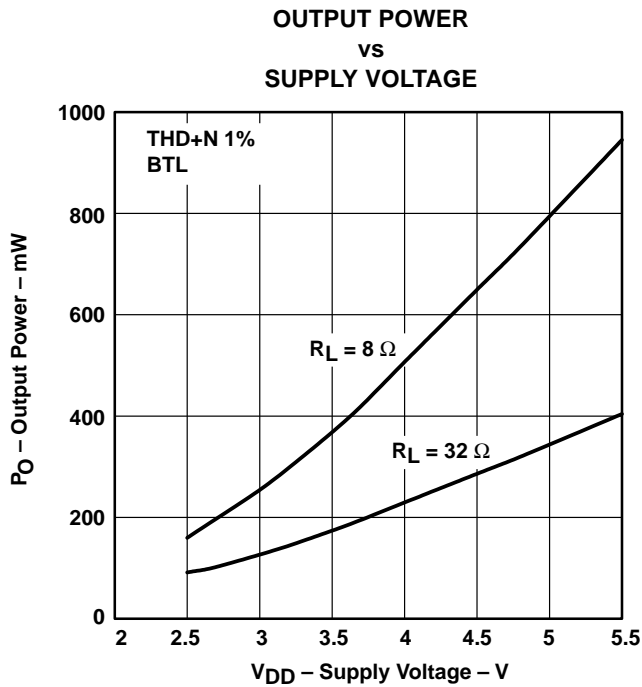


Figure 8

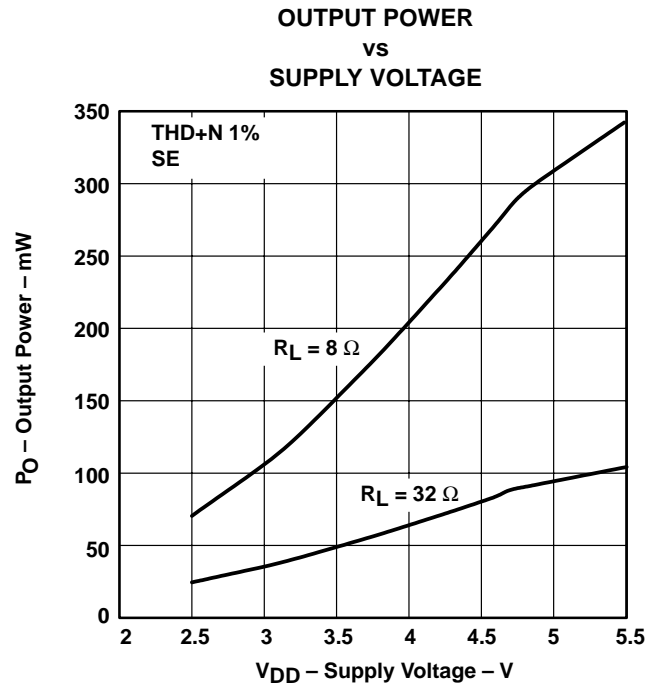


Figure 9

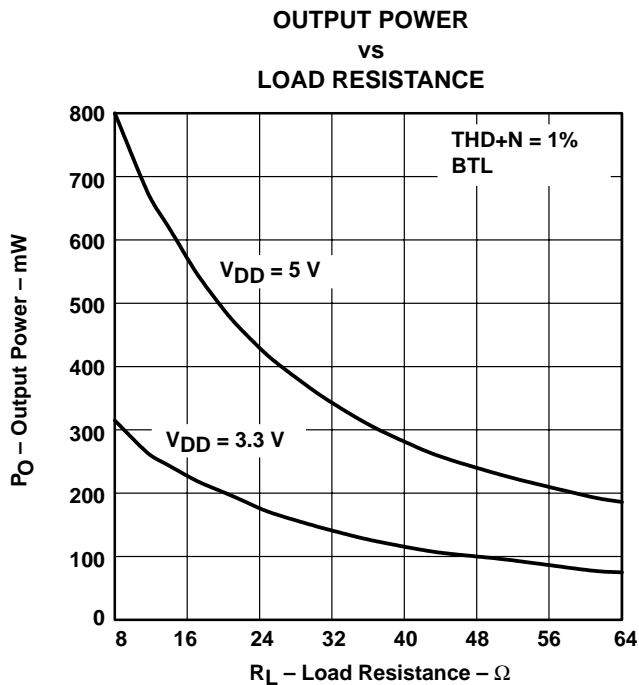


Figure 10

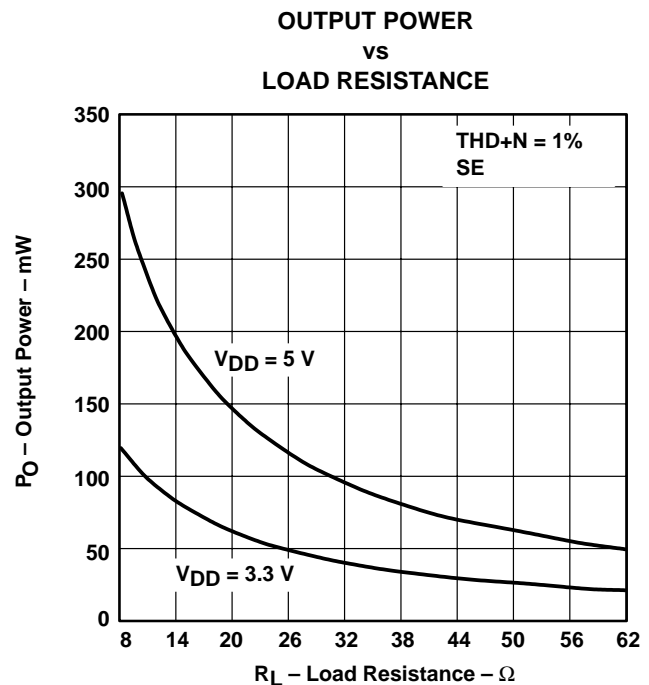


Figure 11



TYPICAL CHARACTERISTICS

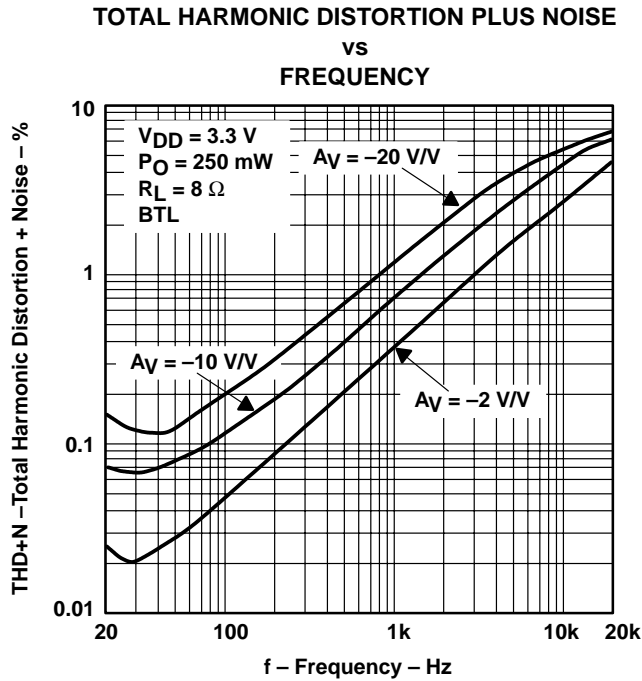


Figure 12

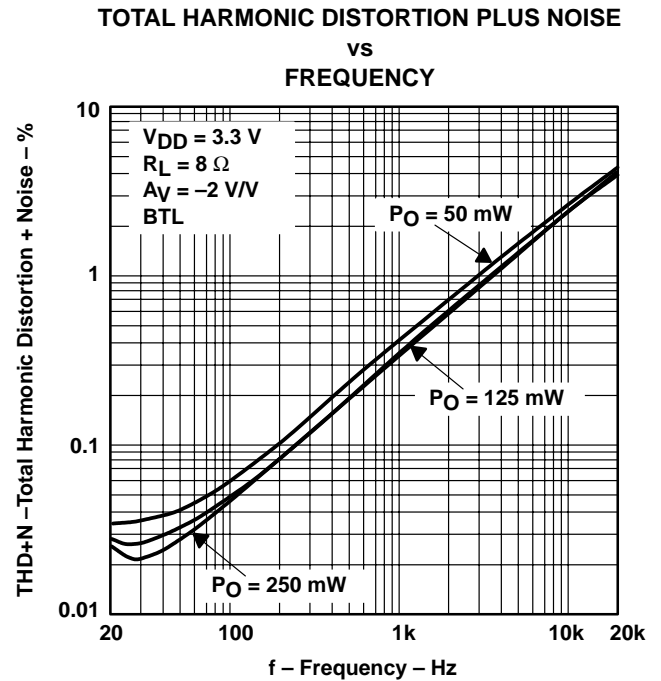


Figure 13

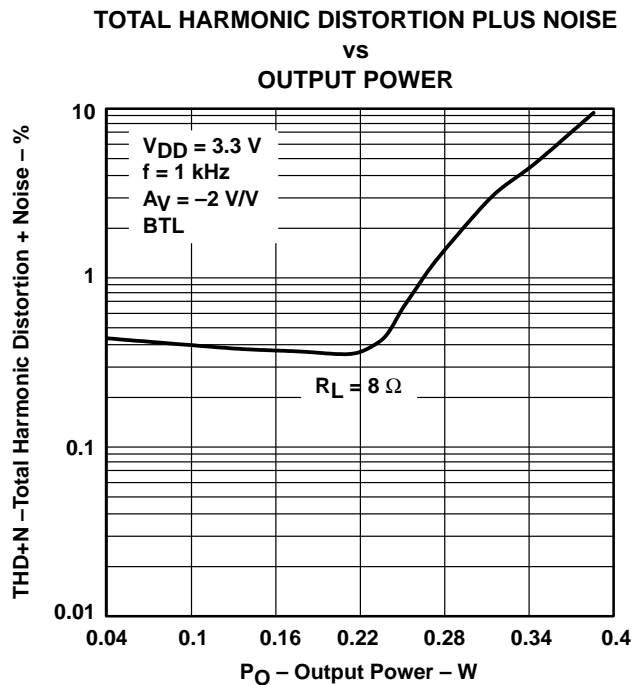


Figure 14

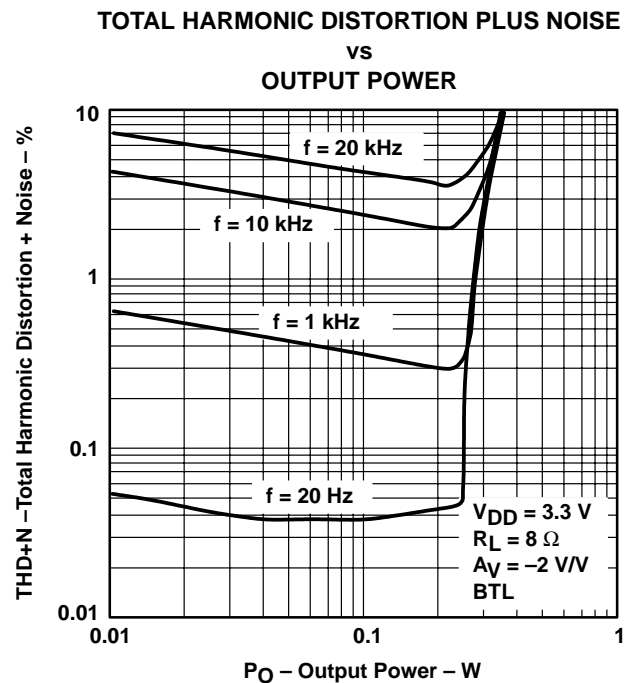


Figure 15

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TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
VS
FREQUENCY

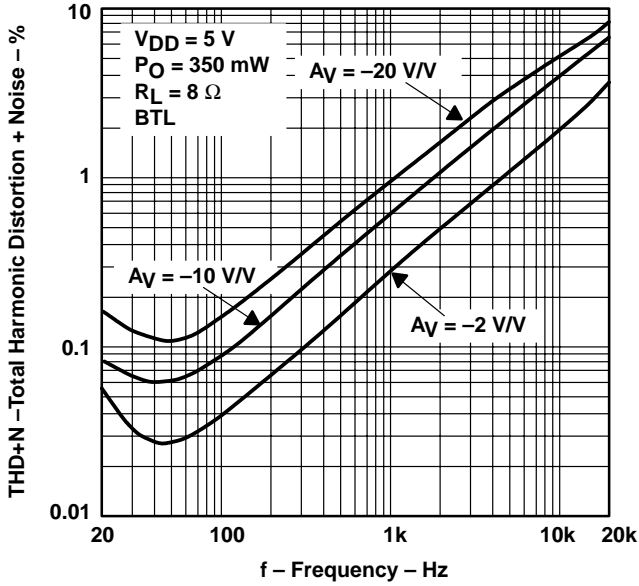


Figure 16

TOTAL HARMONIC DISTORTION PLUS NOISE
VS
FREQUENCY

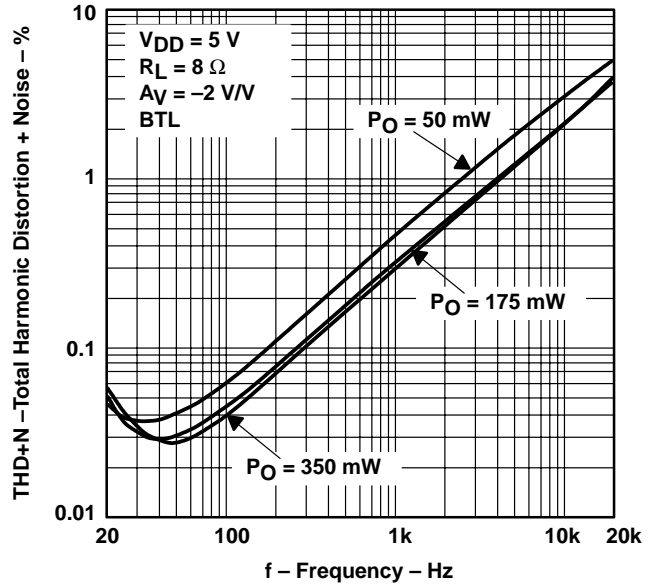


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
VS
OUTPUT POWER

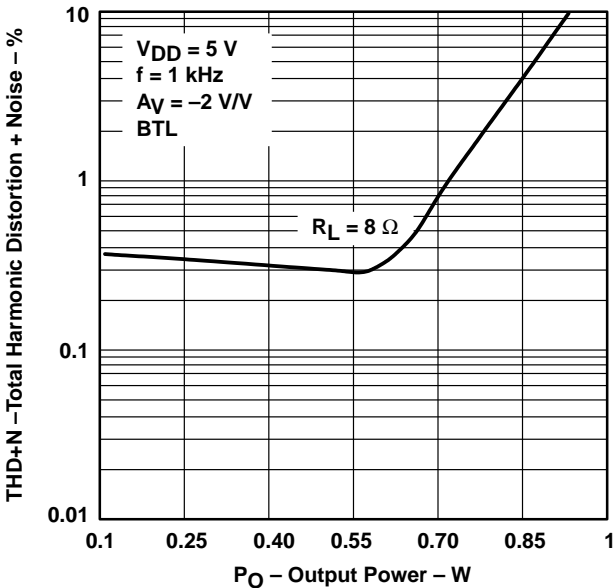


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
VS
OUTPUT POWER

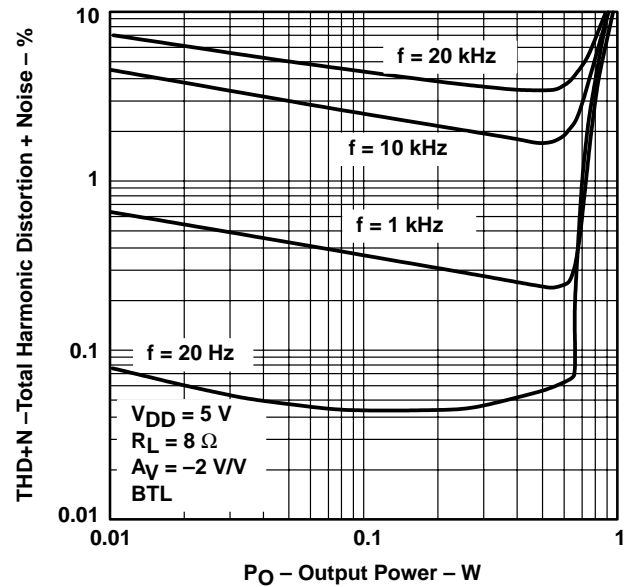


Figure 19



TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

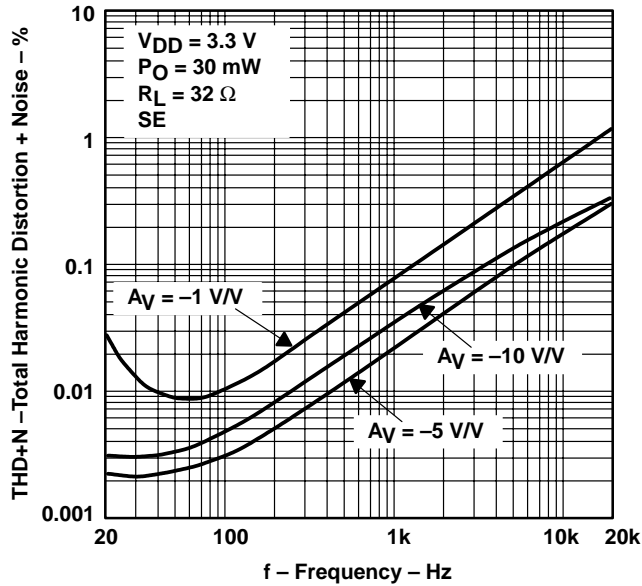


Figure 20

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

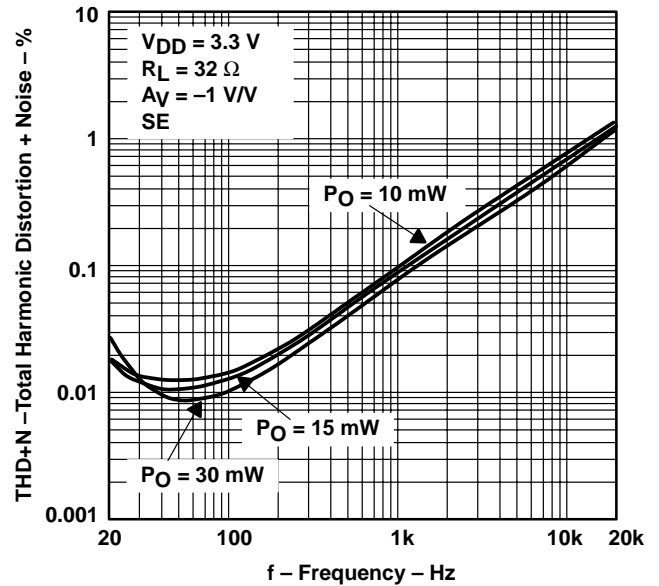


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

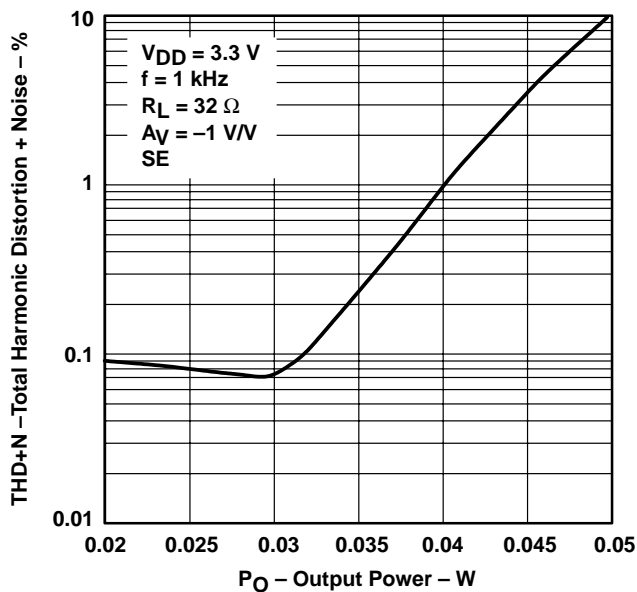


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

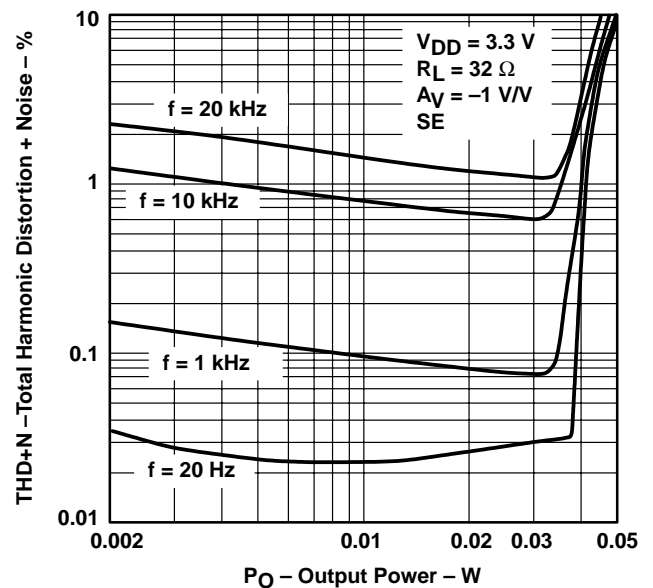


Figure 23

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TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

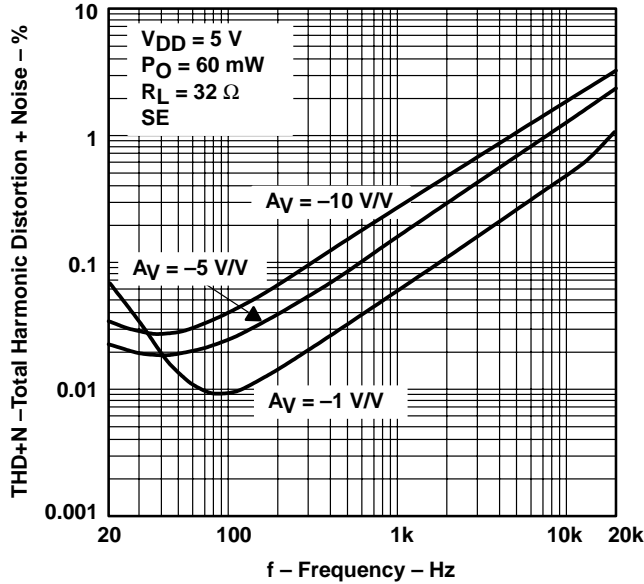


Figure 24

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

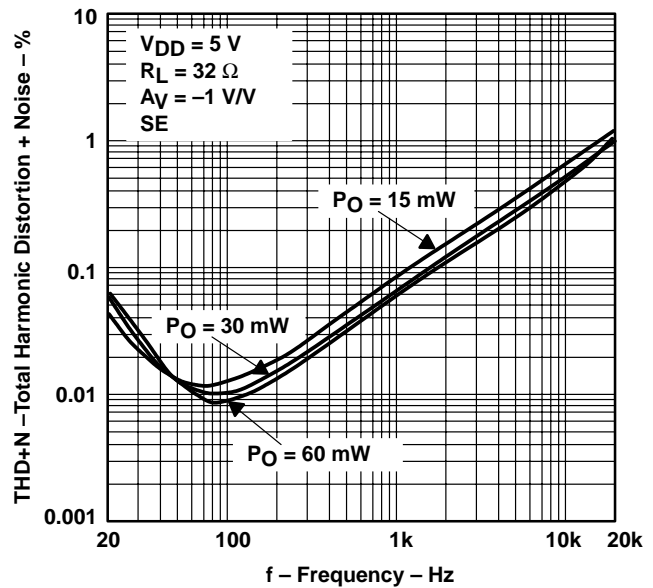


Figure 25

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

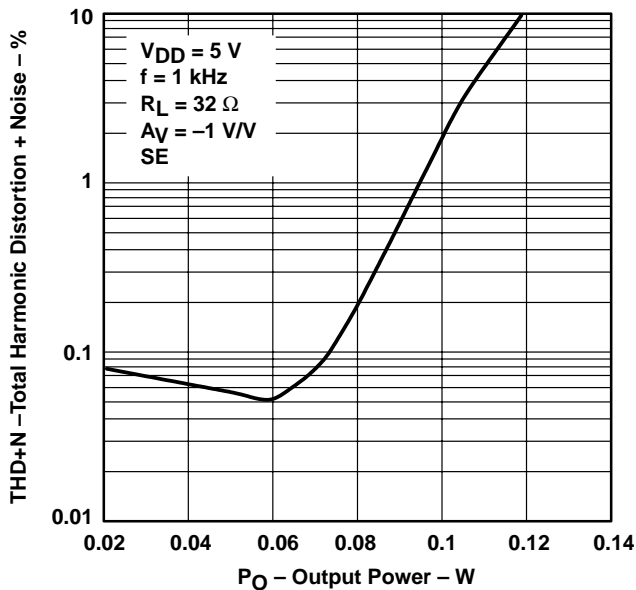


Figure 26

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

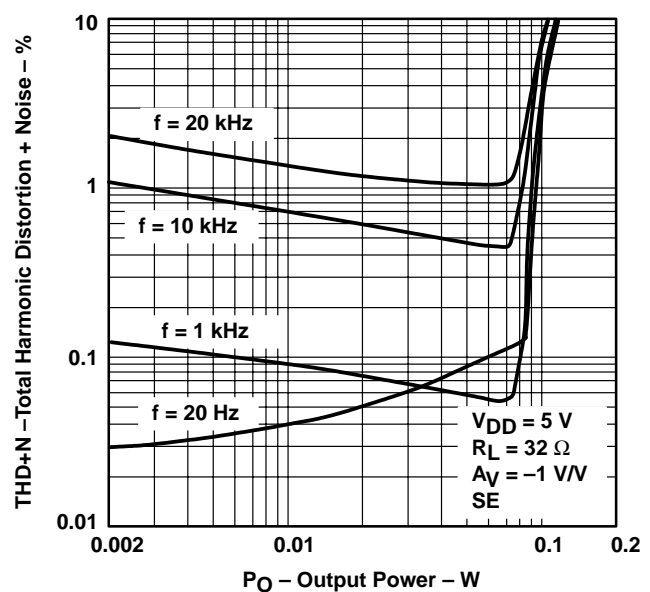


Figure 27



TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

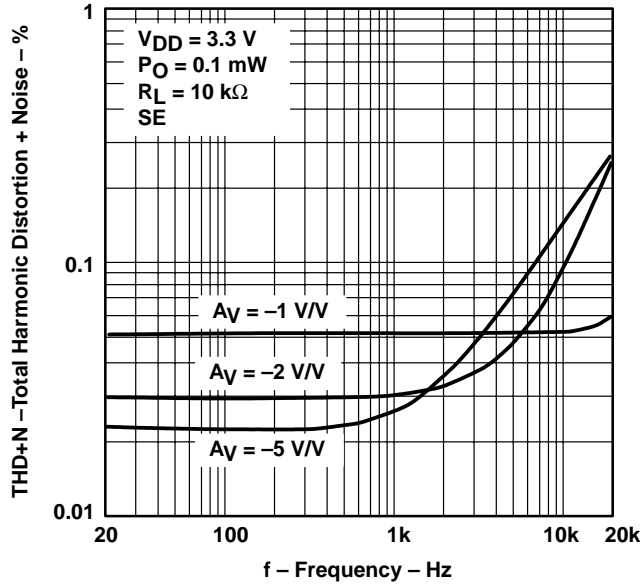


Figure 28

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

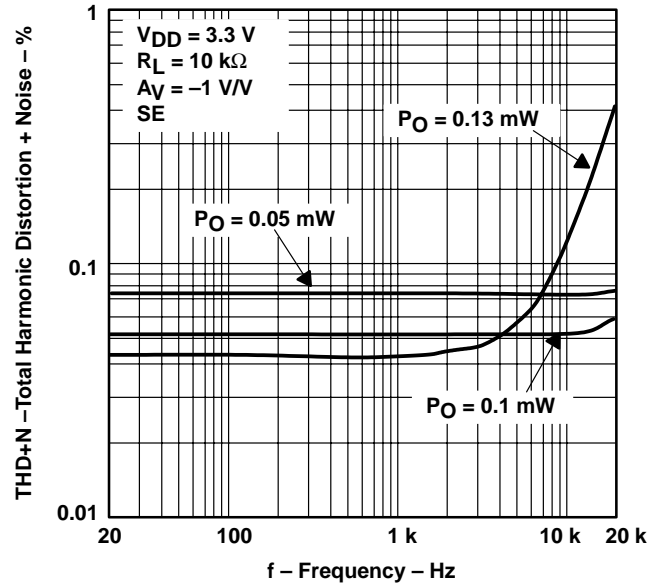


Figure 29

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

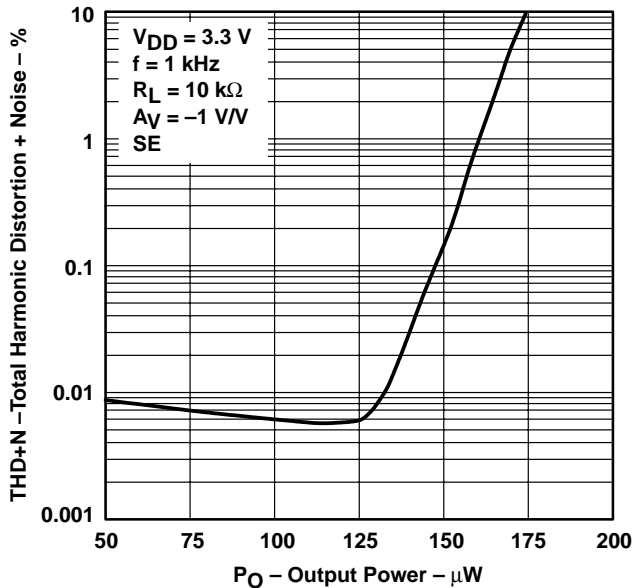


Figure 30

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

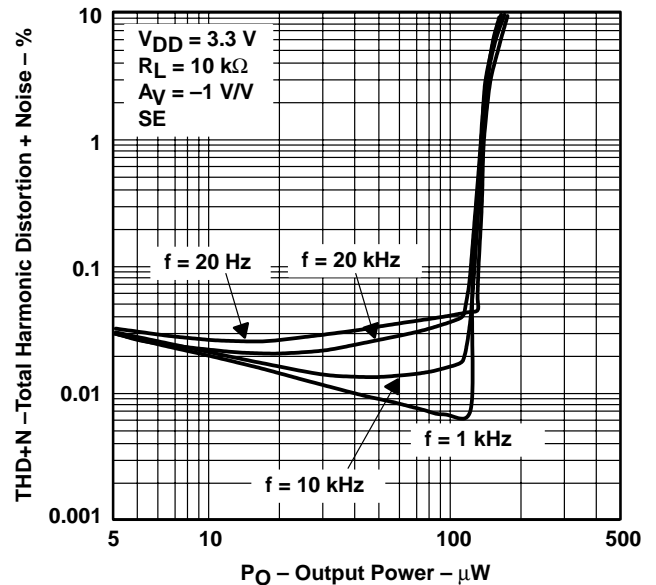


Figure 31

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TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

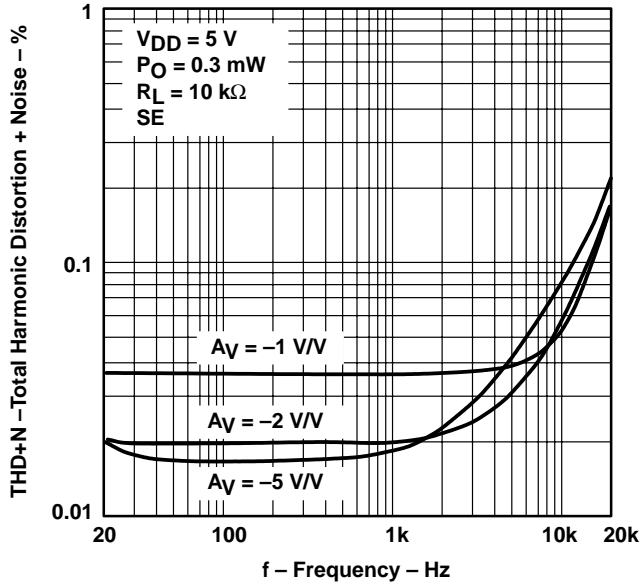


Figure 32

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

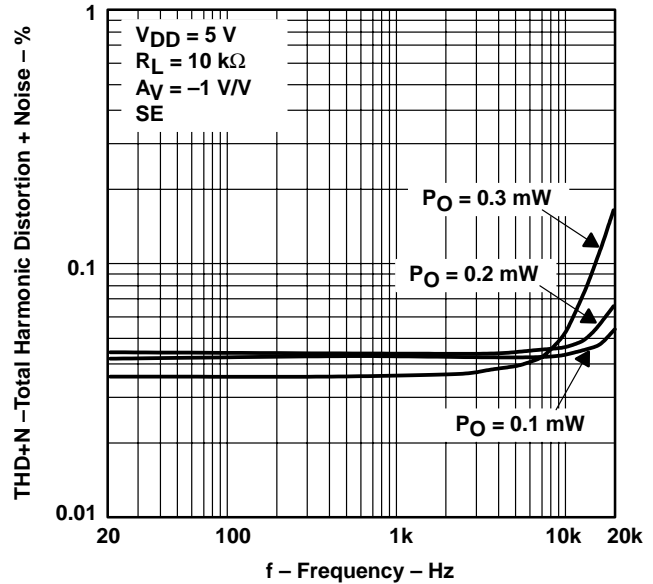


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

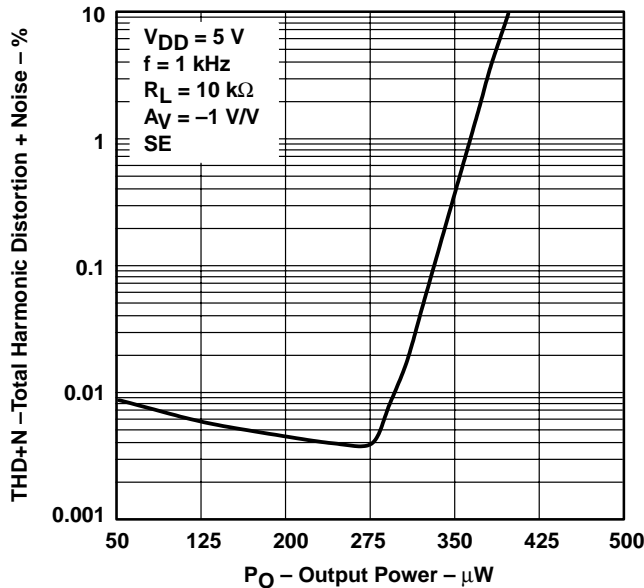


Figure 34

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

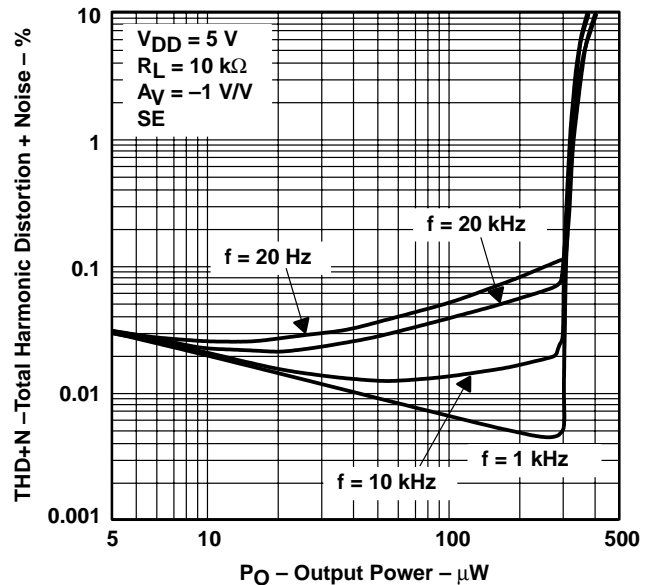


Figure 35



TYPICAL CHARACTERISTICS

OPEN-LOOP GAIN AND PHASE
 vs
 FREQUENCY

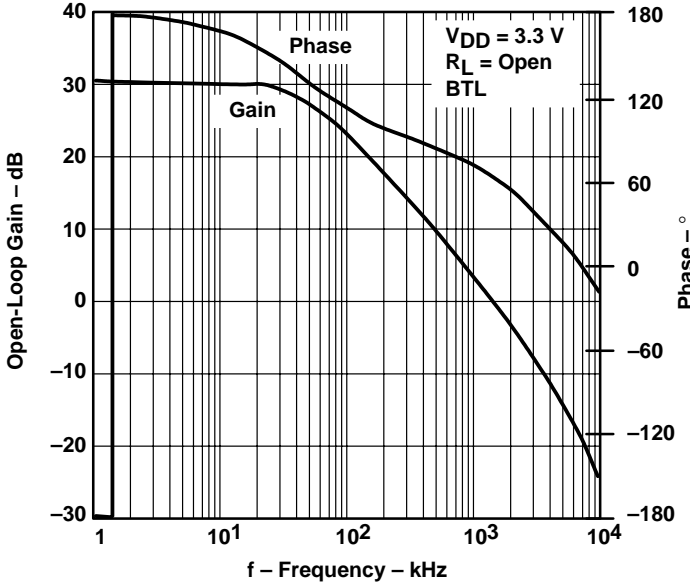


Figure 36

OPEN-LOOP GAIN AND PHASE
 vs
 FREQUENCY

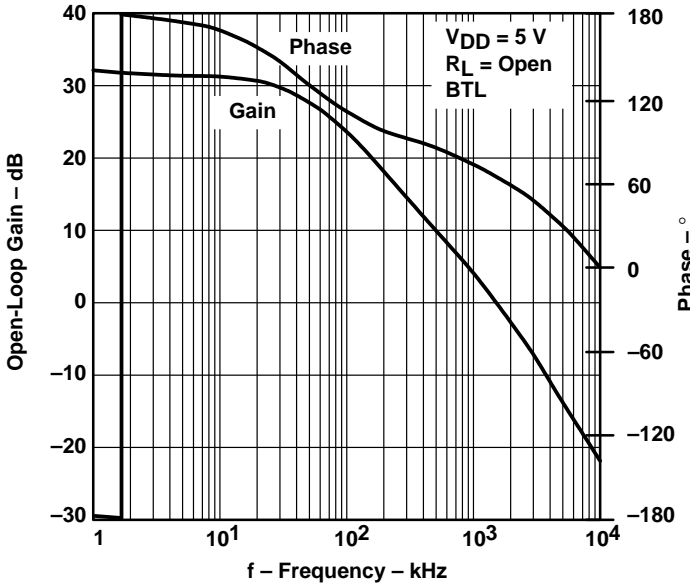


Figure 37

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350-mW MONO AUDIO POWER AMPLIFIER

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TYPICAL CHARACTERISTICS

**CLOSED-LOOP GAIN AND PHASE
 vs
 FREQUENCY**

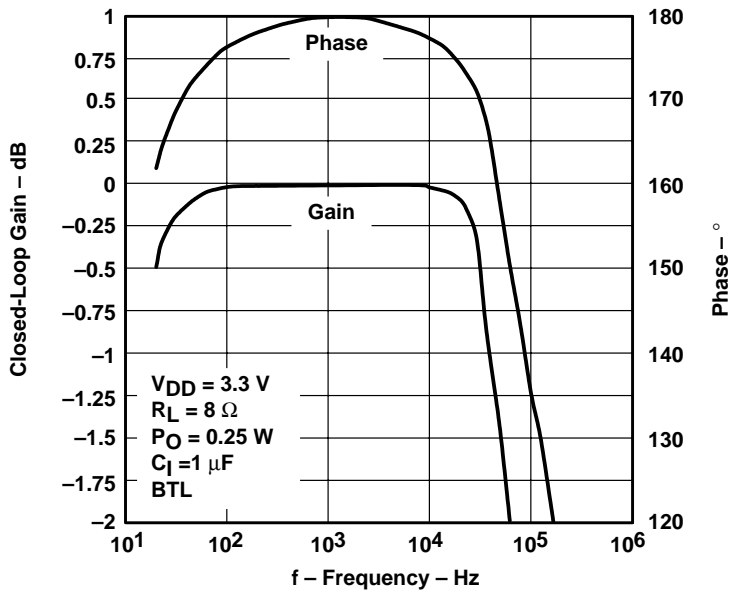


Figure 38

**CLOSED-LOOP GAIN AND PHASE
 vs
 FREQUENCY**

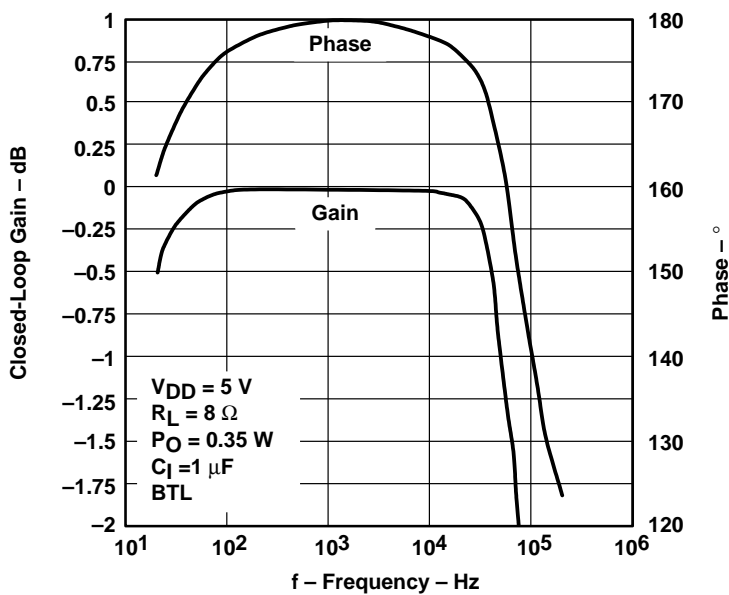


Figure 39



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TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY

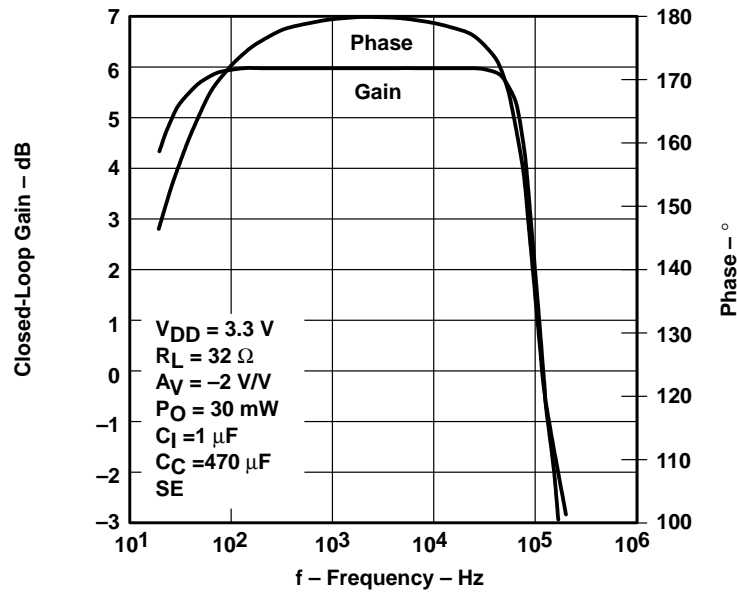


Figure 40

CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY

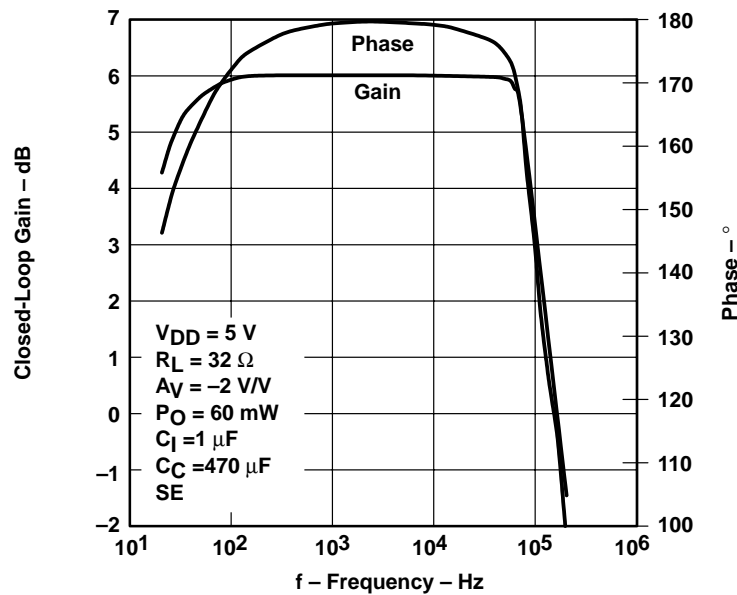


Figure 41

TPA311 350-mW MONO AUDIO POWER AMPLIFIER

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TYPICAL CHARACTERISTICS

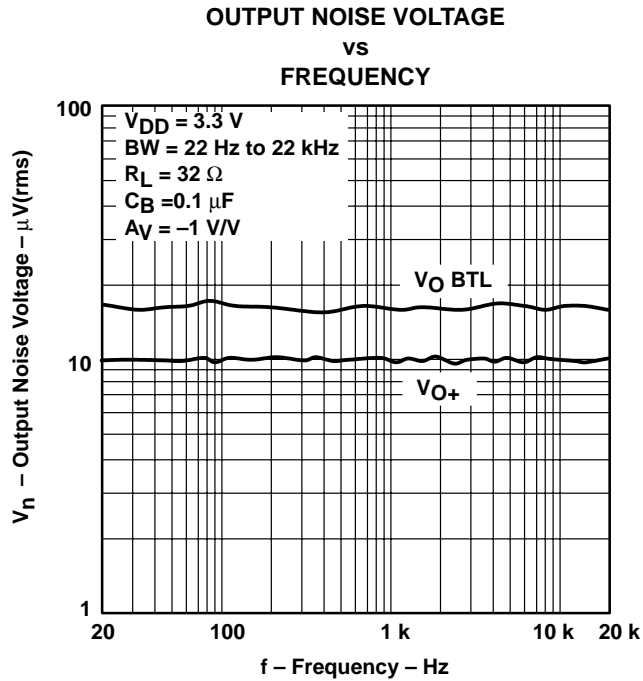


Figure 42

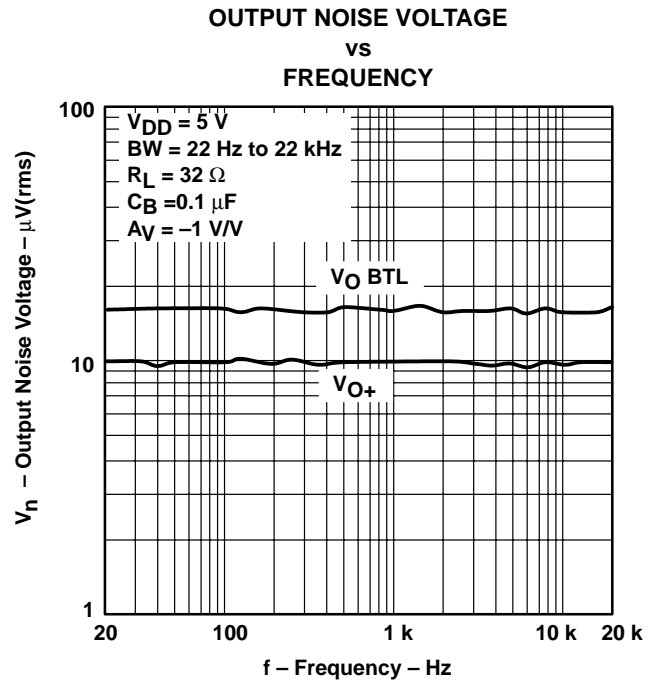


Figure 43

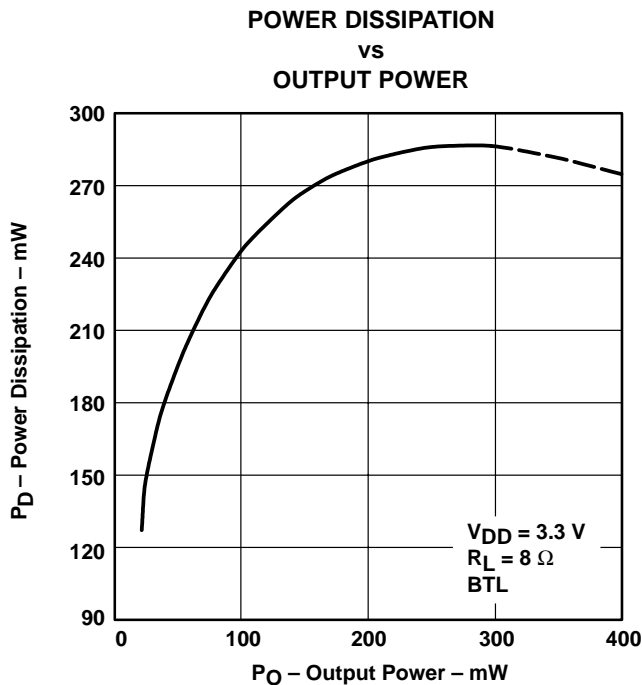


Figure 44

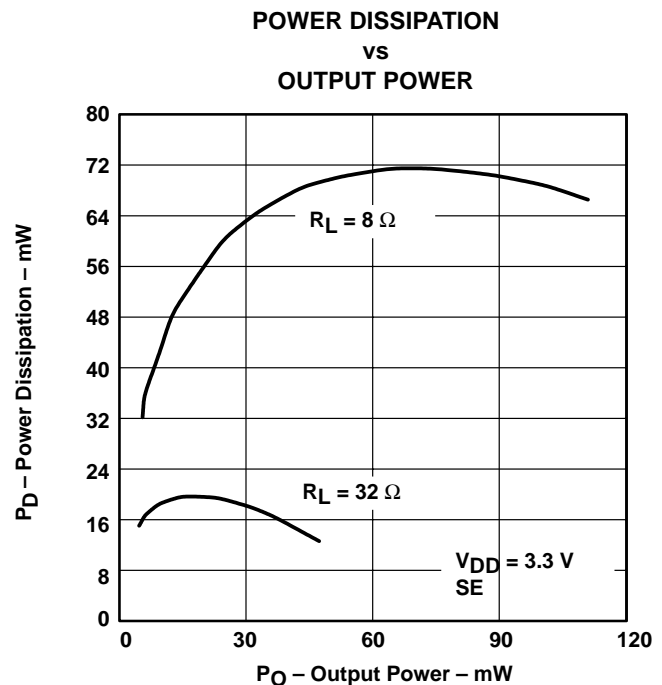


Figure 45



TYPICAL CHARACTERISTICS

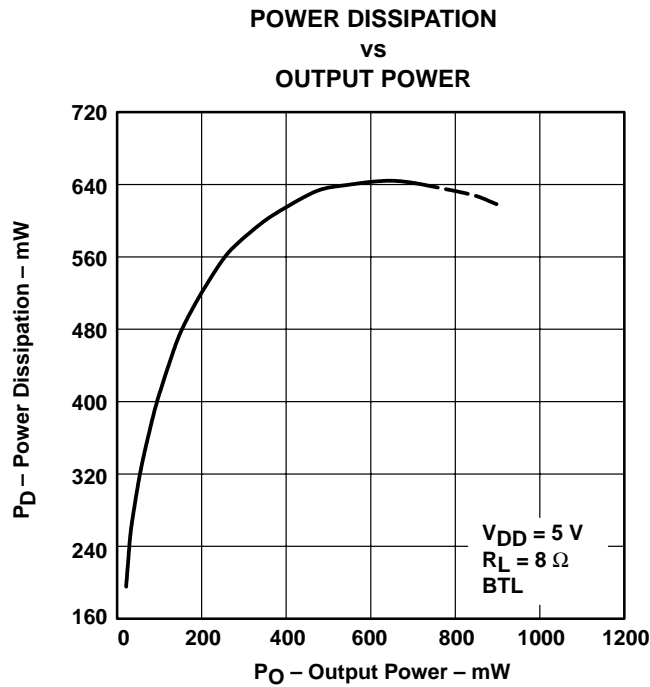


Figure 46

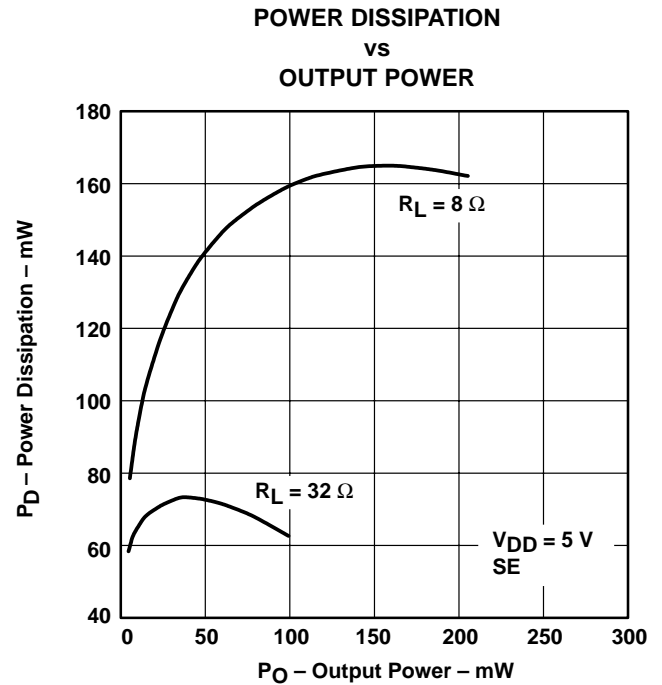


Figure 47

APPLICATION INFORMATION

bridge-tied load versus single-ended mode

Figure 48 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA311 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields $4 \times$ the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$Power = \frac{V_{(rms)}^2}{R_L} \tag{1}$$

APPLICATION INFORMATION

bridge-tied load versus single-ended mode (continued)

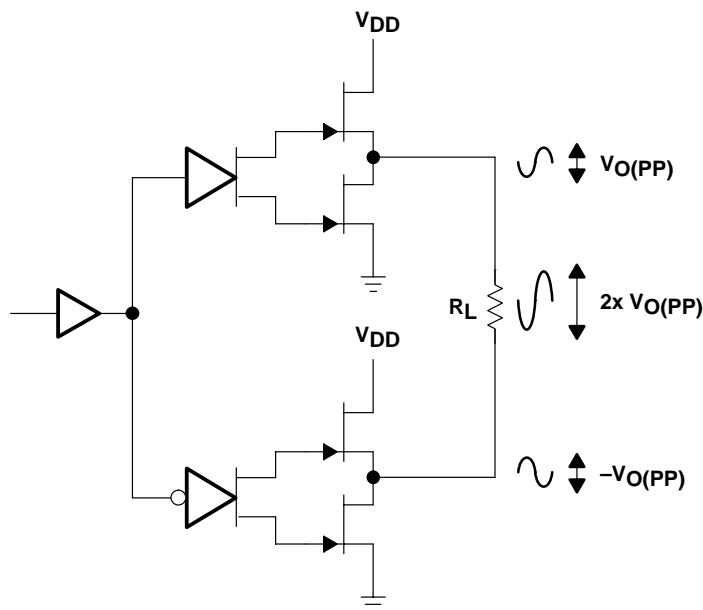


Figure 48. Bridge-Tied Load Configuration

In typical portable handheld equipment, a sound channel operating at 3.3 V and using bridging raises the power into an 8-Ω speaker from a single-ended (SE, ground reference) limit of 62.5 mW to 250 mW. In terms of sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 49. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF), tend to be expensive, heavy, and occupy valuable PCB area. These capacitors also have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_c = \frac{1}{2\pi R_L C_C} \tag{2}$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

APPLICATION INFORMATION

bridge-tied load versus single-ended mode (continued)

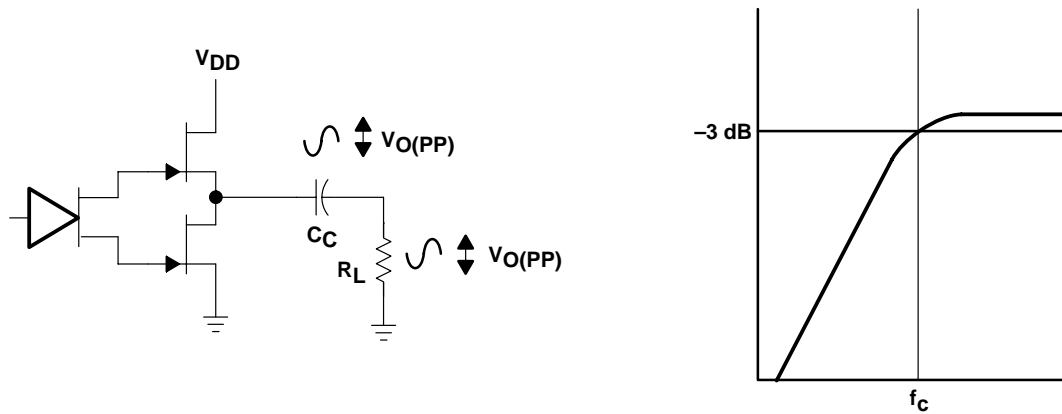


Figure 49. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable, considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD} . The internal voltage drop multiplied by the RMS value of the supply current, $I_{DD\text{rms}}$, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 50).

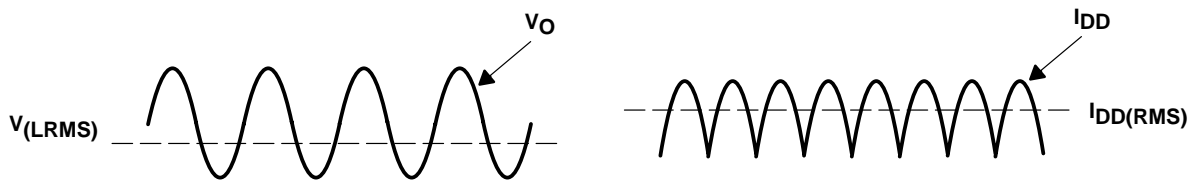


Figure 50. Voltage and Current Waveforms for BTL Amplifiers

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BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas, in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform, both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{\text{SUP}}} \quad (3)$$

where

$$P_L = \frac{V_{L\text{rms}}^2}{R_L} = \frac{V_P^2}{2R_L}$$

$$V_{L\text{rms}} = \frac{V_P}{\sqrt{2}}$$

$$P_{\text{SUP}} = V_{\text{DD}} I_{\text{DDrms}} = \frac{V_{\text{DD}} 2V_P}{\pi R_L}$$

$$I_{\text{DDrms}} = \frac{2V_P}{\pi R_L}$$

$$\text{Efficiency of a BTL Configuration} = \frac{\pi V_P}{2V_{\text{DD}}} = \frac{\pi \left(\frac{P_L R_L}{2} \right)^{1/2}}{2V_{\text{DD}}} \quad (4)$$

Table 1 employs equation 4 to calculate efficiencies for three different output power levels. The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. The internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design.

Table 1. Efficiency Vs Output Power in 3.3-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-TO-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.125	33.6	1.41	0.26
0.25	47.6	2.00	0.29
0.375	58.3	2.45†	0.28

† High-peak voltage values cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. In equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

application schematic

Figure 51 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of -10 V/V .

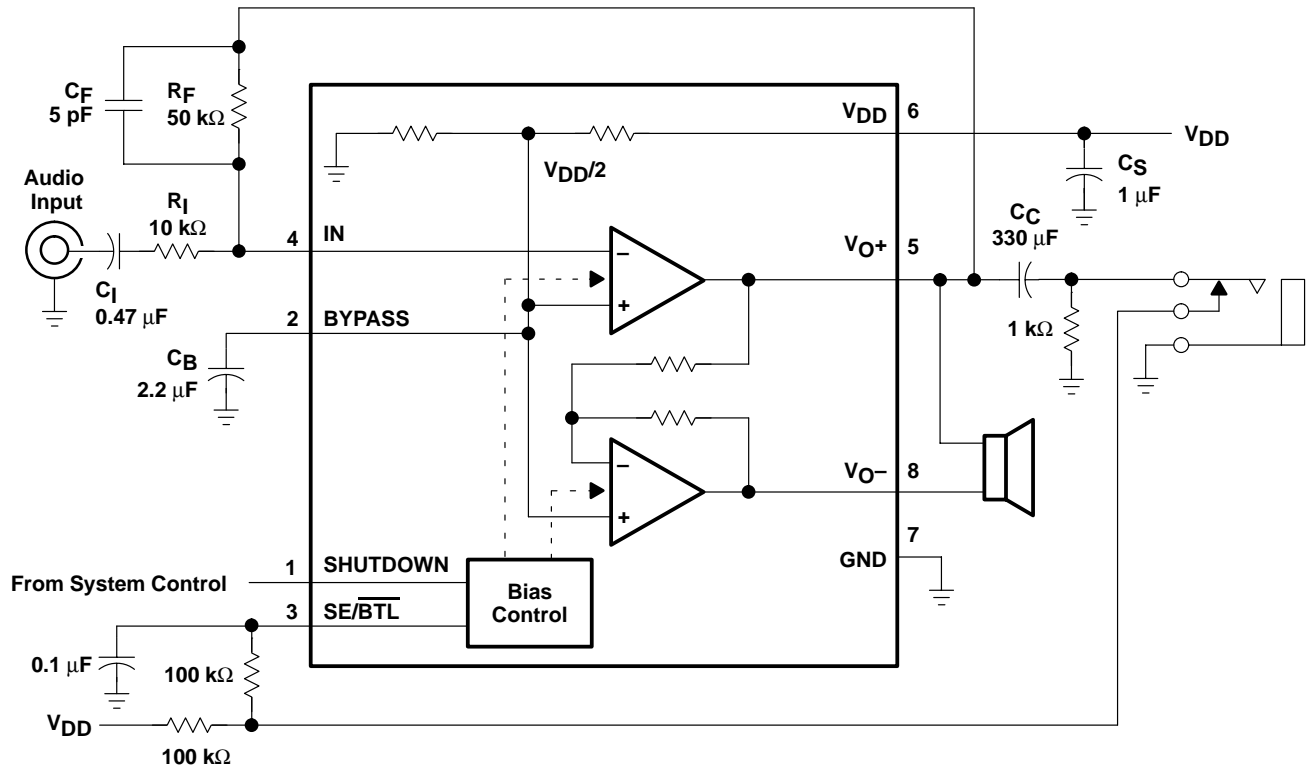


Figure 51. TPA311 Application Circuit

The following sections discuss the selection of the components used in Figure 51.

component selection

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA311 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = A_V = -2 \left(\frac{R_F}{R_I} \right) \quad (5)$$

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA311 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between $5\text{ k}\Omega$ and $20\text{ k}\Omega$. The effective impedance is calculated in equation 6.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \quad (6)$$

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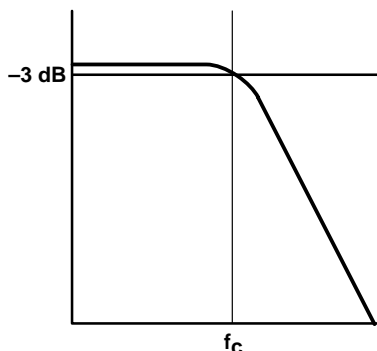
APPLICATION INFORMATION

component selection (continued)

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be -10 V/V and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor, C_F, of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{c(\text{lowpass})} = \frac{1}{2\pi R_F C_F} \quad (7)$$

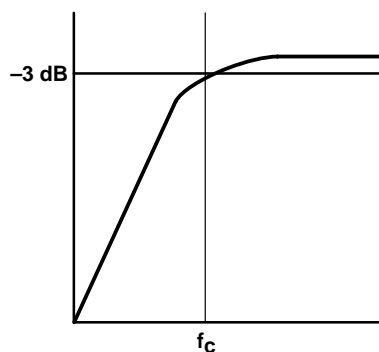


For example, if R_F is 100 kΩ and C_F is 5 pF then f_c is 318 kHz, which is well outside the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(\text{highpass})} = \frac{1}{2\pi R_I C_I} \quad (8)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (9)$$

APPLICATION INFORMATION

component selection (continued)

In this example, C_I is $0.40\ \mu\text{F}$, so one would likely choose a value in the range of $0.47\ \mu\text{F}$ to $1\ \mu\text{F}$. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I , C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA311 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically $0.1\ \mu\text{F}$ placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of $10\ \mu\text{F}$ or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B , is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD + N. The capacitor is fed from a $250\text{-k}\Omega$ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained, which insures the input capacitor is fully charged before the bypass capacitor is fully charged and the amplifier starts up.

$$\frac{10}{(C_B \times 250\ \text{k}\Omega)} \leq \frac{1}{(R_F + R_I) C_I} \quad (10)$$

As an example, consider a circuit where C_B is $2.2\ \mu\text{F}$, C_I is $0.47\ \mu\text{F}$, R_F is $50\ \text{k}\Omega$ and R_I is $10\ \text{k}\Omega$. Inserting these values into the equation 10 we get: $18.2 \leq 35.5$ which satisfies the rule. Bypass capacitor, C_B , values of $0.1\ \mu\text{F}$ to $2.2\ \mu\text{F}$ ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

single-ended operation

In SE mode (see Figure 51), the load is driven from the primary amplifier output (V_{O+} , terminal 5).

In SE mode the gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2, from equation 5, is not included.

$$\text{SE Gain} = A_V = - \left(\frac{R_F}{R_I} \right) \quad (11)$$

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APPLICATION INFORMATION

single-ended operation (continued)

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

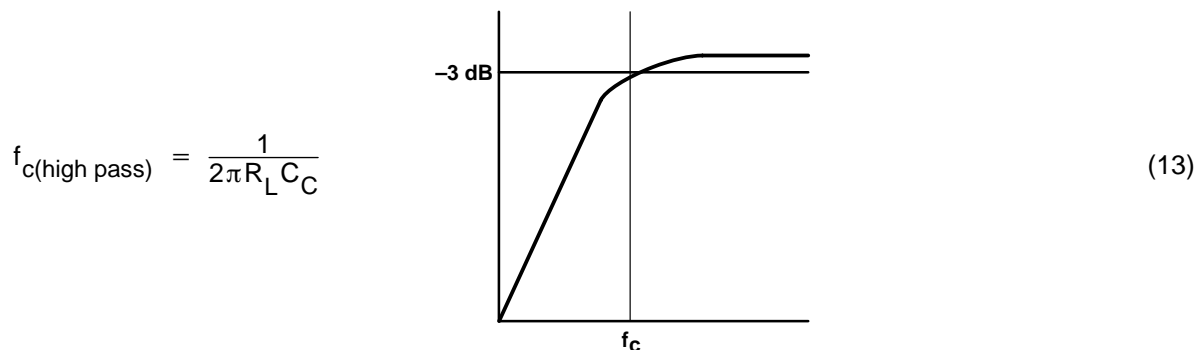
$$\frac{10}{(C_B \times 250 \text{ k}\Omega)} \leq \frac{1}{(R_F + R_I) C_I} \ll \frac{1}{R_L C_C} \quad (12)$$

As an example, consider a circuit where C_B is $0.2.2 \mu\text{F}$, C_I is $0.47 \mu\text{F}$, C_C is $330 \mu\text{F}$, R_F is $50 \text{ k}\Omega$, R_L is 32Ω , and R_I is $10 \text{ k}\Omega$. Inserting these values into the equation 12 we get:

$$18.2 < 35.5 \ll 94.7 \text{ which satisfies the rule.}$$

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 13.



The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of $330 \mu\text{F}$ is chosen and loads vary from 8Ω , 32Ω , to $47 \text{ k}\Omega$. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
8Ω	$330 \mu\text{F}$	60 Hz
32Ω	$330 \mu\text{F}$	15 Hz
$47,000 \Omega$	$330 \mu\text{F}$	0.01 Hz

As Table 2 indicates an $8\text{-}\Omega$ load is adequate, earphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

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SE/BTL operation

The ability of the TPA311 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional earphone amplifier in applications where internal speakers are driven in BTL mode but external earphone or speaker must be accommodated. Internal to the TPA311, two separate amplifiers drive V_{O+} and V_{O-} . The SE/BTL input (terminal 3) controls the operation of the follower amplifier that drives V_{O-} (terminal 8). When SE/BTL is held low, the amplifier is on and the TPA311 is in the BTL mode. When SE/BTL is held high, the V_{O-} amplifier is in a high output impedance state, which configures the TPA311 as an SE driver from V_{O+} (terminal 5). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/BTL input can be from a logic-level TTL source or, more typically, from a resistor divider network as shown in Figure 52.

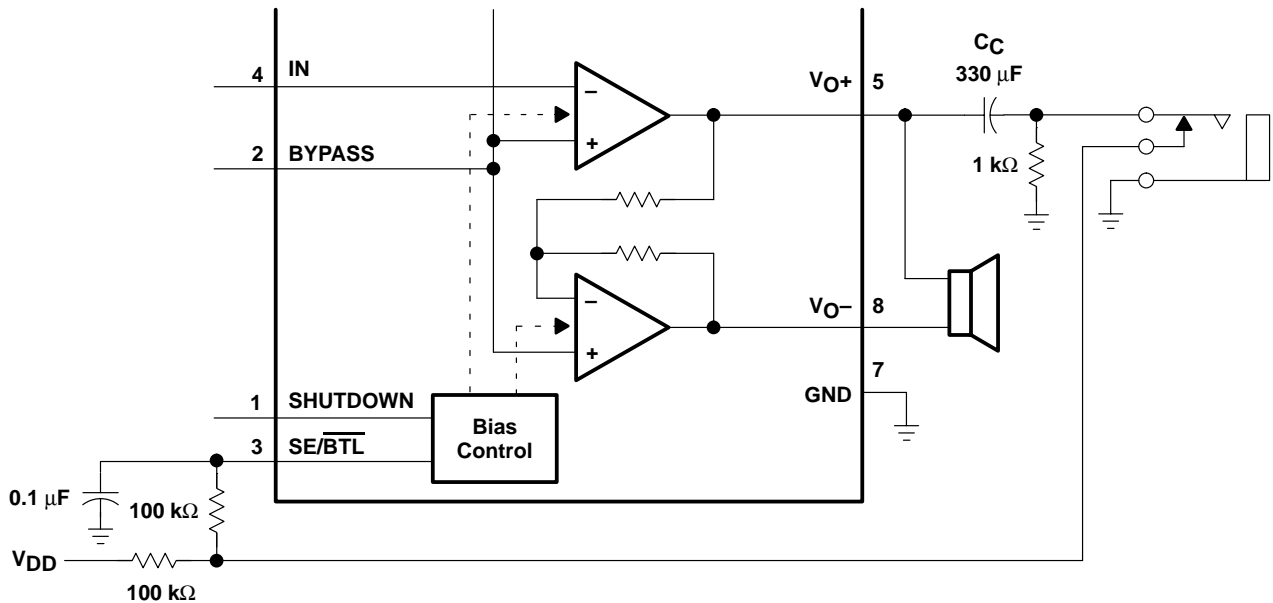


Figure 52. TPA311 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3,5 mm) mono earphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/BTL input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/BTL input is pulled high. When the input goes high, the V_{O-} amplifier is shutdown causing the BTL speaker to mute (virtually open-circuits the speaker). The V_{O+} amplifier then drives through the output capacitor (C_C) into the earphone jack.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

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5-V versus 3.3-V operation

The TPA311 operates over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation with respect to supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in TPA311 can produce a maximum voltage swing of $V_{DD} - 1$ V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)} = 2.3$ V as opposed to $V_{O(PP)} = 4$ V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8- Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level of operation from 5-V supplies.

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA311 data sheet, one can see that when the TPA311 is operating from a 5-V supply into a 8- Ω speaker that 350 mW peaks are available. Converting watts to dB:

$$\begin{aligned} P_{dB} &= 10 \text{Log} \left(\frac{P_W}{P_{ref}} \right) \\ &= 10 \text{Log} \left(\frac{350 \text{ mW}}{1 \text{ W}} \right) \\ &= -4.6 \text{ dB} \end{aligned}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

$$\begin{aligned} -4.6 \text{ dB} - 15 \text{ dB} &= -19.6 \text{ dB (15 dB headroom)} \\ -4.6 \text{ dB} - 12 \text{ dB} &= -16.6 \text{ dB (12 dB headroom)} \\ -4.6 \text{ dB} - 9 \text{ dB} &= -13.6 \text{ dB (9 dB headroom)} \\ -4.6 \text{ dB} - 6 \text{ dB} &= -10.6 \text{ dB (6 dB headroom)} \\ -4.6 \text{ dB} - 3 \text{ dB} &= -7.6 \text{ dB (3 dB headroom)} \end{aligned}$$

Converting dB back into watts:

$$\begin{aligned} P_W &= 10^{P_{dB}/10} \times P_{ref} \\ &= 11 \text{ mW (15 dB headroom)} \\ &= 22 \text{ mW (12 dB headroom)} \\ &= 44 \text{ mW (9 dB headroom)} \\ &= 88 \text{ mW (6 dB headroom)} \\ &= 175 \text{ mW (3 dB headroom)} \end{aligned}$$



APPLICATION INFORMATION

headroom and thermal considerations (continued)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 350 mW of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 8-Ω system, the internal dissipation in the TPA311 and maximum ambient temperatures is shown in Table 3.

Table 3. TPA311 Power Rating, 5-V, 8-Ω, BTL

PEAK OUTPUT POWER (mW)	AVERAGE OUTPUT POWER	POWER DISSIPATION (mW)	MAXIMUM AMBIENT TEMPERATURE	
			0 CFM SOIC	0 CFM DGN
350	350 mW	600	46°C	114°C
350	175 mW (3 dB)	500	64°C	120°C
350	88 mW (6 dB)	380	85°C	125°C
350	44 mW (9 dB)	300	98°C	125°C
350	22 mW (12 dB)	200	115°C	125°C
350	11 mW (15 dB)	180	119°C	125°C

Table 3 shows that the TPA311 can be used to its full 350-mW rating without any heat sinking in still air up to 46°C.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA311D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		311	Samples
TPA311DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		AAB	Samples
TPA311DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		AAB	Samples
TPA311DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		311	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

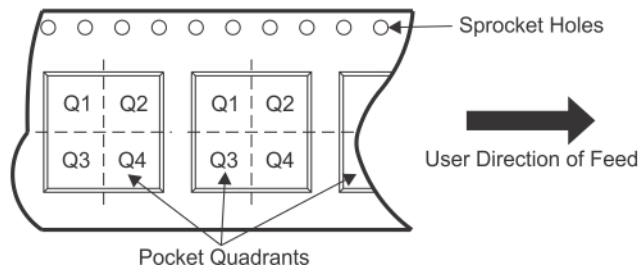
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA311DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA311DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA311DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPA311DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPA311D	D	SOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

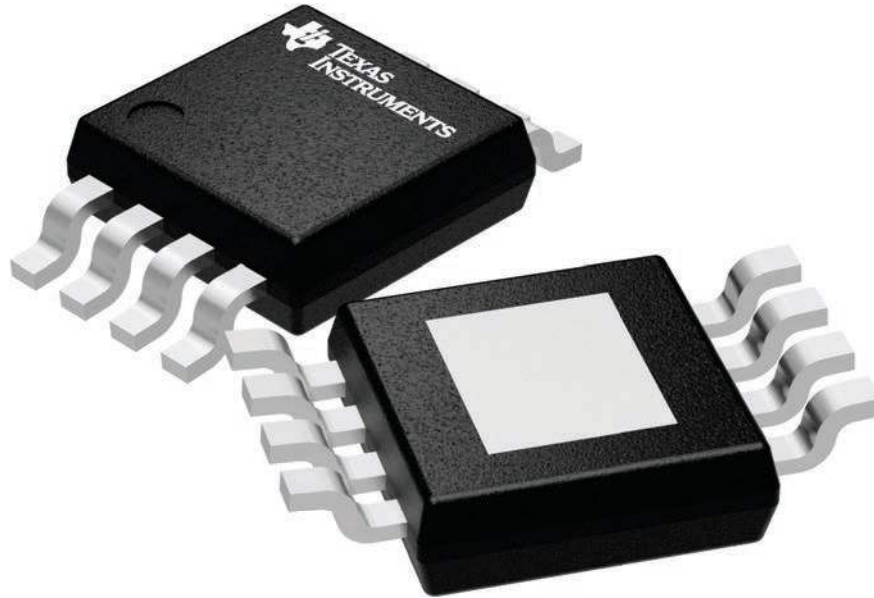
DGN 8

PowerPAD VSSOP - 1.1 mm max height

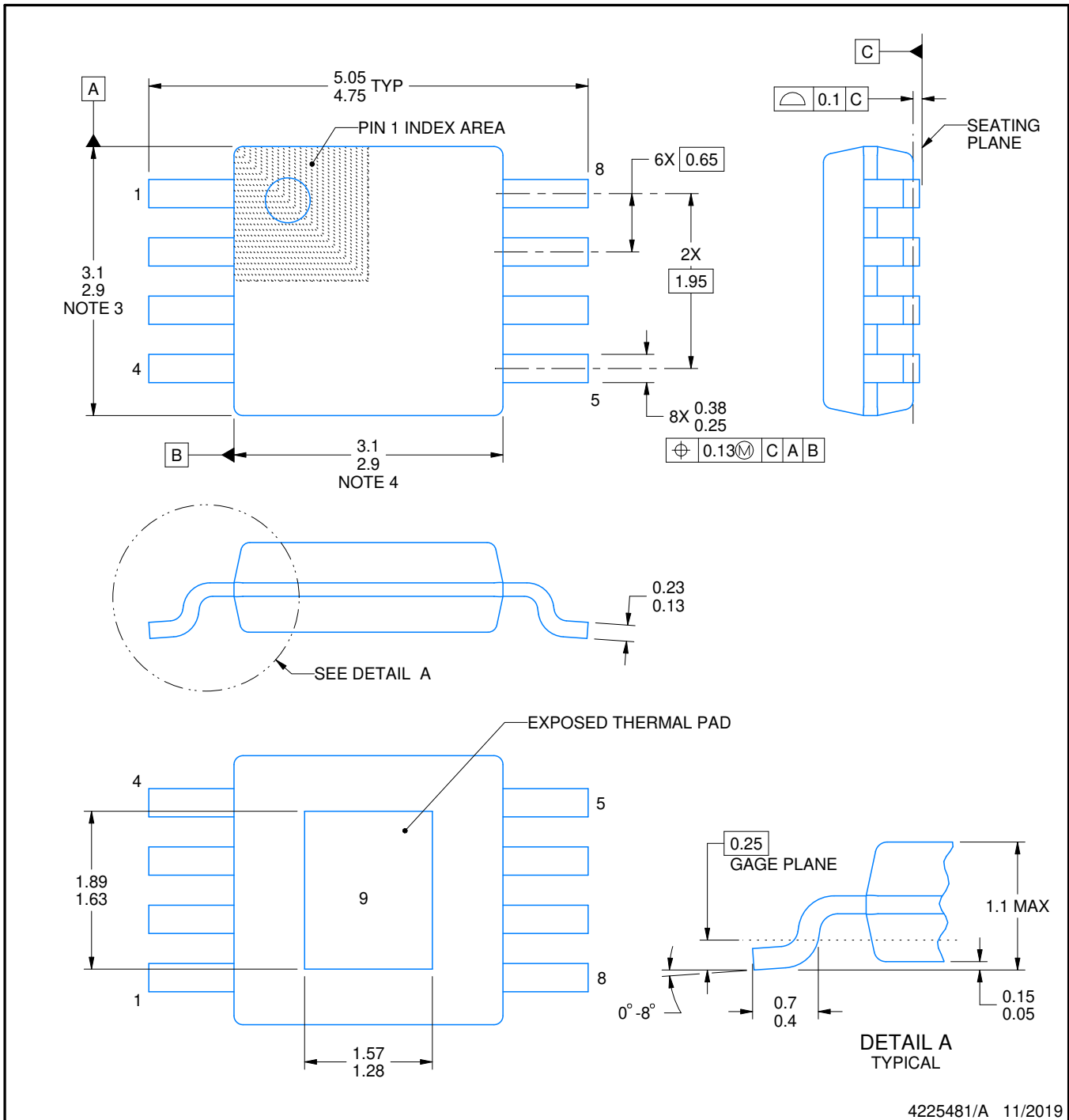
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A



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NOTES:

PowerPAD is a trademark of Texas Instruments.

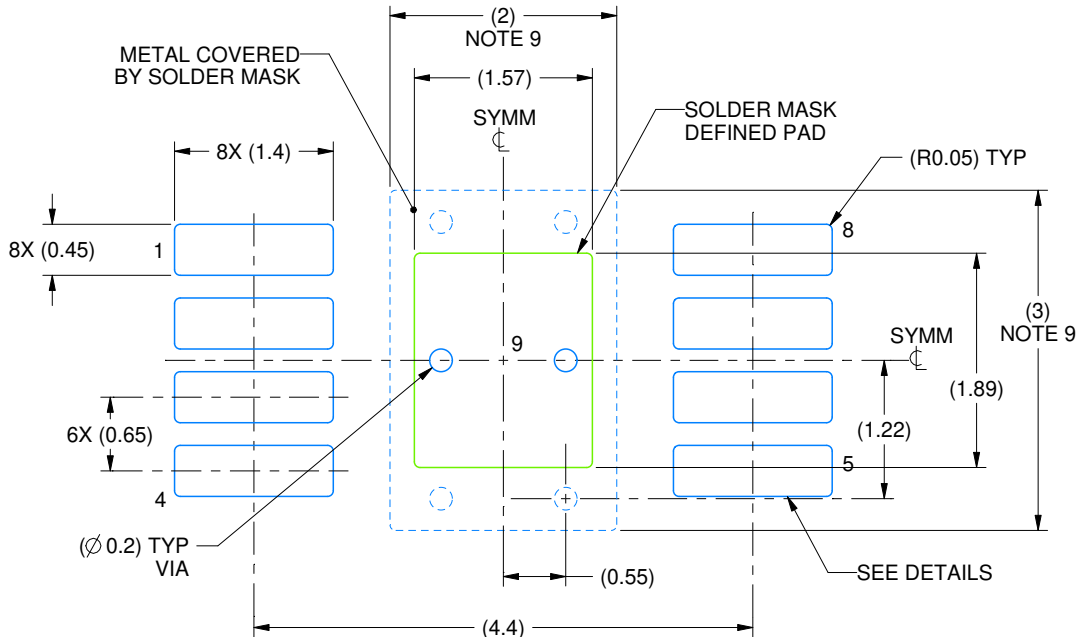
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

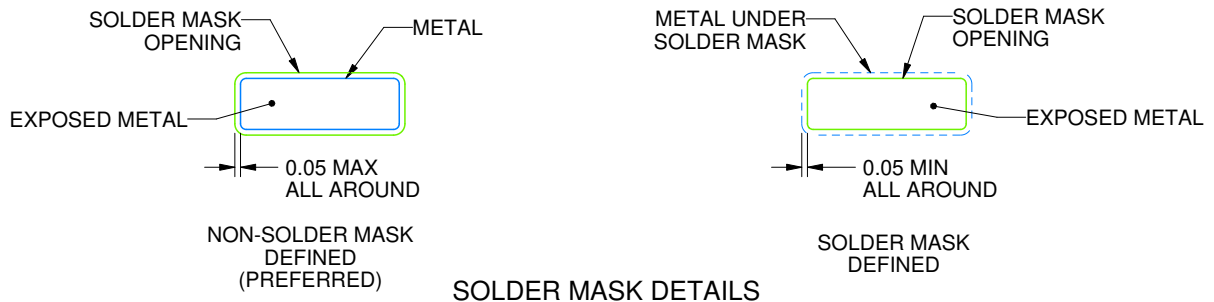
DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



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NOTES: (continued)

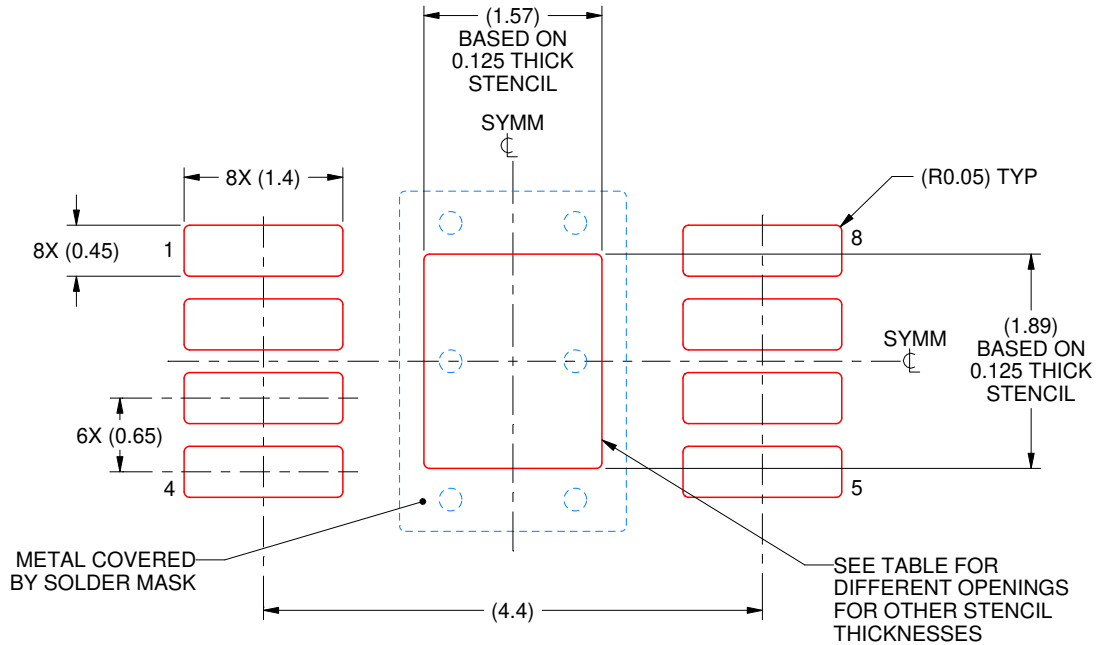
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

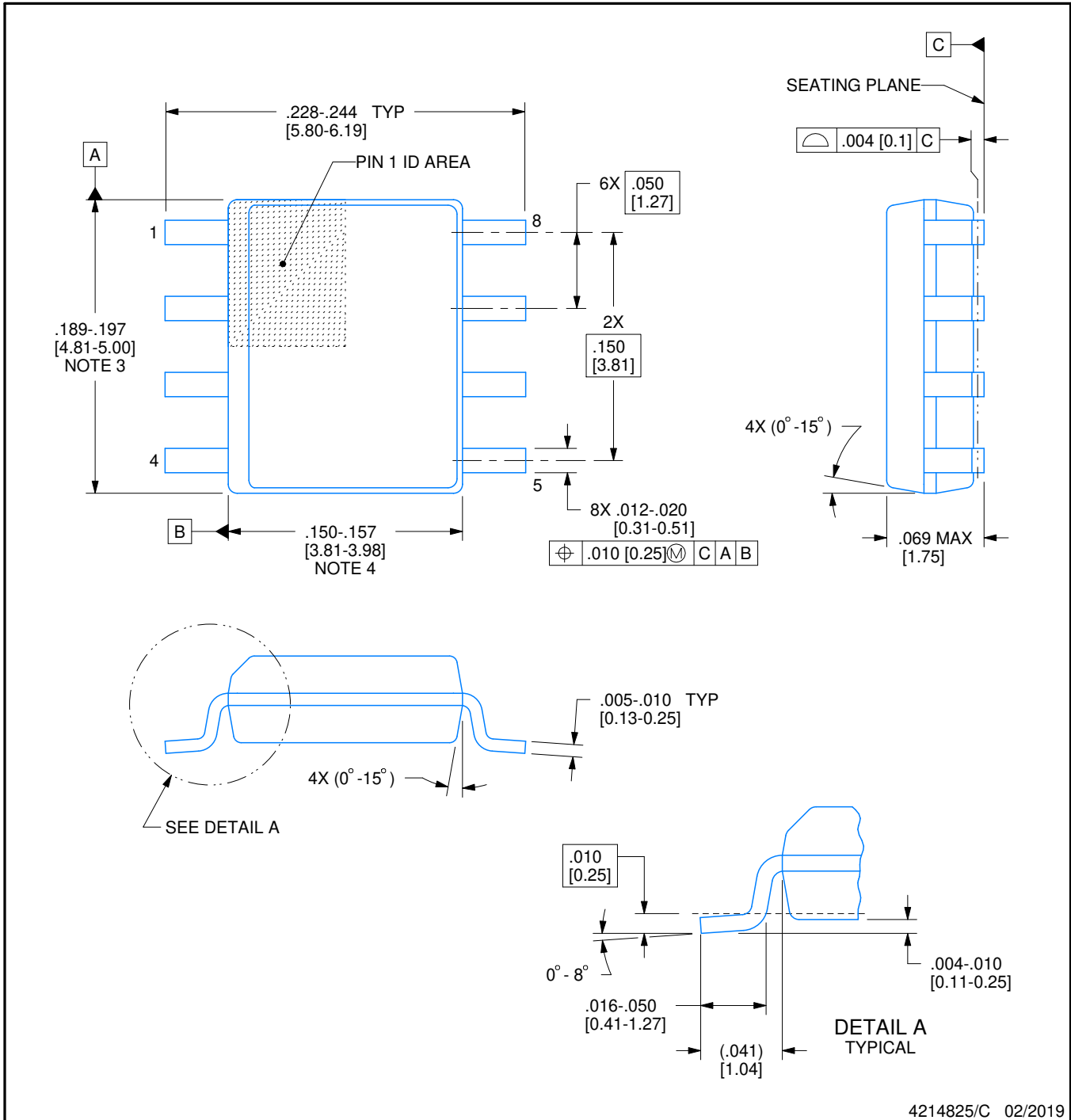
D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

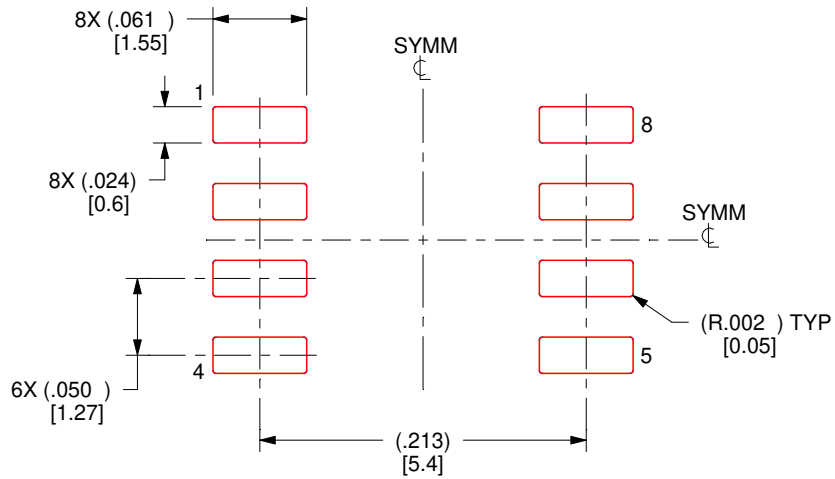
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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