

Dual N-Channel Power MOSFET

 $20V, 6.0A, 30m\Omega$

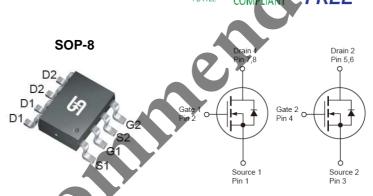
FEATURES

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low Onresistance

KEY PERFORMANCE PARAMETERS				
PARAMETER		TER VALUE		
V _{DS}		20	V	
R _{DS(on)} (max)	$V_{GS} = 4.5V$	30		
	$V_{GS} = 2.5V$	40	mΩ	
Q	g	4.86	nC	

APPLICATION

- Specially Designed for Li-on Battery Packs
- Battery Switch Application



Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS (TA = 25°C unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V _{DS}	20	V	
Gate-Source Voltage		V _{GS}	±12	V	
Continuous Drain Current (Note 1) T _c	= 25°C	Ι _D	6	А	
Pulsed Drain Current (Note 2)		I _{DM}	30	А	
Continuous Source Current (Diode Conduction)		I _S	1.7	А	
Tatal Davies Disingtion	= 25°C	P _{DTOT} -	1.6	W	
Total Power Dissipation T _A	= 75°C		1.1		
Operating Junction and Storage Temperature Rar	nge	T _J , T _{STG}	- 55 to +150	°C	

THERMAL PERFORMANCE					
PARAMETER	SYMBOL	LIMIT	UNIT		
Junction to Case Thermal Resistance	R _{eJC}	40	°C/W		
Junction to Ambient Thermal Resistance	R _{eja}	77	°C/W		

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.





Taiwan Semiconductor

PARAMETER	CONDITIONS	SYMBOL	MIN	ТҮР	MAX	UNIT
Static (Note 3)			ı		ı	I
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV _{DSS}	20			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	V _{GS(TH)}	0.6			V
Gate Body Leakage	$V_{GS} = \pm 12V, V_{DS} = 0V$	I _{GSS}			±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 20V, V_{GS} = 0V$	I _{DSS}			1	μA
On-State Drain Current	$V_{DS} = 5V, V_{GS} = 4.5V$	I _{D(ON)}	30	🗶		Α
	$V_{GS} = 4.5V, I_D = 6.0A$		21	30		
Drain-Source On-State Resistance	$V_{GS} = 2.5V, I_D = 5.2A$	R _{DS(ON)}		30	40	mΩ
Forward Transconductance	$V_{DS} = 10V, I_{D} = 6A$	g _{fs}	7	30		S
Dynamic ^(Note 4)						
Total Gate Charge	$V_{DS} = 10V, I_D = 6A,$ $V_{GS} = 4.5V$	Qg		4.86		
Gate-Source Charge		Q _{gs}		0.92		nC
Gate-Drain Charge		Q _{gd}		1.4		
Input Capacitance		C _{iss}		562		. 5
Output Capacitance	$V_{\rm DS} = 8V, V_{\rm GS} = 0V,$	C _{oss}		106		pF
Reverse Transfer Capacitance	F = 1.0MHz	C _{rss}		75		
Switching (Note 5)						
Turn-On Delay Time		t _{d(on)}		8.1		
Turn-On Rise Time	$V_{DD} = 10V,$ $R_{GEN} = 6\Omega,$	t _r		9.95		
Turn-Off Delay Time		t _{d(off)}		21.85		ns
Turn-Off Fall Time	$I_{D} = 1A, V_{GS} = 4.5V,$	t _f		5.35		
Source-Drain Diode (Note 3)						
Forward Voltage	$I_{\rm S} = 1.7$ A, $V_{\rm GS} = 0$ V	V _{SD}		0.7	1.2	V

Notes:

2 Pulse width limited by the Maximum junction temperature. 1.

Surface Mounted on FR4 Board, t ≤ 5 sec. 2.

Pulse test: $PW \le 300\mu s$, duty cycle $\le 2\%$. 3.

For DESIGN AID ONLY, not subject to production testing. 4.

Switching time is essentially independent of operating temperature. 5.



ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM9926DCS RLG	SOP-8	2,500pcs / 13" Reel

Note:

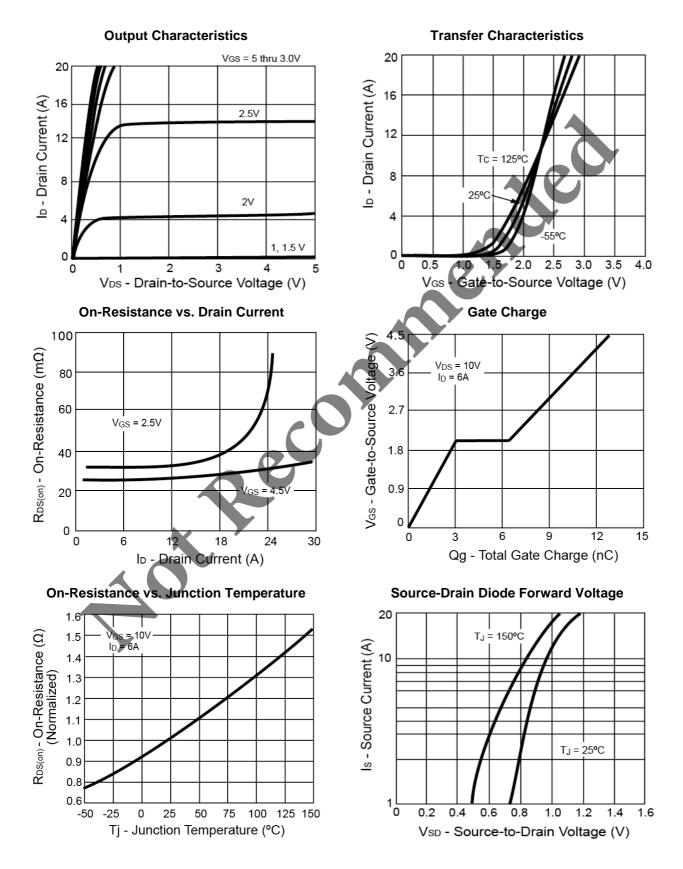
Reconnection 1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC

Halogen-free according to IEC 61249-2-21 definition 2.



CHARACTERISTICS CURVES

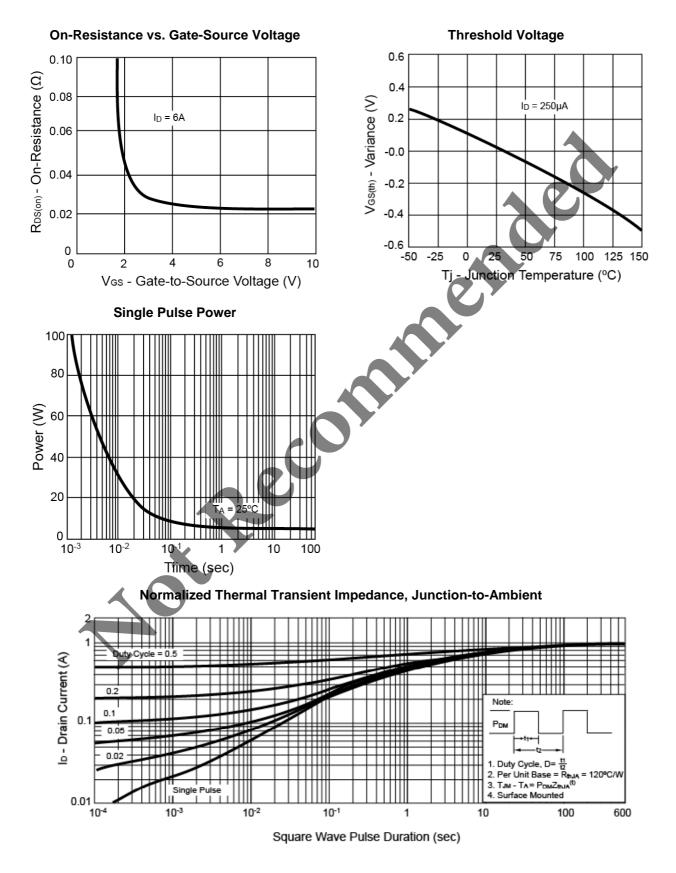
 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$





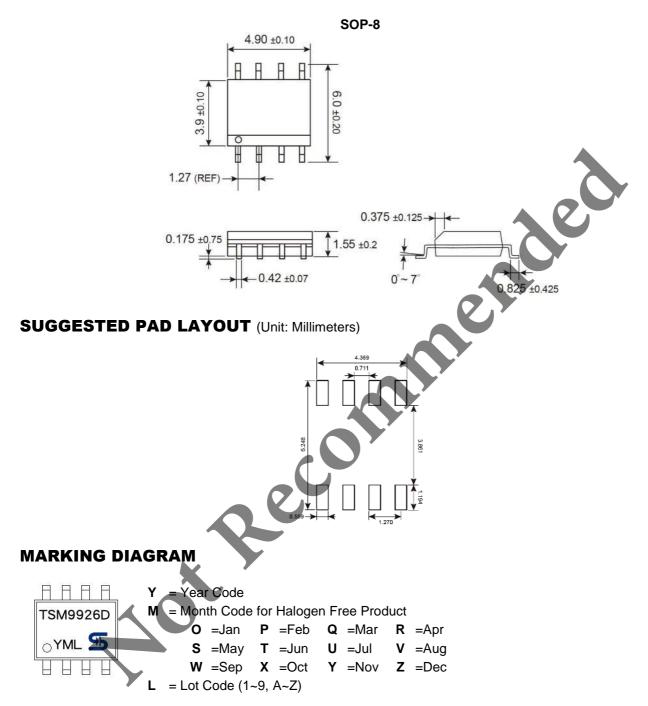
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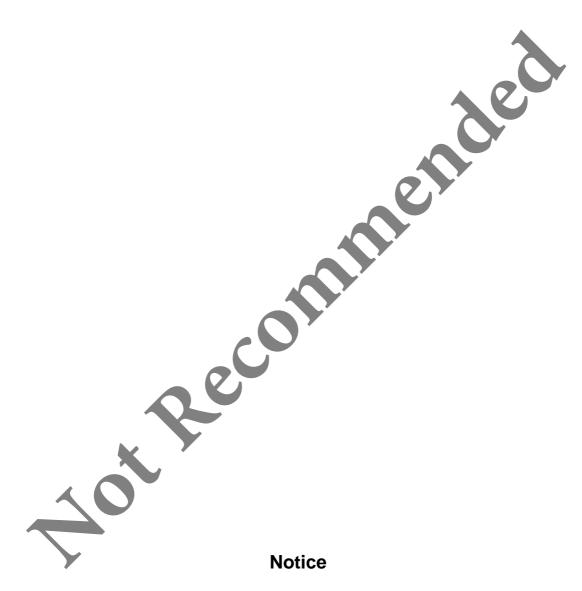




PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)







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