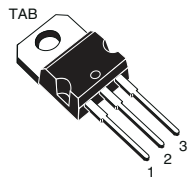
STP240N10F7

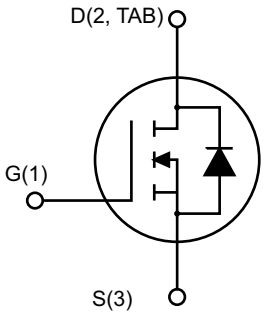
N-channel 100 V, 2.85 mΩ typ., 110 A STripFET™ F7 Power MOSFET in a TO-220 package

Datasheet - production data



TO-220

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$max.	I_D
STP240N10F7	100 V	3.2 mΩ	110 A

- Ultra low on-resistance
- 100% avalanche tested

Applications

- High current switching applications

Description

This N-channel Power MOSFET utilizes the STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packaging
STP240N10F7	240N10F7	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25°C	110	A
I_D (1)	Drain current (continuous) at T_C=100°C	110	A
I_{DM} (2)	Drain current (pulsed)	440	A
P_{TOT}	Total dissipation at T_C = 25°C	300	W
E_{AS} (3)	Single pulse avalanche energy	500	mJ
T_j	Operating junction temperature	- 55 to 175	°C
T_{stg}	Storage temperature		

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Starting T_j=25°C, I_d=45A, V_{dd}=50V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS}= 100 V			1	µA
		V_{GS} = 0, V_{DS}= 100 V, T_C= 125°C			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = +20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 60 A		2.85	3.2	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	-	11550	-	pF
C_{oss}	Output capacitance		-	2950	-	pF
C_{rss}	Reverse transfer capacitance		-	217	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 110 A, V_{GS} = 10 V (see *Figure 14*)	-	160	-	nC
Q_{gs}	Gate-source charge		-	48	-	nC
Q_{gd}	Gate-drain charge		-	38	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 90 A R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 13*, *Figure 18*)	-	49	-	ns
t_r	Rise time		-	139	-	ns
$t_{d(off)}$	Turn-off delay time		-	110	-	ns
t_f	Fall time		-	112	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		110	A
I_{SDM}(1)	Source-drain current (pulsed)		-		440	A
V_{SD}(2)	Forward on voltage	V_{GS}=0, I_{SD}=110 A	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD}=110 A, di/dt = 100 A/µs, V_{DD}=80 V, Tj=150°C (see *Figure 15*)	-	108		ns
Q_{rr}	Reverse recovery charge		-	315		nC
I_{RRM}	Reverse recovery current		-	5.8		A

1. Pulse width limited by safe operating area.
2. Pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

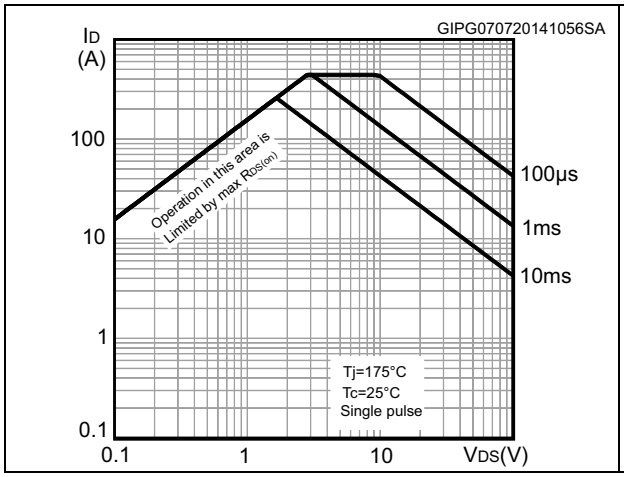


Figure 3. Thermal impedance

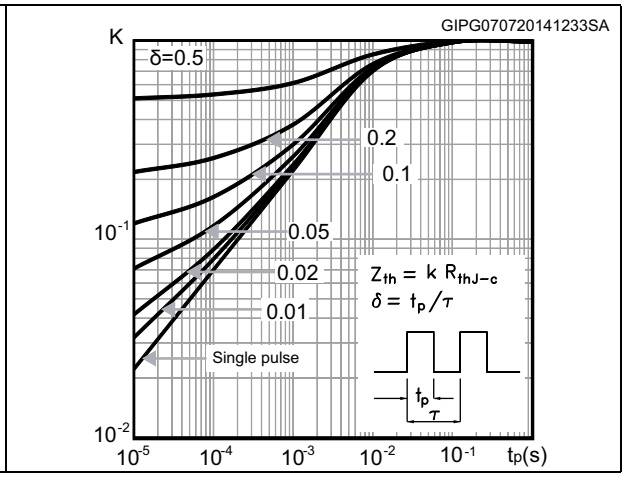


Figure 4. Output characteristics

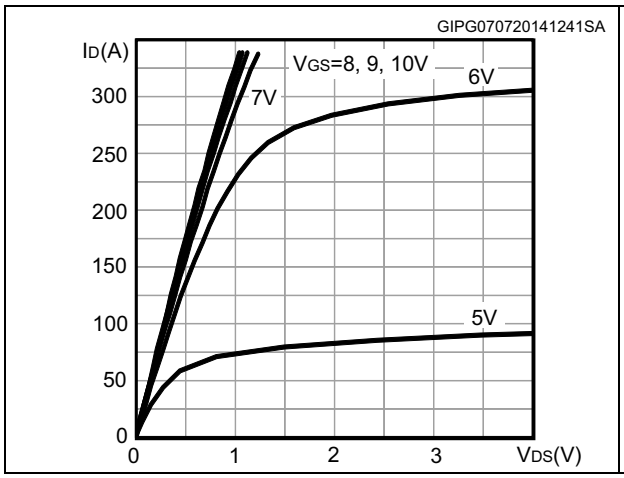


Figure 5. Transfer characteristics

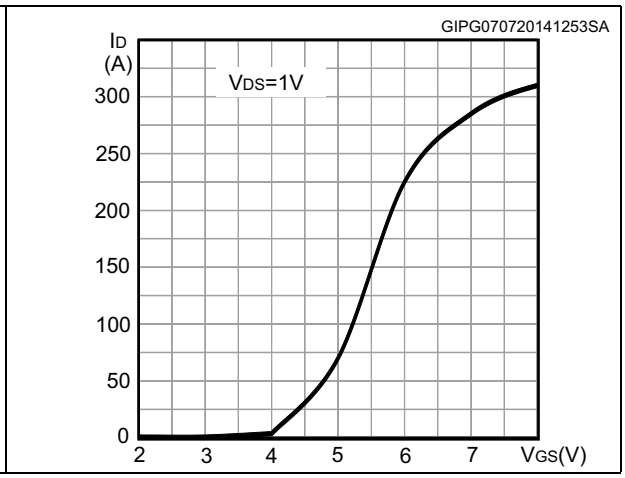


Figure 6. Gate charge vs gate-source voltage

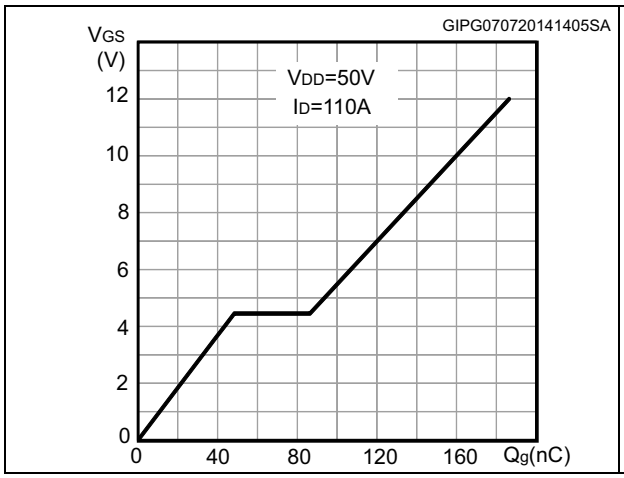


Figure 7. Static drain-source on-resistance

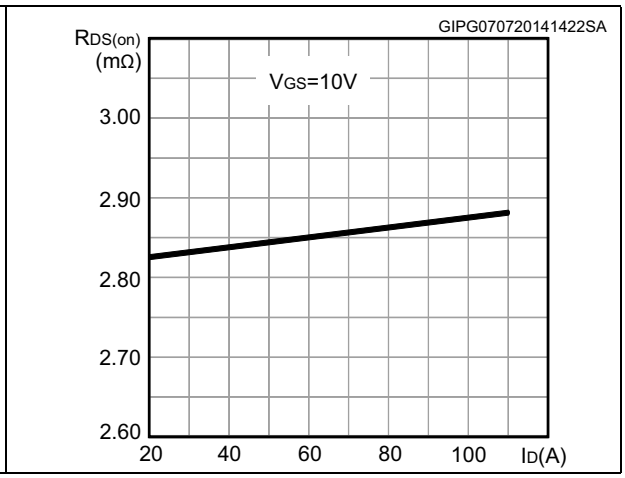


Figure 8. Capacitance variations

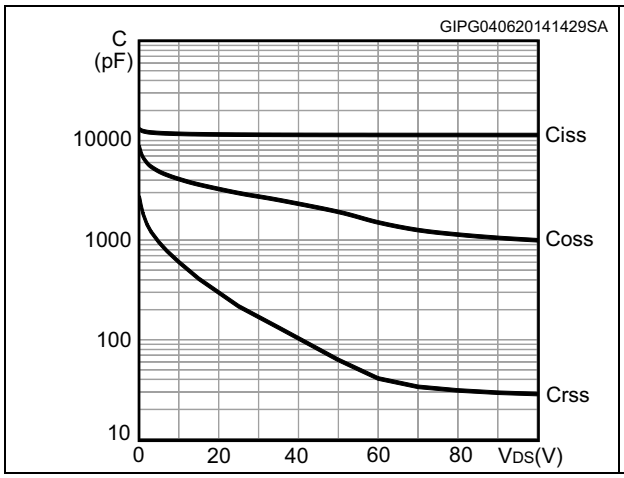


Figure 9. Normalized gate threshold voltage vs temperature

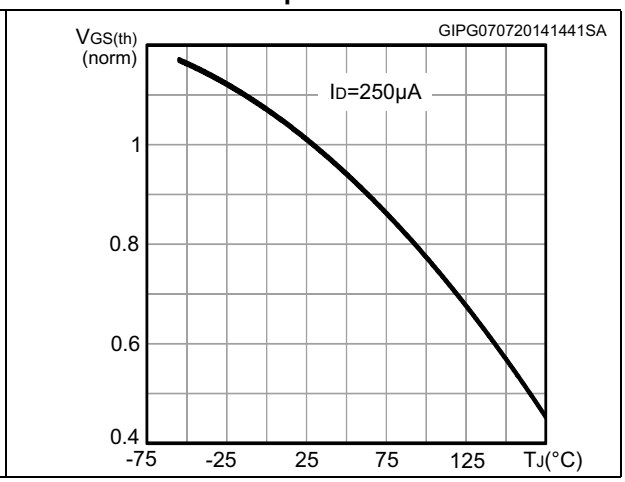


Figure 10. Normalized on-resistance vs temperature

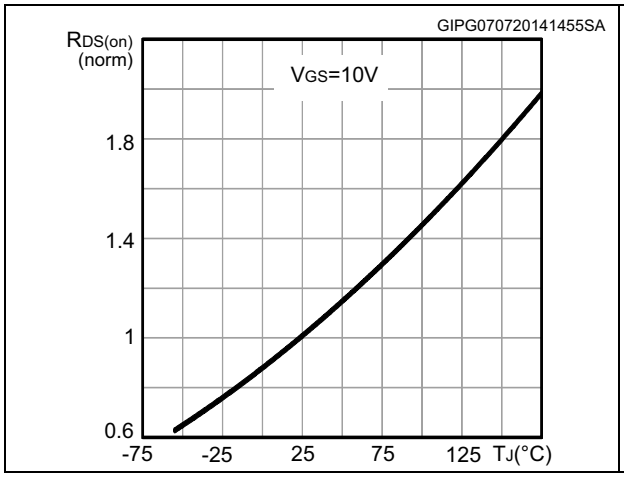


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

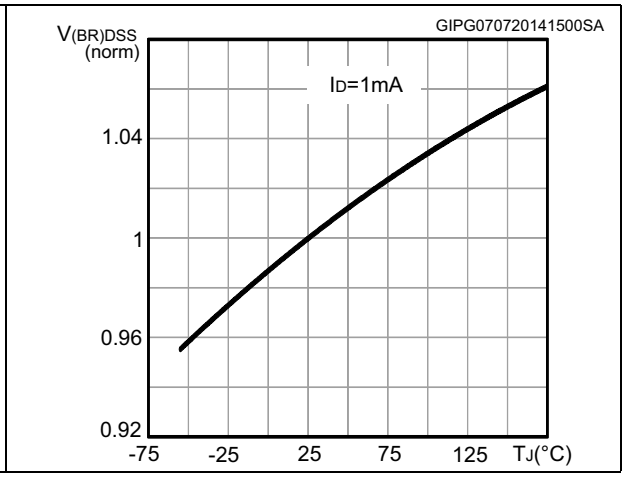
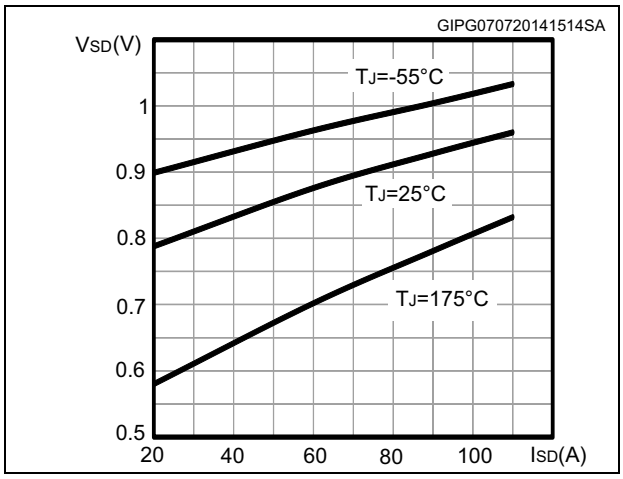


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

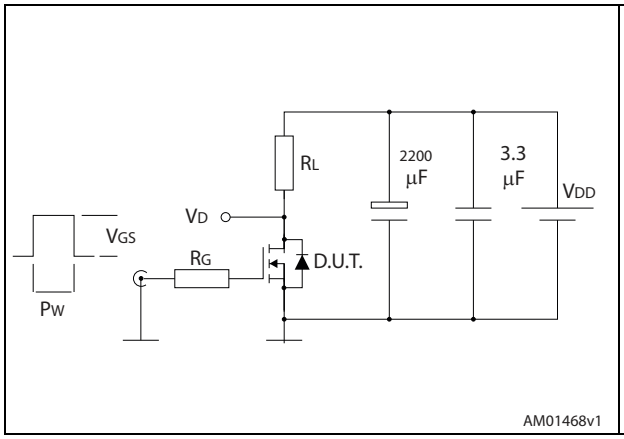


Figure 14. Gate charge test circuit

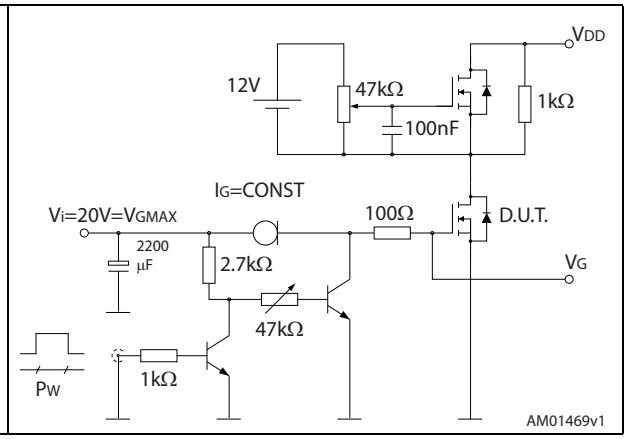


Figure 15. Test circuit for inductive load switching and diode recovery times

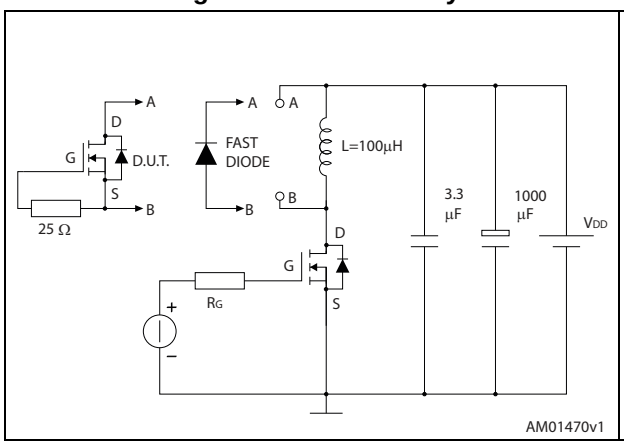


Figure 16. Unclamped inductive load test circuit

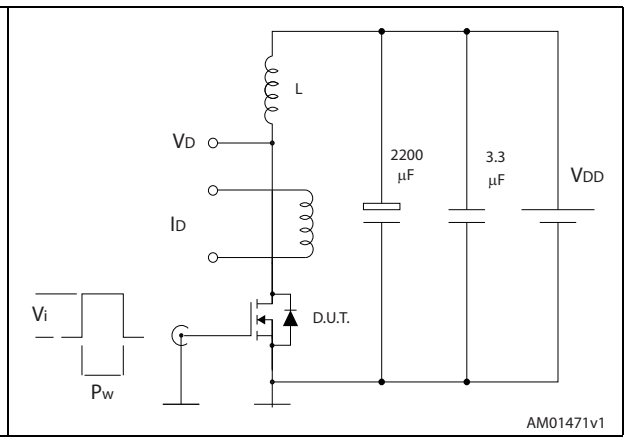


Figure 17. Unclamped inductive waveform

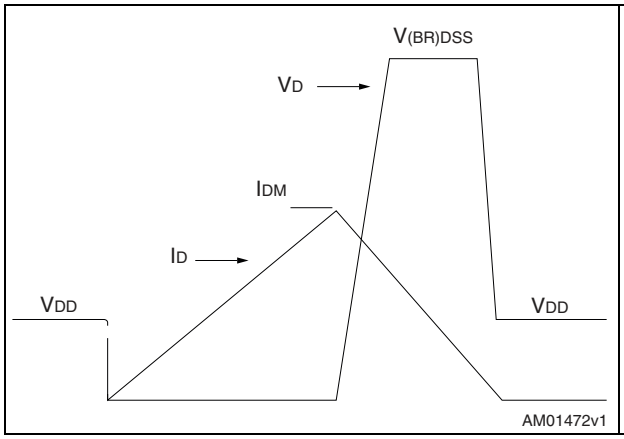
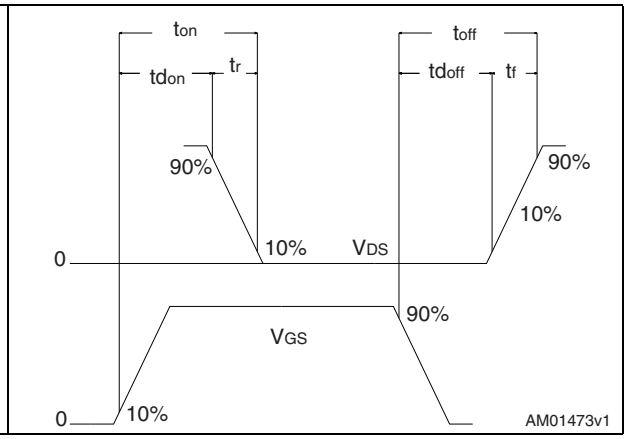


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 19. TO-220 type A drawing

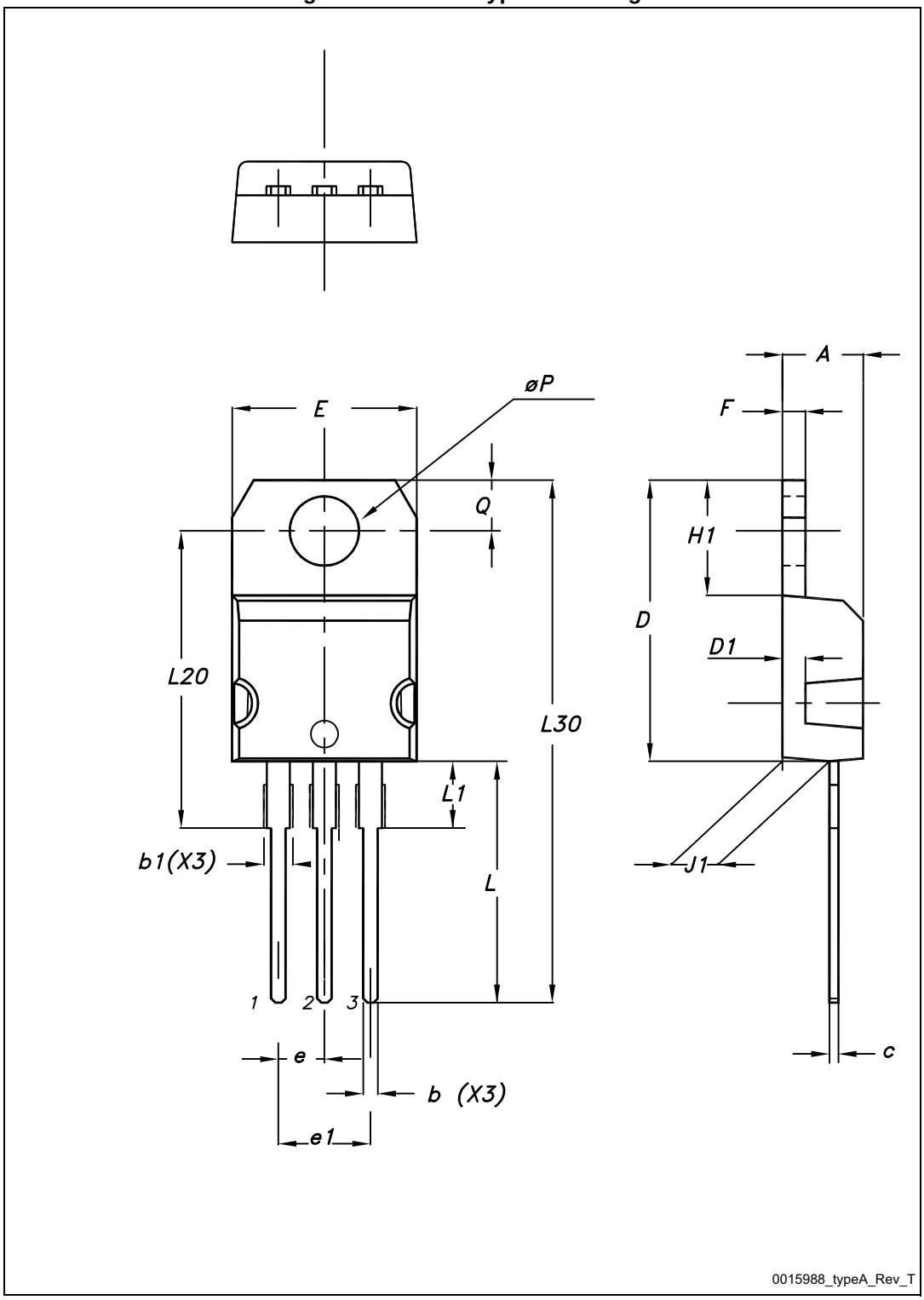


Table 8. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Nov-2012	1	Initial version.
08-Oct-2013	2	Updated $V_{GS(th)}$ typical value in *Table 4: On/off states*.
14-Jul-2014	3	– Document status promoted from preliminary data to production data – Modified: title – Modified: I_D values in cover page – Modified: I_D and I_{DM} values in *Table 2* – Added: E_{AS} value and note *3* in *Table 2* – Modified: I_{DSS}, I_{GSS} and $V_{GS(th)}$ values in *Table 4* – Modified: the entire typical values in *Table 5* and *6* – Modified: max values and I_{SD} values – Added: *Section 2.1: Electrical characteristics (curves)* – Updated: *Section 4: Package mechanical data* – Minor text changes