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BCM8156 PRODUCT Brief

MULTIRATE LOW-POWER 10G XFI TO SFI-4.1 TRANSCEIVER

FEATURES

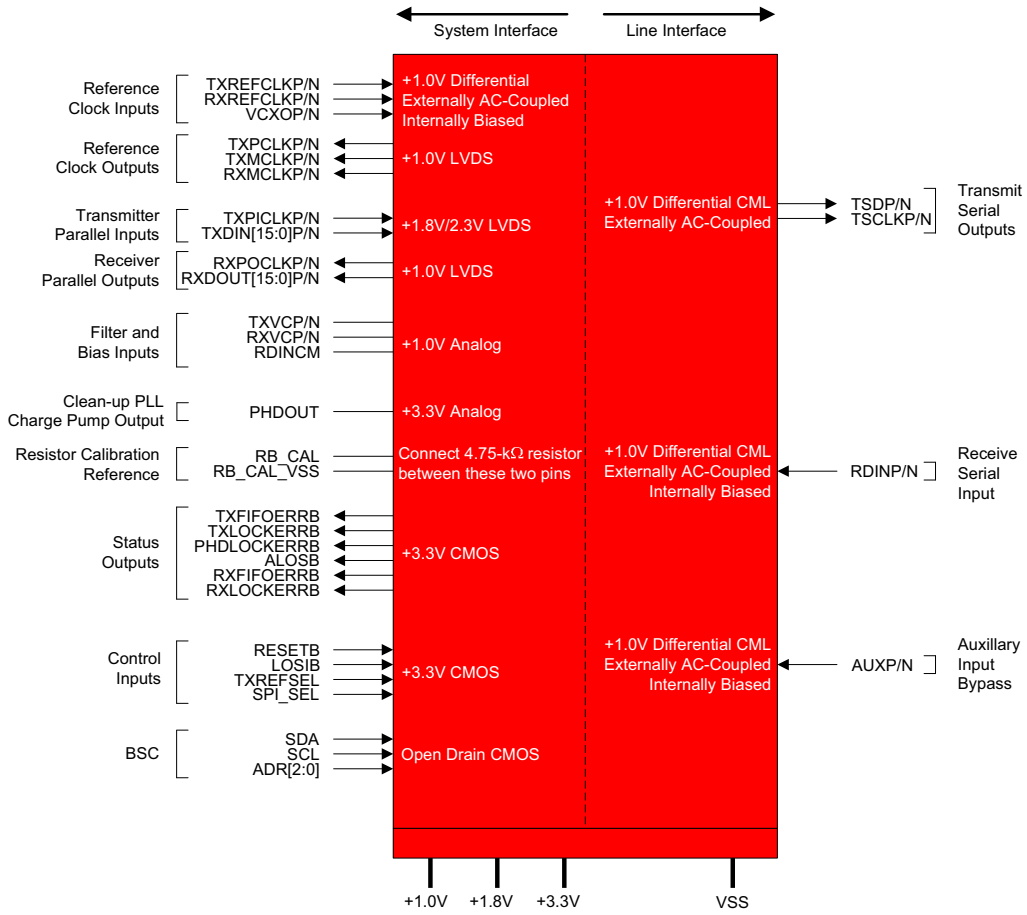
- Fully integrated multirate CDR, DEMUX, MUX, CMU
- 300-pin Multisource Agreement (MSA) compatible
- Compliant to ITU GR-253, XFP, and SFP+ specifications
- 16-bit LVDS interface compliant to Optical Internetworking Forum (OIF) SFI-4
- RX equalization for ISI compensation
- Limiting amplifier
- RX phase adjustment
- 10G serial TX preemphasis
- PRBS generator/checker for built-in self-test (BIST)
- Data rates from 9.95 Gbps to 11.352 Gbps
- Line and system loopback modes
- Receiver and transmitter serial data polarity inversion
- LVDS polarity inversion and bit order reversal
- Analog loss-of-signal output (ALOSB) and loss-of-signal input (LOSIB)
- CMU and CDR lock detect
- FIFO overflow alarm
- Reference clock: 1/16 or 1/64 of the line data rate
- Selectable RX clock and RX data squelch
- Selectable timing modes/cleanup are field configurable
- Internal phase detector and charge pump for cleanup phase-locked loop (PLL) (external VCXO required)
- Broadcom Serial Control (BSC) interface compatible with Philips® I^2C standard
- Optional SPI interface
- Core voltage, 1V
- Low-power: 650 mW

SUMMARY OF BENEFITS

- Compliant to OIF, Telcordia®, ITU-T, XFI specification, and IEEE 802.3ae standards
- Fault isolation with loopbacks, pattern generator, and checker
- Reduces design cycle and time-to-market
- High-level of integration allows for higher port density solutions.
- Lowest power SFI-4 to 10G serial transceiver
- Standard CMOS 65-nm fabrication process

APPLICATIONS

- OC-192/STM-64/10-GbE/FEC transmission equipment
- ADD/DROP multiplexers
- Digital cross-connects
- ATM switch backbone
- Terabit and edge routers
- Multi-port XFP-based designs



BCM8156 Interface Block Diagram

The BCM8156 is a fully integrated MSA-compatible multirate SONET/SDH/10-GbE/Fibre-Channel/FEC transceiver operating at 9.953 Gbps, 10.3125 Gbps, 10.519 Gbps, 10.664 Gbps, 10.709 Gbps, 11.095 Gbps, 11.318 Gbps, or 11.352 Gbps. On-chip clock synthesis is performed by the high-frequency, low-jitter PLL, allowing the use of a low-frequency reference clock selectable to the line rate divided by either 16 or 64. The 10G TX clock phase is adjustable for clocked driver applications. An on-chip phase detector and charge pump plus external VCXO implement a cleanup PLL. The cleanup PLL can be used to attenuate jitter on the CDR recovered clock for loop timing applications or to provide a low-jitter reference clock from a noisy system clock. Any SONET timing mode may be configured with the new BCM8156 timing architecture, making the timing mode and cleanup functions user-selectable in the field rather than during manufacturing, therefore, simplifying engineering and manufacturing requirements.

New features added to the BCM8156 include:

- PRBS generator/checker for BIST
- 10G RX equalization for ISI compensation
- 10G TX preemphasis
- BSC interface (compatible with Philips I^2C standard) or optional SPI interface

The low-jitter LVDS interface guarantees compliance with the bit error rate requirements of the Telcordia (formerly Bellcore), ANSI, and ITU-T standards. The BCM8156 is offered in two different packages:

1. 15 mm x 15 mm, 301-pin BGA compatible with the BCM8152 (0.8-mm ball pitch)
2. 15 mm x 15 mm, 196-pin BGA (1-mm ball pitch)

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