- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Output Circuitry
- Highly Stable Operation over Specified Temperature and/or Supply Voltage Ranges

DEVICE	SIMILAR	NUMBER	COMP'L	ENABLE	RANGE	В
TYPE	то	VCO's	Z OUT	ENABLE	INPUT	R <sub>ext</sub>
'LS624	'LS324	single	yes	yes	yes	no
'LS625	'LS325	dual	yes	no	no	no
'LS626	'LS326	dual	yes	yes	no	no
'LS627	'LS327	dual	no	no	no	no
'LS628	'LS324	single	yes	yes	yes	yes
'LS629	'LS124	dual	no	yes	yes	no

#### description

These voltage-controlled oscillators (VCOs) are improved versions of the original VCO family: SN54LS124, SN54LS324 thru SN54LS327, SN74LS124, and SN74LS324 thru SN74LS327. These new devices feature improved voltage-to-frequency linearity, range, and compensation. With the exception of the 'LS624 and 'LS628, all of these devices feature two independent VCOs in a single monolithic chip. The 'LS624, 'LS625, 'LS626, and 'LS628 have complementary Z outputs. The output frequency for each VCO is established by a single external component (either a capacitor or crystal) in combination with voltage-sensitive inputs used for frequency control and frequency range. Each device has a voltage-sensitive input for frequency control; however, the 'LS624, 'LS628, and 'LS629 devices also have one for frequency range. (See Figures 1 thru 6).

The 'LS628 offers more precise temperature compensation than its 'LS624 counterpart. The 'LS624 features a 600 ohm internal timing resistor. The 'LS628 requires a timing resistor to be connected externally across R<sub>ext</sub> pins. Temperature compensation will be improved dur to the temperature coefficient of the external resistor.

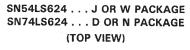
Figure 3 and Figure 6 contain the necessary information to choose the proper capacitor value to obtain the desired operating frequency.

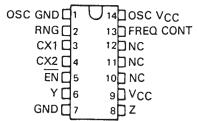
A single 5-volt supply can be used: however, one set of supply voltage and ground pins ( $V_{CC}$  and GND) is provided for the enable, synchronization-gating, and output sections, and a separate set (OSC  $V_{CC}$  and OSC GND) is provided for the oscillator and associated frequency-control circuits so that effective isolation can be accomplished in the system. For operation of frequencies greater than 10 MHz, it is recommended that two independent supplies be used. Disabling either VCO of the 'LS625 and 'LS625 and 'LS627 can be achieved by removing the appropriate OSC  $V_{CC}$ . An enable input is provided on the 'LS624, 'LS626, 'LS628, and 'LS629. When the enable input is low, the output is enabled: when the enable input is high, the internal oscillator is disabled, Y is high, and Z is low. Caution! Crosstalk may occur in the dual devices ('LS625, 'LS626, 'LS627 and 'LS629) when both VCOs are operated simultaneously. To minimize crosstalk, either of the following are recommended: (A) If frequencies are widely separated, use a 10- $\mu$ h inductor between  $V_{CC}$  pins. (B) If frequencies are closely spaced, use two separate  $V_{CC}$  supplies or place two series diodes between the  $V_{CC}$  pins.

The pulse-synchronization-gating section ensures that the first output pulse is neither clipped nor extended. The duty cycle of the square-wave output is fixed at approximately 50 percent.

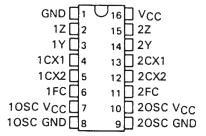
The SN54LS624 thru SN54LS629 are characterized for operation over the full military temperature range of  $-55\,^{\circ}$ C to 125 °C. The SN74LS624 thru SN74LS629 are characterized for operation from 0 °C to 70 °C.



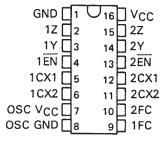




#### SN54LS625 . . . J OR W PACKAGE SN74LS625 . . . D OR N PACKAGE (TOP VIEW)

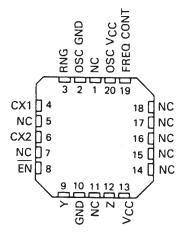


#### SN54LS626 . . . J OR W PACKAGE SN74LS626 . . . D OR N PACKAGE (TOP VIEW)

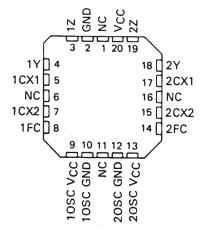


NC - No internal connection

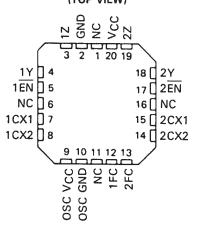
# SN54LS624 . . . FK PACKAGE (TOP VIEW)



# SN54LS625 . . . FK PACKAGE (TOP VIEW)

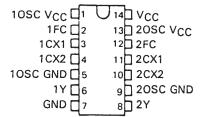


# SN54LS626 . . . FK PACKAGE (TOP VIEW)

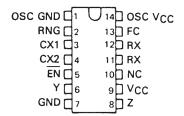




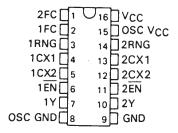
SN54LS627 . . . J OR W PACKAGE SN74LS627 . . . D OR N PACKAGE (TOP VIEW)



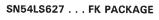
SN54LS628 . . . J OR W PACKAGE SN74LS628 . . . D OR N PACKAGE (TOP VIEW)

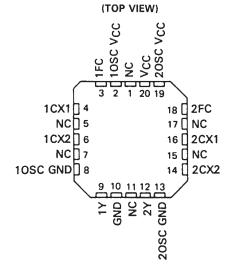


SN54LS629 . . . J OR W PACKAGE SN74LS629 . . . D OR N PACKAGE (TOP VIEW)

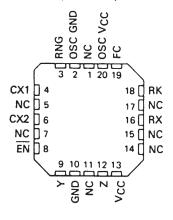


NC-No internal connection

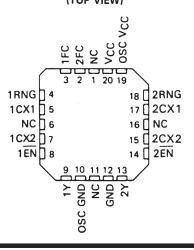




# SN54LS628 . . . FK PACKAGE (TOP VIEW)

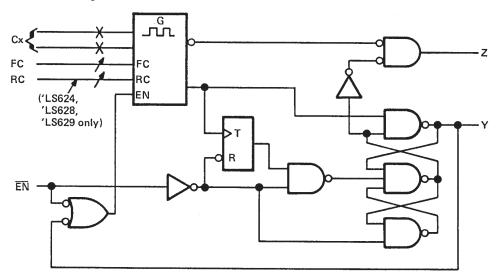


# SN54LS629 . . . FK PACKAGE (TOP VIEW)

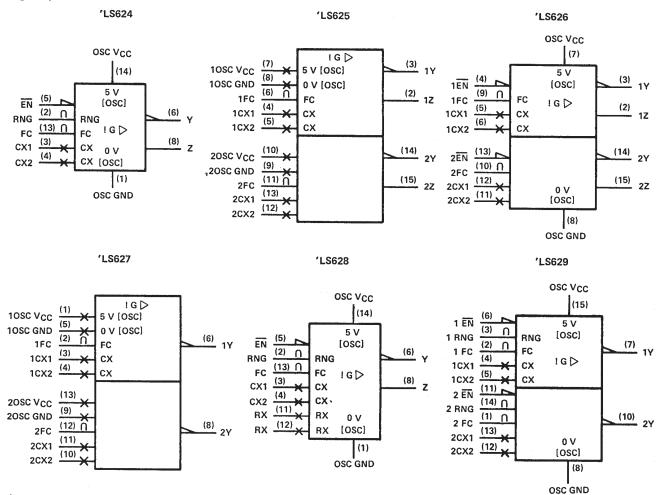




### logic diagram (positive logic)



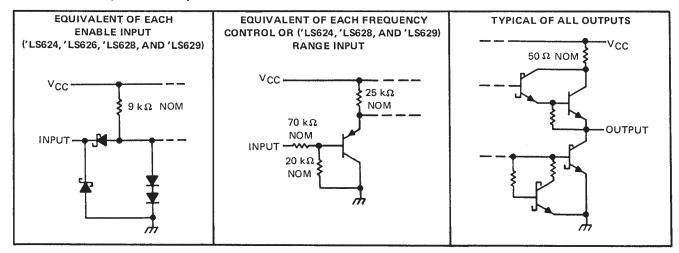
#### logic symbols†



<sup>&</sup>lt;sup>†</sup>These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.



### schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Notes 1 and 2)	V
Input voltage: Enable input <sup>†</sup>	V
Frequency control or range input‡	C
Operating free-air temperature range: SN54LS' Circuits	C
SN74LS' Circuits	'C
Storage temperature range	'C

<sup>†</sup> The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.

NOTE: 1. Voltage values are with respect to the appropriate ground terminal.



<sup>‡</sup> The range input is provided only on 'LS624, 'LS628, and 'LS629.

<sup>2.</sup> Throughout the data sheet, the symbol V<sub>CC</sub> is used for the voltage applied to both the V<sub>CC</sub> and OSC V<sub>CC</sub> terminals, unless otherwise noted.

## SN54LS624 THRU SN54LS629, **SN74LS624 THRU SN74LS629** VOLTAGE-CONTROLLED OSCILLATORS

SDLS186 - JANUARY 1980 - REVISED MARCH 1988

#### recommended operating conditions

	SN54LS'			SN74LS'			LINUT
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
Input voltage at frequency control or range input, V <sub>I(freq)</sub> or V <sub>I(rng)</sub>	0		5	0		5	V
High-level output current, IOH			-1.2			-1.2	mA
Low-level output current, IOL			12			24	mA
Output frequency, fo	1			1			Hz
Surper frequency, 10			20			20	MHz
Operating free-air temperature, TA	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†				SN54LS	3						
	FARAME	IEN	1531	1EST CONDITIONS			TYP‡	MAX	MIN	TYP‡	MAX	UNIT	
VIH	High-level inpu voltage at ena					2			2			٧	
VIL	Low-level inpu voltage at ena							0.7			0.8	V.	
VIK	Input clamp vo	ltage at enable#	VCC = MIN,	$I_1 = -18 \text{ mA}$				-1.5		•	-1.5	V	
Vон	High-level outp	out voltage	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -1.2 mA,	EN at V <sub>IL</sub> ma See Note 3	ıx,	2.5	3.4		2.7	3.4		٧	
VOL	Low-level outp	ut voltage	VCC = MIN, EN at V <sub>IL</sub> max,	See Note 3	I <sub>OL</sub> = 12 mA		0.25	0.4		0.25 0.35	0.5	V	
41	Input current	Freq control or range¶	V <sub>CC</sub> = MAX		V <sub>1</sub> = 5 V V <sub>1</sub> = 1 V		50 10	250 50		50 10	250 50	μΑ	
lj	Input current at maximum input voltage	Enable#	VCC = MAX,	V <sub>I</sub> = 7 V				0,2			0.2	mA	
ЧΗ	High-level input current	Enable#	VCC = MAX,	V <sub>I</sub> = 2.7 V			·	40			40	μА	
ЦL	Low-level input current	Enable#	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 0.4 V				-0.8			-0.8	mA	
los	Short-circuit output current §		V <sub>CC</sub> = MAX	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		-40		-225	-40		-225	mA	
					'LS624		20	35		20	35		
			V <sub>CC</sub> = MAX,		'LS625		'35	55		35	55	1	
Icc	Supply current	•	Enable# = 4.5 V		'LS626		35	55		35	55	]	
	VCC and OSC	VCC pins	See Note 4		'LS627		35	55		35	55	mA	
			'LS628			ļ	20 35	35		20	35	]	
				'LS				55		35	55		

<sup>&</sup>lt;sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



 $<sup>^{\</sup>ddagger}$ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C.

Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

 $<sup>\</sup>P$ The range input is provided only on the 'LS624, 'LS628, and 'LS629.

<sup>\*</sup>The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.

NOTES: 3.  $V_{OH}$  for Y outputs and  $V_{OL}$  for Z outputs are measured while enable inputs are at  $V_{IL}$  MAX, with individual 1-k $\Omega$  resistors connected from CX1 to VCC and from CX2 to ground. The resistor connections are reversed for testing VOH for Z outputs and VOL for Y inputs.

<sup>4.</sup> For 'LS624, 'LS626, 'LS628, and 'LS629, ICC is measured with the outputs disabled and open. For 'LS625 and 'LS627, ICC is measured with one OSC VCC = MAX, and with the other OSC VCC and outputs open.

## switching characteristics, V<sub>CC</sub> = 5 V (unless otherwise noted), R<sub>L</sub> = 667 $\Omega$ , C<sub>L</sub> = 45 pF, T<sub>A</sub> = 25 °C

PARAMETER		TE	ST CONDITIONS	'LS624,	'LS628	B, 'LS629	'LS625,			
· Anamatan				MIN	TYP	MAX	MIN	TYP	MAX	UNIT
		C <sub>ext</sub> = 50 pF	$V_{I(freq)} = 5 V, V_{I(rng)} = 0 V$	15	20	25				
fo	Output frequency		$V_{I(freq)} = 1 V, V_{I(rng)} = 5 V$	1.1	1.6	2.1				1
			V <sub>i(freq)</sub> = 5 V				7	9.5	12	MHz
			V <sub>1(freq)</sub> = 0 V				0.9	1.2	1.5	1

#### TYPICAL CHARACTERISTICS

'LS624, 'LS628, 'LS629 OUTPUT FREQUENCY

FREQUENCY-CONTROL INPUT VOLTAGE†

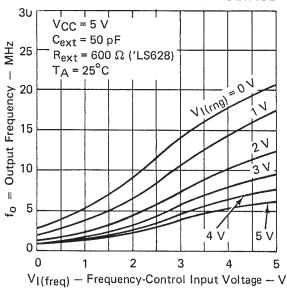
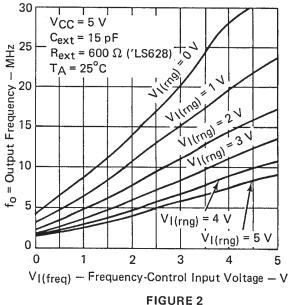


FIGURE 1

'LS624, 'LS628, 'LS629 OUTPUT FREQUENCY

FREQUENCY-CONTROL INPUT VOLTAGE†



†Due to the effects of stray capacitance the output frequency may be unstable when the frequency control voltage is less than 1 volt.

#### TYPICAL CHARACTERISTICS

**OUTPUT FREQUENCY** EXTERNAL CAPACITANCE 100 M VCC = 5 V ₩ 10 M  $T_A = 25^{\circ}C$ -Output Frequency 1 M 100 K 10 k 1 k 100 ٩ 10 10-11 10-10 10-9 10-8 10-7 10-6 10-5

'LS624, 'LS628, 'LS629

'LS625, 'LS626, 'LS627

Cext - External Capacitance - F

FIGURE 3

**OUTPUT FREQUENCY** 

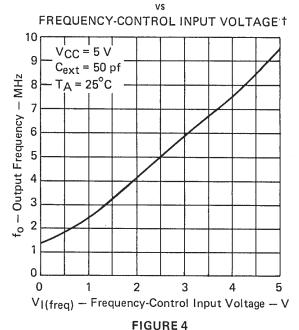
FREQUENCY-CONTROL INPUT VOLTAGE

30
VCC = 5 V
Cext = 15 pF
TA = 25°C

1 20
0 1 2 3 4 5
VI(freq) - Frequency-Control Input Voltage - V

FIGURE 5

'LS625, 'LS626, 'LS627 OUTPUT FREQUENCY



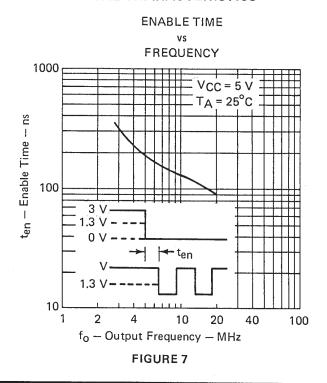
'LS625, 'LS626, 'LS627 OUTPUT FREQUENCY

**EXTERNAL CAPACITANCE** 100 M 10 M HZ  $V_{I(freq)} = 5 V$ 1 1 M  $V_{I(freq)} = 2.5 V$ Output Frequency 100 k 10 k 1 k  $V_{I(freq)} = 0 V_{I}$ 100  $V_{CC} = 5 V$ 10  $T_A = 25^{\circ}C$ 10-11 10-10 10-9 10-8 10-7 10-6 Cext - External Capacitance - F FIGURE 6

† Due to the effects of stray capacitance the output frequency may be unstable when the frequency control voltage is less than 1 volt.



### TYPICAL CHARACTERISTICS



#### TYPICAL APPLICATIONS DATA

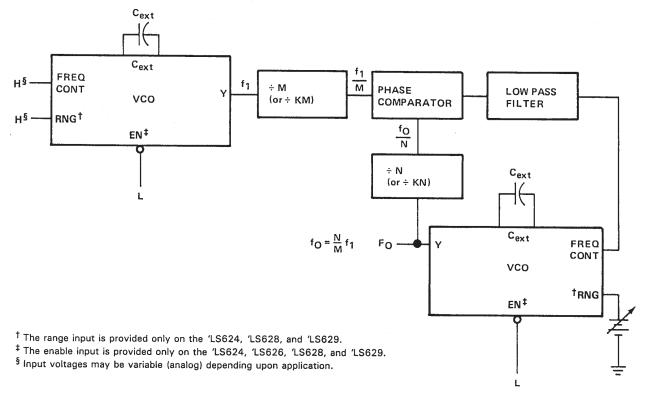


FIGURE A-PHASE-LOCKED LOOP.

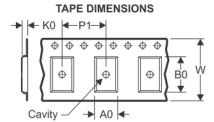


PACKAGE MATERIALS INFORMATION

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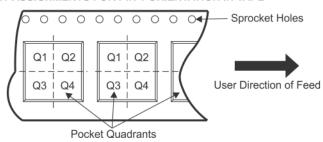
### TAPE AND REEL INFORMATION





		Dimension designed to accommodate the component width
		Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
1	P1	Pitch between successive cavity centers

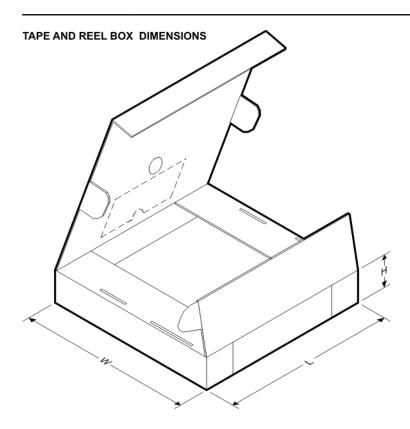
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All differsions are normal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS624DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS624NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS628DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

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\*All dimensions are nominal

7 till diffrierene die Freihinds							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS624DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS624NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74LS628DR	SOIC	D	14	2500	367.0	367.0	38.0

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