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$\frac{\text{MOSFET}}{\text{SUPERFET}^{\text{@}}} - \text{Single N-Channel,} \\ \text{SUPERFET}^{\text{@}} \text{III, FRFET}^{\text{@}} \\ \text{650 V, 30 A, 110 m} \\ \Omega$

NVH4L110N65S3F

Features

- Ultra Low Gate Charge & Low Effective Output Capacitance
- Lower FOM (R_{DS(on) max.} x Q_{g typ.} & R_{DS(on) max.} x E_{OSS})
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	650	V
Gate-to-Source Voltage - DC	V_{GSS}	±30	V
Gate-to-Source Voltage - AC (f > 1 Hz)	V_{GSS}	±30	V
Drain Current – Continuous (T _C = 25°C)	I _D	30	Α
Drain Current – Continuous (T _C = 100°C)	I _D	19.5	Α
Drain Current – Pulsed (Note 3)	I _{DM}	69	Α
Power Dissipation (T _C = 25°C)	P_{D}	240	W
Power Dissipation – Derate Above 25°C	P_{D}	1.92	W/°C
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C
Single Pulsed Avalanche Energy (Note 4)	E _{AS}	380	mJ
Repetitive Avalanche Energy (Note 3)	E _{AR}	2.4	mJ
MOSFET dv/dt	dv/dt	100	V/ns
Peak Diode Recovery dv/dt (Note 5)	dv/dt	50	V/ns
Max. Lead Temperature for Soldering Purposes (1/8" from case for 5 s)	TL	300	°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max. (Notes 1, 2)	$R_{\theta JC}$	0.52	°C/W
Thermal Resistance, Junction-to-Ambient, Max. (Notes 1, 2)	$R_{\theta JA}$	40	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

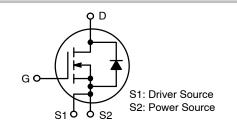
- The entire application environment impacts the thermal resistance values shown.
 They are not constants and are only valid for the particular conditions noted.
- Assembled to an infinite heatsink with perfect heat transfer from the case (assumes 0 K/W thermal interface).
- 3. Repetitive rating: pulse-width limited by maximum junction temperature.
- 4. $I_{AS} = 3.5 \text{ A}$, $R_G = 25 \Omega$, starting $T_J = 25^{\circ}\text{C}$.
- 5. $I_{SD} \le 15$ A, di/dt ≤ 200 A/ μ s, $V_{DD} \le 400$ V, starting $T_J = 25$ °C.



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V _{DSS}	R _{DS(ON)} MAX	I _D MAX
650 V	650 V 110 mΩ @ 10 V	



POWER MOSFET

MARKING DIAGRAM



TO-247-4LD CASE 340CJ



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)

&K = Lot

NVH4L110N65S3F = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NVH4L110N65S3F	TO-247-4LD (Pb-Free)	30 Units / Tube

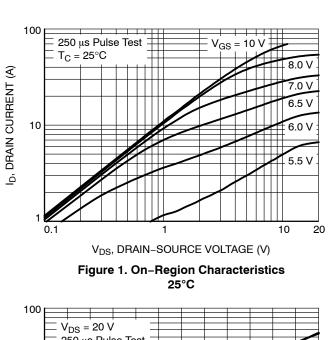
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
OFF CHARACTERISTICS				•	•	
Drain-to-Source Breakdown Voltage	BV _{DSS}	$V_{GS} = 0 \text{ V, } I_D = 1 \text{ mA, } T_J = 25^{\circ}\text{C}$	650			V
Drain-to-Source Breakdown Voltage	BV _{DSS}	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 150^{\circ}\text{C}$	700			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_{J}$	I _D = 20 mA, Referenced to 25°C		610		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 650 V			10	μΑ
		$V_{DS} = 520 \text{ V}, T_{C} = 125^{\circ}\text{C}$		44		
Gate-to-Body Leakage Current	I _{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS	,		•			•
Gate Threshold Voltage	V _{GS(th)}	$V_{GS} = V_{DS}, I_D = 0.74 \text{ mA}$	3.0		5.0	V
Threshold Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T_J$	$V_{GS} = V_{DS}, I_D = 0.74 \text{ mA}$		-9.2		mV/°C
Static Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A		93	110	mΩ
Forward Transconductance	9 _{FS}	$V_{DS} = 20 \text{ V}, I_D = 15 \text{ A}$		17		S
DYNAMIC CHARACTERISTICS					!	1
Input Capacitance	C _{iss}			2530		pF
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 400 \text{ V}, f = 1 \text{ MHz}$		55.4		
Reverse Transfer Capacitance	C _{rss}			7.5		
Effective Output Capacitance	C _{oss(eff.)}	$V_{DS} = 0 \text{ V to } 400 \text{ V}, V_{GS} = 0 \text{ V}$		512		pF
Energy Related Output Capacitance	C _{oss(er.)}	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		96		pF
Total Gate Charge at 10 V	Q _{G(TOT)}			59		nC
Threshold Gate Charge	Q _{G(TH)}	$V_{GS} = 10 \text{ V}, V_{DS} = 400 \text{ V}, I_D = 15 \text{ A}$		11		
Gate-to-Source Gate Charge	Q _{GS}	(Note 6)		18		
Gate-to-Drain "Miller" Charge	Q_{GD}			24		
Equivalent Series Resistance	ESR	f = 1 MHz		1.6		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t _{d(on)}			24.6		ns
Turn-On Rise Time	t _r	$V_{GS} = 10 \text{ V}, V_{DD} = 400 \text{ V},$		16.4		ns
Turn-Off Delay Time	t _{d(off)}	$I_D = 15 \text{ A}, R_g = 4.7 \Omega$ (Note 6)		59.5		ns
Turn-Off Fall Time	t _f			6.4		ns
SOURCE-DRAIN DIODE CHARACTER	ISTICS					
Maximum Continuous Source-to- Drain Diode Forward Current	I _S	V _{GS} = 0 V			30	Α
Maximum Pulsed Source-to-Drain Diode Forward Current	I _{SM}	V _{GS} = 0 V			69	Α
Source-to-Drain Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _{SD} = 15 A			1.3	V
Reverse Recovery Time	t _{rr}			89.2		ns
Charge Time	ta	$V_{GS} = 0 \text{ V, } dI_F/dt = 100 \text{ A/}\mu\text{s,}$		78.2		
Discharge Time	t _b	I _{SD} = 15 A		11.5		
Reverse Recovery Charge	Q _{rr}			312		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

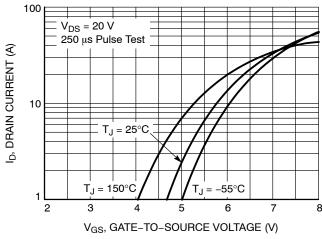
6. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS



100 250 μ s Pulse Test $V_{GS} = 10 \text{ V}$ $V_{GS} = 10 \text{ V}$

Figure 2. On–Region Characteristics 150°C



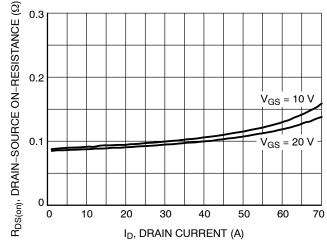
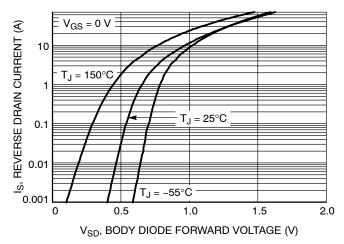


Figure 3. Transfer Characteristics

Figure 4. On-Resistance Variation vs. Drain Current and Gate Voltage



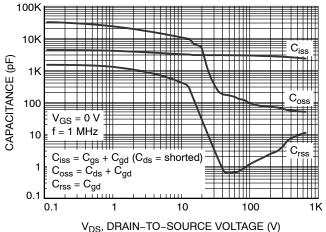


Figure 5. Body Diode Forward Voltage Variation vs. Source Current and Temperature

Figure 6. Capacitance Characteristics

TYPICAL CHARACTERISTICS

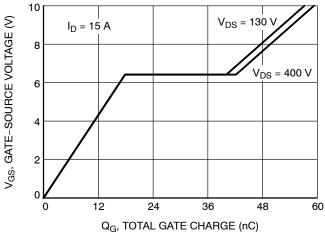


Figure 7. Gate Charge Characteristics

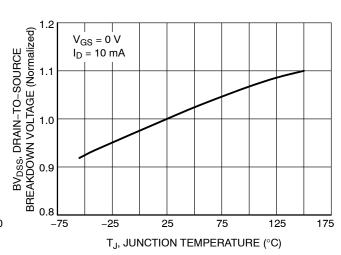


Figure 8. Breakdown Voltage Variation vs. Temperature

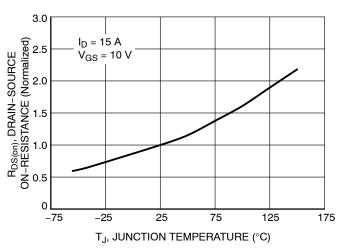


Figure 9. On-Resistance Variation vs. Temperature

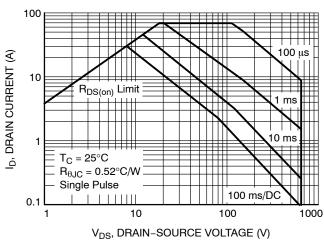


Figure 10. Maximum Safe Operating Area

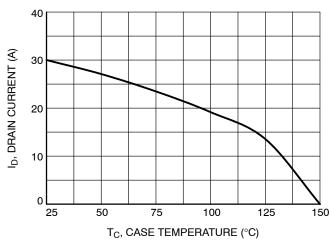


Figure 11. Maximum Drain Current vs. Case Temperature

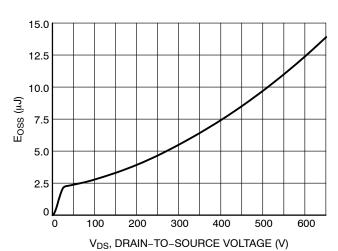
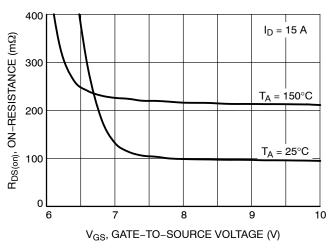


Figure 12. E_{OSS} vs. Drain-to-Source Voltage

TYPICAL CHARACTERISTICS



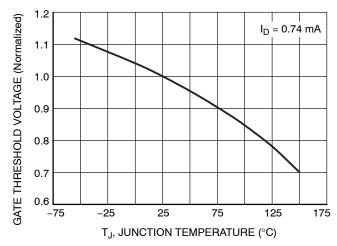


Figure 13. R_{DS(on)} vs. Gate Voltage

Figure 14. Normalized Gate Threshold Voltage vs. Temperature

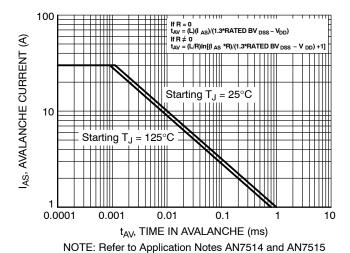


Figure 15. Unclamped Inductive Switching

Capability

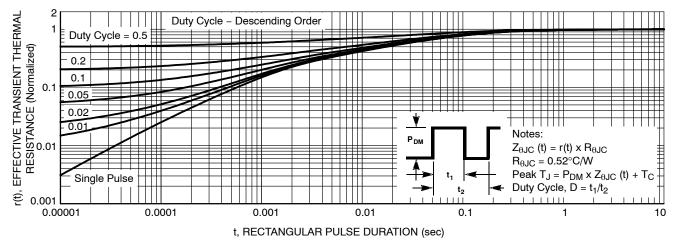


Figure 16. Transient Thermal Response

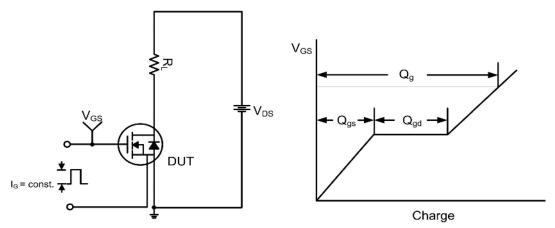


Figure 17. Gate Charge Test Circuit & Waveform

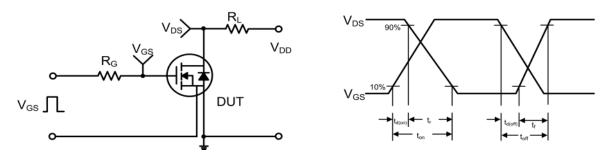


Figure 18. Resistive Switching Test Circuit & Waveforms

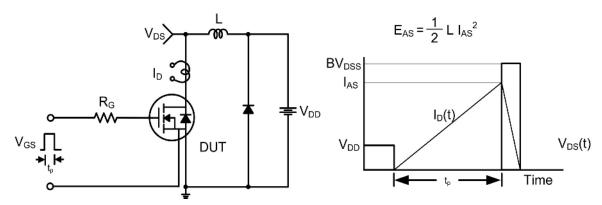


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms

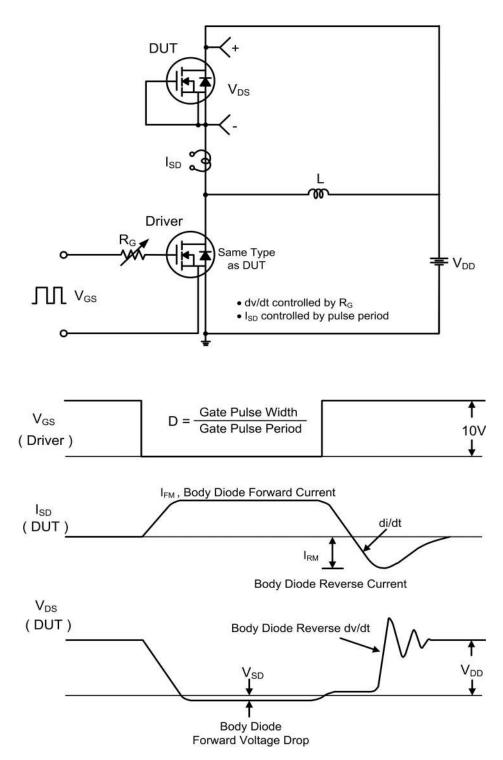
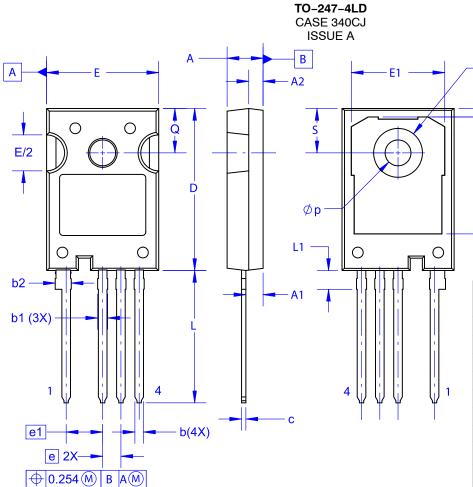


Figure 20. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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DIM	MILLIMETERS		
DIM	MIN	NOM	MAX
Α	4.80	5.00	5.20
A1	2.10	2.40	2.70
A2	1.80	2.00	2.20
b	1.07	1.20	1.33
b1	1.20	1.40	1.60
b2	2.02	2.22	2.42
С	0.50	0.60	0.70
D	22.34	22.54	22.74
D1	16.00	16.25	16.50
D2	0.97	1.17	1.37
е	2.54 BSC		
e1	5.08 BSC		
E	15.40	15.60	15.80
E1	12.80	13.00	13.20
E/2	4.80	5.00	5.20
L	18.22	18.42	18.62
L1	2.42	2.62	2.82
р	3.40	3.60	3.80
p1	6.60	6.80	7.00
Q	5.97	6.17	6.37
S	5.97	6.17	6.37

 \emptyset p1

D1

D2

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