AK4495S/95

Quality-oriented Premium 32-Bit 2ch DAC

1. General Description

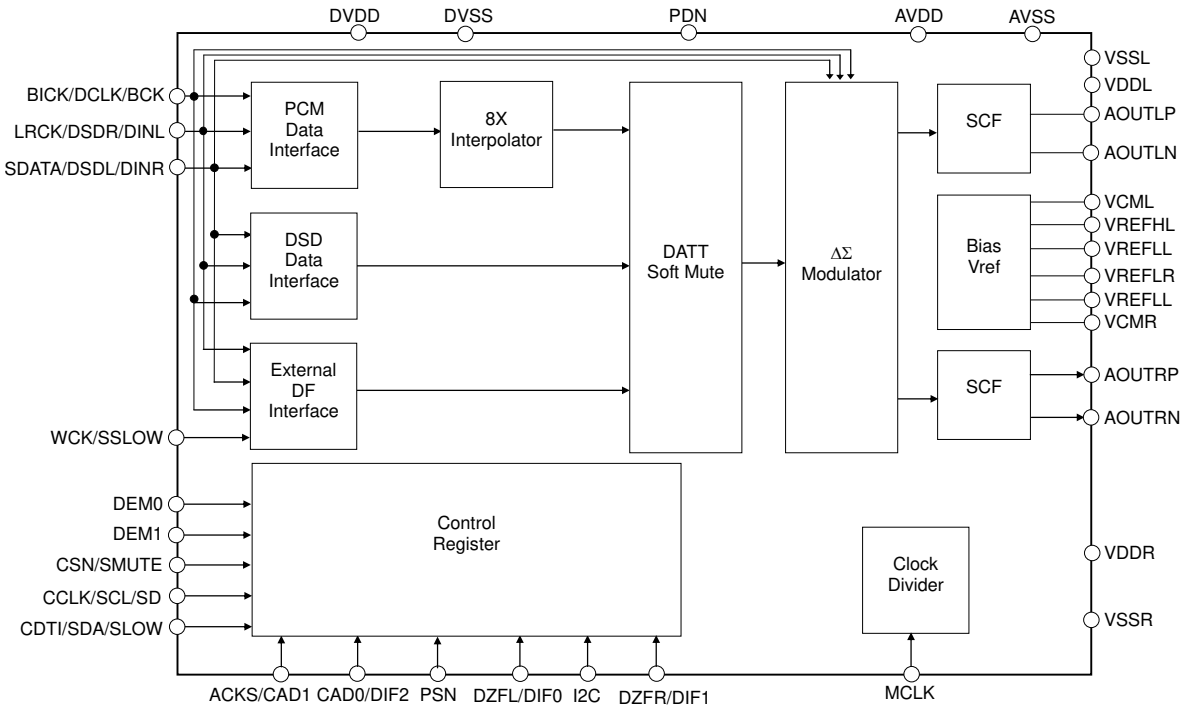
The AK4495S/95 is a 32-bit DAC, which corresponds to high-performance, high sound quality digital audio systems such as DVD-Audio and BD. An internal circuit includes newly developed 32-bit digital filters for better sound quality, achieving low distortion characteristics and wide dynamic range. The AK4495S/95 has full differential SCF outputs, removing the need for AC coupling capacitors and increasing performance for systems with excessive clock jitter. The AK4495S/95 accepts up to 768kHz PCM data and 5.6MHz DSD data, ideal for a wide range of applications including Network Audio and SACD.

2. Features

- **128x Over sampling**
- **Sampling Rate: 30kHz ~ 768kHz**
- **32-bit 8x Digital Filter**
  - **Ripple: ±0.005dB, Attenuation: 100dB**
  - **Short Delay Sharp Roll-off, GD=6.25/fs**
  - **Short Delay Slow Roll-off, GD=5.3/fs**
  - **Sharp Roll-off**
  - **Slow Roll-off**
  - **Super Slow Roll-off**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **2.8MHz, 5.6MHz DSD Input Support**
- **Digital De-emphasis for 32, 44.1, 48kHz sampling**
- **Soft Mute**
- **Digital Attenuator (255 levels and 0.5dB step)**
- **Mono Mode**
- **External Digital Filter Mode**
- **THD+N: -101dB, -105dB (Analog Block Power Supply 7V)**
- **DR, S/N: 120dB, 123dB (Mono mode: 126dB, Analog Block Power Supply 7V)**
- **I/F Format: 24/32bit MSB justified, 16/20/24/32bit LSB justified, I^2S, DSD**
- **Master Clock:**
  - **30kHz ~ 32kHz: 1152fs**
  - **30kHz ~ 54kHz: 512fs or 768fs**
  - **30kHz ~ 108kHz: 256fs or 384fs**
  - **108kHz ~ 216kHz: 128fs or 192fs**
  - **~ 384kHz: 64fs or 128fs**
  - **~ 768kHz: 64fs**
- **Power Supply: DVDD=AVDD=3.0~ 3.6V, VDD1/2=4.75 ~ 7.2V**
- **Digital Input Level: CMOS**
- **Package: 44-pin LQFP**

3. Table of Contents

4. Block Diagram and Functions



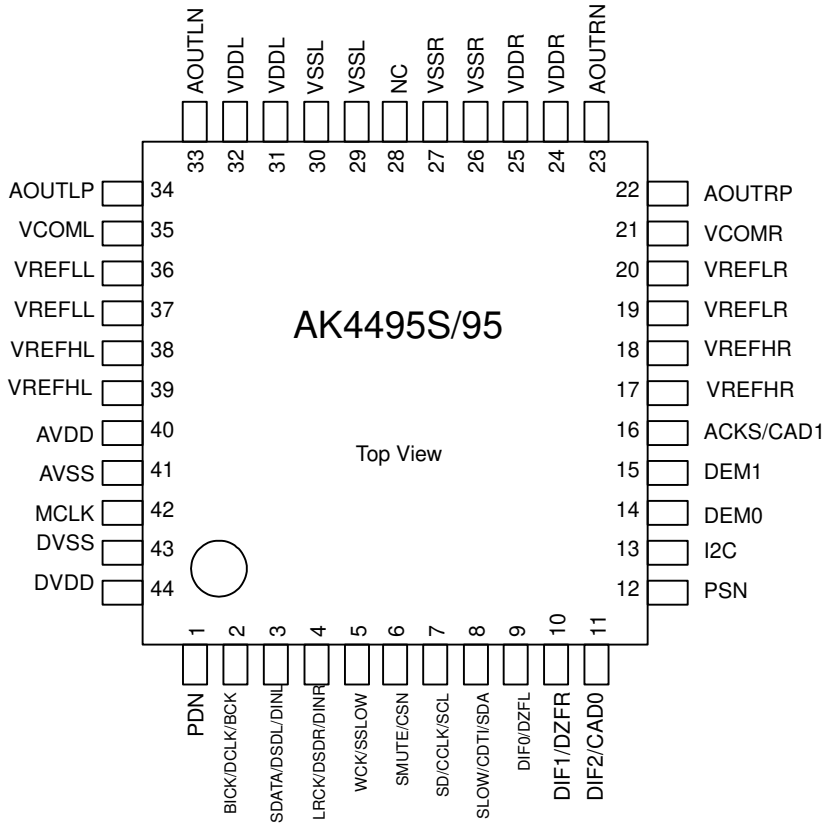
Block Diagram

5. Pin Configuration and Functions

■ Ordering Guide

AK4495EQ	–40 ~ +85°C	44-pin LQFP (0.8mm pitch)
AK4495SEQ	–40 ~ +85°C	44-pin LQFP (0.8mm pitch), Special Sound Quality Package
AKD4495	Evaluation Board for AK4495	
AKD4495S	Evaluation Board for AK4495S	

■ Pin Configuration



■ Functions

No.	Pin Name	I/O	Function
1	PDN	I	Power-Down Mode Pin When at "L", the AK4495S/95 is in power-down mode and is held in reset. The AK4495S/95 must always be reset upon power-up.
2	BICK	I	Audio Serial Data Clock Pin in PCM Mode
	DCLK	I	DSD Clock Pin in DSD Mode
	BCK	I	Audio Serial Data Clock Pin
3	SDATA	I	Audio Serial Data Input Pin in PCM Mode
	DSDL	I	DSD Lch Data Input Pin in DSD Mode
	DINL	I	Lch Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin in PCM Mode
	DSDR	I	DSD Rch Data Input Pin in DSD Mode in Serial Control Mode
	DINR	I	Rch Audio Serial Data Input Pin in Serial Control Mode
5	SSLOW	I	Digital filter setting in Parallel Control Mode
	WCK	I	Word Clock input pin in Serial Control Mode
6	SMUTE	I	Soft Mute Pin in Parallel Control Mode When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases.
	CSN	I	Chip Select Pin in Serial Control Mode in Serial Control Mode, I2C="L"
7	SD	I	Digital filter setting in Parallel Control Mode
	CCLK	I	Control Data Clock Pin in Serial Control Mode in Serial Control Mode, I2C="L"
	SCL	I	Control Data Clock Pin in Serial Control Mode in Serial Control Mode, I2C="H"
8	SLOW	I	Digital filter setting in Parallel Control Mode
	CDTI	I	Control Data Input Pin in Serial Control Mode in Serial Control Mode, I2C="L"
	SDA	I/O	Control Data Clock Pin in Serial Control Mode in Serial Control Mode, I2C="H"
9	DIF0	I	Digital Input Format 0 Pin in PCM Mode
	DZFL	O	Lch Zero Input Detect Pin in Serial Control Mode
10	DIF1	I	Digital Input Format 1 Pin in PCM Mode
	DZFR	O	Rch Zero Input Detect Pin in Serial Control Mode
11	DIF2	I	Digital Input Format 2 Pin in PCM Mode
	CAD0	I	Chip Address 0 Pin in Serial Control Mode (Internal pull-down pin)
12	PSN	I	Parallel or Serial Select Pin (Internal pull-up pin) "L": Serial Control Mode, "H": Parallel Control Mode
13	I2C	I	I2C mode select pin in Serial mode (Internal pull-down pin)
14	DEM0	I	De-emphasis Enable 0 Pin in Parallel Control Mode (Internal pull-up pin)

Note: All input pins except internal pull-up/down pins must not be left floating.

15	DEM1	I	De-emphasis Enable 1 Pin in Parallel Control Mode (Internal pull-down pin)
16	ACKS	I	Master Clock Auto Setting Mode Pin in Parallel Mode (Internal pull-down pin)
	CAD1	I	Chip Address 1 Pin in Serial Control Mode
17	VREFHR	I	Rch High Level Voltage Reference Input Pin
18	VREFHR	I	Rch High Level Voltage Reference Input Pin
19	VREFLR	I	Rch Low Level Voltage Reference Input Pin
20	VREFLR	I	Rch Low Level Voltage Reference Input Pin
21	VCOMR	-	Right channel Common Voltage Pin, Normally connected to VREFLL with a 10uF electrolytic cap.
22	AOUTRP	O	Rch Positive Analog Output Pin
23	AOUTRN	O	Rch Negative Analog Output Pin
24	VDDR	-	Rch Analog Power Supply Pin, 4.75 ~ 7.2V
25	VDDR	-	Rch Analog Power Supply Pin, 4.75 ~ 7.2V
26	VSSR		Ground Pin
27	VSSR		Ground Pin
28	NC	-	No internal bonding. Connect to GND.
29	VSSL		Ground Pin
30	VSSL		Ground Pin
31	VDDL	-	Lch Analog Power Supply Pin, 4.75 ~ 7.2V
32	VDDL	-	Lch Analog Power Supply Pin, 4.75 ~ 7.2V
33	AOUTLN	O	Lch Negative Analog Output Pin
34	AOUTLP	O	Lch Positive Analog Output Pin
35	VCOML	-	Left channel Common Voltage Pin, Normally connected to VREFLR with a 10uF electrolytic cap.
36	VREFLL	I	Lch Low Level Voltage Reference Input Pin
37	VREFLL	I	Lch Low Level Voltage Reference Input Pin
38	VREFHL	I	Lch High Level Voltage Reference Input Pin
39	VREFHL	I	Lch High Level Voltage Reference Input Pin
40	AVDD	-	Analog Power Supply Pin, 3.0 ~ 3.6V
41	AVSS	-	Ground Pin
42	MCLK	I	Master Clock Input Pin
43	DVSS	-	Ground Pin
44	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V

Note: All input pins except internal pull-up/down pins must not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

(1) Parallel Mode (PCM Mode only)

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	SMUTE	This pin must be connected to DVSS.

(2) Serial Mode

1. PCM Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
Digital	DIF2	These pins must be connected to DVSS.
	DZFL, DZFR	These pins must be open.

2. DSD Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	These pins must be open.
	AOUTRP, AOUTRN	These pins must be open.
	DZFL, DZFR	These pins must be open.

6. Absolute Maximum Ratings

(AVSS=DVSS=VSSL=VSSR=VREFLL=VREFLR=0V; Note 1)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	−0.3	4.6	V
	Analog	VDDL/R	−0.3	7.5	V
	Digital	DVDD	−0.3	4.6	V
	|AVSS − DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	−0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operation Conditions

(AVSS=DVSS=VSSL=VSSR =0V; Note 1)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 3)	Analog	AVDD	3.0	3.3	3.6	V
	Analog	VDDL/R	4.75	5.0	7.2	V
	Digital	DVDD	3.0	3.3	3.6	V
Voltage Reference (Note 4)	"H" voltage reference	VREFHL/R	VDDL/R−0.5	-	VDDL/R	V
	"L" voltage reference	VREFLL/R		VSS	-	V
	VREFH − VREFL	ΔVREF	3.0	-	VDDL/R	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD, VDDL/R and DVDD is not critical.
Note 4. The analog output voltage scales with the voltage of (VREFH − VREFL).
AOUT (typ.@0dB) = (AOUT+) − (AOUT−) = ±2.8Vpp × (VREFHL/R − VREFLL/R)/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

■ Handling of Unused Pin

(Ta=25°C; AVDD=DVDD=3.3V; AVSS=DVSS=VSSL/R=0V; VREFHL/R=VDDL/R=5V, VREFLL/R= VSSL/R=0V; Input data = 24bit; $R_L \geq 1k\Omega$; BICK=64fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: Figure 39; unless otherwise specified.)

Parameter			min	typ	max	Unit
Resolution			-	-	32	Bits
Dynamic Characteristics (Note 5)						
THD+N	fs=44.1kHz BW=20kHz	0dBFS	-	-101	-93	dB
		0dBFS (VDDL/R=VREFHL/R=7.0V)	-	-105	-	dB
		–60dBFS	-	-57	-47	dB
	fs=96kHz BW=40kHz	0dBFS	-	-98	-88	dB
		–60dBFS	-	-54	-44	dB
	fs=192kHz BW=40kHz	0dBFS	-	-98	-88	dB
		–60dBFS	-	-54	-44	dB
	BW=80kHz	–60dBFS	-	-51	-41	dB
Dynamic Range (–60dBFS with A-weighted) (Note 6)			114	120	-	dB
S/N (A-weighted) (Note 7)			114	120	-	dB
S/N (A-weighted, VDDL/R=7.0V)			100	123	-	dB
S/N (Mono mode, A-weighted, VDDL/R=7.0V)			100	126	-	dB
Interchannel Isolation (1kHz)			110	120	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.15	0.3	dB
Gain Drift (Note 8)			-	-	20	ppm/°C
Output Voltage (Note 9)			±2.65	±2.8	±2.95	Vpp
Load Capacitance			-	-	25	pF
Load Resistance (Note 10)			1	-	-	kΩ
Power Supplies						
Power Supply Current						
	Normal operation (PDN pin = "H")					
		VDDL/R		33	42	mA
		AVDD		1	2	mA
		DVDD (fs= 44.1kHz)	-	8	12	mA
		DVDD (fs= 96kHz)	-	14	20	mA
		DVDD (fs = 192kHz)	-	15	23	mA
	Power down (PDN pin = "L") (Note 11)					
		AVDD+VDDL/R+DVDD	-	10	100	μA

Note 5. Measured by Audio Precision, System Two. Averaging mode. Refer to the evaluation board manual. When SC2:SC1:SC0 bit = "010".

Note 6. Figure 39 External LPF Circuit Example 2. 101dB for 16-bit data and 118dB for 20-bit data.

Note 7. Figure 39 External LPF Circuit Example 2. S/N does not depend on input data size.

Note 8. The voltage on (VREFH – VREFL) is held +5V externally.

Note 9. Full-scale voltage(0dB). Output voltage scales with the voltage of (VREFHL/R – VREFLL/R). AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFHL/R – VREFLL/R)/5.

Note 10. Regarding Load Resistance, AC load is 1kΩ (min) with a DC cut capacitor (Figure 39). DC load is 1.5k ohm (min) without a DC cut capacitor (Figure 38). The load resistance value is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore the capacitive load must be minimized.

Note 11. In the power down mode. The PSN pin = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.

■ Sharp Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Normal Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 12)		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	29.4	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-	±0.2	-	dB

■ Sharp Roll-Off Filter Characteristics (fs = 96kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Double Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		43.5	kHz
	−6.0dB		-	48.0	-	kHz
Stopband (Note 12)		SB	52.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	28.8	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-	±0.3	-	dB

■ Sharp Roll-Off Filter Characteristics (fs = 192kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Quad Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband (Note 12)		SB	105			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	92			dB
Group Delay (Note 13)		GD	-	28.8	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-	+0/−1	-	dB

Note 12. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

Note 13. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

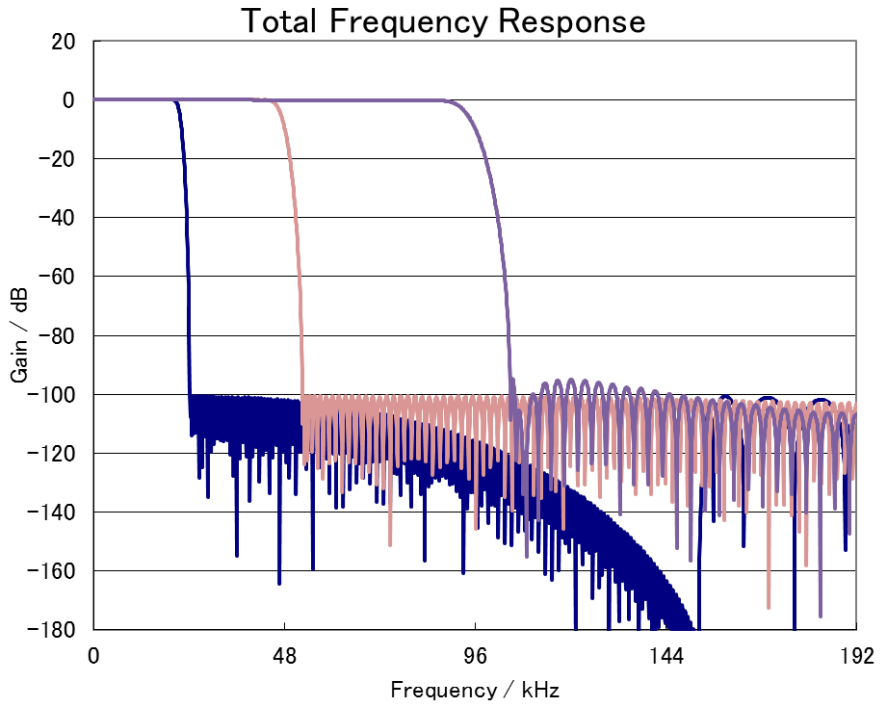


Figure 1. Sharp Roll-off Filter Frequency Response

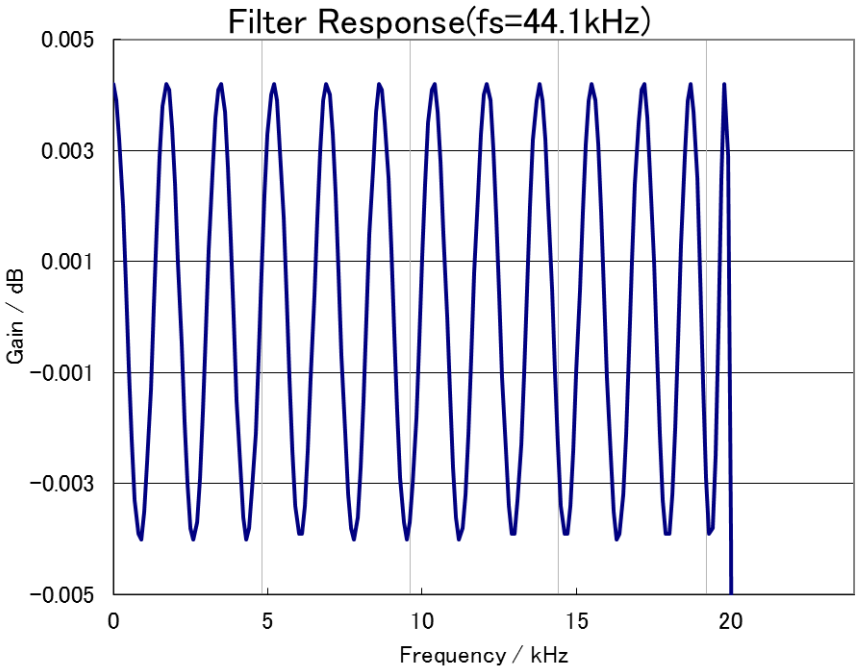


Figure 2. Sharp Roll-off Filter PassBand Ripple

■ Short Delay Sharp Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Normal Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 22.05	20.0 -	kHz kHz
Stopband (Note 12)		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	6.25	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 20.0kHz			-	±0.2	-	dB

■ Short Delay Sharp Roll-Off Filter Characteristics (fs = 96kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Double Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 48.0	43.5 -	kHz kHz
Stopband (Note 12)		SB	52.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	5.63	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 40.0kHz			-	±0.3	-	dB

■ Short Delay Sharp Roll-Off Filter Characteristics (fs = 192kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Quad Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H", SLOW bit="0" or SLOW pin = "L")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 96.0	87.0 -	kHz kHz
Stopband (Note 12)		SB	105			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	92			dB
Group Delay (Note 13)		GD	-	5.63	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 80.0kHz			-	+0/−1	-	dB

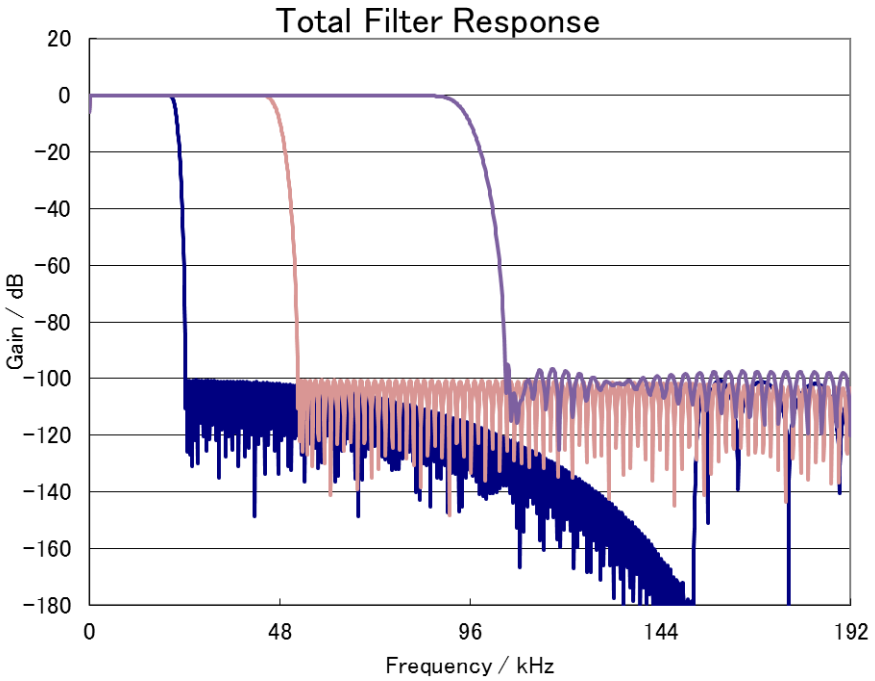


Figure 3. Short Delay Sharp Roll-off Filter Frequency Response

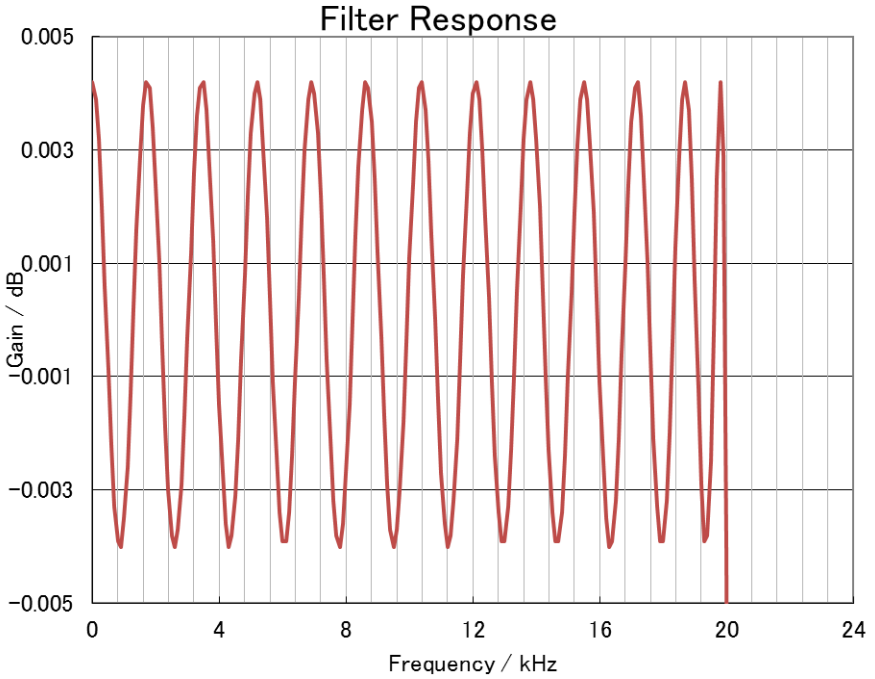


Figure 4. Short Delay Sharp Roll-off Filter Passband Ripple

■ Slow Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Normal Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 18.2	8.1 -	kHz kHz
Stopband (Note 12)		SB	39.2			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	94			dB
Group Delay (Note 13)		GD	-	6.63	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-	±0.2	-	dB

■ Slow Roll-Off Filter Characteristics (fs = 96kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Double Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 39.6	17.7 -	kHz kHz
Stopband (Note 12)		SB	85.3			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	6.00	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-	±0.3	-	dB

■ Slow Roll-Off Filter Characteristics (fs = 192kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Quad Speed Mode; DEM=OFF; SD bit="0" or SD pin = "L", SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 79.1	35.5 -	kHz kHz
Stopband (Note 12)		SB	171			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	97			dB
Group Delay (Note 13)		GD	-	6.00	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-	+0/−1	-	dB

Note 14. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.

Note 15. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

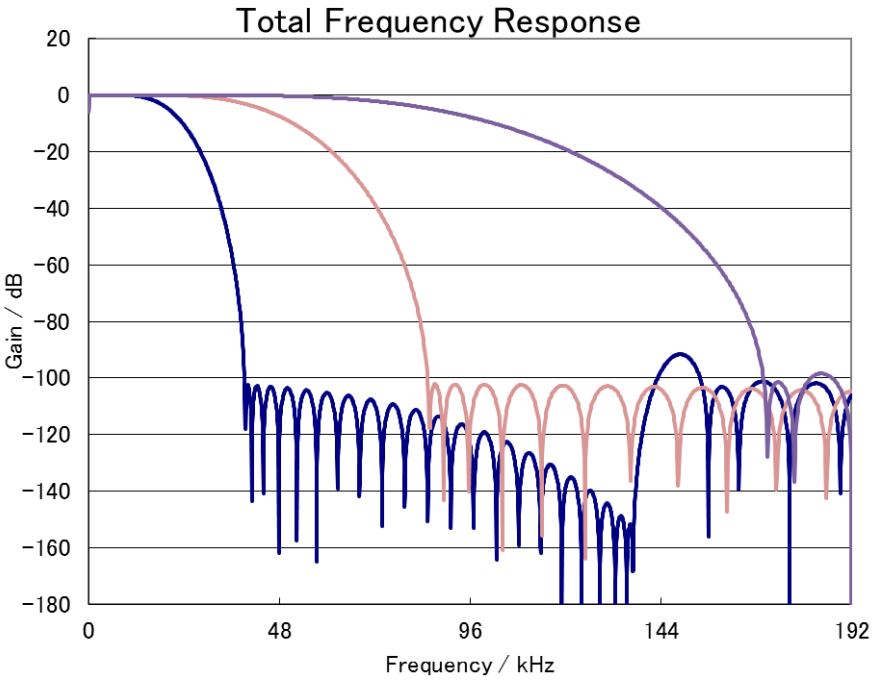


Figure 5. Slow Roll-off Filter Frequency Response

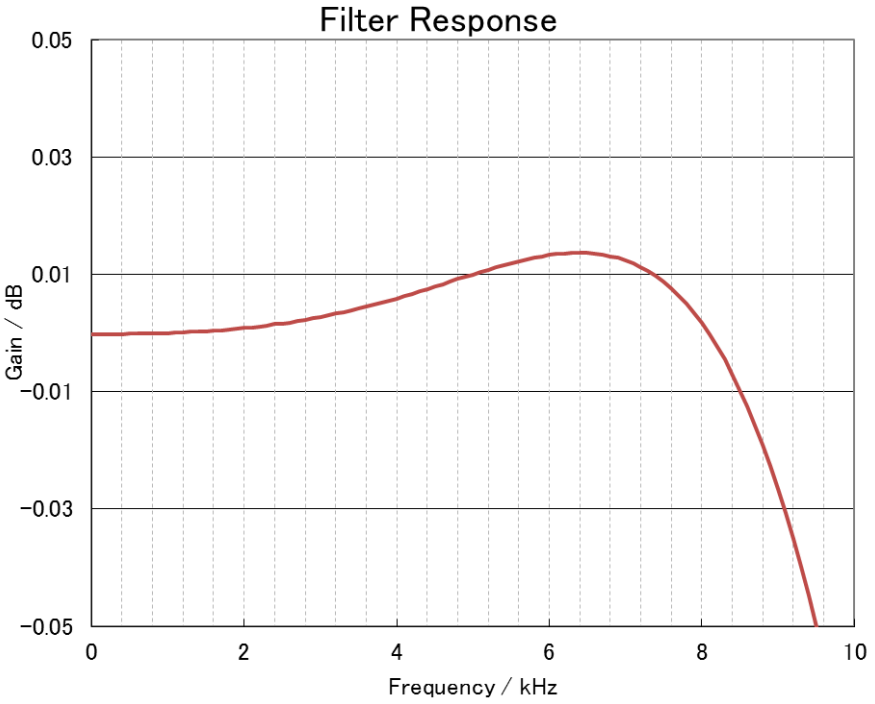


Figure 6. Slow Roll-off Filter Passband Ripple

■ Short Delay Slow Roll-Off Filter Characteristics (fs = 44.1kHz)

(Ta=25°C; AVDD= DVDD=3.0~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Normal Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H" , SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 18.2	8.1 -	kHz kHz
Stopband (Note 12)		SB	39.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	94			dB
Group Delay (Note 13)		GD	-	5.3	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 20.0kHz			-	±0.2	-	dB

■ Short Delay Slow Roll-Off Filter Characteristics (fs = 96kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Double Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H" , SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 48.0	43.5 -	kHz kHz
Stopband (Note 12)		SB	85.0			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 13)		GD	-	4.68	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 40.0kHz			-	±0.3	-	dB

■ Short Delay Slow Roll-Off Filter Characteristics (fs = 192kHz)

(Ta=25°C; AVDD= DVDD=3.0 ~ 3.6V, VREFHL/R= VDDL/R =4.75 ~ 7.2V; Quad Speed Mode; DEM=OFF; SD bit="1" or SD pin = "H" , SLOW bit="1" or SLOW pin = "H")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 96.0	87.0 -	kHz kHz
Stopband (Note 12)		SB	170			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	97			dB
Group Delay (Note 13)		GD	-	4.68	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 80.0kHz			-	+0/−1	-	dB

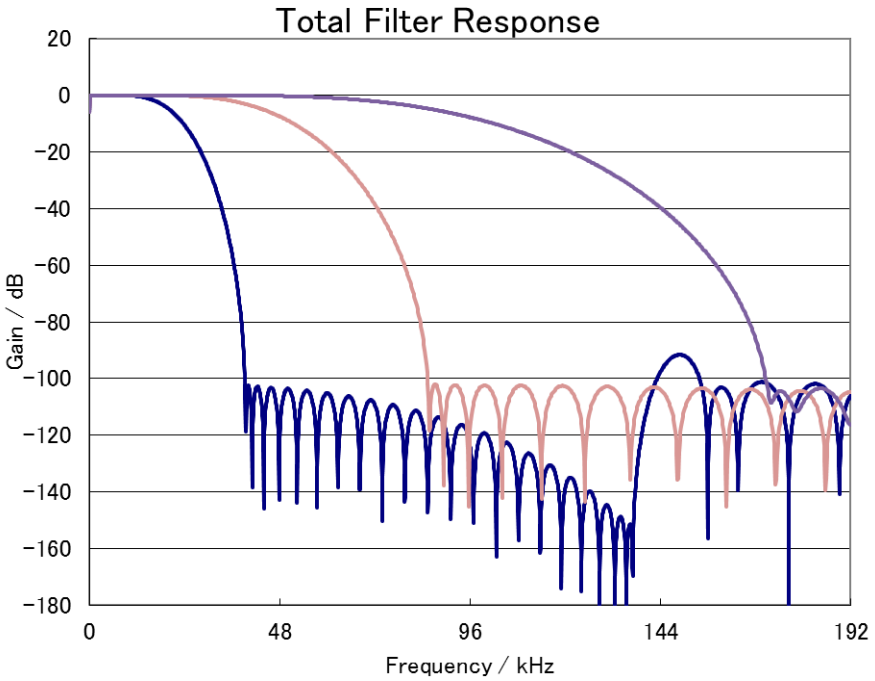


Figure 7. Short Delay Slow Roll-off Filter Frequency Response

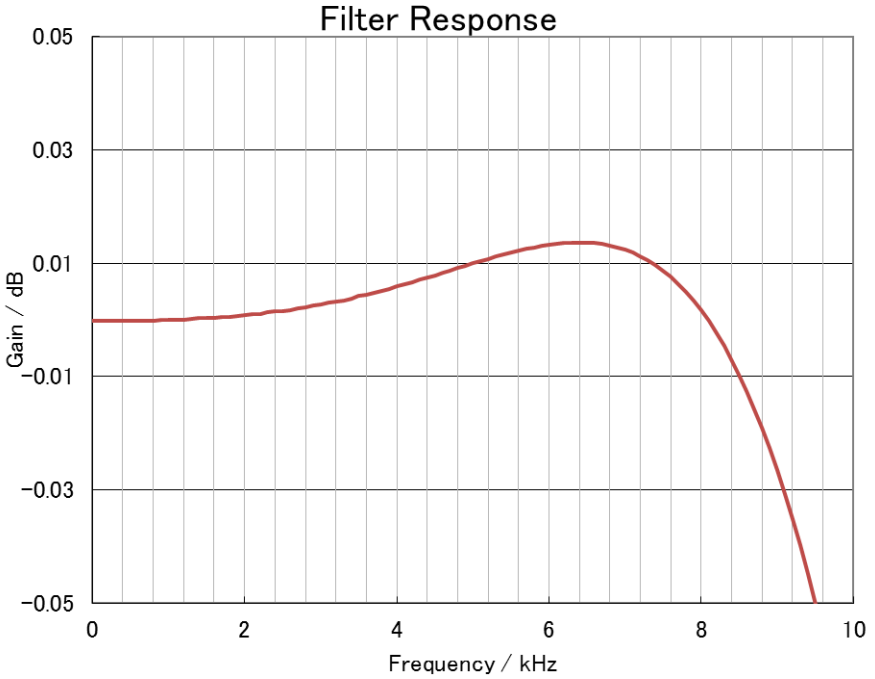


Figure 8. Short Delay Slow Roll-off Filter Passband Ripple

■ DC Characteristics

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6, VREFHL/R=VDDL/R=4.75 ~ 7.2V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout=−100μA)	VOH	DVDD−0.5	-	-	V
Low-Level Output Voltage					
(DZFL, DZFR pins: Iout=100μA)	VOL	-	-	0.5	V
(SDA pin: Iout=3mA)	VOL	-	-	0.5	V
Input Leakage Current (Note 16)	Iin	-	-	±10	μA

Note 16. The TST1/CAD0 and P/S pins have internal pull-up devices, nominally 100kΩ. Therefore The TST1/CAD0 and P/S pins are not included.

■ Switching Characteristics

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V, VREFHL/R= 4.75 ~ 7.2V)

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
Frequency	fCLK	7.7		49.152	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency (Note 17)					
1152fs, 512fs or 768fs	fsn	30		54	kHz
256fs or 384fs	fsd	54		108	kHz
128fs or 192fs	fsq	108		216	kHz
64fs	fsoc		384		kHz
64fs	fssd		768		kHz
Duty Cycle	Duty	45		55	%
PCM Audio Interface Timing					
BICK Period					
1152fs, 512fs or 768fs	tBCK	1/128fsn			ns
256fs or 384fs	tBCK	1/64fsd			ns
128fs or 192fs	tBCK	1/64fsq			ns
64fs	tBCK	1/64fso			ns
64fs	tBCK	1/64fsh			ns
BICK Pulse Width Low	tBCKL	10			ns
BICK Pulse Width High	tBCKH	10			ns
BICK "↑" to LRCK Edge (Note 18)	tBLR	5			ns
LRCK Edge to BICK "↑" (Note 18)	tLRB	5			ns
SDATA Hold Time	tSDH	5			ns
SDATA Setup Time	tSDS	5			ns
External Digital Filter Mode					
BICK Period	tB	27			ns
BCK Pulse Width Low	tBL	10			ns
BCK Pulse Width High	tBH	10			ns
BCK "↑" to WCK Edge	tBW	5			ns
WCK Edge to BCK "↑"	tWB	5			ns
WCK Pulse Width Low	tWCK	54			ns
WCK Pulse Width High	tWCH	54			ns
DATA Hold Time	tDH	5			ns
DATA Setup Time	tDS	5			ns
DSD Audio Interface Timing (64 mode, fs=44.1kHz)					
DCLK Period	tDCK		1/64fs		ns
DCLK Pulse Width Low	tDCKL	160			ns
DCLK Pulse Width High	tDCKH	160			ns
DCLK Edge to DSDL/R (Note 19)	tDDD	−20		20	ns
DSD Audio Interface Timing (128 mode, fs=44.1kHz)					
DCLK Period	tDCK		1/128fs		ns
DCLK Pulse Width Low	tDCKL	80			ns
DCLK Pulse Width High	tDCKH	80			ns
DCLK Edge to DSDL/R (Note 19)	tDDD	−10		10	ns

Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN High Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 20)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Reset Timing					
PDN Pulse Width (Note 21)	tPD	150			ns

Note 17. When the 1152fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK4495S/95 should be reset by the PDN pin or RSTN bit.

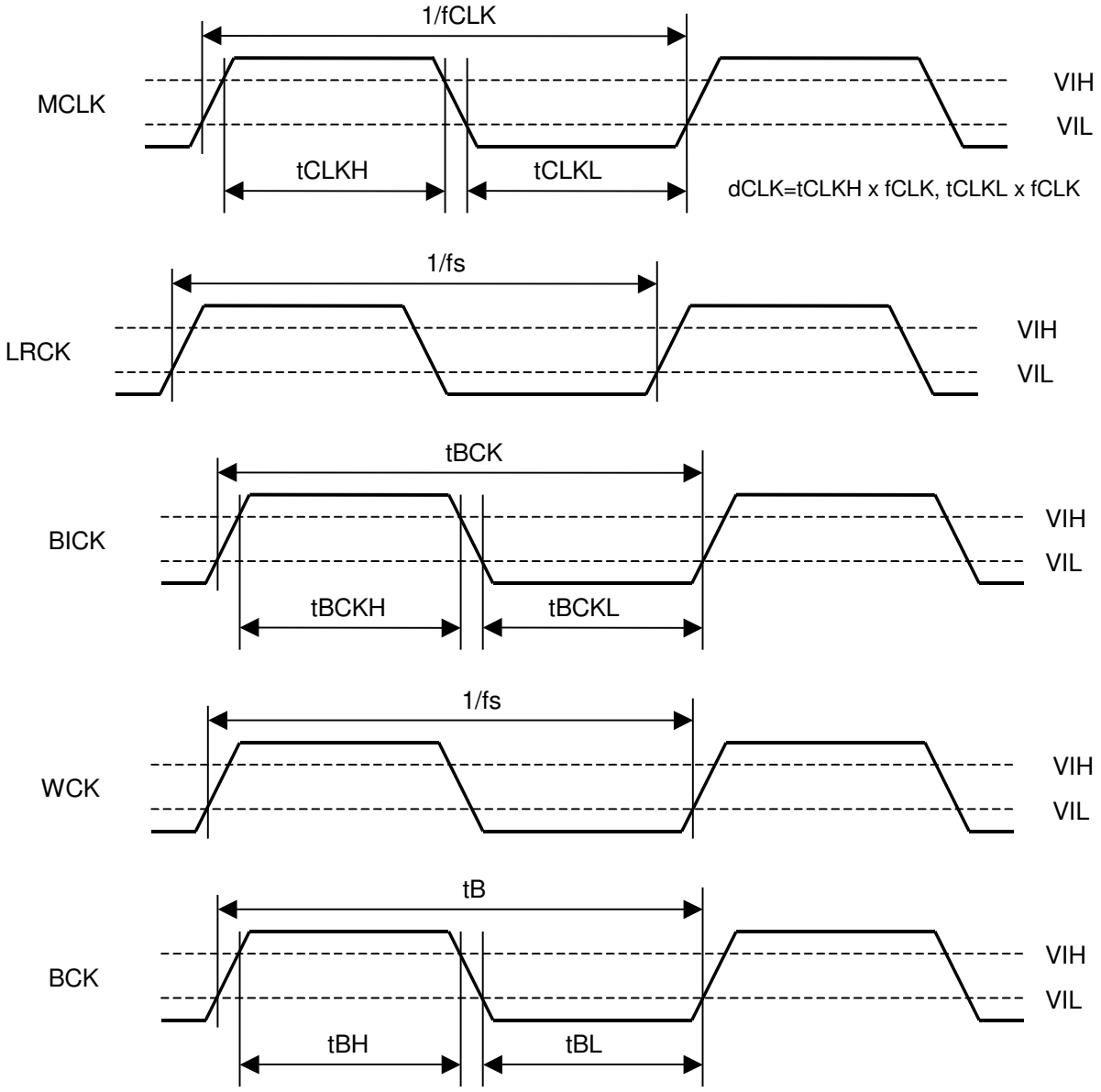
Note 18. BICK rising edge must not occur at the same time as LRCK edge.

Note 19. DSD data transmitting device must meet this time.

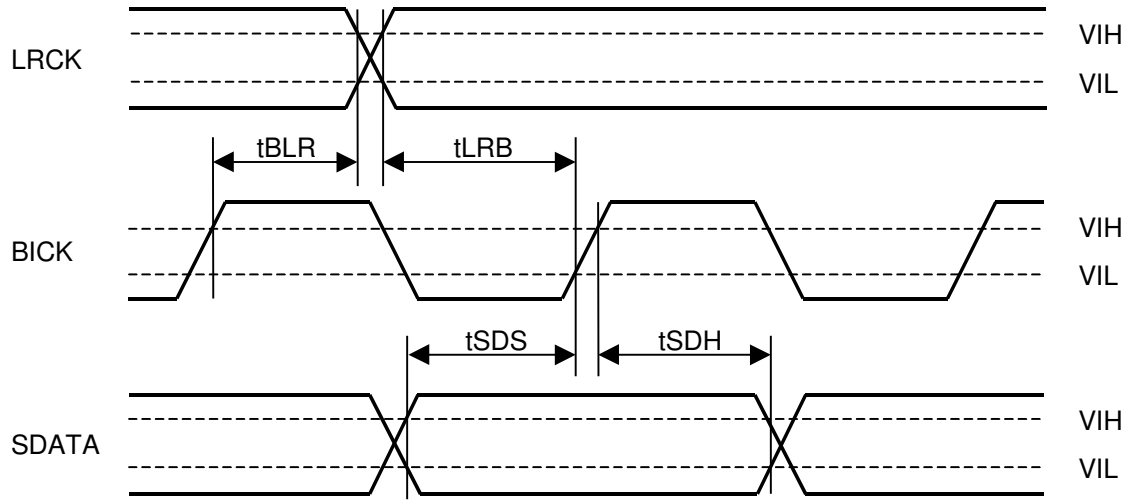
Note 20. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 21. The AK4495S/95 can be reset by bringing the PDN pin to "L".

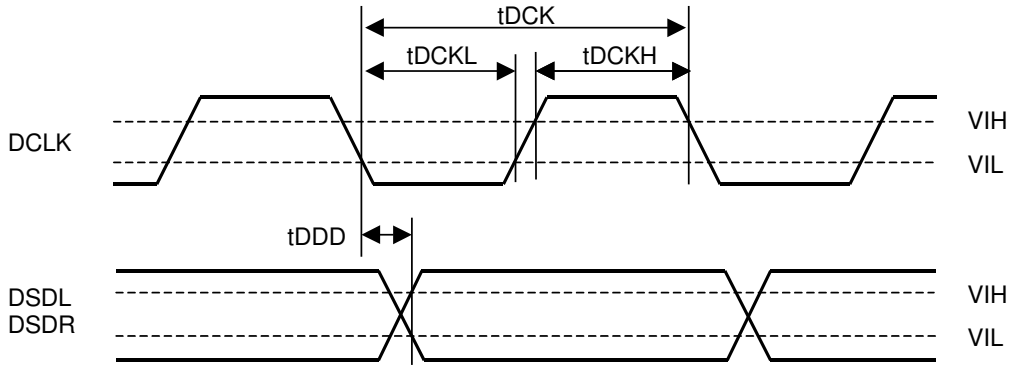
■ Timing Diagram



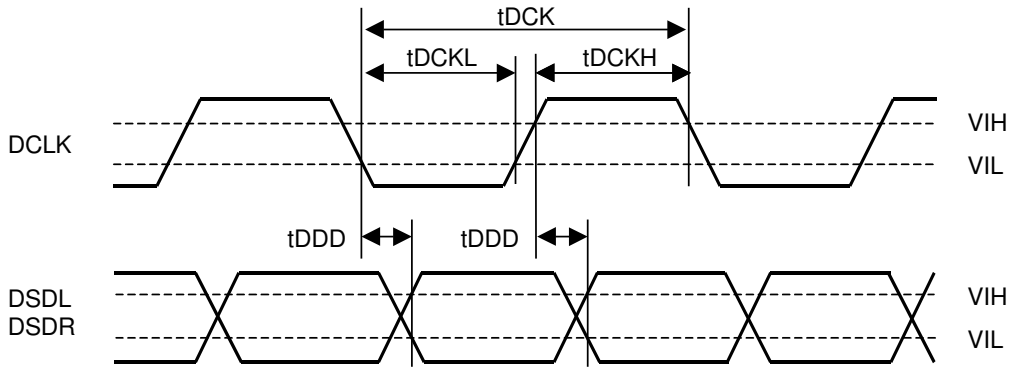
Clock Timing



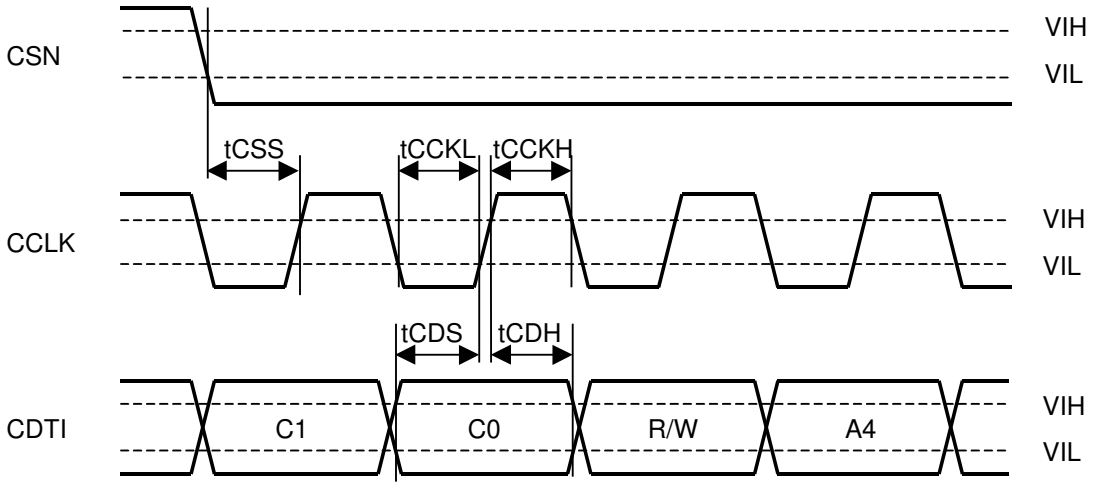
Audio Interface Timing (PCM Mode)



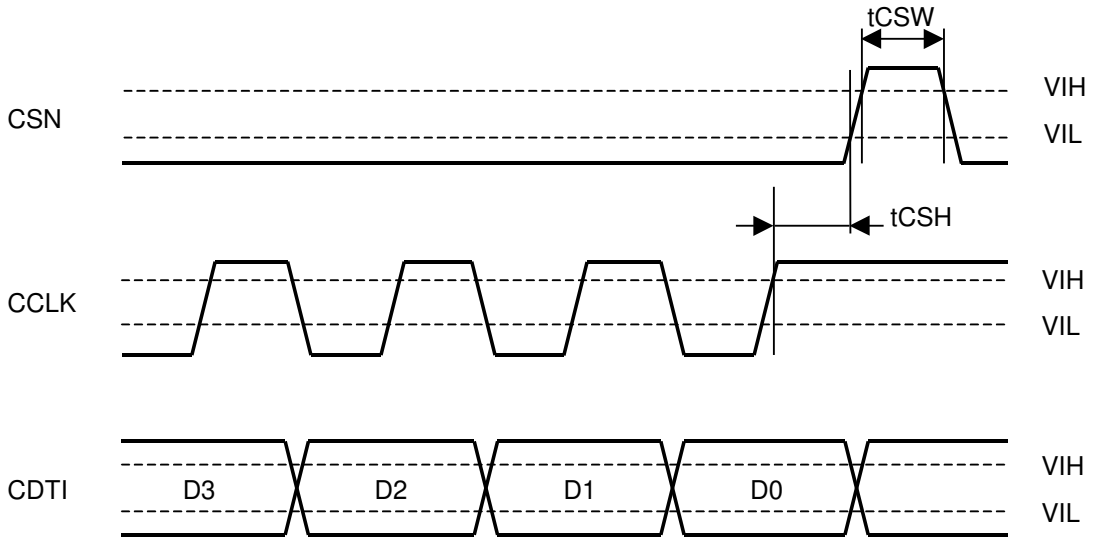
Audio Serial Interface Timing (DSD Normal Mode, DCKB bit = "0")



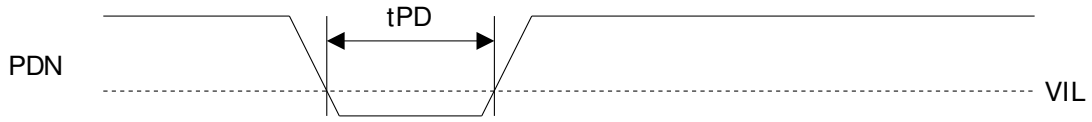
Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB bit = "0")



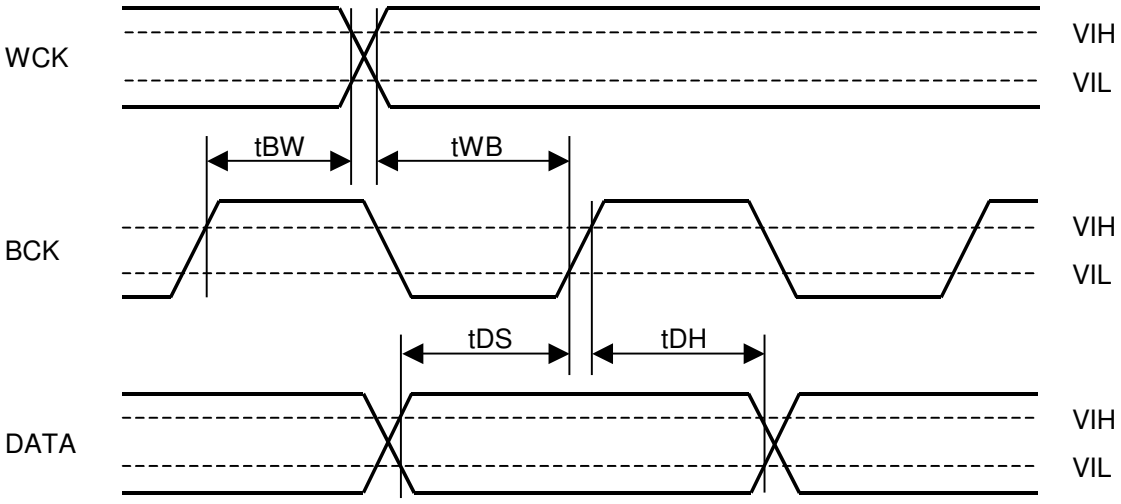
WRITE Command Input Timing



WRITE Data Input Timing



Power Down & Reset Timing



External Digital Filter I/F mode

9. Functional Descriptions

■ D/A Conversion Mode

In serial mode, the AK4495S/95 can perform D/A conversion for either PCM data or DSD data. The D/P bit controls PCM/DSD mode. When DSD mode, DSD data can be input from DCLK, DSDL and DSDR pins. When PCM mode, PCM data can be input from BICK, LRCK and SDATA pins. When PCM/DSD mode is changed by D/P bit, the AK4495S/95 should be reset by RSTN bit. It takes about 2/fs to 3/fs to change the mode. In parallel mode, the AK4495S/95 performs for only PCM data.

DP bit	Interface
0	PCM
1	DSD

Table 1. PCM/DSD Mode Control

When DP bit= "0", an internal digital filter or external digital filter can be selected. When using an external digital filter (EX DF I/F mode), data is input to each MCLK, BCK, WCK, DINL and DINR pin. EXDF bit controls the modes. When switching internal and external digital filters, the AK4495S/95 must be reset by RSTN bit. A Digital filter switching takes 2~3k/fs.

EXDF bit	Interface
0	PCM
1	EX DF I/F

Table 2. Digital Filter Control (DP bit = "0")

■ System Clock

[1] PCM Mode

The external clocks, which are required to operate the AK4495S/95, are MCLK, BICK and LRCK. MCLK should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two modes for MCLK frequency setting: Manual Setting Mode and Auto Setting Mode. In manual setting mode, MCLK frequency is set automatically (Table 4). In auto setting mode, sampling speed and MCLK frequency are detected automatically (Table 5) and then the initial master clock is set to the appropriate frequency (Table 6). When the reset is released (PDN pin = "↑"), the AK4495S/95 is in auto setting mode.

The AK4495S/95 is automatically placed in reset state when MCLK and LRCK are stopped during a normal operation (PDN pin ="H"), and the analog output becomes VDDR/2 and VDDL/2 voltages (typ). When MCLK and LRCK are input again, the AK4495S/95 exits reset state and starts operation. After exiting system reset (PDN pin ="L"→"H") at power-up and other situations, the AK4495S/95 is in power-down mode until MCLK and LRCK are supplied.

The MCLK frequency corresponding to each sampling speed should be provided externally (Table 3).

(1) Parallel Mode (PSN pin = "H")

1. Manual Setting Mode (ACKS pin = "L")

The MCLK frequency corresponding to each sampling speed should be provided externally (Table 3). DFS1 bit is fixed to "0". In this mode, quad speed mode is not available.

LRCK	MCLK (MHz)							BICK
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	64fs
32.0kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	2.0480MHz
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	2.8224MHz
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	3.0720MHz

Table 3. System Clock Example (Manual Setting Mode @Parallel Mode) (N/A: Not available)

In manual setting mode, the AK4495S/95 supports sampling rate from 32kHz to 96kHz (Table 4). However, the DR and S/N performances of when MCLK=256fs/384fs will degrade approximately 3dB as compared to when MCLK=512fs/768fs if the sampling rate is 32kHz~48kHz.

ACKS pin	MCLK	DR,S/N
L	256fs/384fs/512fs/768fs	120dB
H	256fs/384fs	117dB
H	512fs/768fs	120dB

Table 4. Relationship of MCLK Frequency and DR, S/N Performance (fs = 44.1kHz)

2. Auto Setting Mode (ACKS pin = "H")

In auto setting mode, MCLK frequency and sampling frequency are detected automatically (Table 5). MCLK of corresponded frequency to each sampling speed mode should be input externally. (Table 6)

MCLK		Sampling Speed
1152fs		Normal (fs≤32kHz)
512/256fs	768/384fs	Normal
256fs	384fs	Double
128fs	192fs	Quad
64fs	96fs	Oct
32fs	48fs	Hex

Table 5. Sampling Speed (Auto Setting Mode @Parallel Mode)

LRCK	MCLK(MHz)											Sampling Speed
fs	32fs	48fs	64fs	96fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	(8.192*)	(12.288*)	16.384	24.576	36.864	Normal/ (Double*)
44.1kHz	N/A	N/A	N/A	N/A	N/A	N/A	(11.2896*)	(16.9344*)	22.5792	33.8688	N/A	
48.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	(12.288*)	(18.432*)	24.576	36.864	N/A	
88.2kHz	N/A	N/A	N/A	N/A	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	24.576	36.864	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	N/A	N/A	N/A	N/A	24.576	36.864	N/A	N/A	N/A	N/A	N/A	Quad
384kHz	N/A	N/A	24.576	36.864	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768kHz	24.576	36.864	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Hex

Table 6. System Clock Example (Auto Setting Mode @Parallel Mode) (N/A: Not available)

When MCLK= 256fs/384fs, auto setting mode supports sampling rate of 32kHz~96kHz (Table 7). However, the DR and S/N performances will degrade approximately 3dB as compared to when MCLK= 512fs/768fs when the sampling rate is 32kHz~48kHz.

ACKS pin	MCLK	DR,S/N
L	256fs/384fs/512fs/768fs	120dB
H	256fs/384fs	117dB
H	512fs/768fs	120dB

Table 7. Relationship of MCLK Frequency and DR, S/N Performance (fs = 44.1kHz)

3. Digital filter

The AK4495S/95 has four kind of digital filters selected by SD and SLOW bits. Different sound qualities on playback can be selected by these filters.

SD pin	SLOW pin	Mode	
L	L	Sharp roll-off filter	
L	H	Slow roll-off filter	
H	L	Short delay Sharp roll-off filter	(default)
H	H	Short delay Slow roll-off filter	

Table 8. Digital Filter Setting

The AK4495S/95 can be operated on a slower sampling frequency. This mode is available when the SSLOW pin = “H”.

(2) Serial Mode (PSN pin = “L”)

1. Manual Setting Mode (ACKS bit = “0”)

MCLK frequency is detected automatically and the sampling speed is set by DFS2-0 bits (Table 9). The MCLK frequency corresponding to each sampling speed should be provided externally (Table 10). The AK4495S/95 is set to Manual Setting Mode at power-up (PDN pin = “L” →“H”). When DFS2-0 bits are changed, the AK4495S/95 should be reset by RSTN bit.

DFS2	DFS1	DFS0	Sampling Rate (fs)		
0	0	0	Normal Speed Mode	30kHz ~ 54kHz	(default)
0	0	1	Double Speed Mode	54kHz ~ 108kHz	
0	1	0	Quad Speed Mode	120kHz ~ 216kHz	
0	1	1	Reserved	-	
1	0	0	Oct Speed Mode	384kHz	
1	0	1	Hex Speed Mode	768kHz	
1	1	0	Reserved	-	
1	1	1	Reserved	-	

Table 9. Sampling Speed (Manual Setting Mode @Serial Mode)

LRCK	MCLK (MHz)											Sampling Speed
fs	32fs	48fs	64fs	96fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	Normal
44.1kHz	N/A	N/A	N/A	N/A	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A	
48.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A	
88.2kHz	N/A	N/A	N/A	N/A	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	24.5760	36.8640	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	22.5792	33.8688	45.1584	N/A	N/A	N/A	N/A	Quad
192.0kHz	N/A	N/A	N/A	N/A	24.5760	36.8640	49.152	N/A	N/A	N/A	N/A	Quad
384kHz	12.288	18.432	24.576	36.864	49.152	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768kHz	24.576	36.864	49.152	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Hex

Table 10. System Clock Example (Manual Setting Mode @Serial Mode)

2. Auto Setting Mode (ACKS bit = "1")

MCLK frequency and the sampling speed are detected automatically (Table 11) and DFS2-0 bits are ignored. The MCLK frequency corresponding to each sampling speed should be provided externally (Table 12).

MCLK		Sampling Speed
1152fs		Normal (fs≤32kHz)
512/256fs	768/384fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 11. Sampling Speed (Auto Setting Mode @Serial Mode)

LRCK	MCLK(MHz)											Sampling Speed
fs	32fs	48fs	64fs	96fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	(8.192*)	(12.288*)	16.384	24.576	36.864	Normal/ (Double*)
44.1kHz	N/A	N/A	N/A	N/A	N/A	N/A	(11.2896*)	(16.9344*)	22.5792	33.8688	N/A	
48.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	(12.288*)	(18.432*)	24.576	36.864	N/A	
88.2kHz	N/A	N/A	N/A	N/A	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	24.576	36.864	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	N/A	N/A	N/A	N/A	24.576	36.864	N/A	N/A	N/A	N/A	N/A	Quad
384kHz	N/A	N/A	24.576	36.864	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768kHz	24.576	36.864	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Hex

Table 12. System Clock Example (Auto Setting Mode @Serial Mode)

When MCLK= 256fs/384fs, auto setting mode supports sampling rate of 32kHz~96kHz (Table 13). However, the DR and S/N performances will degrade approximately 3dB as compared to when MCLK= 512fs/768fs when the sampling rate is 32kHz~48kHz.

ACKS bit	MCLK	DR,S/N
0	256fs/384fs/512fs/768fs	120dB
1	256fs/384fs	117dB
1	512fs/768fs	120dB

Table 13. Relationship of MCLK Frequency and DR, S/N Performance (fs = 44.1kHz)

3. Digital filter

The AK4495S/95 has four kind of digital filters selected by SD and SLOW bits. Different sound qualities on playback can be selected by these filters.

SD bit	SLOW bit	Mode	
0	0	Sharp roll-off filter	
0	1	Slow roll-off filter	
1	0	Short delay Sharp roll-off filter	(default)
1	1	Short delay Slow roll-off filter	

Table 14. Digital Filter Setting

The AK4495S/95 can be operated on a slower sampling frequency. This mode is available when SSLOW bit = "1" (05H D0).

[2] DSD Mode

The external clocks, which are required to operate the AK4495S/95, are MCLK and DCLK. MCLK should be synchronized with DCLK but the phase is not critical. The frequency of MCLK is set by DCKS bit.

The AK4495S/95 is automatically placed in reset state when MCLK is stopped during a normal operation (PDN pin ="H"), and the analog output becomes VDDR/2 and VDDL/2 voltages (typ.).

DCKS bit	MCLK Frequency	DCLK Frequency	
0	512fs	64fs	(default)
1	768fs	64fs	

Table 15. System Clock (DSD Mode)

The AK4495S/95 supports DSD data stream of 2.8224MHz (64fs) and 5.6448MHz (128fs). The data sampling speed is selected by DSDSEL bit. 2.8224MHz (64fs) is supported when DSDSEL bit = "0" and 5.6448MHz (128fs) is supported when DSDSEL bit = "1".

DSDSEL bit	DSD data stream	
0	2.8224MHz	(default)
1	5.6448MHz	

Table 16. DSD Sampling Speed Control

The AK4495S/95 has a Volume pass function. Three modes are selectable by DSDD1-0 bits.

DSDD1 bit	DSDD0 bit	Mode	
0	0	Normal path	(default)
0	1	Volume pass	
1	0	Reserved	
1	1	Reserved	

Table 17. DSD Play Back Mode Control

The AK4495S/95 has an internal mute function that mutes the output when DSD audio data becomes all "1" or all "0" for 2048 samples (1/fs). DDM bit controls this function. When the output is muted, L channel and R channel flags are indicated on DML bit and DMR bit, respectively. DMC bit controls mute release whether releasing the mute automatically when the signal level returns to a normal level or releasing the mute manually by a register. DMRE bit releases the mute when manual controlling is selected.

■ Audio Interface Format

[1] PCM Mode

Data is shifted in via the SDATA pin using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF2-0 pins (Parallel control mode) or DIF2-0 bits (Serial control mode) as shown in Table 18. In all formats the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 20-bit and 16-bit MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	Input Format	BICK	Figure	
0	0	0	0	16-bit LSB justified	≥ 32fs	Figure 9	
1	0	0	1	20-bit LSB justified	≥ 48fs	Figure 10	
2	0	1	0	24-bit MSB justified	≥ 48fs	Figure 11	(default)
3	0	1	1	24-bit I^{2}S compatible	≥ 48fs	Figure 12	
4	1	0	0	24-bit LSB justified	≥ 48fs	Figure 10	
5	1	0	1	32-bit LSB justified	≥ 64fs	Figure 13	
6	1	1	0	32-bit MSB justified	≥64fs	Figure 14	
7	1	1	1	32-bit I^{2}S compatible	≥ 64fs	Figure 15	

Table 18. Audio Interface Format

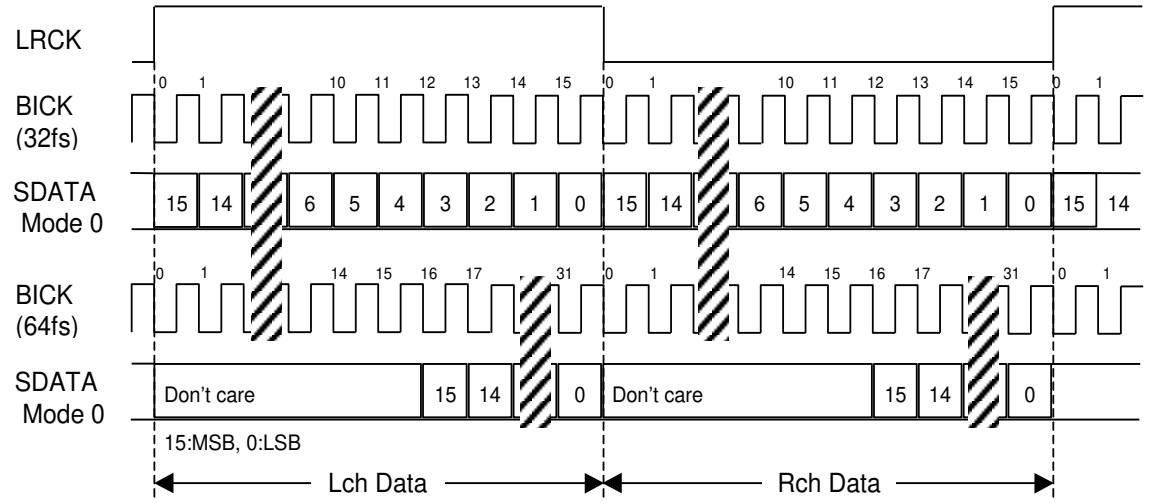


Figure 9. Mode 0 Timing

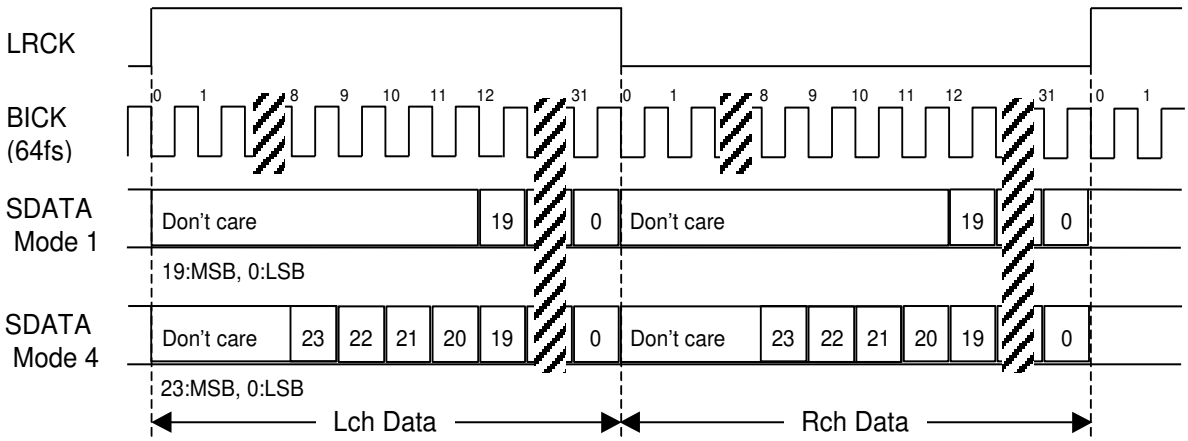


Figure 10. Mode 1/4 Timing

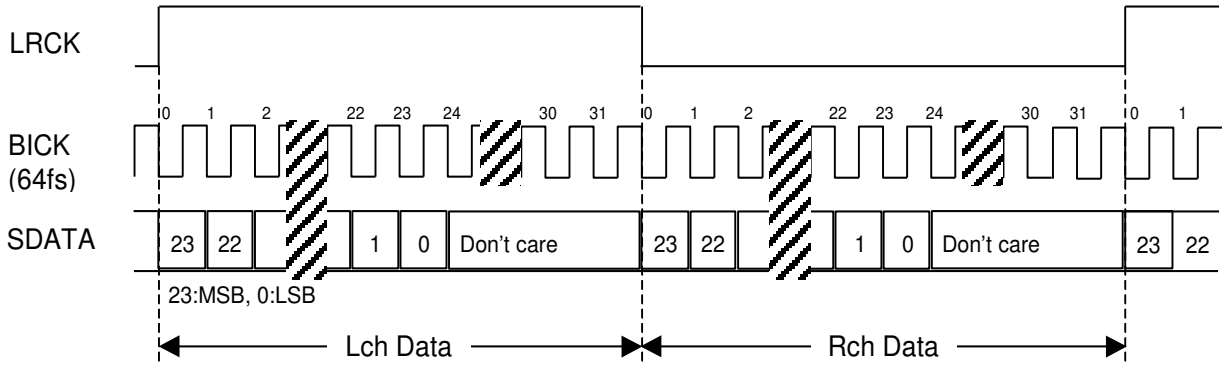


Figure 11. Mode 2 Timing

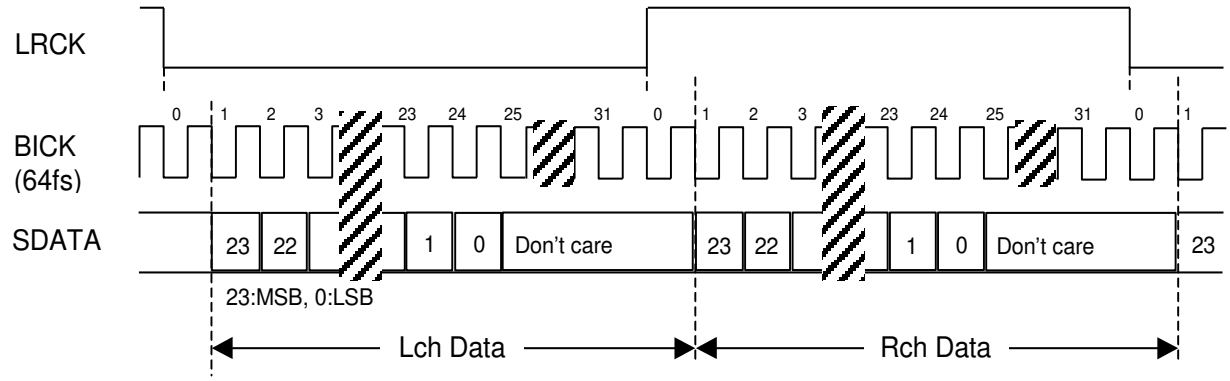


Figure 12. Mode 3 Timing

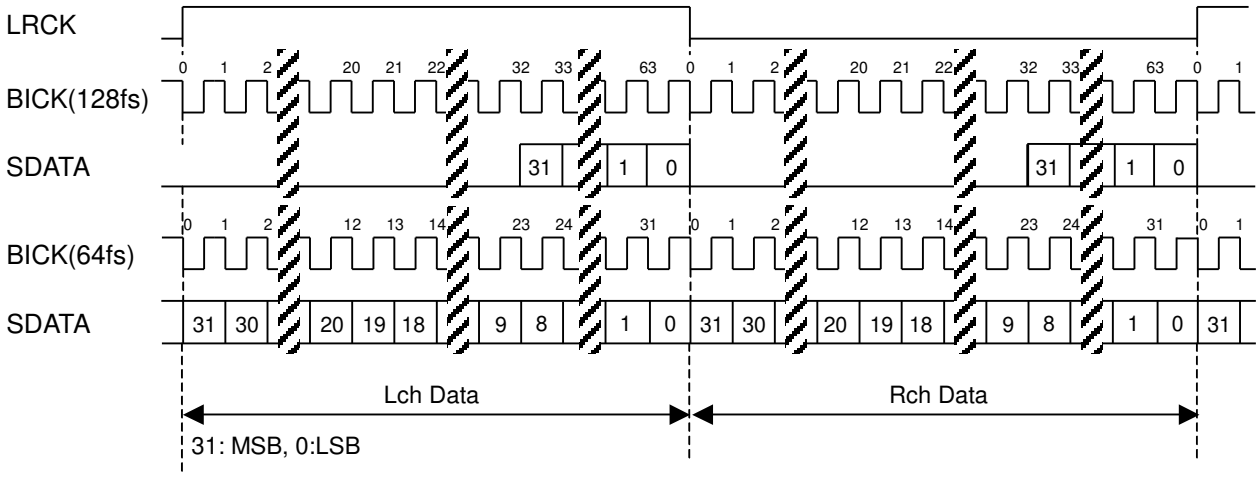


Figure 13. Mode 5 Timing

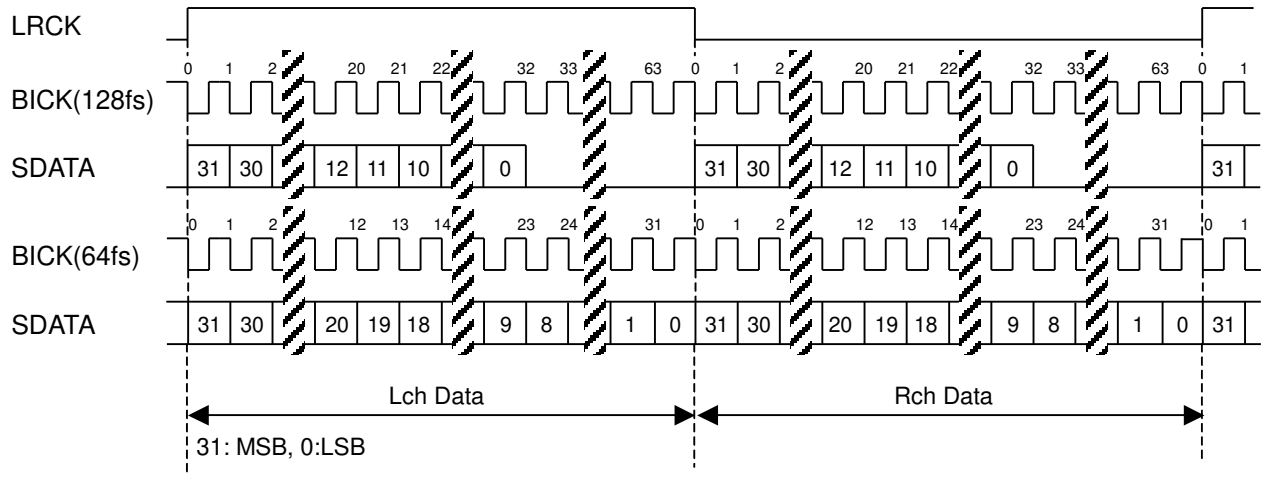


Figure 14. Mode 6 Timing

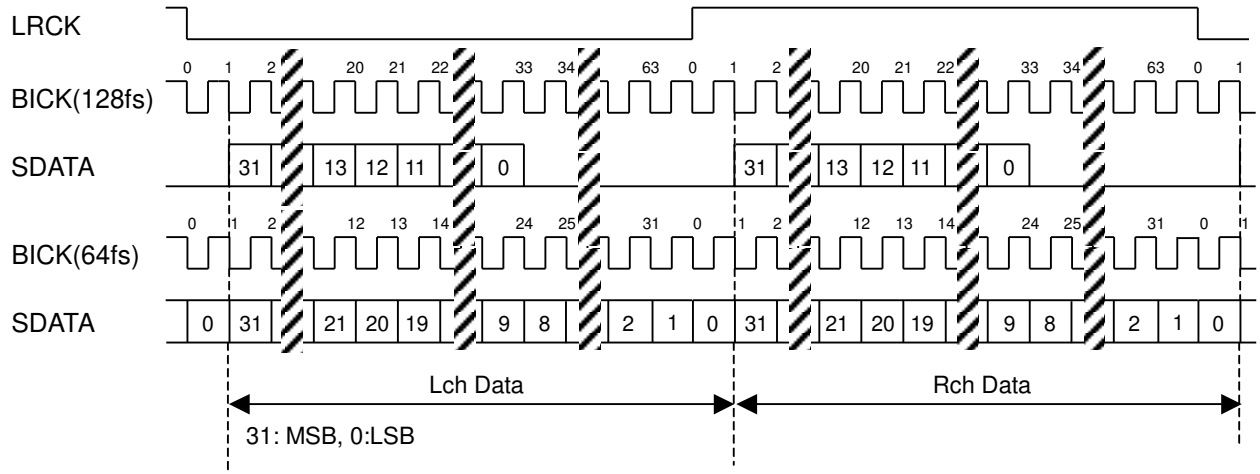


Figure 15. Mode 7 Timing

[2] DSD Mode

In case of DSD mode, DIF2-0 pins and DIF2-0 bits are ignored. The frequency of DCLK is 64fs or 128fs. DCKB bit can invert the polarity of DCLK.

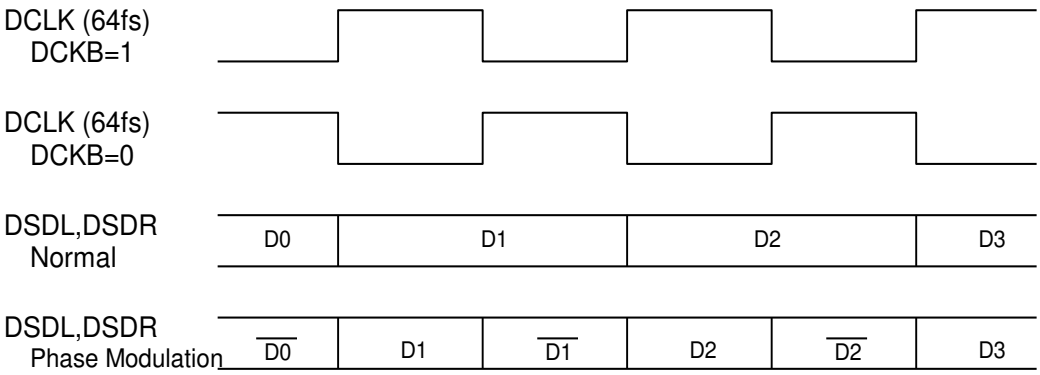


Figure 16. DSD Mode Timing

[3] External Digital Filter Mode (EX DF I/F Mode)

DW indicates the number of BCK in one WCK cycle. The audio data is input by MCLK, BCK and WCK from the DINL and DINR pins. Three formats are available (Table 20) by DIF2-0 bits setting. The data is latched on the rising edge of BCK. The BCK and MCLK clocks must be the same frequency and must not burst. BCK and MCLK frequencies for each sampling speed are shown in Table 19.

Sampling Speed[kHz]	MCLK&BCK [MHz]				WCK	ECS	
	256fs	384fs	512fs	768fs			
768	N/A	N/A	24.576	36.864	16fs	0	(default)
(432-864)			32	48	DW		
384	12.288	18.432	24.576	36.864	8fs	1	
(216-432)	32	48	64	96	DW		

Table 19 System Clock Example (EX DF I/F mode) (N/A: Not available)

Mode	DIF2	DIF1	DIF0	Input Format	
0	0	0	0	16-bit LSB justified	
1	0	0	1	N/A	
2	0	1	0	N/A	
3	0	1	1	N/A	
4	1	0	0	24-bit LSB justified	
5	1	0	1	32-bit LSB justified	(default)
6	1	1	0	N/A	
7	1	1	1	N/A	

Table 20 Audio Interface Format (EX DF I/F mode) (N/A: Not available)

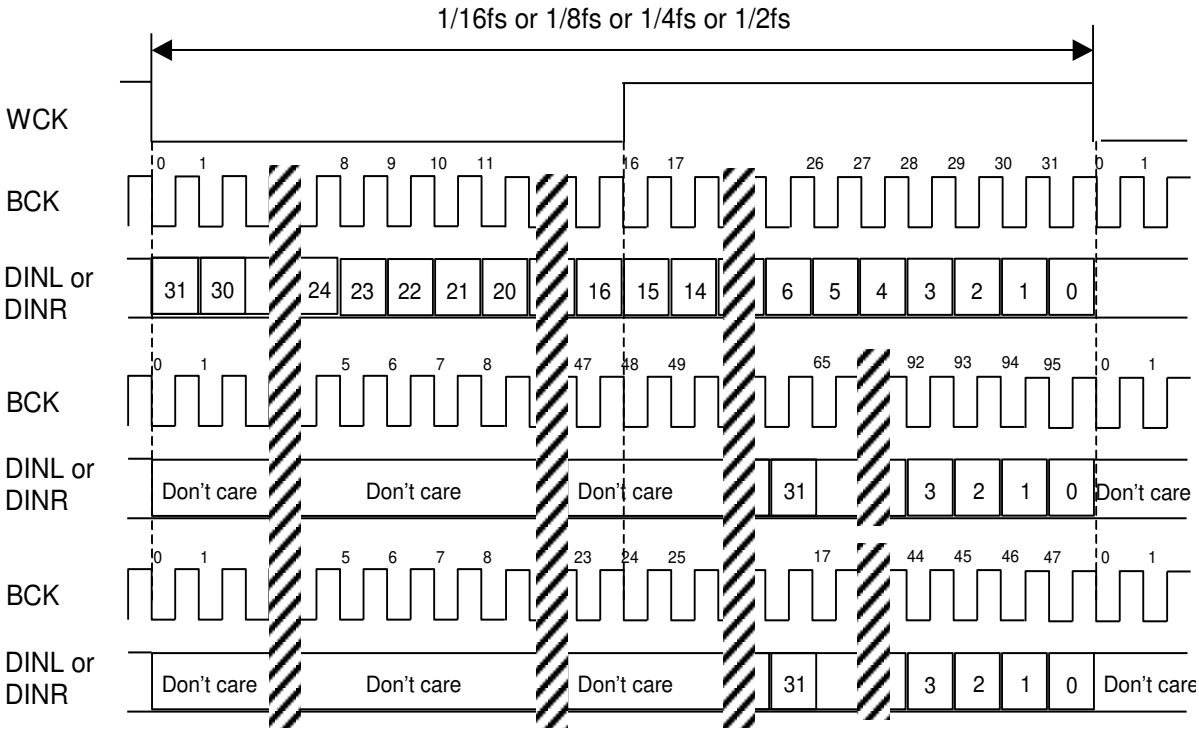


Figure 17 EX DF I/F Mode Timing

■ D/A Conversion Mode Switching Timing

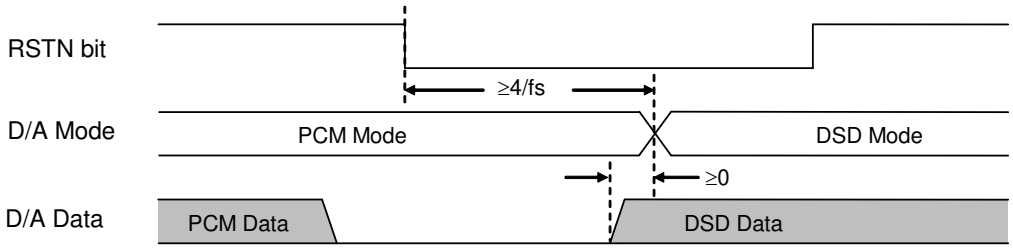


Figure 18. D/A Mode Switching Timing (PCM to DSD)

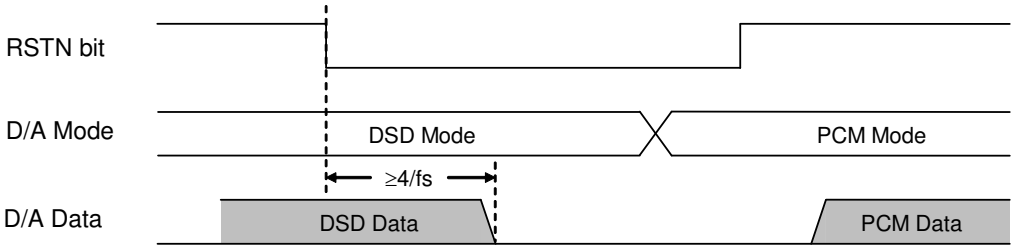


Figure 19. D/A Mode Switching Timing (DSD to PCM)

Note. The signal range is identified as 25% ~ 75% duty ratios in DSD mode. DSD signal must not go beyond this duty range at the SACD format book (Scarlet Book).

■ De-emphasis Filter

A digital de-emphasis filter is available for 32kHz, 44.1kHz or 48kHz sampling rates (tc = 50/15μs) and is enabled or disabled with DEM1-0 pins or DEM1-0 bits. In case of 256fs/384fs and 128fs/192fs, the digital de-emphasis filter is always off. When DSD mode, DEM1-0 bits are ignored. The setting value is held even if PCM mode and DSD mode are switched.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 21. De-emphasis Control

■ Output Volume (PCM, DSD)

The AK4495S/95 includes channel independent digital output volumes (ATT) with 255 levels at 0.5dB step including MUTE. This volume control is in front of the DAC and it can attenuate the input data from 0dB to –127dB or mute. When changing output levels, transitions are executed in soft change; thus no switching noise occurs during these transitions. It takes 7424/fs to attenuate from FFH (dB) to 00H (MUTE). When initial timing reset is executed, the attenuation level is reset to FFH. Setting RSTN bit to "0" initializes the attenuation level to FFH and setting RSTN bit to "1" release the attenuation level to the setting value. Register values will not be changed by switching PCM mode and DSD mode.

Sampling Speed	Transition Time
	0dB to MUTE
fs = 44.1kHz	168.3ms
fs = 96kHz	77.3ms
fs = 192kHz	38.6ms

Table 22. ATT Transition Time

■ Zero Detection (PCM, DSD)

The AK4495S/95 has a channel-independent zeros detect function. When the input data at each channel is continuously zeros for 8192 LRCK cycles, the DZF pin of each channel goes to "H". The DZF pin of each channel immediately returns to "L" if the input data of each channel is not zero after going to "H". If the RSTN bit is "0", the DZF pins of both L and R channels go to "H". The DZF pin of each channel returns to "L" in 4 ~ 5/fs after the input data of each channel becomes "1" when RSTN bit is set to "1". If DZFM bit is set to "1", the DZF pins of both L and R channels go to "H" only when the input data for both channels are continuously zeros for 8192 LRCK cycles. The zero detect function can be disabled by setting the DZFE bit. In this case, DZF pins of both channels are always "L". The DZFB bit can invert the polarity of the DZF pin.

DZFE	DZFB	Data	DZF-pin
0	0	-	L
	1	-	H
1	0	not zero	L
		Zero detect	H
	1	not zero	H
		Zero detect	L

Table 23. Zero Detect Function and DZF Pin Output

■ Mono Output (PCM, DSD, EX DF I/F)

The AK4495S/95 can select input/output for both output channels by setting the MONO bit and SELLR bit. This function is available for any audio format.

MONO bit	SELLR bit	Lch Out	Rch Out
0	0	Lch In	Rch In
0	1	Rch In	Lch In
1	0	Lch In	Lch In
1	1	Rch In	Rch In

Table 24 MONO Mode Output Select

■ Sound Quality Control (PCM, DSD, Ex DF I/F)

Sound quality of the AK4495S/95 can be selected by SC2-0 bits.

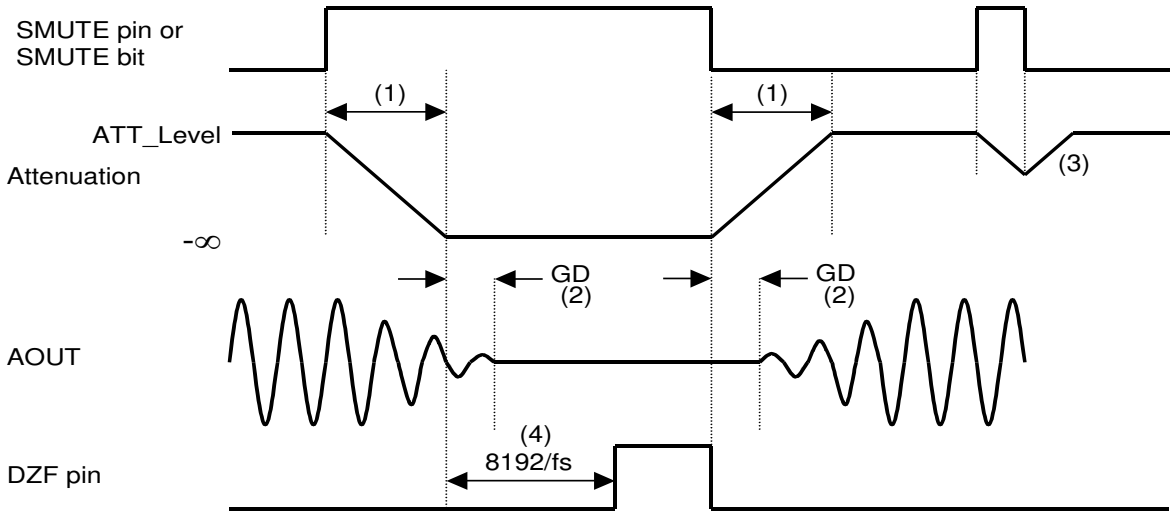
SC1	SC0	Mode	
0	0	1	(default)
0	1	2	
1	0	3	
1	1	4	

Table 25. SC1-0 bits Control

When SC2 bit="1", the AK4495S/95 operates in Mode 5.

■ Soft Mute Operation (PCM, DSD)

The soft mute operation is performed at digital domain. When the SMUTE pin goes to "H" or the SMUTE bit set to "1", the output signal is attenuated by −∞ during ATT_DATA × ATT transition time from the current ATT level. When the SMUTE pin is returned to "L" or the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA × ATT transition time. If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA × ATT transition time. For example, this time is 7424LRCK cycles (1020/fs) at ATT_DATA=255 in Normal Speed Mode.

(2) The analog output corresponding to the digital input has group delay (GD).

(3) If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

(4) When the input data for each channel is continuously zeros for 8192 LRCK cycles, the DZF pin for each channel goes to "H". The DZF pin immediately returns to "L" if input data are not zero.

Figure 20. Soft Mute Function

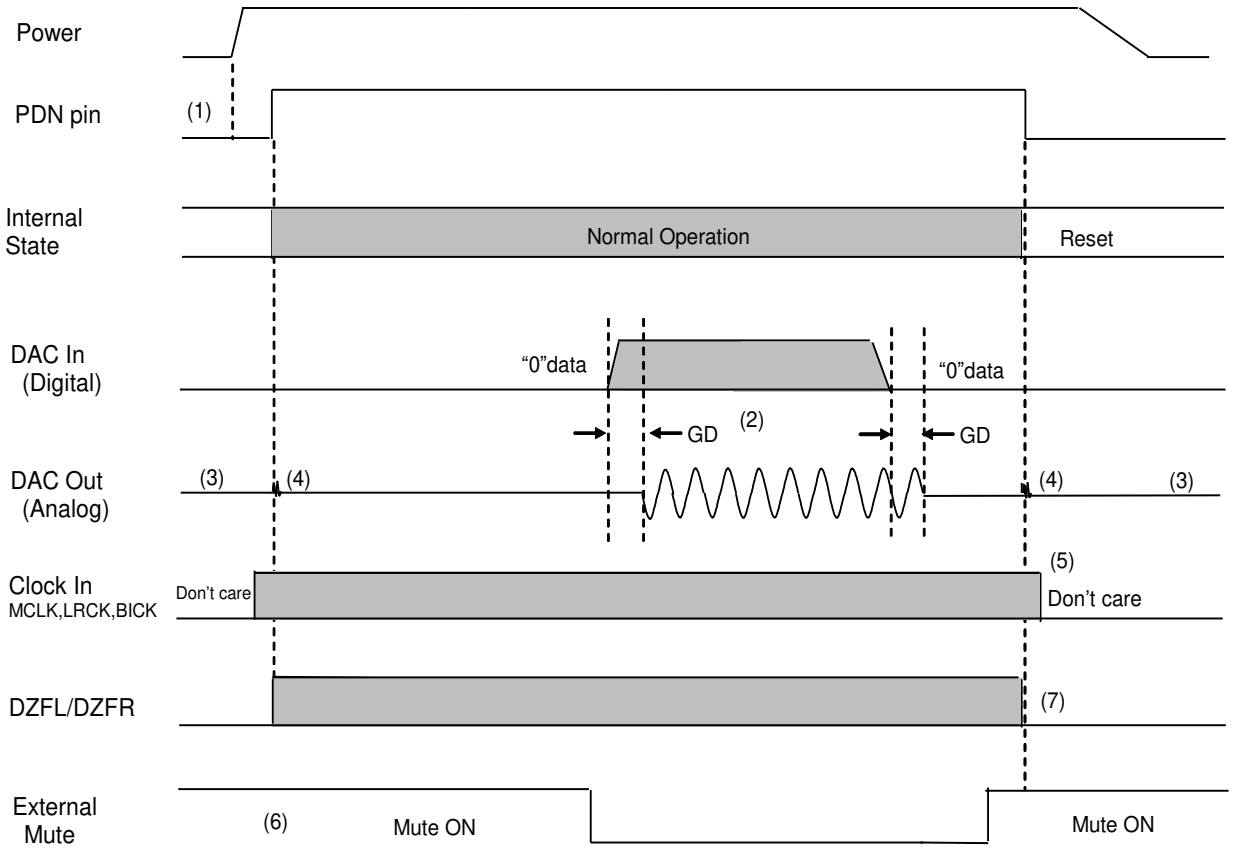
■ System Reset

The AK4495S/95 should be reset once by bringing the PDN pin = "L" upon power-up. It initializes register settings of the device. The analog block of the AK4495S/95 exits power-down mode by MCLK input, and the digital block exits power-down mode after the internal counter counts MCLK for 4/fs.

■ Power ON/OFF timing

The AK4495S/95 is placed in the power-down mode by bringing the PDN pin "L" and the registers are initialized. The analog outputs are floating (Hi-Z). As some click noise occurs at the edge of the PDN pin signal, the analog output should be muted externally if the click noise influences system application.

The DAC can be reset by setting RSTN bit to "0". In this case, registers are not initialized and the corresponding analog outputs go to VCML/R. As some click noise occurs at the edge of RSTN signal, the analog output should be muted externally if click noise adversely affect system performance.



Notes:

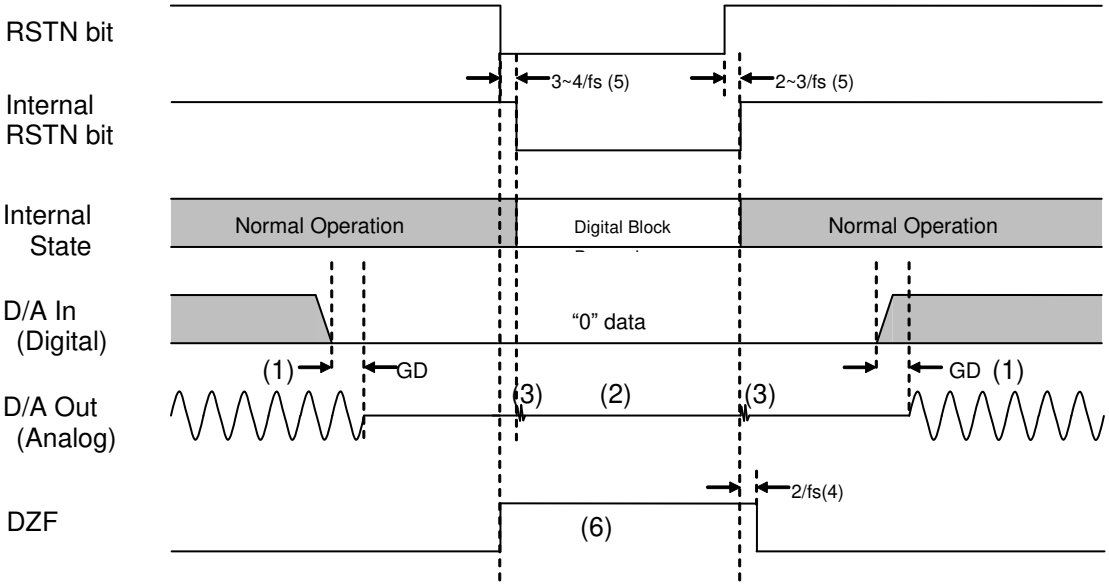
(1) After AVDD and DVDD are powered-up, the PDN pin should be "L" for 150ns.
(2) The analog output corresponding to digital input has group delay (GD).
(3) Analog outputs are floating (Hi-Z) in power-down mode.
(4) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.
(5) MCLK, BICK and LRCK clocks can be stopped in power-down mode (PDN pin= "L").
(6) Mute the analog output externally if click noise (3) adversely affect system performance The timing example is shown in this figure.
(7) DZFL/R pins are "L" in the power-down mode (PDN pin = "L").

Figure 21. Power-down/up Sequence Example

■ Reset Function

(1) RESET by RSTN bit = "0"

When the RSTN bit = "0", the AK4495S/95's digital block is powered down, but the internal register values are not initialized. In this time, the analog outputs go to VCML/R voltage and DZFL/DZFR pins are "H". Figure 22 shows an example of reset by RSTN bit.



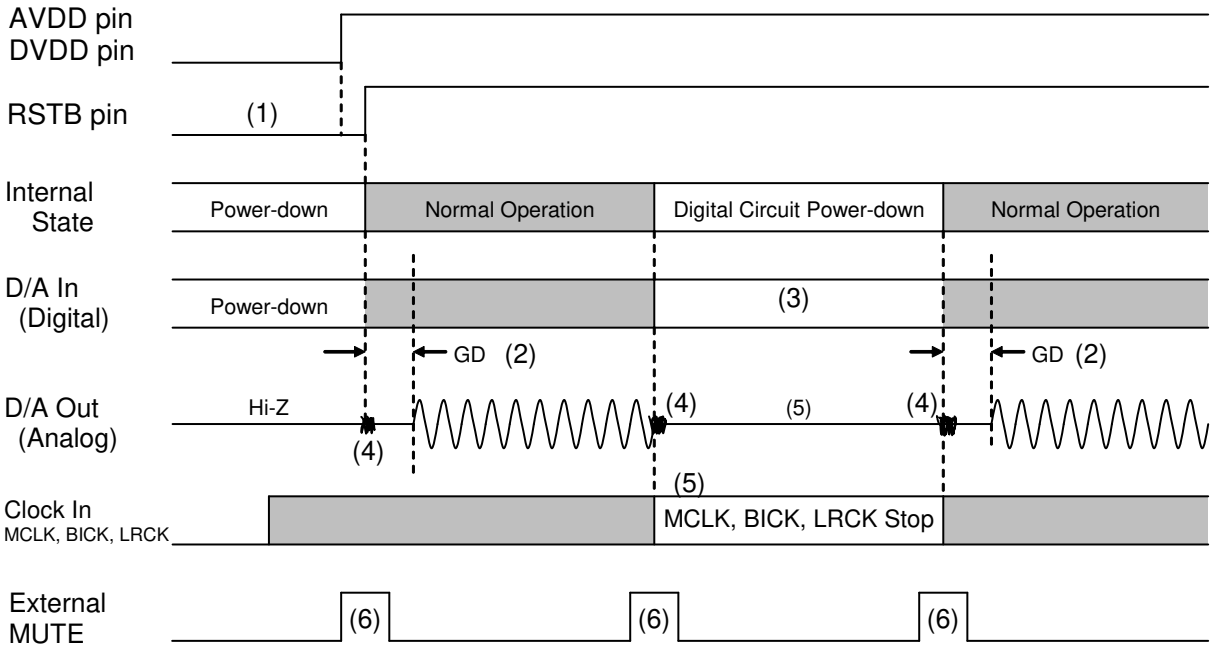
Notes:

(1) The analog output corresponding to digital input has group delay (GD).
(2) Analog outputs settle to VCOM voltage.
(3) Small pop noise occurs at the edges("↑ ↓") of the internal timing of RSTN bit. This noise is output even if "0" data is input.
(4) The DZF pins change to "H" when the RSTN bit becomes "0", and return to "L" at 2/fs after RSTN bit becomes "1".
(5) There is a delay, 3~4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2~3/fs from RSTN bit "1" to the internal RSTN bit "1".
(6) Mute the analog output externally if click noise (3) and Hi-Z (2) adversely affect system performance

Figure 22. Reset Sequence Example 1

(2) RESET by MCLK or LRCK/WCK Stop

The AK4495S/95 is automatically placed in reset state when MCLK or LRCK is stopped during PDM mode (PDN pin ="H"), and the analog outputs are floating (Hi-Z). When MCLK and LRCK are input again, the AK4495S/95 exits reset state and starts the operation. Zero detect function is disable when MCLK or LRCK is stopped. In DSD mode the AK4495S/95 is in reset state when MCLK is stopped, and it is in reset state when MCLK and WCK are stopped in external digital filter mode.



Notes:

(1) After AVDD and DVDD are powered-up, the PDN pin should be "L" for 150ns.
(2) The analog output corresponding to digital input has group delay (GD).
(3) The digital data can be stopped. Click noise after MCLK and LRCK are input again can be reduced by inputting "0" data during this period.
(4) Click noise occurs within 3 ~ 4LRCK cycles from the riding edge ("↑") of the PDN pin or MCLK inputs. This noise occurs even when "0" data is input.
(5) Clocks (MCLK, BICK, LRCK/WCK) can be stopped in the reset state (MCLK or LRCK/WCK is stopped).
(6) Mute the analog output externally if click noise (4) influences system applications. The timing example is shown in this figure.

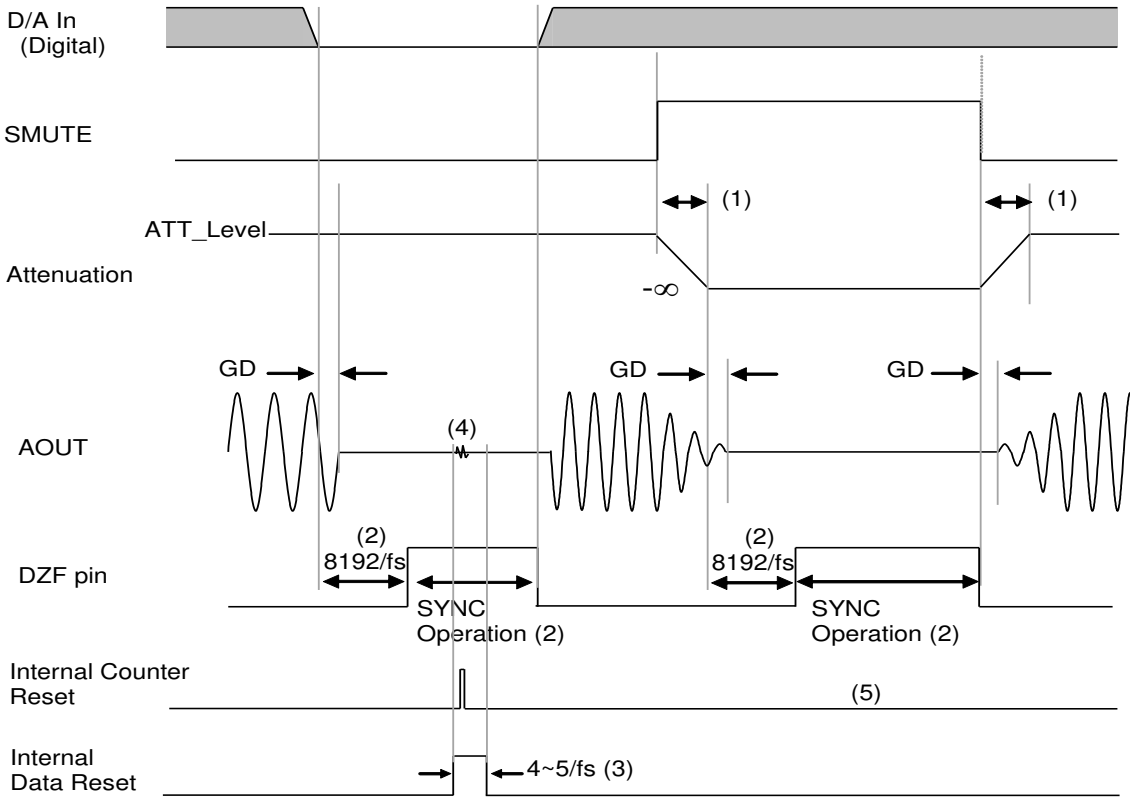
Figure 23. Reset Sequence Example 2

■ Synchronize Function

The AK4495S/95 has a function that resets the internal counter to synchronize with the external clock edge in a range of 3/256fs. Clock synchronize function becomes valid if SYNCE bit is set to "1" during operation in PCM mode or EXDF mode and input data of both L and R channels are "0" for 8129 times continuously or RESTN bit is "1". In PCM mode, the internal counter is synchronized with a falling edged of LRCK (rising edge of LRCK in I2C mode), and it is synchronized with a falling edge of WCK in EXDF mode. In this case, the analog output has the same voltage as VCML/R. Figure 24 shows a synchronizing sequence when the input data is "0" for 8192 times continuously. Figure 25 shows a synchronizing sequence by RSTN bit.

(1) Synchronization by continuous "0" data input for 8192 times

If the input data is "0" for 8192 times continuously, or if the data becomes "0" for 8192 times continuously by attenuation, the DZFL/DZFR pin goes to "H" and the synchronize function becomes valid. The synchronize function is enabled only when both L and R channels data are "0" for 8192 times continuously. Figure 24 shows a synchronizing sequence when the input data is "0" for 8192 times continuously.



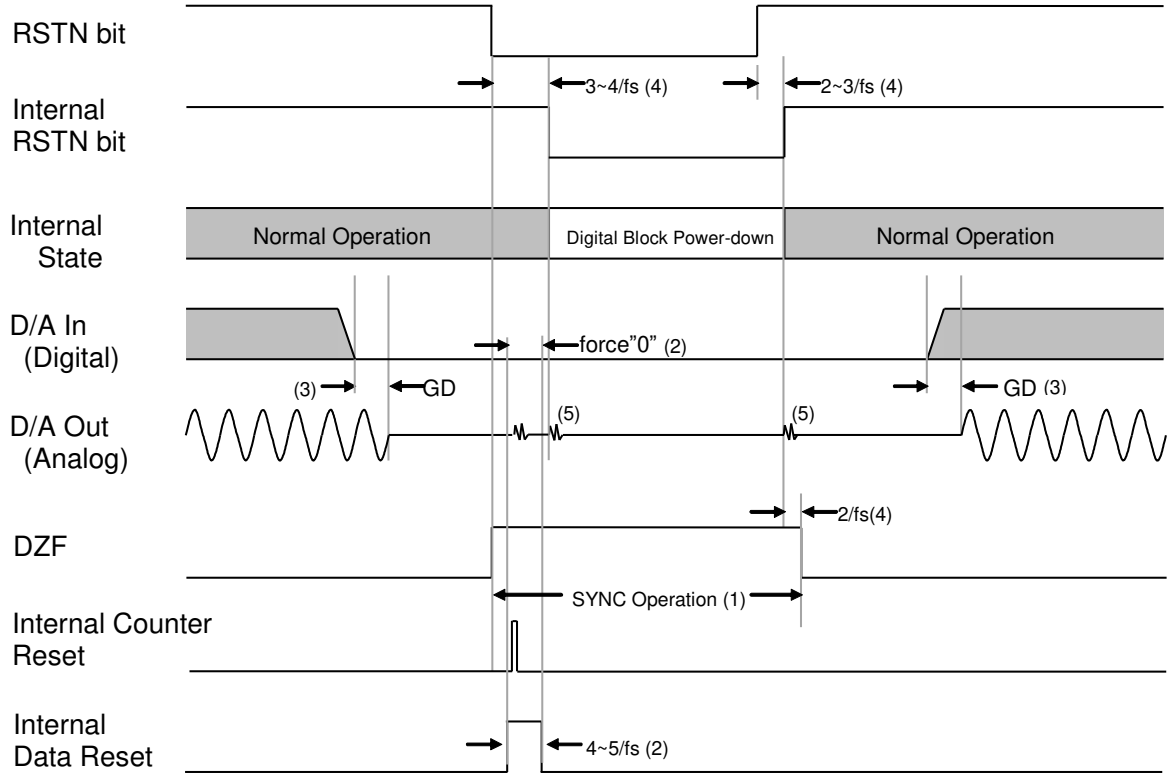
Note:

(1) ATT_DATA × ATT transition time. For example, this time is 7424LRCK cycles (1020/fs) at ATT_DATA=255 in Normal Speed Mode.
(2) When both L and R channels data are "0" for 8192 times continuously, DZFL/R pins become "H" and the synchronize function is valid.
(3) Internal data is fixed to "0" forcibly for 4 to 5/fs when internal counter is reset.
(4) A click noise may occur when the internal counter is reset. This noise is output even if a "0" data is input. Mute the analog output externally if this click noise affects the system performance.
(5) When the internal clock and external clock are in synchronization, the internal counter is not reset even if the synchronize function is valid.

Figure 24. Synchronizing Sequence by Continuous "0" Data Input for 8192 Times

(2) Synchronization by RSTN bit

If RSTN bit is set to "0", the output signal of the DZFL/DZFR pin becomes "H". Then, the DAC is reset 3 to 4/fs after the DZFL/DZFR pin = "H" and the analog output becomes the same voltage as VCML/R. The synchronize function becomes valid when both of the DZFL and DZFR pins output "H". Figure 25 shows a synchronizing sequence by RSTN bit.



Note:

(1) DZFL/R pin becomes "H" by a rising edge of RSTN bit, and becomes "L" 2/fs after a falling edge of internal signal of RSTN bit. The synchronize function is valid During the DZFL/R pin = "H".

(2) Internal data is fixed to "0" forcibly for 4 to 5/fs when the internal counter is reset.

(3) Since the analog output corresponding to digital input has group delay (GD), it is recommended to have a no-input period longer than the group delay before writing "0" to RSTN bit.

(4) It takes 3 to 4/fs when falling to change the internal RSTN signal of the LSI after writing to RSTN bit. It also takes 3 to 4/fs when rising to change the internal RSTN signal of the LSI. The synchronize function becomes valid immediately when "0" is written to RSTN bit. Therefore, there is a case that the internal counter is reset before internal RSTN signal of the LSI is changed.

(5) A click noise occurs on the rising or falling edge of the internal RSTN signal and when the internal counter is reset. This noise is output even if a "0" data is input. Mute the analog output externally if this click noise affects the system performance.

Figure 25. Synchronizing Sequence by RSTN bit

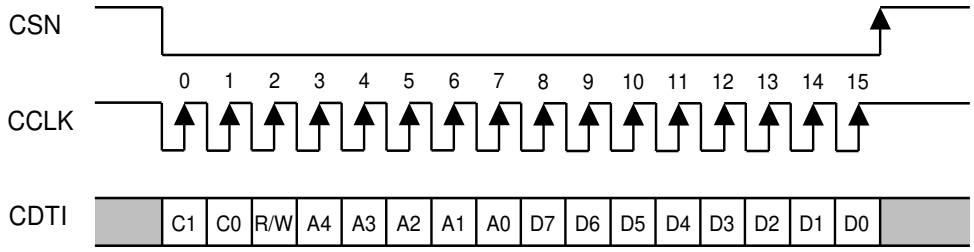
■ Register Control Interface

(1) 3-wire Serial Control Mode (I2C pin = "L")
Pins (parallel control mode) or registers (serial control mode) can control the functions of the AK4495S/95. In parallel control mode, the register setting is ignored, and in serial control mode the pin settings are ignored. When the state of the PSN pin is changed, the AK4495S/95 should be reset by the PDN pin. The serial control interface is enabled by the PSN pin = "L". Internal registers may be written to through3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2-bits, C1/0), Read/Write (1-bit; fixed to "1"), Register address (MSB first, 5-bits) and Control data (MSB first, 8-bits). The data is output on a falling edge of CCLK and the data is received on a rising edge of CCLK. The writing of data is valid when CSN "↑". The clock speed of CCLK is 5MHz (max).

Function	Parallel Control Mode	Serial Control Mode
Audio Format	Y	Y
Auto Setting Mode	Y	Y
De-emphasis	Y	Y
SMUTE	Y	Y
DSD Mode	-	Y
EX DF I/F	-	Y
Zero Detection	-	Y
Sharp Roll off filter	Y	Y
Slow Roll off filter	Y	Y
Minimum delay Filter	Y	Y
Digital Attenuator	-	Y
Sound Quality Adjustment	-	Y
Clock Synchronize	-	Y

Table 26. Function List1 (Y: Available, -: Not available)

Setting the PDN pin to "L" resets the registers to their default values. In serial control mode, the internal timing circuit is reset by the RSTN bit, but the registers are not initialized.



C1-C0: Chip Address (C1 bit =CAD1 pin, C0 bit =CAD0 pin)
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data
Figure 26. Control I/F Timing

* 3-wire serial control mode does not support read commands.
* When the AK4495S/95 is in power down mode (PDN pin = "L") or the MCLK is not provided, writing into control registers is prohibited.
* The control data can not be written when the CCLK rising edge is 15 times or less or 17 times or more during CSN is "L".

(2) I²C-bus Control Mode (I2C pin = "H")

The AK4495S/95 supports the fast-mode I²C-bus (max: 400kHz, Ver 1.0).

(2)-1. WRITE Operations

Figure 27 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 33). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1 and CAD0 (device address bits). This bit identifies the specific device on the bus. The hard-wired input pin (cAD1pins, CAD0 pin) sets these device address bits (Figure 28). If the slave address matches that of the AK4495S/95, the AK4495S/95 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 34). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4495S/95 and the format is MSB first. (Figure 29). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 30). The AK4495S/95 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 33).

The AK4495S/95 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4495S/95 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 2FH prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 35) except for the START and STOP conditions.

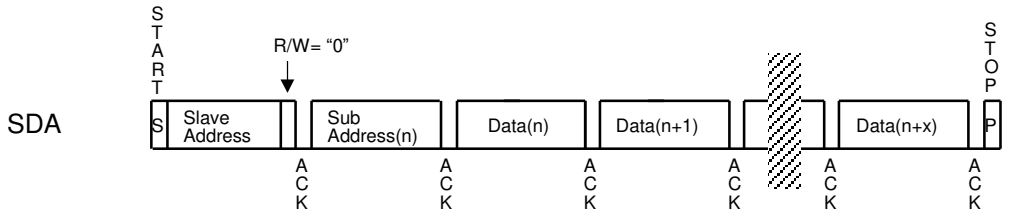


Figure 27. Data Transfer Sequence at I²C Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(CAD0 is set by the pin)

Figure 28. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 29. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 30. The Third Byte and After The Third Byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4495S/95. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 09H prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK4495S/95 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4495S/95 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4495S/95 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4495S/95 ceases the transmission.

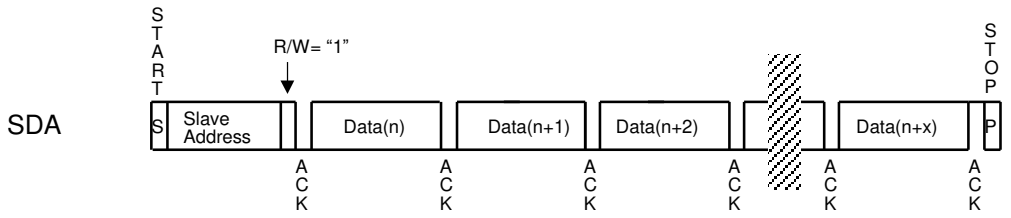


Figure 31. Current Address Read

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4495S/95 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4495S/95 ceases the transmission.

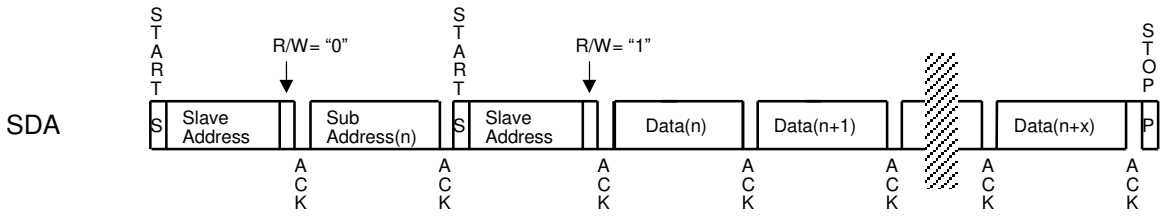


Figure 32. Random Address Read

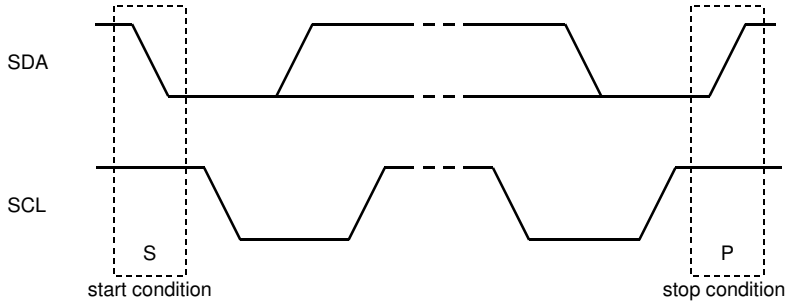


Figure 33. Start Condition and Stop Condition

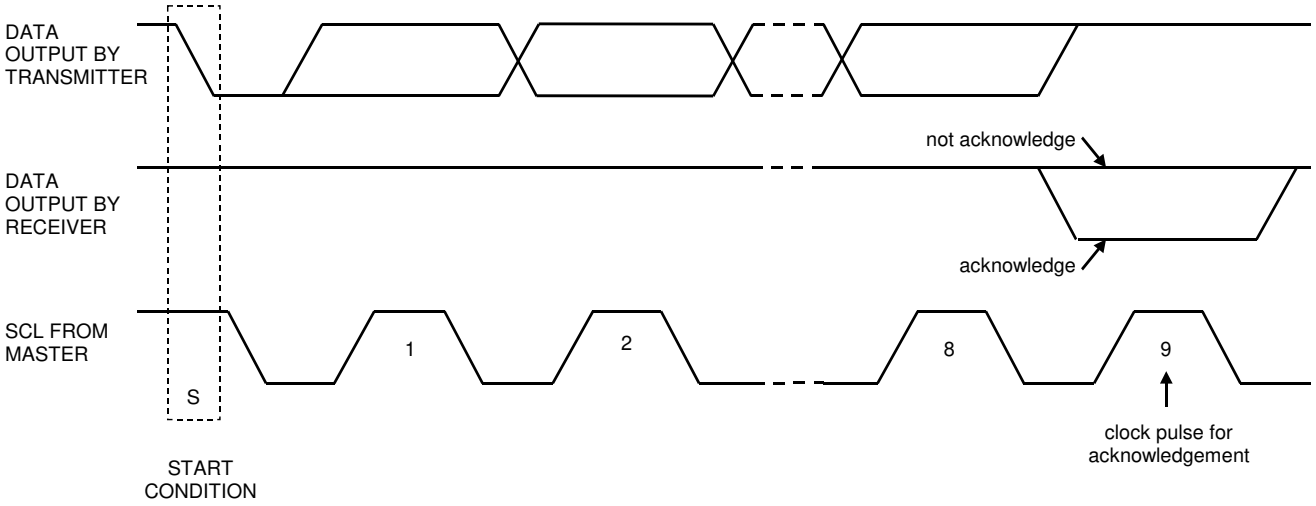


Figure 34. Acknowledge (I^2C Bus)

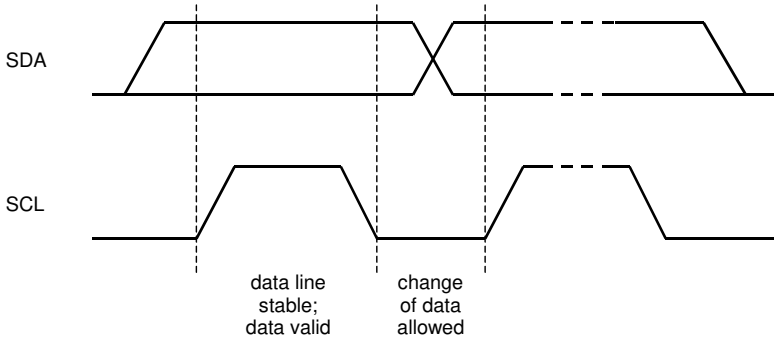


Figure 35. Bit Transfer (I^2C Bus)

Function List

Function	Default	Address	Bit	PCM	DSD	EX DF I/F
Attenuation Level	0dB	03H 04H	ATT7-0	Y	Y	-
External Digital Filter I/F Mode	Disable	00H	EXDF	Y	-	Y
Ex DF I/F mode clock setting	16fs(fs=44.1kHz)	00H	ECS	-	-	Y
Audio Data Interface Modes	24bit MSB justified	00H	DIF2-0	Y	-	Y
Data Zero Detect Enable	Disable	01H	DZFE	Y	Y	-
Data Zero Detect Mode	Separated	01H	DZFM	Y	Y	-
Minimum delay Filter Enable	Sharp roll-off filter	01H	SD	Y	-	-
De-emphasis Response	OFF	01H	DEM1-0	Y	-	-
Soft Mute Enable	Normal Operation	01H	SMUTE	Y	Y	-
DSD/PCM Mode Select	PCM mode	02H	DP	Y	Y	-
Master Clock Frequency Select at DSD mode	512fs	02H	DCKS	-	Y	-
MONO mode Stereo mode select	Stereo	02H	MONO	Y	Y	Y
Inverting Enable of DZF	"H" active	02H	DZFB	Y	Y	-
The data selection of L channel and R channel	R channel	02H	SELLR	Y	Y	Y
Sound Quality Adjustment	Natural Sound	08H	SC[2:0]	Y	Y	Y
Clock Synchronize	Not Available	07H	SYNCE	Y	-	-

Table 27. Function List2 (Y: Available, -: Not available)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	DP	0	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	Control4	INVL	INVR	0	0	0	0	DFS2	SSLOW
06H	Control5	DDM	DML	DMR	DMC	DMRE	DSDD1	DSDD0	DSDSEL
07H	Control6	0	0	0	0	0	0	0	SYNCE
08H	Control7	0	0	0	0	0	SC2	SC1	SC0
09H	Reserved	0	0	0	0	0	0	0	0

Notes:

Data must not be written into addresses from 07H to 1FH.

When the PDN pin goes to “L”, the registers are initialized to their default values.

When RSTN bit is set to “0”, only the internal timing is reset, and the registers are not initialized to their default values.

When the state of the PSN pin is changed, the AK4495S/95 should be reset by the PDN pin.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	EXDF	ECS	0	DIF2	DIF1	DIF0	RSTN
Default		0	0	0	0	0	1	0	0

RSTN: Internal Timing Reset

0: Reset. All registers are not initialized. (default)

1: Normal Operation

Writing “0” to this bit resets the internal timing circuit but register values are not initialized.

When the PSN pin = “H”, the AK4495S/95 operates regardless of the register setting.

DIF2-0: Audio Data Interface Modes (Table 18)

Initial value is “010” (Mode 2: 24-bit MSB justified).

ECS: EX DF I/F mode clock setting (Table 19)

0: 768kHz sampling rate (default)

1: 386kHz sampling rate

EXDF: External Digital Filter I/F Mode (Serial mode only)

0: Disable: Internal Digital Filter mode (default)

1: Enable: External Digital Filter mode

ACKS: Master Clock Frequency Auto Setting Mode Enable (PCM only)

0: Disable: Manual Setting Mode (default)

1: Enable: Auto Setting Mode

When ACKS bit = “1”, MCLK frequency and the sampling frequency are detected automatically.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
Default		0	0	1	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal Operation (default)
1: DAC outputs soft-muted.

DEM1-0: De-emphasis Response
Initial value is "01" (OFF).

DFS1-0: Sampling Speed Control
Initial value is "000" (Normal Speed). Click noise occurs when DFS2-0 bits are changed.

DFS2	DFS1	DFS0	Sampling Rate (fs)		
0	0	0	Normal Speed Mode	30kHz ~ 54kHz	(default)
0	0	1	Double Speed Mode	54kHz ~ 108kHz	
0	1	0	Quad Speed Mode	120kHz ~ 216kHz	
0	1	1	Reserved	-	
1	0	0	Oct Speed Mode	384kHz	
1	0	1	Hex Speed Mode	768kHz	
1	1	0	Reserved	-	
1	1	1	Reserved	-	

Table 9. Sampling Speed (Manual Setting Mode @Serial Mode)

SD: Minimum delay Filter Enable
0: Traditional filter
1: Short delay filter (default)

SD	SLOW	Mode	
0	0	Sharp roll-off filter	
0	1	Slow roll-off filter	
1	0	Short delay sharp roll off filter	(default)
1	1	Short delay slow roll off filter	

Table 14. Digital Filter Setting

DZFM: Data Zero Detect Mode
0: Channel Separated Mode (default)
1: Channel ANDed Mode
If the DZFM bit is set to "1", the DZF pins of both L and R channels go to "H" only when the input data at both channels are continuously zeros for 8192 LRCK cycles.

DZFE: Data Zero Detect Enable
0: Disable (default)
1: Enable
Zero detect function can be disabled by DZFE bit "0". In this case, the DZF pins of both channels are always "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	DP	0	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
Default		0	0	0	0	0	0	0	0

SLOW: Slow Roll-off Filter Enable
0: Sharp roll-off filter (default)
1: Slow roll-off filter

SD	SLOW	Mode	
0	0	Sharp roll-off filter	
0	1	Slow roll-off filter	
1	0	Short delay sharp roll off filter	(default)
1	1	Short delay slow roll off filter	

Table 14. Digital Filter Setting

SELLR: The data selection of L channel and R channel, when MONO mode
0: All channels output L channel data, when MONO mode. (default)
1: All channels output R channel data, when MONO mode.
This bit is enabled when MONO bit is "1". The AK4495S/95 outputs Lch data to both channels when SELLR bit is "0" and outputs Rch data to both channels when SELLR bit is "1".

DZFB: Inverting Enable of DZF
0: DZF pin goes "H" at Zero Detection (default)
1: DZF pin goes "L" at Zero Detection

DZFE	DZFB	Data	DZF-pin
0	0	-	L
	1	-	H
1	0	not zero	L
		Zero detect	H
	1	not zero	H
		Zero detect	L

Table 23. Zero Detect Function and DZF Pin Output

MONO: MONO mode Stereo mode select
0: Stereo mode (default)
1: MONO mode
When MONO bit is "1", MONO mode is enabled.

DCKB: Polarity of DCLK (DSD Only)
0: DSD data is output from DCLK falling edge. (default)
1: DSD data is output from DCLK rising edge.

DCKS: Master Clock Frequency Select at DSD mode (DSD only)
0: 512fs (default)
1: 768fs

DP: DSD/PCM Mode Select
0: PCM Mode (default)
1: DSD Mode
When D/P bit is changed, the AK4495S/95 should be reset by RSTN bit.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
Default		1	1	1	1	1	1	1	1

ATT7-0: Attenuation Level

255 levels, 0.5dB step

Data	Attenuation
FFH	0dB
FEH	-0.5dB
FDH	-1.0dB
:	:
:	:
02H	-126.5dB
01H	-127.0dB
00H	MUTE (-∞)

The transition between set values is soft transition of 7425 levels. It takes 7424/fs (168ms@fs=44.1kHz) from FFH (0dB) to 00H (MUTE). If the PDN pin goes to "L", the ATTs are initialized to FFH. The ATTs are FFH when RSTN bit= "0". When RSTN return to "1", the ATTs fade to their current value. This digital attenuator is independent of soft mute function.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Control 4	INVL	INVR	0	0	0	0	DFS2	SSLOW
Default		0	0	0	0	0	0	0	0

SSLOW: Super Slow roll off Filter Enable

0: Disable (default)

1: Enable

DFS2: Sampling Speed Control (Table 9)

Initial value is "000" (Normal Speed). Click noise occurs when DFS2-0 bits are changed. (01H, D4, D3: DFS1-0 bits)

DFS2	DFS1	DFS0	Sampling Rate (fs)		
0	0	0	Normal Speed Mode	30kHz ~ 54kHz	(default)
0	0	1	Double Speed Mode	54kHz ~ 108kHz	
0	1	0	Quad Speed Mode	120kHz ~ 216kHz	
0	1	1	Reserved	-	
1	0	0	Oct Speed Mode	384kHz	
1	0	1	Hex Speed Mode	768kHz	
1	1	0	Reserved	-	
1	1	1	Reserved	-	

Table 9. Sampling Speed (Manual Setting Mode @Serial Mode)

INVR: AOUTR Output Phase Inverting

0: Disable (default)

1: Enable

INVL: AOUTL Output Phase Inverting

0: Disable (default)

1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Control 5	DDM	DML	DMR	DMC	DMRE	DSDD1	DSDD0	DSDSEL
Default		0	0	0	0	0	0	0	0

DSDSEL: DSD sampling speed control
0: 2.8MHz (64fs) (default)
1: 5.6MHz (128fs)

DSDSEL bit	DSD data stream	
0	2.8224MHz	(default)
1	5.6448MHz	

Table 16. DSD Sampling Speed Control

DSDD1-0: DSD play back path control

DSDD1	DSDD0	Mode	
0	0	Normal path	(default)
0	1	Volume pass	
1	0	Reserved	
1	1	Reserved	

Table 17. DSD Play Back Mode Control

DMRE: DSD mute release
0: Hold (default)
1: Release Mute
This register is only valid when DDM bit = "1" and DMC bit = "1". When the AK4495S/95 mutes DSD data by DDM and DMC bits settings, the mute is released by setting DMRE bit to "1".

DMC: DSD mute control
0: Auto Return (default)
1: Mute Hold (manual return)
This register is only valid when DDM bit = "1". It selects the mute releasing mode of when the DSD data level becomes under full-scale after the AK4495S/95 mutes DSD data by DDM bit setting.

DDM: DSD data mute
0: Disable (default)
1: Enable
The AK4495S/95 has an internal mute function that mutes the output when DSD audio data becomes all "1" or all "0" for 2048sample (1/fs). DDM bit controls this function.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Control 6	0	0	0	0	0	0	0	SYNCE
Default		0	0	0	0	0	0	0	0

SYNCE: Synchronization control
0: Disable (default)
1: Enable
This register enables the function that synchronizes multiple AK4495S/95s when using more than one AK4495S/95s in a system.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Control 7	0	0	0	0	0	SC2	SC1	SC0
Default		0	0	0	0	0	0	0	0

SC1-0: Sound control bit

SC1	SC0	Mode	
0	0	1	(default)
0	1	2	
1	0	3	
1	1	4	

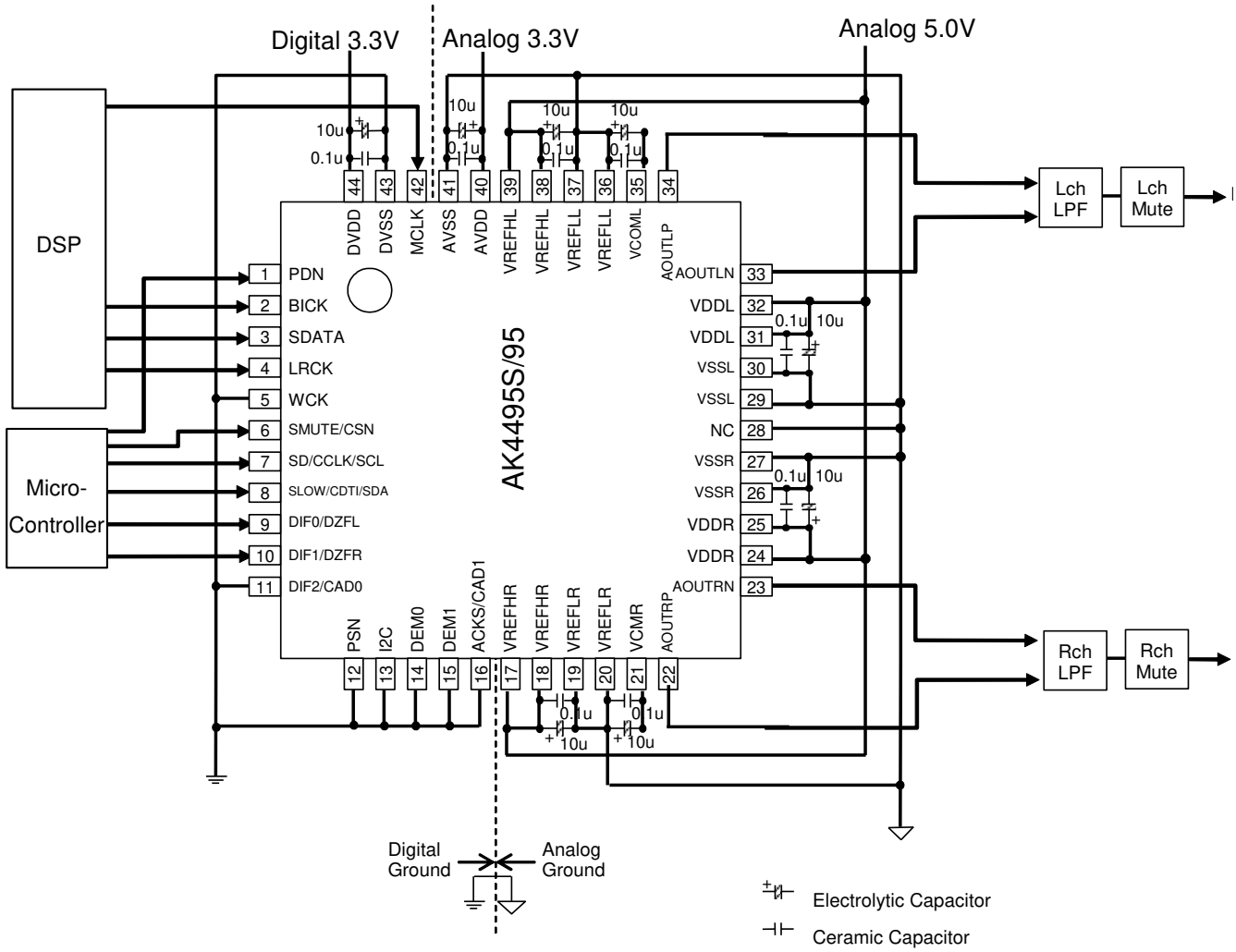
Table 25. SC1-0 bits Control

SC2: Sound position control bit
0: Disable (default)
1: Sound Mode 5

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Reserved	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0

10. Recommended External Circuits

Figure 36 shows the system connection diagram. Figure 38, Figure 39 and Figure 40 show the analog output circuit examples. The evaluation board (AKD4495/AKD4495S) demonstrates the optimum layout, power supply arrangements and measurement results.



Notes:

- Chip Address = "00". BICK = 64fs, LRCK = fs
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- AVSS, DVSS, VSSL, VSSR, VREFLL, VREFLR must be connected to the same analog ground plane.
- When AOUT drives a capacitive load, some resistance should be connected in series between AOUT and the capacitive load.
- All input pins except pull-down/pull-up pins should not be allowed to float.

Figure 36. Typical Connection Diagram (AVDD=3.3V, VDDL/R = 5.0V, DVDD=3.3V, Serial control mode)

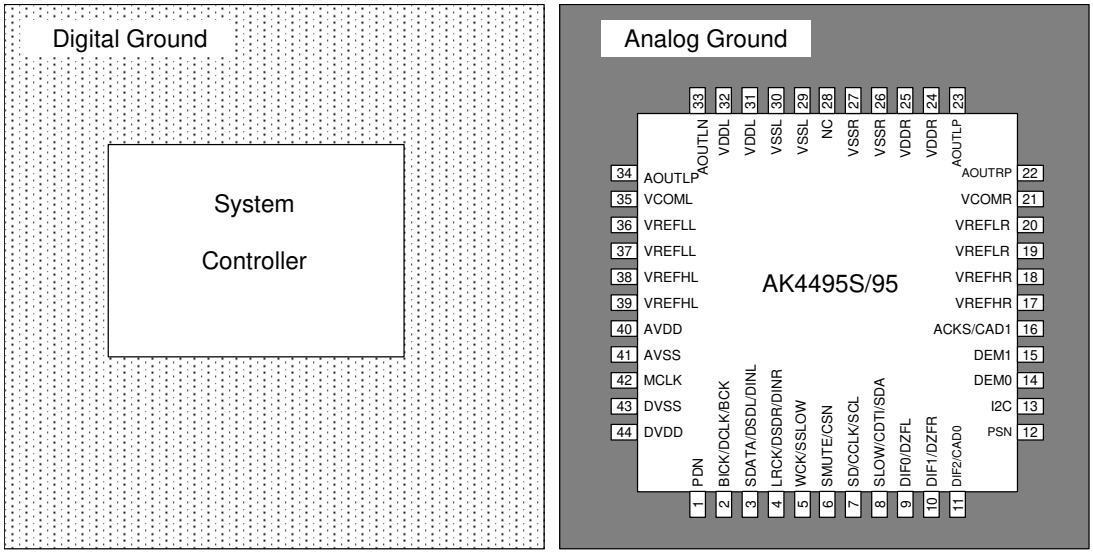


Figure 37. Ground Layout

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD, VDDL/R and DVDD respectively. AVDD and VDDL/R are supplied from analog supply in system and DVDD is supplied from digital supply in system. Power lines of AVDD, VDDL/R and DVDD should be distributed separately from the point with low impedance of regulator etc. The power up sequence between AVDD, VDDL/R and DVDD is not critical. AVSS, DVSS, VSSL, VSSR **must be connected to the same analog ground plane.** Decoupling capacitors for high frequency should be placed as near as possible to the supply pin.

2. Voltage Reference

The differential voltage between VREFHL/R and VREFLL/R sets the analog output range. The VREFHL/R pin is normally connected to AVDD, and the VREFLL/R pin is normally connected to VSS1/2/3. VREFHL/R and VREFLL/R should be connected with a 0.1µF ceramic capacitor as near as possible to the pin to eliminate the effects of high frequency noise. No load current may be drawn from VCML/R pin. All signals, especially clocks, should be kept away from the VREFHL/R and VREFLL/R pins in order to avoid unwanted noise coupling into the AK4495S/95.

3. Analog Outputs

The analog outputs are full differential outputs and 2.8Vpp (typ, VREFHL/R − VREFLL/R = 5V) centered around VDDR/2 and VDDL/2 voltages. The differential outputs are summed externally, V_{AOUT} = (AOUT+) − (AOUT−) between AOUT+ and AOUT−. If the summing gain is 1, the output range is 5.6Vpp (typ, VREFHL/R − VREFLL/R = 5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage (V_{AOUT}) is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal V_{AOUT} is 0V for 000000H(@24bit).

The internal switched-capacitor filters attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Figure 38 shows an example of external LPF circuit summing the differential outputs by an op-amp. Figure 39 shows an example of differential outputs and LPF circuit example by three op-amps.

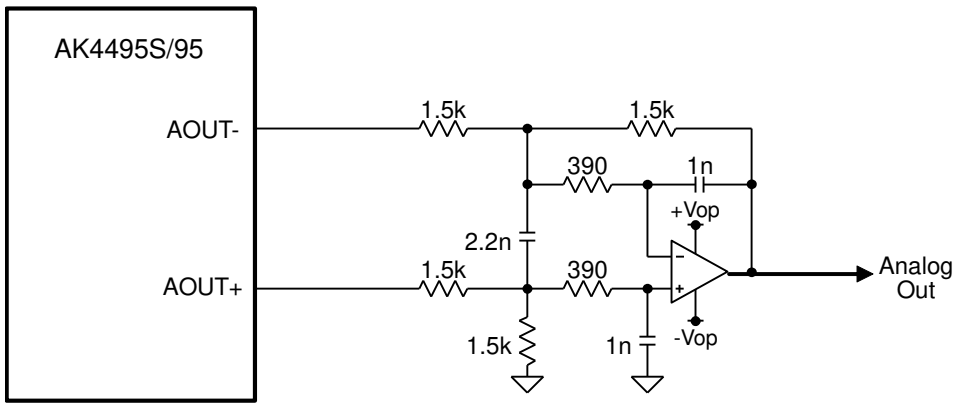


Figure 38. External LPF Circuit Example 1 for PCM (fc = 99.2kHz, Q=0.704)

Frequency Response	Gain
20kHz	–0.011dB
40kHz	–0.127dB
80kHz	–1.571dB

Table 28. Frequency Response of External LPF Circuit Example 1 for PCM

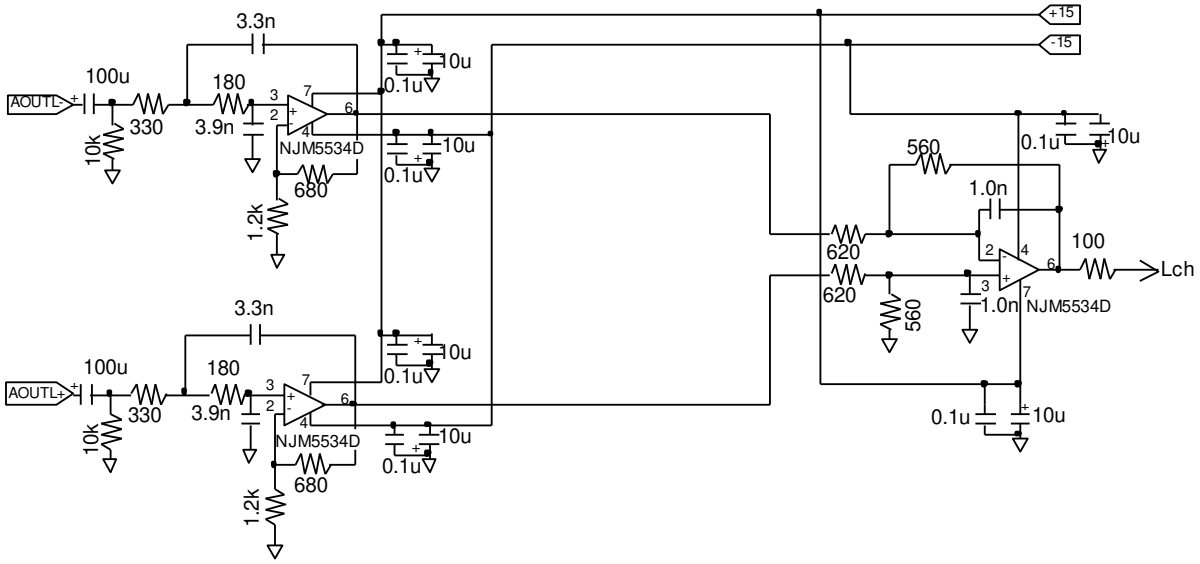


Figure 39. External LPF Circuit Example 2 for PCM

		1st Stage	2nd Stage	Total
Cut-off Frequency		182kHz	284kHz	-
Q		0.637	-	-
Gain		+3.9dB	-0.88dB	+3.02dB
Frequency Response	20kHz	-0.025	-0.021	-0.046dB
	40kHz	-0.106	-0.085	-0.191dB
	80kHz	-0.517	-0.331	-0.848dB

Table 29. Frequency Response of External LPF Circuit Example 2 for PCM

It is recommended for SACD format book (Scarlet Book) that the filter response at SACD playback is an analog low pass filter with a cut-off frequency of maximum 50kHz and a slope of minimum 30dB/Oct. The AK4495S/95 can achieve this filter response by combination of the internal filter (Table 30) and an external filter (Figure 40).

Frequency	Gain
20kHz	–0.4dB
50kHz	–2.8dB
100kHz	–15.5dB

Table 30. Internal Filter Response at DSD Mode

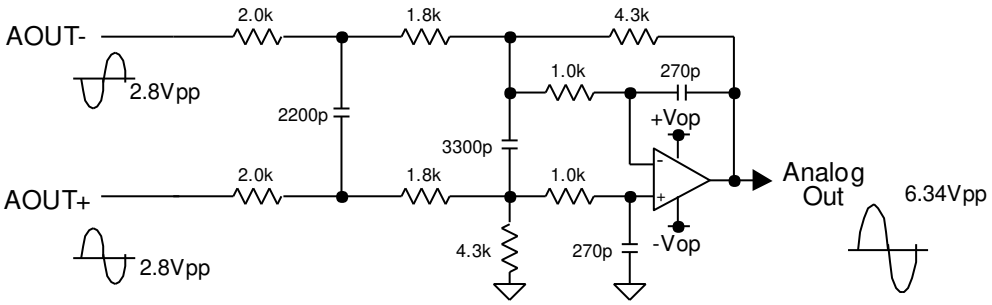


Figure 40. External 3rd Order LPF Circuit Example for DSD

Frequency	Gain
20kHz	–0.05dB
50kHz	–0.51dB
100kHz	–16.8dB

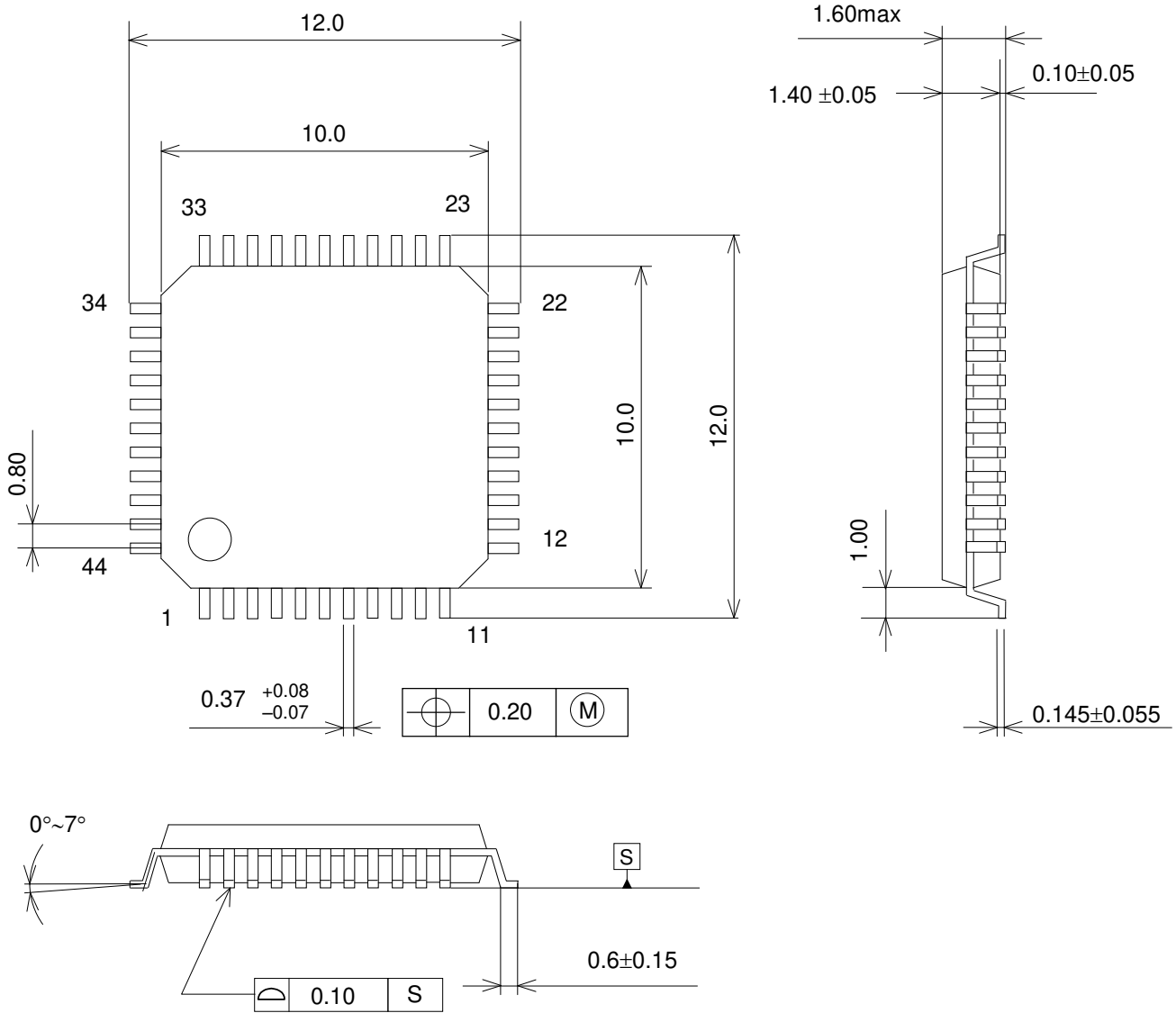
DC gain = 1.07dB

Table 31. 3rd Order LPF (Figure 40) Response

11. Package

■ Outline Dimensions (AK4495S)

44-pin LQFP (Unit: mm)

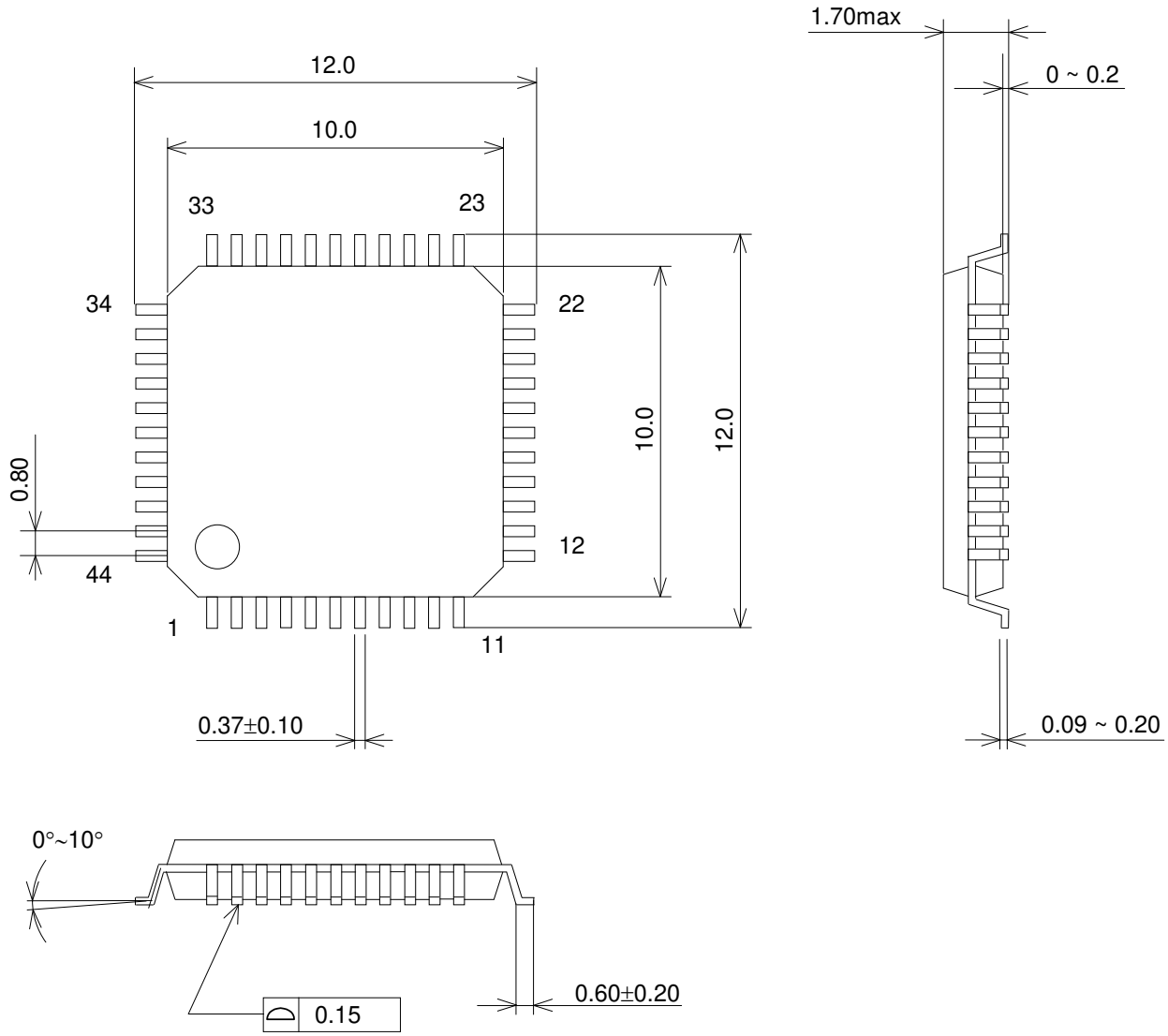


■ Material & Lead finish

Package molding compound:	Epoxy, Halogen (bromine and chlorine) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

■ Outline Dimensions (AK4495)

44-pin LQFP (Unit: mm)



■ Material & Lead finish

Package molding compound:	Epoxy, Halogen (bromine and chlorine) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

■ Marking (AK4495S)

1) AKM Logo
2) Pin #1 indication
3) Date Code: XXXXXXX(7 digits)
4) Marking Code: AK4495S
5) Audio 4 pro Logo

■ Marking (AK4495)

1) AKM Logo
2) Pin #1 indication
3) Date Code: XXXXXXX(7 digits)
4) Marking Code: AK4495
5) Audio 4 pro Logo

12. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
13/11/15	00	First Edition		
14/02/25	01	Error Correction	47	■ Register Definitions The description of SELLR bit was changed.
14/04/17	02	Description Addition	5, 56, 57	■ Ordering Guide, Outline Dimensions, Marking The AK4495 was added to this document.
			2	2. Features THD+N: "-105dB (Analog Block Power Supply 7V)" was added. DR, S/N: "120dB" was added.
			10	8. Electrical Characteristics Dynamic Characteristics, THD+N fs=44.1kHz, 0dBFS VDDL/R=VREFHL/R=7.0Vwas added: -105dB (typ)
			12, 14, 16, 18	Figure 1 ~ 8 were added.
		Error Correction	27	■ System Clock Table 3 was changed.
			27, 29	Table 6 and Table 12 were changed.
			53-54	■ Register Definitions Address 0x06: "Control 4" → "Control 5" Address 0x07: "Control 5" → "Control 6" Address 0x08: "Control 6" → "Control 7" Address 0x09: "Control 7" → "Reserved"

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