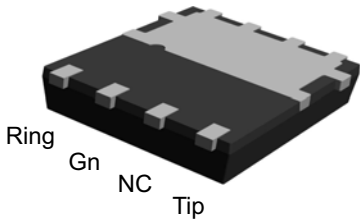
LCP154DJF

Programmable transient voltage suppressor for SLIC protection

Datasheet - production data



PowerFLAT™ 5x6

Features

- Programmable transient suppressor
- Wide negative firing voltage range: V_{Gn} = -175 V max.
- Low dynamic switching voltages: V_{FP} and V_{DGL}
- Low gate triggering current: I_{GT} = 5 mA max.
- Peak pulse current:
  - I_{PP} = 100 A (10/1000 µs)
  - I_{PP} = 150 A (5/310 µs)
  - I_{PP} = 500 A (2/10 µs)
- Holding current: I_H = 150 mA min.

Benefits

- Trisil™ is not subject to ageing and provides a fail safe mode in short circuit for a better level of protection.
- Trisils are used to ensure equipment meets various standards such as UL60950, IEC 60950 / CSA C22.2, UL1459, TIA-968-A (formerly FCC part 68)
- Trisils have UL94 V0 approved resin (Trisils are UL497B approved [file: E136224]).

Description

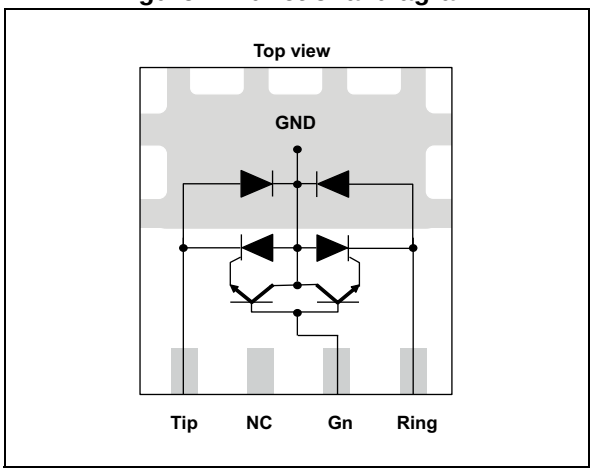
This device has been especially designed to protect new high voltage, as well as classical SLICs, against transient overvoltages.

Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to -V_{BAT} through the gate.

LCP154DJF is specified to comply with ITU-T K20/21/45 and GR1089-Core when associated with Cooper Bussmann Telecom Circuit Protector fuse TCP 1.25 A.

LCP154DJF is packaged in a PowerFLAT™ 5x6 to meet IEC/UL 60950 clearance requirements.

Figure 1. Functional diagram



TM: Trisil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Standards compliance

Standard	Peak surge voltage (V)	Voltage waveform	Required peak current (A)	Current waveform	Minimum serial resistor to meet standard (Ω)
GR-1089 Core First level	2500 1000	2/10 µs 10/1000 µs	500 100	2/10 µs 10/1000 µs	0 0
GR-1089 Core Second level	5000	2/10 µs	500	2/10 µs	0
GR-1089 Core Intra-building	1500	2/10 µs	100	2/10 µs	0
ITU-T-K20/K21	6000 1500	10/700 µs	150 37.5	5/310 µs	0 0
ITU-T-K20 (IEC 61000-4-2)	8000 15000	1/60 ns	ESD contact discharge ESD air discharge		0 0
IEC 61000-4-5	4000 4000	10/700 µs 1.2/50 µs	100 100	5/310 µs 8/20 µs	0 0
TIA-968-A, lightning surge type A	1500 800	10/160 µs 10/560 µs	200 100	10/160 µs 10/560 µs	0 0
TIA-968-A, lightning surge type B	1000	9/720 µs	25	5/320 µs	0

Table 2. Absolute ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current(1)	10/1000 µs 8/20 µs 10/560 µs 5/310 µs 10/160 µs 1/20 µs 2/10 µs	100 400 140 150 200 400 500	A
I_{TSM}	Non repetitive surge peak on-state current (50 Hz sinusoidal)(1)	t = 10 ms t = 0.2 s t = 1 s t = 2 s t = 15 min t = 30 min	35 18 12 10 4 3	A
V_{GN}	Negative battery voltage		-175	V
T_{stg} T_j	Storage temperature range Operating junction temperature range		-55 to +150 -55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

1. The rated current values may be applied either to the RING to GND or to the Tip to GND terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the GND terminal current will be twice the rated current value of an individual terminal pair).

Figure 2. Electrical characteristics (definitions)

Symbol		Parameter
I_{GT}	=	Gate triggering current
V_{FP}	=	Peak forward voltage LINE / GND
V_{GT}	=	Gate triggering voltage
V_F	=	Forward drop voltage LINE /GND
I_{RG}	=	Reverse leakage current GATE / LINE
I_H	=	Holding current
V_{RG}	=	Reverse voltage GATE / LINE
V_{DGL}	=	Dynamic switching voltage GATE / LINE
I_{PP}	=	Peak pulse current
I_R	=	Breakdown current
V_F	=	Forward drop voltage LINE / GND
C	=	Capacitance LINE /GND

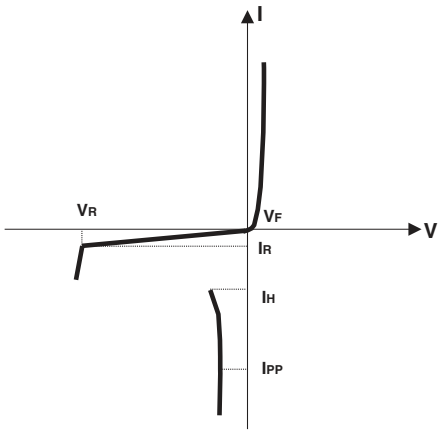


Figure 3. Pulse waveform

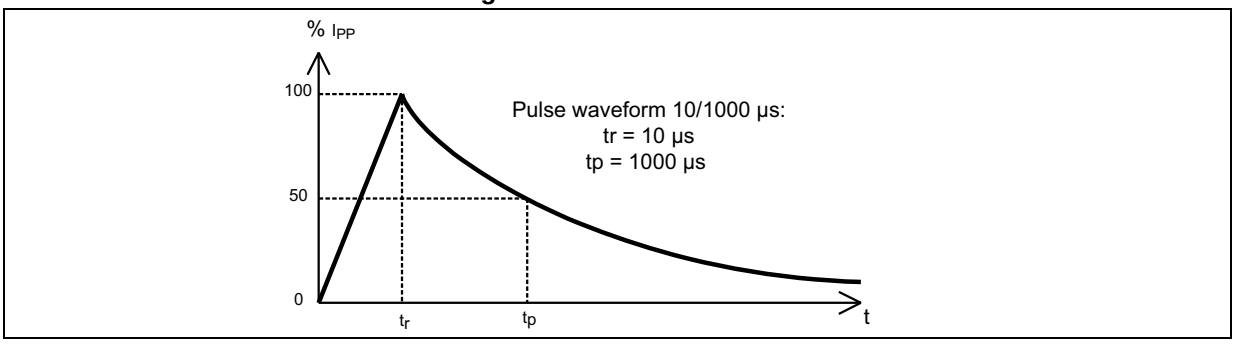


Table 3. Parameters (T_{amb} = 25 °C unless otherwise specified)

Symbol	Test conditions			Min	Typ	Max	Unit
I_{GT}	V_{LINE} = -48 V			0.1		5	mA
I_H	V_{Gn} = -48 V			150			mA
V_{GT}(1)	at I_{GT}					2.5	V
I_{RG}	V_{RG} = -175 V V_{RG} = -175 V		T_j = 25 °C T_j = 85 °C			5 50	µA
V_{DGL}(1)	V_{Gn} = -48 V(1)	10/700 µs 2/10 µs	I_{PP} = 150 A I_{PP} = 200 A			12 20	V
V_F	I_F = 5 A		t = 500 µs			3	V
$V_{FP(I)}$	10/700 µs 2/10 µs		I_{pp} = 150 A I_{pp} = 200 A			7 10	V
I_R	$V_{Gn\ /\ LINE}$ = -1 V V_{LINE} = -175 V $V_{Gn\ /\ LINE}$ = -1 V V_{LINE} = -175 V		T_j = 25 °C T_j = 85 °C			5 50	µA
C	V_{LINE} = -50 V, V_{RMS} = 1 V, f = 1 MHz V_{LINE} = -2 V, V_{RMS} = 1 V, f = 1 MHz				35 100		pF
C_G	Gate decoupling capacitance			100	220		nF

1. The oscillations with a time duration lower than 50 ns are not taken into account.

2 Technical information

Figure 4. Example of PCB layout based on LCP154DJF protection

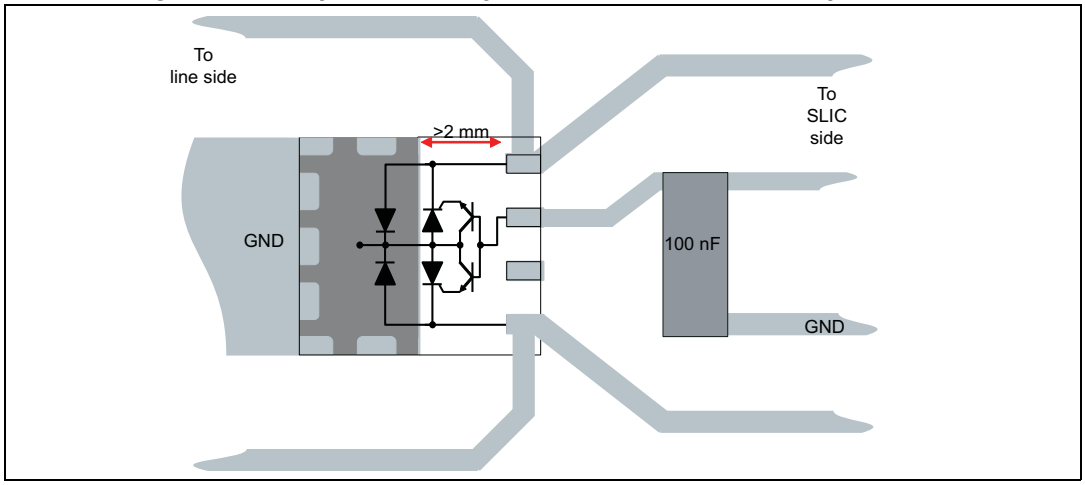


Figure 4 shows the classical PCB layout used to optimize line protection. The 2 mm distance is used to comply with IEC/UL 60950 clearance requirements.

The capacitor C is used to speed up the crowbar structure firing during the fast surge edges.

This allows minimization of the dynamic breakover voltage at the SLIC Tip and Ring inputs during fast strikes. Note that this capacitor is generally present around the SLIC - Vbat pin.

So to be efficient it has to be as close as possible from the LCP Gate pin and from the reference ground track (or plan).

The schematics of *Figure 5* give the topology used to protect all SLICs according to ITU-T K20/21/45 and GR1089-Core.

Figure 5. Protection of high voltage SLIC

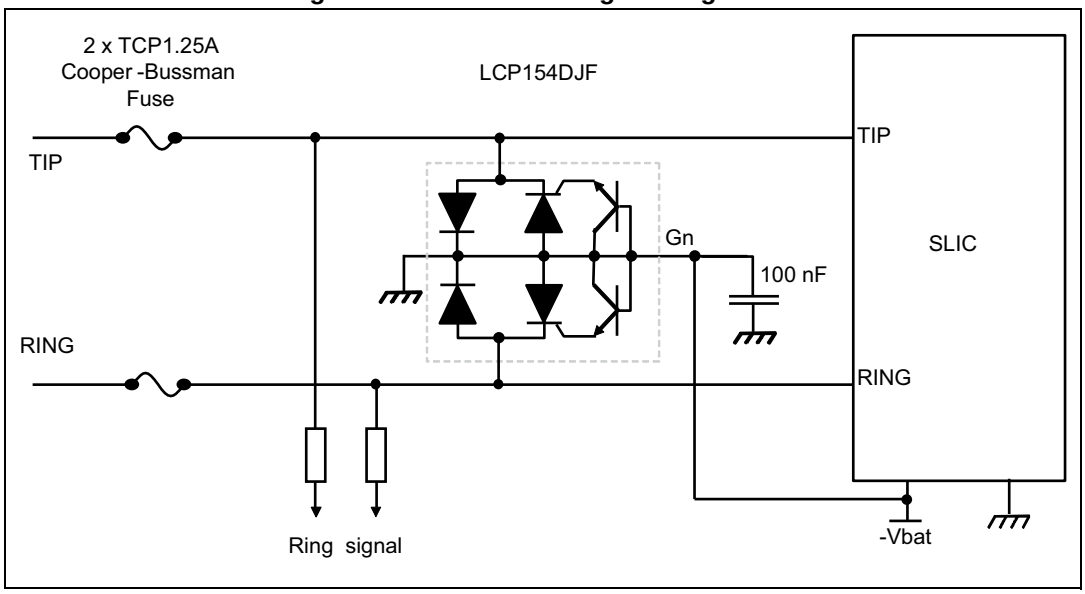


Figure 6. Surge peak current versus duration

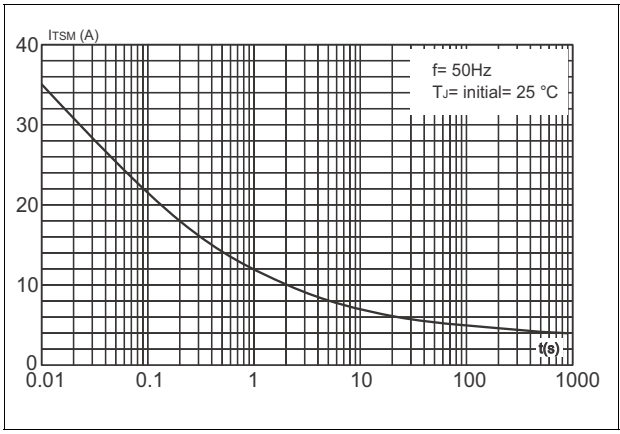
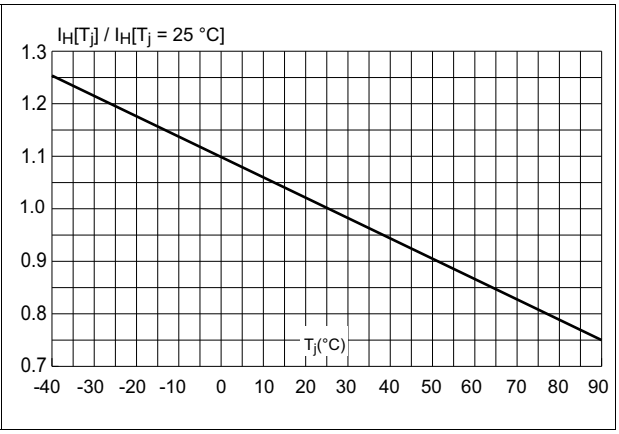


Figure 7. Relative variation of holding current versus junction temperature



3 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.*
ECOPACK® is an ST trademark.

3.1 PowerFLAT™ 5x6 package information

Figure 8. PowerFLAT™ 5x6 package outline

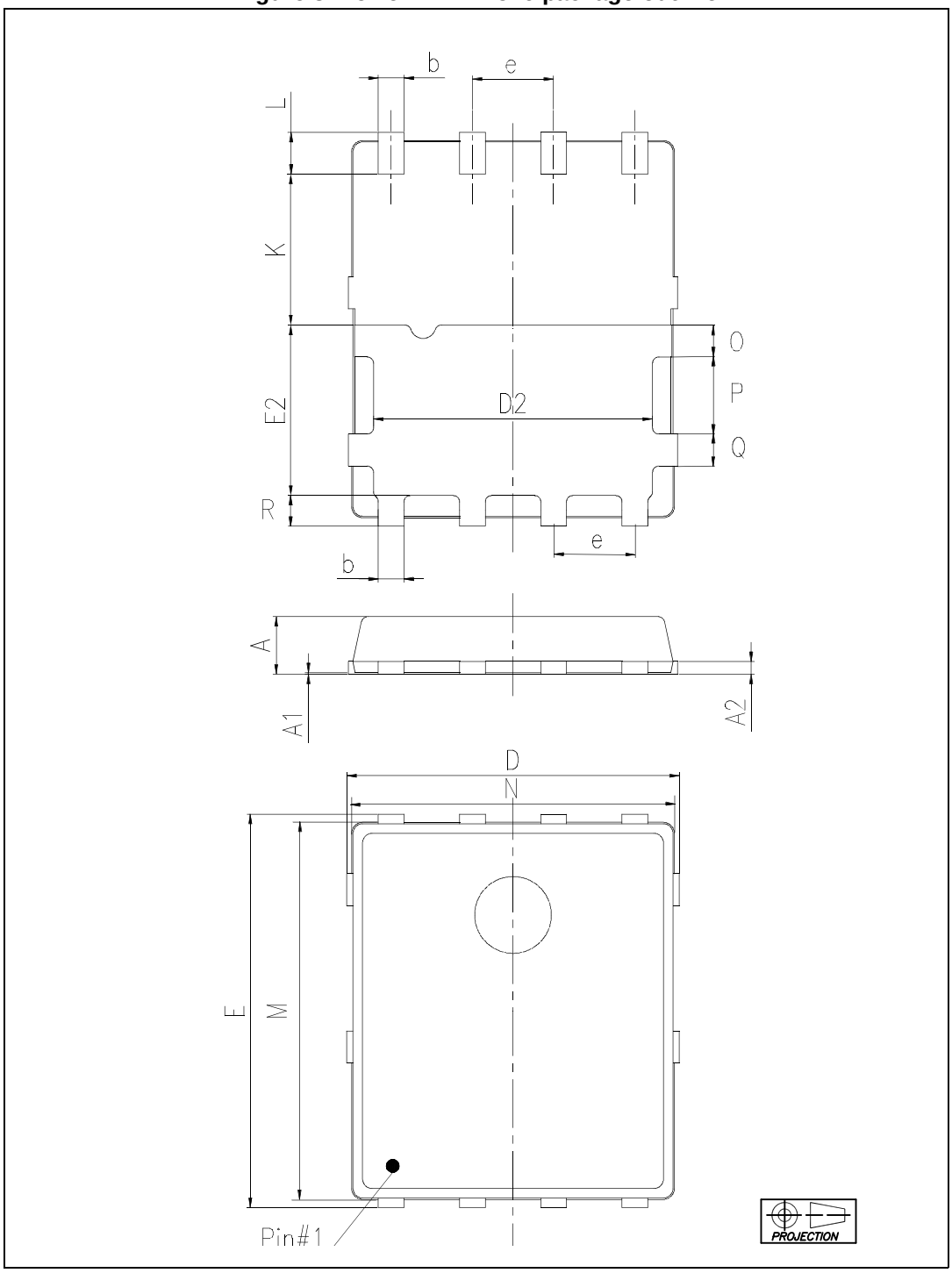


Table 4. PowerFLAT™ 5x6 mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.00	0.315		0.394
A1	0.02		0.05	0.008		0.020
A2		0.25			0.098	
b	0.30		0.50	0.118		0.197
D	5.0		5.4	1.969		2.126
E	5.95		6.35	2.343		2.500
D2	4.25		4.45	1.673		1.752
E2	2.56		2.76	1.008		1.087
e		1.27			0.500	
L	0.50		0.80	0.197		0.315
K	2.25			0.886		
M	5.75		5.95	2.264		2.343
N	4.90		5.10	1.929		2.008
O	0.40		0.60	0.157		0.236
P	1.10		1.30	0.433		0.512
Q	0.40		0.60	0.157		0.236
R	0.35		0.65	0.138		0.256

Figure 9. PowerFLAT™ 5x6 recommended footprint (all dimensions are in mm.)

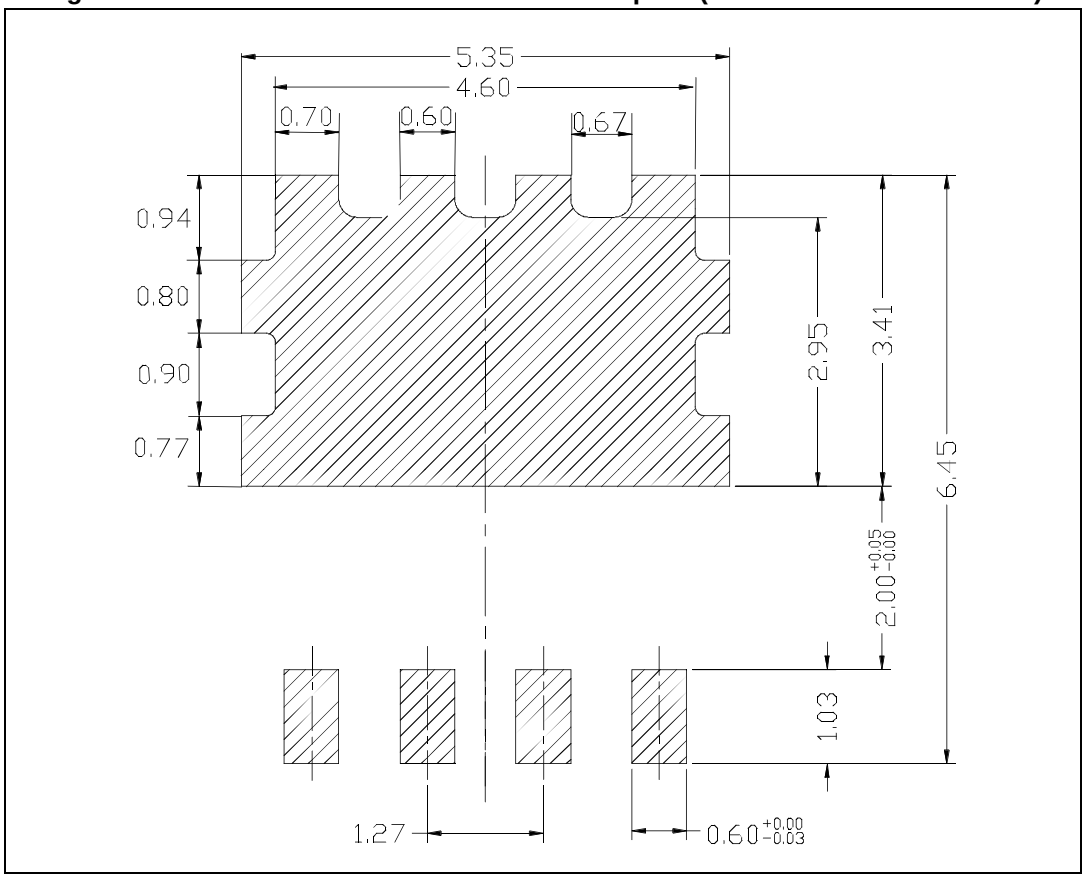
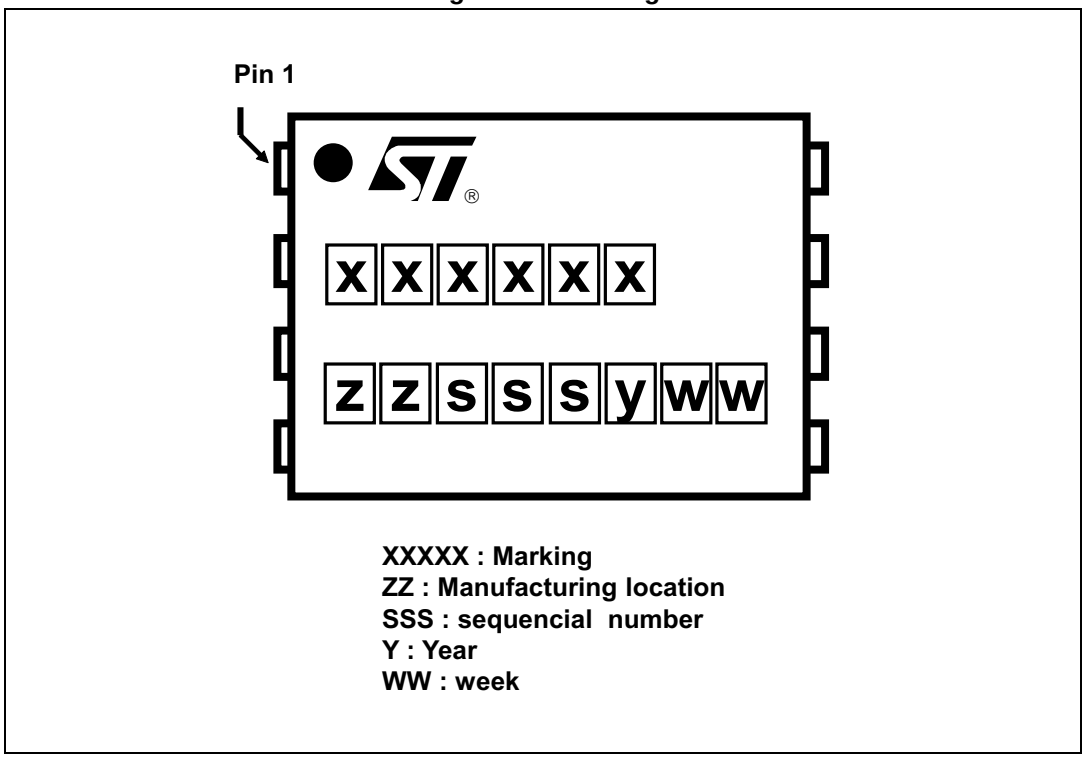


Figure 10. Marking



4 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
LCP154DJF	CP154	PowerFLAT 5x6	91 mg	3000	Tape and reel

5 Revision history

Table 6. Document revision history

Date	Revision	Changes
25-Sep-2015	1	First issue.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.