

**MOTOROLA**  
**SEMICONDUCTOR**  
**TECHNICAL DATA**

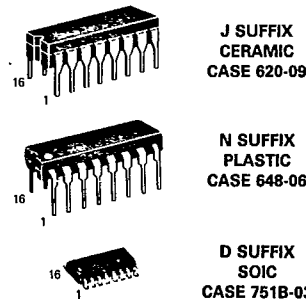
**MC54/74HC259**

*Advance Information*  
**8-Bit Addressable Latch/  
1-of-8 Decoder**  
**High-Performance Silicon-Gate CMOS**

The MC54/74HC259 is identical in pinout to the LS259. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode all outputs are LOW and unaffected by the address and data inputs. When operating the HC259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 202 FETs or 50.5 Equivalent Gates



**ORDERING INFORMATION**

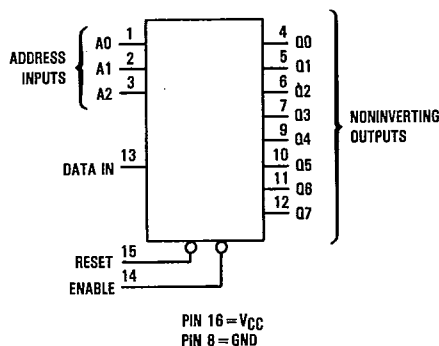
MC74HCXXXN Plastic  
MC54HCXXXJ Ceramic  
MC74HCXXXD SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
Dimensions in Chapter 7.

**PIN ASSIGNMENT**

A0	1	16	V <sub>CC</sub>
A1	2	15	RESET
A2	3	14	ENABLE
DATA IN	4	13	DATA IN
Q1	5	12	Q7
Q2	6	11	Q6
Q3	7	10	Q5
GND	8	9	Q4

**LOGIC DIAGRAM**



**MODE SELECTION TABLE**

Enable	Reset	Mode
L	H	Addressable Latch
H	H	Memory
L	L	8-Line Demultiplexer
H	L	Reset

**LATCH SELECTION TABLE**

Address Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54/74HC259

T-66-21-55

MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Packaget	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260	°C
		300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-65	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V	0	1000	ns
		V <sub>CC</sub> =4.5 V	0	500	
		V <sub>CC</sub> =6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -65°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.70	μA
			6.0	5.48	5.34	5.20	
			6.0	0.26	0.33	0.40	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	4.5	0.26	0.33	0.40	μA
			6.0	0.26	0.33	0.40	
			6.0	±0.1	±1.0	±1.0	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

5

MC54/74HC259

T-66-21-55

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Data to Output (Figures 1 and 6)	2.0	185	230	280	ns
		4.5	37	46	56	
		6.0	31	39	48	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Address Select to Output (Figures 2 and 6)	2.0	215	270	325	ns
		4.5	43	54	65	
		6.0	37	46	55	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Enable to Output (Figures 3 and 6)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Output (Figures 4 and 6)	2.0	155	195	235	ns
		4.5	31	39	47	
		6.0	26	33	40	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	--	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		30	

TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, Address or Data to Enable (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Enable to Address or Data (Figure 5)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t <sub>w</sub>	Minimum Pulse Width, Reset or Enable (Figure 3 or 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

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T-66-21-55

MC54/74HC259

SWITCHING WAVEFORMS

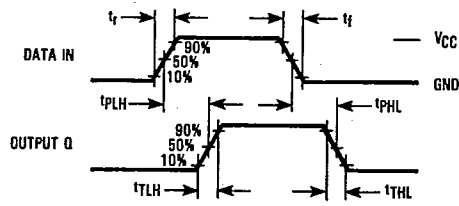


Figure 1

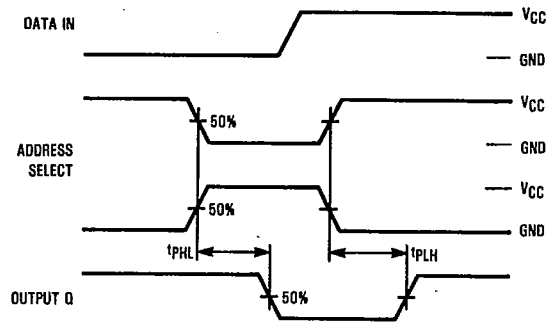


Figure 2

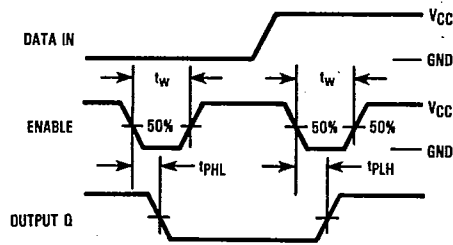


Figure 3

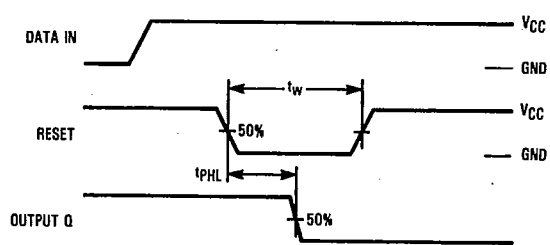


Figure 4

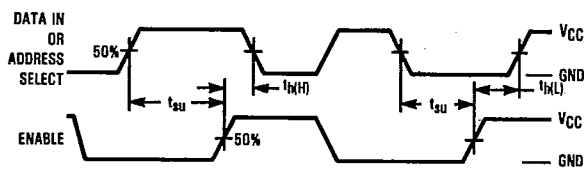
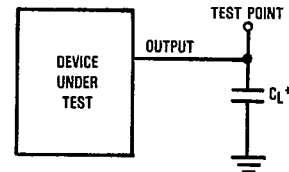


Figure 5



\*Includes all probe and jig capacitance.

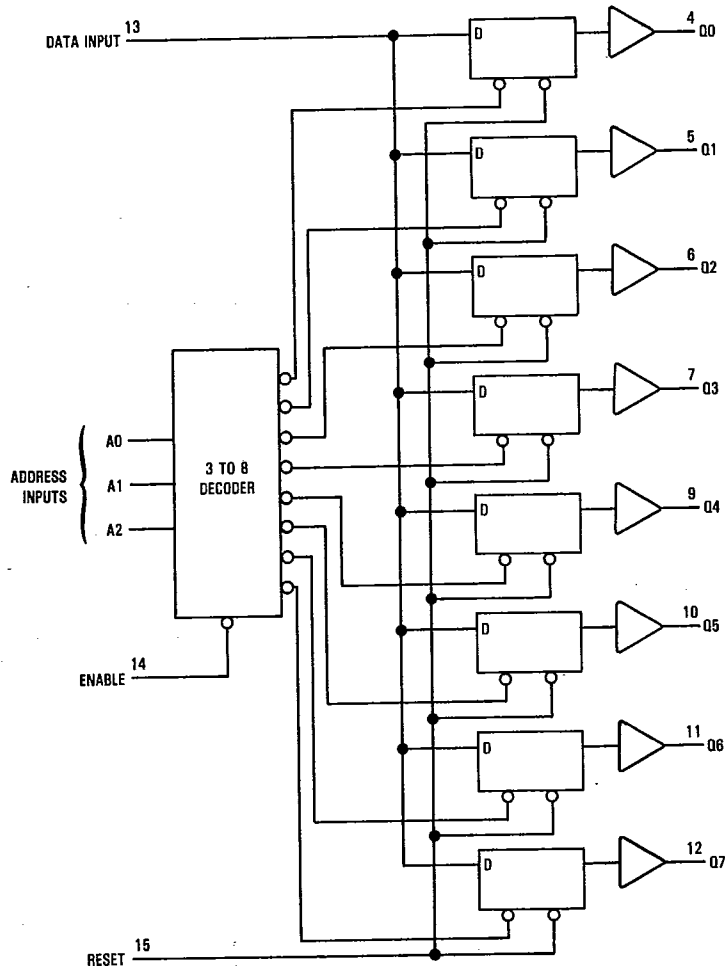
Figure 6. Test Circuit

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MC54/74HC259

T-66-21-55

EXPANDED LOGIC DIAGRAM



5