

## Low Skew, 1-To-2 LVC MOS / LV TTL Fanout Buffer

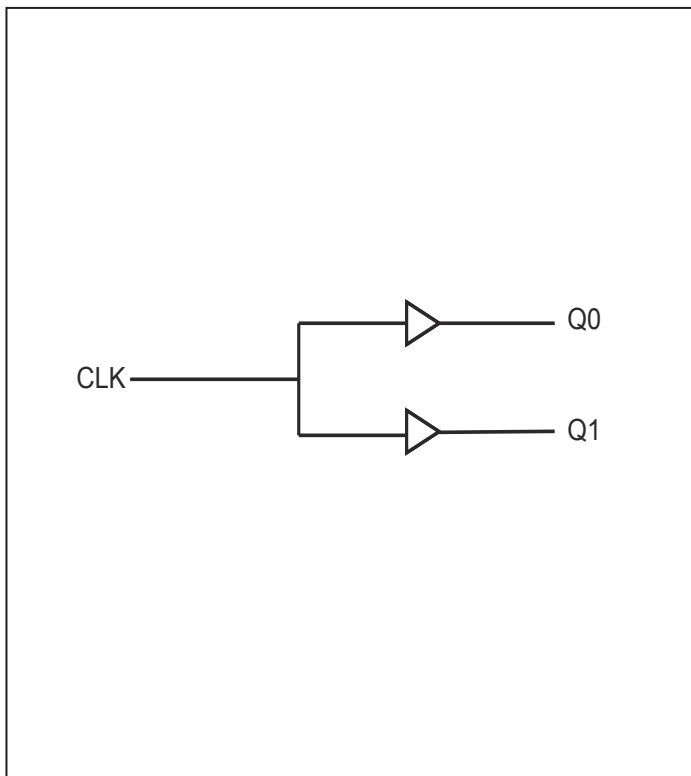
### Features

- 2 LVC MOS / LV TTL outputs
- LVC MOS / LV TTL clock input accepts LVC MOS or LV TTL input levels
- Maximum output frequency: 250MHz
- Output skew: 25ps (typical)
- Part-to-part skew: 250ps (typical)
- Small 8 lead SOIC package saves board space
- Full 3.3V, 2.5V operation modes
- -40°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

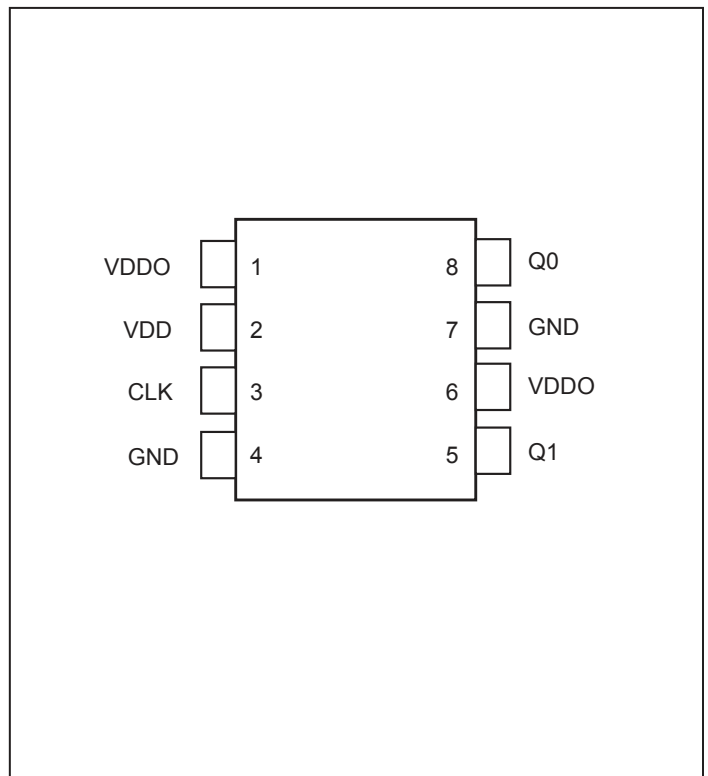
### Description

The PI6C49X0202 is a low skew, 1-to-2 LVC MOS/LV TTL High Performance Fanout Buffer. The PI6C49X0202 has a single ended clock input. The single ended clock input accepts LVC MOS or LV TTL input levels. The PI6C49X0202 features a pair of LVC MOS/LV TTL outputs. Guaranteed output and part-to-part skew characteristics make the PI6C49X0202 ideal for clock distribution applications demanding well defined performance and repeatability.

### Block Diagram



### Pin Assignment



**Pin Descriptions**

Pin#	Pin Name	Pin Type		Pin Description
1, 6	VDDO	Power		Output supply pins.
2	VDD	Power		Core supply pin.
3	CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
4, 7	GND	Power		Power supply ground.
5	Q1	Output		Single clock output. LVCMOS / LVTTL interface levels.
8	Q0	Output		Single clock output. LVCMOS / LVTTL interface levels.

Note: *Pulldown* refer to internal input resistors, typical values in Pin Characteristics table.

**Pin Characteristics**

Symbol	Parameter	Test Conditions	Min.	Typical	Max.	Units
$C_N$	Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k $\Omega$
$R_{OUT}$	Output Impedance		5	7	12	$\Omega$

**Maximum Ratings**

(Above which useful life may be impaired. For user guidelines, not tested.)

Maximum Supply Voltage, VDD, VDDO .....	4.6V
Inputs, $V_I$ .....	-0.5V to VDD+0.5V
Output, $V_O$ .....	-0.5V to VDDO+0.5V
Storage Temperature .....	-65°C to 150°C
ESD Protection (HBM).....	2000V

Note:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics

is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**POWER SUPPLY DC CHARACTERISTICS,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Core Supply Voltage	3.3V Operation	3.135	3.3	3.465	V
		2.5V Operation	2.375	2.5	2.625	
VDDO	Output Power Supply Voltage	3.3V Supply	3.135	3.3	3.465	V
		2.5V Supply	2.375	2.5	2.625	
IDD	Power Supply Current				5	mA
IDDO	Output Supply Current	unloaded, 25MHz			6.5	mA

 Note: Parameters measured up to  $f_{\max}$  unless otherwise noted.

**LVCMOS / LVTTTL DC CHARACTERISTICS,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$** 

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{IH}$	Input High Voltage	VDD = 3.3V	2		VDD+0.3	V
		VDD = 2.5V	1.7		VDD+0.3	
$V_{IL}$	Input Low Voltage	VDD = 3.3V	-0.3		0.8	V
		VDD = 2.5V	-0.3		0.8	
$I_{IH}$	Input High Current	VDD = $V_{IN} = 3.465\text{V}$			100	$\mu\text{A}$
		VDD = $V_{IN} = 2.625\text{V}$			80	
$I_{IL}$	Input Low Current	VDD = 3.465V, $V_{IN} = 0\text{V}$	-5			$\mu\text{A}$
		VDD = 2.625V, $V_{IN} = 0\text{V}$	-5			
$V_{OH}$	Output High Voltage	VDDO = 3.3V $I_{OH} = -100\mu\text{A}$	2.9			V
		VDDO = 2.5V $I_{OH} = -100\mu\text{A}$	2.2			V
$V_{OL}$	Output Low Voltage	VDDO = 3.3V $I_{OL} = 100\mu\text{A}$			0.2	V
		VDDO = 2.5V $I_{OL} = 100\mu\text{A}$			0.2	V

**AC CHARACTERISTICS**, VDD = 3.3V ± 5%, T<sub>A</sub> = -40°C to 85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f <sub>MAX</sub>	Output Frequency	VDDO = 3.3V	4		250	MHz
		VDDO = 2.5V	4		250	
t <sub>pLH</sub>	Propagation Delay, Low-to-High; NOTE 1	VDDO = 3.3V, f ≤ 250MHz	1.4		2.2	ns
		VDDO = 2.5V, f ≤ 250MHz	1.5		3.0	
tsk(o)	Output Skew; NOTE 2			25	80	ps
tsk(pp)	Part-to-Part Skew; NOTE 3			250	800	ps
t <sub>R</sub>	Output Rise Time NOTE 4	VDDO = 3.3V	100	300	400	ps
		VDDO = 2.5V	100	350	500	
t <sub>F</sub>	Output Fall Time NOTE 4	VDDO = 3.3V	100	300	400	ps
		VDDO = 2.5V	100	350	500	
odc	Output Duty Cycle NOTE 5	f ≤ 133MHz	48		52	%
		133MHz < f ≤ 200MHz	47		53	%
		200MHz < f ≤ 250MHz	47		53	%
t <sub>jit</sub>	Additive RMS Jitter	156.25MHz (@12kHz to 20MHz)		0.1		ps
		125MHz (@12kHz to 20MHz)		0.07		ps

Parameters measured at f<sub>MAX</sub> unless otherwise noted.

NOTE 1: Measured from VDD / 2 of the input to VDDO / 2 of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at VDDO / 2.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at VDDO / 2.

NOTE 4: Defined from 20% to 80%

NOTE 5: Measured at VDDO / 2

**AC CHARACTERISTICS**,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ 

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$f_{MAX}$	Output Frequency	$V_{DDO} = 2.5V$	4		250	MHz
$t_{pLH}$	Propagation Delay, Low-to-High; NOTE 1	$V_{DDO} = 2.5V$ , $f \leq 250MHz$	1.5		2.8	ns
$tsk(o)$	Output Skew; NOTE 2			25	75	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3			250	800	ps
$t_R$	Output Rise Time NOTE 4	$V_{DDO} = 2.5V$	100	350	500	ps
$t_F$	Output Fall Time NOTE 4	$V_{DDO} = 2.5V$	100	350	500	ps
odc	Output Duty Cycle NOTE 5	$f \leq 133MHz$	48		52	%
		$133MHz < f \leq 200MHz$	47		53	%
		$200MHz < f \leq 250MHz$	42		58	%
$t_{jit}$	Additive RMS Jitter	156.25MHz (@12kHz to 20MHz)		0.1		ps
		125MHz (@12kHz to 20MHz)		0.07		ps

Parameters measured at  $f_{MAX}$  unless otherwise noted.

NOTE 1: Measured from  $V_{DD} / 2$  of the input to  $V_{DDO} / 2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO} / 2$ .

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO} / 2$ .

NOTE 4: Defined from 20% to 80%

NOTE 5: Measured at  $V_{DDO} / 2$

**AC Test Circuit Load**
