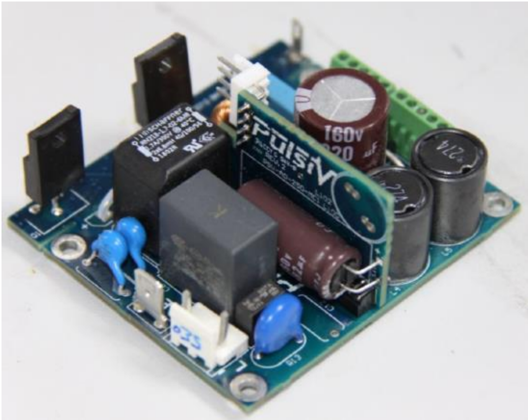
Last updated: 24/08/2022

EVALUATING THE PULSIV OSMIUM ARCHITECTURE FOR "ALWAYS EFFICIENT" POWER SUPPLIES USING THE PSV-AD-250-DS DEVELOPMENT SYSTEM

FEATURES

- Designed for high efficiency, low-cost, compact and lightweight AC/DC power supplies from 1-250W+
- Universal Input AC85 – 264V
- High efficiency (99% peak) across the full load range
- Inrush current completely eliminated
- Compatible with any suitable DC/DC converter
- Meets EMC Class B
- Optional Active Bridge to further improve efficiency
- Suitable for a variety of high-volume consumer applications including Laptops, TV's, Battery Chargers, LED Lighting and Industrial Power Supplies.



L = 70mm x W = 70mm x H = 30mm

OVERVIEW

The PSV-AD-xx controller family has been designed to make power supply designs more sustainable while reducing overall system complexity. This scalable solution delivers efficient AC/DC conversion using smaller, lower cost, and more robust system components. Pulsiv's unique switching architecture and intelligent control techniques have been combined to deliver consistent performance across the full load range and meet strict efficiency requirements at low power. The PSV-AD-250-DS development system can be configured for specific design requirements and interface with any compatible DC/DC converter to produce ultra-compact power supplies up to and beyond 250W.
Please note that the default components recommended by Pulsiv in this document have been fully optimised for cost and customers have the freedom to replace any parts where performance takes priority.

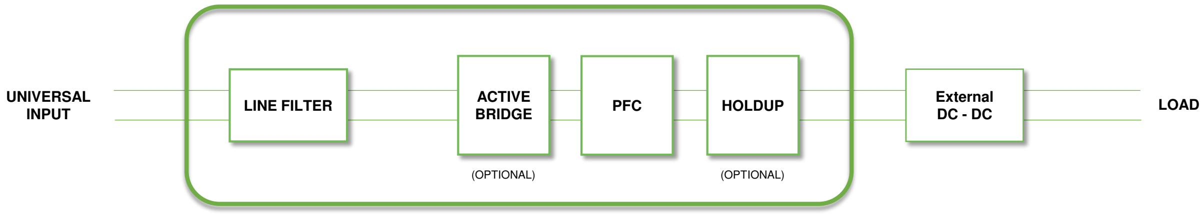


Figure 0a: PSV-AD-250-DS System Block Diagram

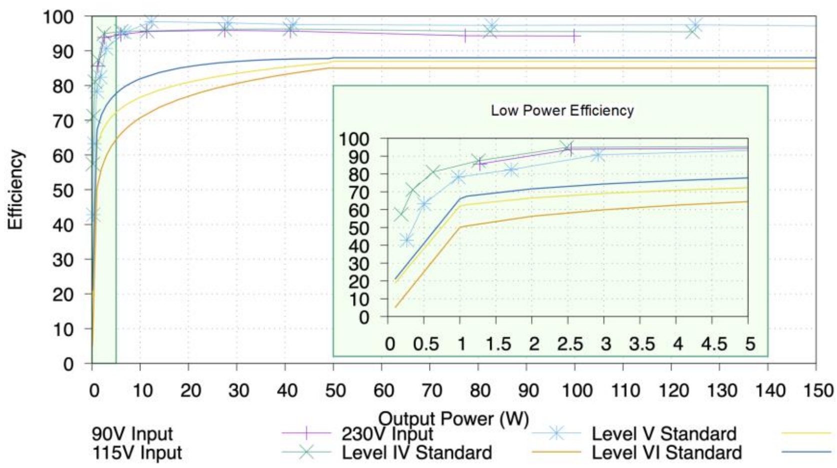


Figure 0b: PSV-AD-xx System Efficiency Compared to Energy Star Standards

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1 DESCRIPTION

Pulsiv has developed a unique way of converting electricity from AC to DC by applying patented switching techniques and integrating many system functions into one controller. Regulating capacitor charging with switch S_1 and discharging using a diode switch S_2 delivers a number of system benefits that will be described later in this document.

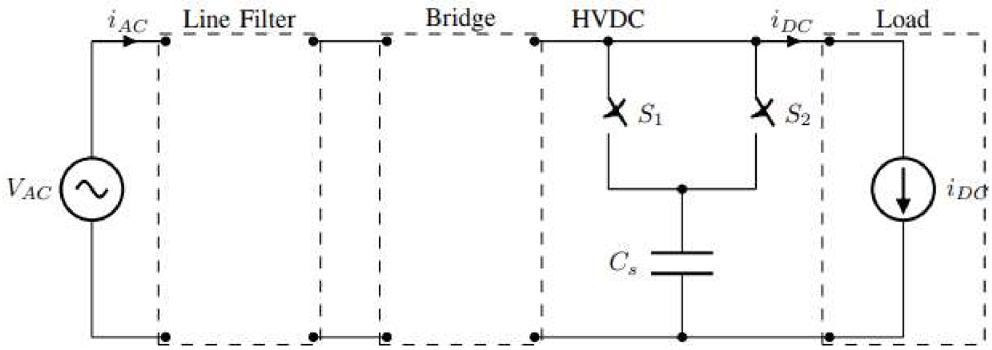

Figure 1a: Unique PFC Switching Architecture

The normalised High Voltage DC (HVDC) line and typical normalised capacitor voltage illustrate Pulsiv's unique approach. Energy is stored in a Capacitor when the AC line is at a high voltage and used to supply the load when the AC line voltage is low. Designs can achieve 0.95 power factor and a peak efficiency of 99%.

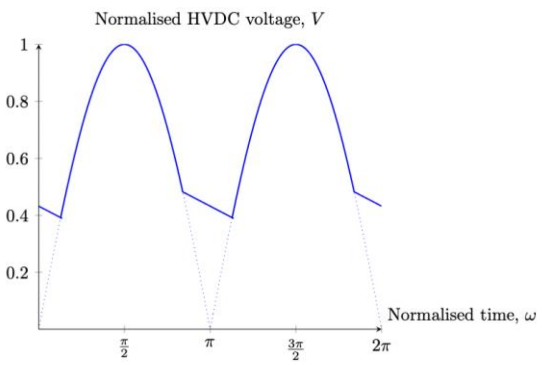

Figure 1c: Normalised HVDC Voltage (V)

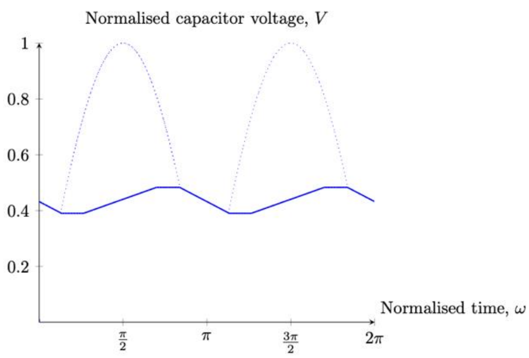

Figure 1d: Normalised C_s Voltage (V)

Standards like IEC61000-3-2, set limits on harmonic currents to improve power factor. Many technical solutions exist to help address this challenge, but none are like the PSV-AD-xx controller family. It maintains high power-factor and efficiency without using a switched PFC inductor; avoiding the need to boost the voltage into the power stage. This provides significant efficiency gains at low power and produces an inherent high efficiency across the power range.

A rich set of signals manage PFC switching, active bridge control, configurable HVDC voltage, X-capacitor discharge, configurable hold-up time, auxiliary power supply management and provides an early-warning if the grid supply fails. The device can be completely disabled and placed into a low-power mode.

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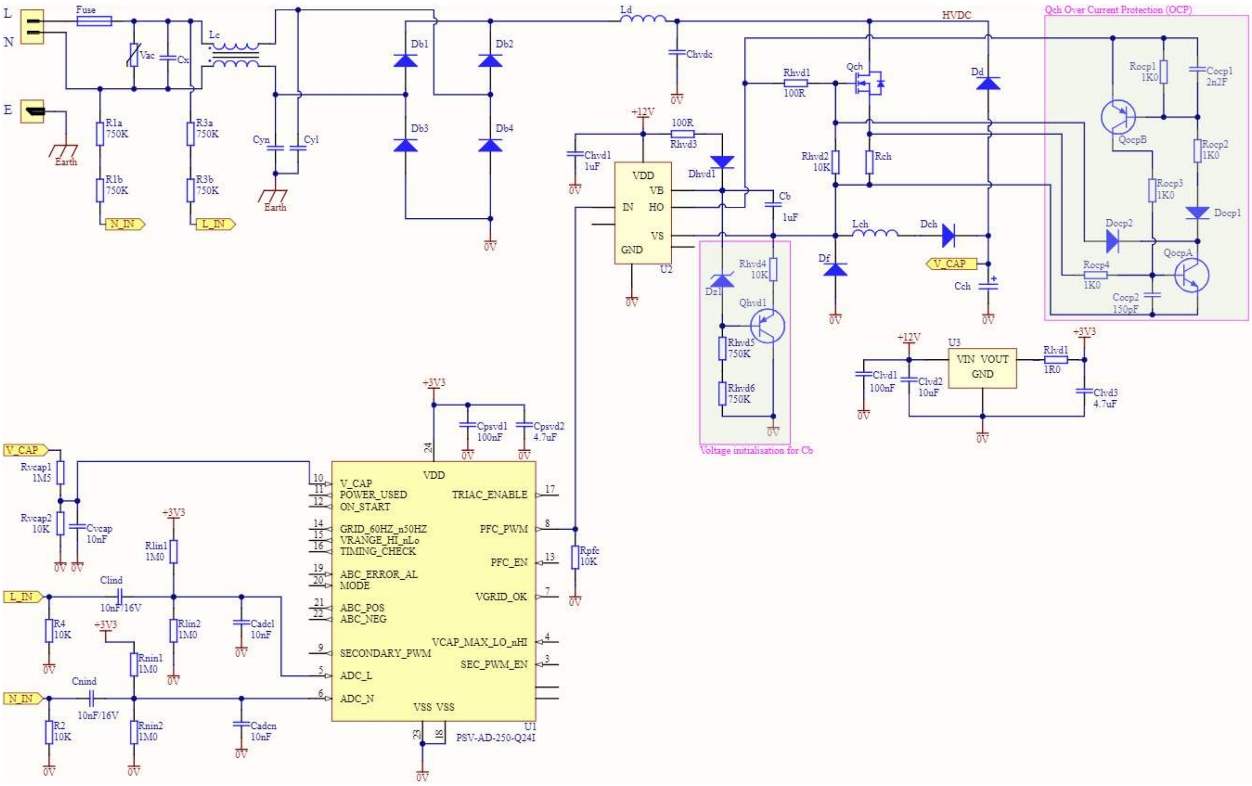

Figure 1b: PSV-AD-xx Controller Basic Functional Schematic

The PSV-AD-xx controller regulates the charging of capacitor Cch by controlling the switching of Qch in a power supply system. Open-loop charging current is limited by Rch with inductor Lch selected to ensure sufficient charge is passed into Cch for the desired load requirements. Discharging Cch is achieved through Dd and controlled by the follow-on DC/DC converter or a load connected to HVDC. Diode Dch prevents Cch discharging through the body diode of Qch. Df is a freewheeling diode associated with Lch.

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1.1 PSV-AD-250-MB Motherboard Pin Connections

The PSV-AD-250-MC1 controller card and PSV-AD-250-MB motherboard provide a flexible evaluation platform to cover the full 1-250W power range. This version is fitted with components tailored for 250W resistive loads (150W constant power loads), but can be modified to test other configurations.

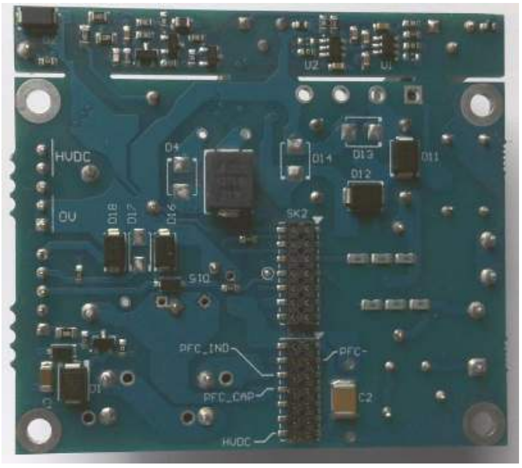

Figure 1.1a - PSV-AD-250-MB Motherboard Main Connections

Please note that the 13.5V supply shares the same ground as HVDC and Pulsiv recommends using an isolated 13.5V source (18V maximum, 12V minimum).

#	Connector	Signal	Description
1	PL4	L	Mains Live voltage input
2	PL4	N	Mains Neutral input

#	Connector	Signal	Description
1	PL3	0V	OSMIUM 0V output to DC/DC stage
2	PL3	0V	OSMIUM 0V output to DC/DC stage
4	PL3	+DC	High-voltage PFC output to DC/DC stage
5	PL3	+DC	High-voltage PFC output to DC/DC stage

#	Connector	Signal	Description
1	PL5	+13.5V	+12V to +18V input required 13.5V recommended
2	PL5	0V	0v input for +13.5V supply
3	PL5	PFC_EN	Digital input to disable (low) the PFC circuit
4	PL5	BULK_EN	External hold up thyristor gate signal
5	PL5	VGRID_OK	Digital output to signal grid condition

#	Connector	Signal	Description
1	J4	E	Mains Earth input
1	J1	SECONDARY_PWM	Digital output for auxiliary power supply

1.2 PSV-AD-250-MC1 Controller Card Pin Connections

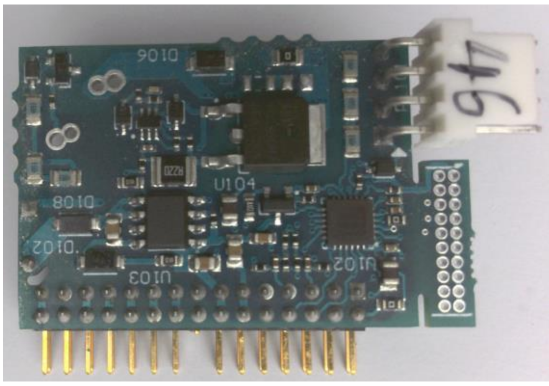
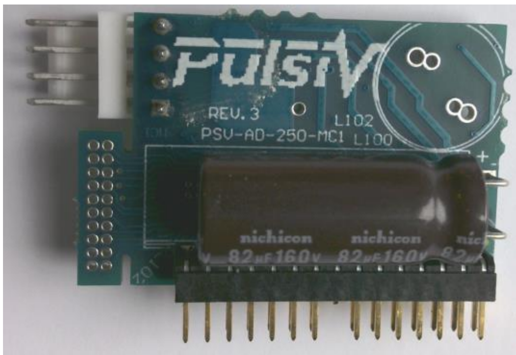

Figure 1.2a - PSV-AD-250-MC1 Controller Card

#	Connector	Signal	Description
1	PL102	VGRID_OK	Digital output to signal Grid condition
2	PL102	0V	0V for the system
3	PL102	SECONDARY_PWM	Digital output for auxiliary power supply
4	PL102	ABC_POS	Digital output for active bridge circuit
5	PL102	Lin	Scaled analogue input from mains Live voltage
6	PL102	ABC_NEG	Digital output for active bridge circuit
7	PL102	Nin	Scaled analogue input from mains Neutral
8	PL102	AB_FAULT_AL	Active bridge fault detect
9	PL102	PFC_EN	Enable PFC circuit to function (low to disable)
10	PL102	TRIAC_ENABLE	Used for additional holdup capacitor if required
11	PL102	0V	0V for the digital system
12	PL102	0V	0V for the digital system
13	PL102	13.5V	13.5V input required
14	PL102	13.5V	13.5V input required
15	PL102	-	Not Connected
16	PL102	-	Not Connected
17	PL102	0V	0V for power system
18	PL102	0V	0V for power system
19	PL102	PFC-	PFC circuit connection
20	PL102	PFC-	PFC circuit connection
21	PL102	PFC_IND	PFC circuit connection
22	PL102	PFC_IND	PFC circuit connection
23	PL102	PFC_CAP	PFC circuit connection
24	PL102	PFC_CAP	PFC circuit connection
25	PL102	-	Not Connected
26	PL102	-	Not Connected
27	PL102	-	Not Connected
28	PL102	-	Not Connected
29	PL102	HVDC	Output voltage
30	PL102	HVDC	Output voltage

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1.3 Schematic Diagram

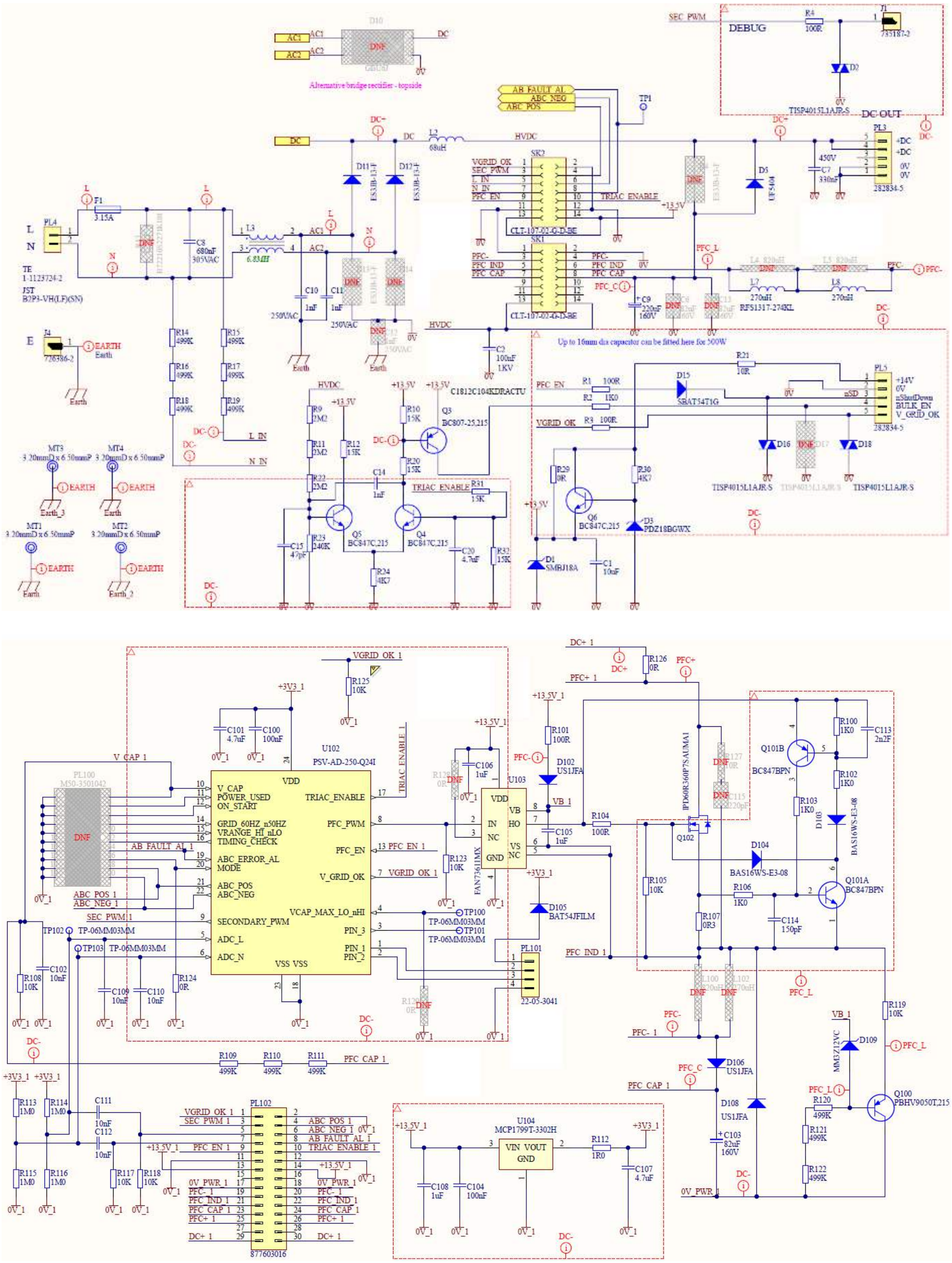

Figure 1.3a: PSV-AD-250-DS Full Circuit Diagram

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1.4 System Components

The PSV-AD-250 development system includes a number of components that aren't required in a commercial design. Please see PSV-CCAD-xx circuit configurations or PSV-RDAD-XX reference designs on pulsiv.co.uk for optimised circuits which are intended for system integration.

Description	Designator	Quantity	MANUF#1	MANUF PN#1
CAP 1206 X7R 10UF 25V 10% -55/+125	C1	1	TAIYO YUDEN	TMK316B7106KL-TD
CAP 1812 X7R 100NF 1KV 10% -55/+125	C2	1	KEMET	C1812X104KDRACTU
CAP 0603 X7R 100NF 50V 10% -55/+125	C3, C18, C104	3	TDK CORPORATION	CGA3E2X7R1H104K080AA
CAP 0603 X7R 1N0F 50V 10% -55/+125	C4, C5, C14, C16	4	TDK	CGA3E2X7R1H102K080AA
CAP PTH PP 0.33uF 450V 10% -55/+125	C7	1	EPCOS	B32672P4334K000
CAP PTH PP 0.68uF 305VAC 10% -40/+110	C8	1	EPCOS	B32922C3684K189
CAP ELEC RAD 220uF 160V 20% -40/+105	C9	1	NICHICON	UCS2C221MHD1TN
CAP PTH CER XY 1nF 250VAC 20% -20/+125	C10, C11	2	KEMET	C901U102MYVDBA7317
CAP 0603 C0G 47pF 50V 10% -55/+125	C15	1	YAGEO	CC0603JRNPO9BN470
CAP 0805 X7R 4U7F 25V 10% -55/+125	C20, C101, C107	3	YAGEO	CC0805KKX7R8BB475
CAP 0402 X7R 100NF 16V 10% -55/+125	C100	1	MURATA	GCM155R71C104KA55D
CAP 0402 X7R 10NF 16V 10% -55/+125	C102, C109, C110, C111, C112	5	TAIYO YUDEN	EMF105B7103KVHF
CAP ELEC RAD 82uF 160V 20% -40/+105	C103	1	UNI CHEMI-CON	EKXJ161ELL820MJ25S
CAP 0805 X7R 1U0F 25V 10% -55/+125	C105, C106, C108	3	KEMET	C0805C105K3RECAUTO
CAP 0402 X7R 2.2NF 50V 10% -55/+125	C113	1	WALSIN	0402B222K500CT
CAP 0402 C0G 150PF 50V 5% -55/+125	C114	1	KEMET	C0402C151J5GACTU
DIO TVS 18V 600W UNIDIRECTIONAL DO214AA	D1	1	VISHAY	SMBJ18D-M3/H
DIO THYRISTOR SURGE PROTECT 8V 120A SMA	D2, D16, D18	3	BOURNS	TISP4015L1AJR-S
DIO ZENER 18V 625mW SOD-123	D3	1	NEXPERIA	PDZ18BGWX
DIO RECTIFIER 1000V 3A DO-201AV	D5	1	DIOTEC SEMI	UF5404
DIO RECTIFIER 600V 3A SMB	D11, D12	2	DIODES	ES3JB-13-F
DIO SCHOTTKY 30V 200MA SOD123	D15	1	ONSEMI	SBAT54T1G
DIO RECTIFIER 600V 1A SOD-123FL	D102, D106, D108	3	ON SEMI	US1JFA
DIO GEN PURP 100V 0.2A SOD323-2 +150	D103, D104	2	VISHAY	BAS16WS-E3-08
DIO SINGLE 40V 0.3A SOD323 +150	D105	1	ST MICRO	BAT54JFILM
DIO ZENER 12V 200mW SOD323FL	D109	1	ONSEMI	MM3Z12VC
FUS PTH MINI 3.15A 250V	F1	1	BEL FUSE	0697A3150-01
CON 1W SPADE TERMINAL TAB 2.8MM ST	J1	1	TE	735187-2
CON 1W SPADE TERMINAL TAB 6.3MM ST	J4	1	TE	726386-2
IND FER 68uH 2A 20% -40/+105	L2	1	WE	7447033
IND CHOKE 6.8mH@ 10kHz 1A 300V -40/+100	L3	1	SCHAFFNER	RN218-1-7-02-6M8
IND SHD PWR 270uH2.05A 10% -40/+85	L7, L8	2	COILCREAFT	RFS1317-274KL
CON 5W TE 2.54MM W-T-B TERM BLOCK ST	PL3, PL5	2	TE	282834-5
CON 2W ST PWR POL 7.92MM PTH	PL4	1	TE	1-1123724-2
CON 4W MOLEX 2.54mmP RA TIN FRICTION LOCK	PL101	1	MOLEX	22-05-3041
CON 30W MILLI-GRID HDR 2.0mmP RA PTH	PL102	1	MOLEX	877603016
TRN MOSFET N-CH 650V 18A TO220V -40/+150	Q1, Q2	2	INFINEON	IPAN60R180P7SXKSA1
TRN PNP 45V 500MA SOT23 -55/+150	Q3	1	NEXPERIA	BC807-25,215
TRN NPN 45V 100MA SOT23 -65/+150	Q4, Q5, Q6	3	NEXPERIA	BC847C,215
TRN PNP 500V 150MA SOT23 -55/+150	Q100	1	NEXPERIA	PBHV9050T,215
TRN NPN/PNP GEN PURP X2 45V 0.1A SOT23-6	Q101	1	NEXPERIA	BC847BPN,115
TRN MOSFET N-CH 600V 9A TO252-3 -40/+150	Q102	1	INFINEON	IPD60R360P7SAUMA1
RES 0603 TF 100R 1% 0.1W -55/+150	R1, R3, R4, R5, R6, R101, R104	7	STACKPOLE ELECTR	RMCF0603FT100R
RES 0603 TF 1K0 1% 0.1W -55/+150	R2	1	VISHAY	CRCW06031K00FKEA
RES 0603 TF 15K 1% 0.1W -55/+155	R7, R10, R12, R20, R26, R31, R32	7	YAGEO	RC0603FR-0715KL
RES 0603 TF 0.025R 1% 0.33W -55/+155	R8, R27	2	PANASONIC	ERJ-3BWFR025V
RES 0805 TF 2M2 1% 0.125W -55/+155	R9, R11, R22	3	YAGEO	RC0805FR-072M2L
RES 0805 TF 499K 1% 0.25W -55/+155	R14, R15, R16, R17, R18, R19, R109, R110, R111, R120, R121, R122	12	KOA SPEER	RK73H2ATTD4993F
RES 0805 TF 10R 1% 0.125W -55/+155	R21	1	YAGEO	RC0805FR-0710RL
RES 0603 TF 240K 1% 0.1W -55/+155	R23	1	YAGEO	RC0603FR-07240KL
RES 0603 TF 4K7 1% 0.1W -55/+155	R24, R30	2	YAGEO	RT0603FRE074K7L
RES 0603 TF 0R 0.1W -55/+155	R25, R28, R29, R124	4	YAGEO	RC0603JR-070RL
VAR TVS 275VAC 400A 3225	R33	1	EPCOS	B72650M0271K072
RES 0402 TF 1K0 1% 0.062W -55/+155	R100, R102, R103, R106	4	ROHM	SFR01MZPF1001
RES 0402 TF 10K 1% 0.062W -55/+155	R105, R108, R117, R118, R119, R123, R125	7	VISHAY	CRCW040210K0FKEDC
RES 1210 TF 0.3R 1% 500mW -55/+155	R107	1	YAGEO	RL1210FR-070R22L
RES 0603 TF 1R0 1% 0.25W -55/+155	R112	1	TE	RC0603FR-071RL
RES 0402 TF 1M0 1% 0.062W -55/+155	R113, R114, R115, R116	4	VISHAY	CRCW04021M00FKEDC
RES 0805 TF 0R 0.125W -55/+155	R126	1	YAGEO	RC0805JR-070RL
CON 14W BE LOW PROFILE SK 2.00MM SMT	SK1, SK2	2	SAMTEC	CLT-107-02-G-D-BE
TRN MOSFET PWR DRIVE 2.6A NON-INV -40/+125	U1, U2	2	INFINEON	1ED44173N01BXTSA1
IC PSV-AD-250-Q24I	U102	1	PULSIV	PSV-AD-250-Q24I
IC FAN73611 PWR MAN GATE DRIVER 20V SOP-8	U103	1	ON SEMI	FAN73611MX
IC MCP1799T-3302H LDO 3.3V 80mA -40/+150	U104	1	MICROCHIP	MCP1799T-3302H

Table 1.4a - PSV-AD-250-DS Full Bill of Materials

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2 DESIGN GUIDE

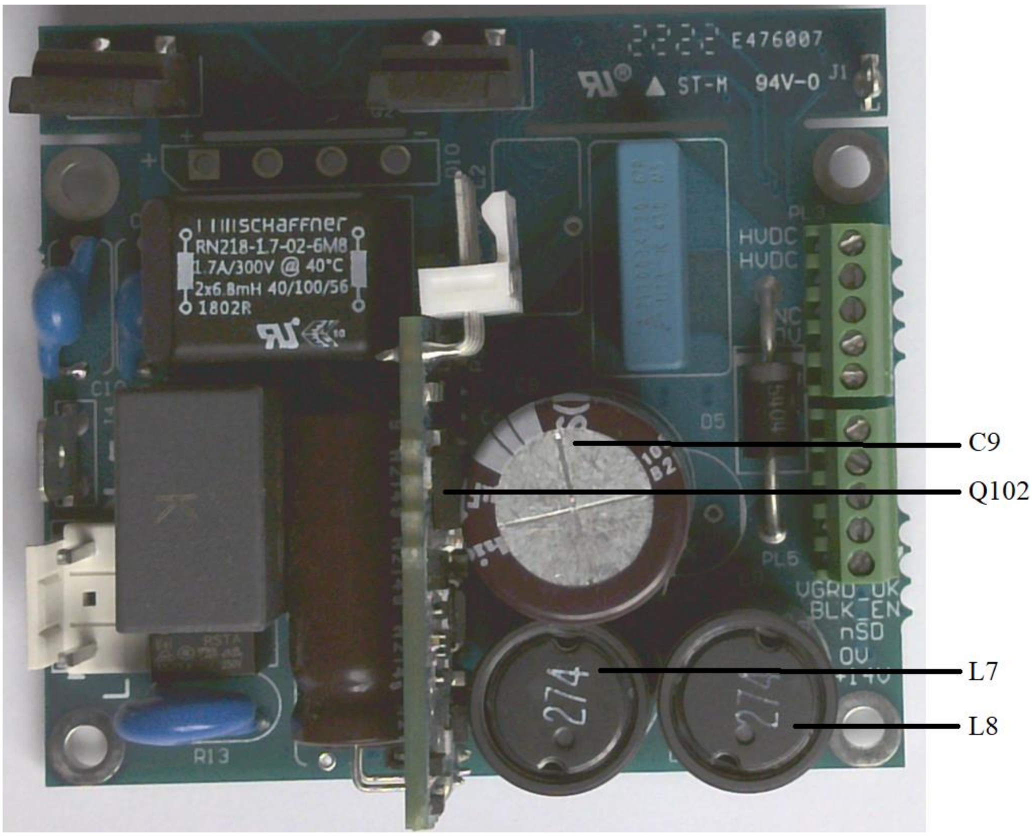
Depending upon power requirements, the PSV-AD-250-DS Development System is configured by selecting the following components in Figure 1.3a:

- C9
  - The PSV-AD-250-DS Development System includes placeholders for C103, C6 and C13 so that different package sizes and configurations can be fitted
- L7 (L8 also fitted to increase inductance in this system configuration)
  - The PSV-AD-250-DS Development System includes placeholders for L100, L102, or L4 and L5 so that different package sizes and configurations can be fitted
- Q102

Note any capacitance from a follow-on DC/DC converter will interact with the PSV-AD-xx. Typically, the capacitance of the follow-on DC/DC should be kept to a minimum (for 120W, it should be less than 0.5uF).

The following DNF components on the PSV-AD-250-DS Development System can be added under certain conditions:

- D10, D13 and D14 are shown as DNF when an active bridge is fitted. These diodes interfere with the over-current protection of the active bridge.
- D13 and D14 replace Q1 and Q2 if an active bridge is not fitted.
- D10 can replace D11, D12, D13 and D14 if an active bridge not fitted.
- D4 can be used in place of D5 if a different package is required.



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2.1 Capacitor Selection (C9)

The storage capacitor selection is determined by output power requirements. Care should be taken so that the capacitor meets the ripple current required by the load during the discharge phase. The capacitor selection assumes a constant power discharge, and sufficient capacitance must be provided to ensure a minimum holdup voltage for the DC/DC converter stage. The storage capacitor is charged based on the value of the input voltage (95V in 115VAC systems and 155V in 220VAC systems). With constant power loads, the potential across a capacitor at a given elapsed time, t, is given by the initial holdup voltage, V_h, the power drawn, P, and capacitance, C:

$$V_c(t) = \sqrt{V_h^2 - 2\frac{P}{C}t}$$

The discharge time of the capacitor determines the minimum voltage reached and is approximated by solving for time in this equation:

$$\sqrt{2}V_{RMS}(2\pi ft) - V_h = \sqrt{V_h^2 - 2\frac{P}{C}t}$$

This gives a simple upper limit of:

$$t \leq \frac{V_h}{\pi f\sqrt{2}V_{RMS}}$$

For common grid voltages and frequencies, this equates to a discharge time of approximately 3mS and the minimum required capacitance is given by:

$$C = \frac{P}{(V_h - V_{min})(V_h + V_{min})} 6 \cdot 10^{-3}$$

For universal input designs, 160V rated capacitors can be used. The relationship between power and capacitance is linear; so sufficient capacitance should be selected. Typical values are provided in Table 2.1a. Ripple current rating for the capacitor will depend on the DC/DC converter stage. The typical capacitor current waveshape is shown by Figure 2.1a; with the capacitor charge being equal (in steady state conditions) during the charge and discharge cycles. The RMS current rating of the capacitor needs to be reviewed based on the current drawn by the DC/DC stage. A simple guide is to use the discharge voltage difference and discharge time to determine the average discharge current.

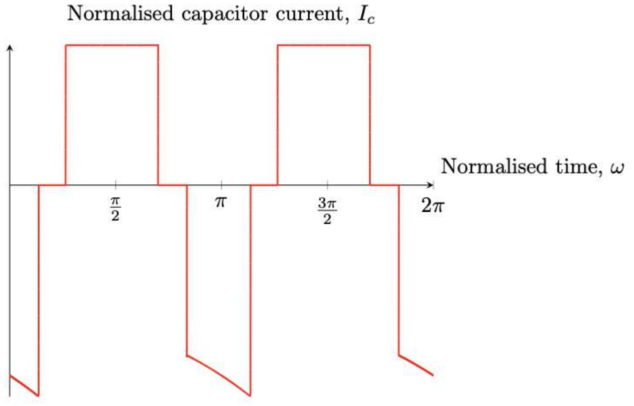

Figure 2.1a – Typical Current Waveshape For C9

The RMS capacitor current can be determined by analysing the capacitor voltage waveform, which shows a constant current charge and constant power discharge. Assuming a typical charge time of 5mS and a discharge time of 3mS; the RMS capacitor current can be estimated as shown in the table below. The actual RMS current needs to be determined once the charge and discharge currents have been estimated as these will be a function of the DC/DC converter used. Typically, the discharge current will be the dominant term in the capacitor RMS current calculation, and this is determined by the DC/DC converter used.

Capacitance (uF)	Max Power (W)	Min. Voltage (V)	RMS current (A)
90	70	50	0.7
75	70	40	0.8
127	100	50	1.0
107	100	40	1.1
190	150	50	1.5
160	150	40	1.6
230	180	50	1.7
192	180	40	1.9

Table 2.1a – Recommended Capacitor Values and RMS current for C9 (Capacitor Holdup Voltage of 95V for universal input)

Pin 4 on the controller can be used to set the maximum voltage stored on the capacitor. If pin 4 is left open, the maximum capacitor voltage is 150V (enabling the use of a 160V rated capacitor). With the pin pulled to ground, the maximum capacitor voltage is 180V (enabling the use of a 200V rated capacitor). Using a higher rated capacitor provides a higher power factor with 230VAC mains.

The Mean Time Between Failure for C9 in the PSV-AD-250-DS development system is given by:

Parameter	Min	Unit	Notes and conditions
Mean Time Between Failure	19000	Khrs	MIL-HDBK-217F, Notice 2, Style: CE CU CUR, 55°C, Non-Established Reliability, G_B

The measured capacitor temperature (180W electronic load) is 45°C with convection cooling at 30°C ambient. The data was calculated using 55°C, assuming heat from the DC/DC converter increases the capacitor temperature by a further 10°C. This represents a worst-case scenario. The actual MTBF will depend on components used and temperatures of the components.

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2.2 Inductor Selection (L7/L8)

To ensure that the capacitor charging current is properly regulated and to help EMC compliance, the charging circuit includes an inductor. The peak current is limited in hardware, and the switching frequency used to regulate the current dithers around 45kHz using an open-loop control system. The duty cycle is controlled by the PSV-AD-xx to ensure a current-profile that maximises power factor.

As the power requirement changes, L7 can be selected to ensure sufficient charge is stored in C9 during the minimum line voltage condition. With a suitable C9 selected (see section 2.1), the charge required is determined by q = Cch (85 – Vmin), where Vmin is the minimum voltage the DC/DC converter will operate from. The typical charging time is 3mS, and using the charge, and assuming the current in the inductor is in critical conduction mode, the peak current is given by

$$i_{pk} = \frac{2}{3 \times 10^{-3}} C_{ch}(85 - V_{in\_min})$$

The value of Rch is selected using this peak current as a limit. The potential developed across R107 will switch-on the Over Current Protection circuit to limit the peak current. For example, with a minimum DC/DC voltage of 65V, and Cch=220uF, ipk is calculated as 2.9A.
The value of Lch is given using the expression below

$$L_{ch} = \frac{(V_{AC\_pk} - V_{in\_min})}{i_{pk} \cdot f} D$$

Where D=0.7 and f=45kHz are set by the PSV-AD-xx and $V_{AC\_pk} = 115\sqrt{2}$ is a typical requirement. With a peak current of 2.9A, and Vin_min = 65 for example, this equates to Lch being 500uH. The expression for Lch assumes charging at the peak of the input line, C9 is at the minimum voltage and current is at critical conduction. It should be noted that the inductor can operate in continuous conduction mode as well; as long as the peak current is below ipk. Various combinations of ipk and L7 can be used.

At the maximum intended power, ipk and L7 can be optimised to ensure that C9 is charged to its maximum value. Suitable starting points for this are provided in the table below.

Max Power (W)	Min Voltage (V)	Min Cch (uF)	ipk (A)	Rch (Ohm)	Typical Lch (uH)
30	65	60	0.80	0.88	1898
60	65	120	1.60	0.44	949
110	65	220	2.93	0.24	518
150	65	300	4.00	0.18	380
180	65	360	4.80	0.15	316
200	65	400	5.33	0.13	285
220	65	440	5.87	0.12	259
250	65	500	6.67	0.11	228

A suitable inductor can be designed to maximise efficiency or minimise cost. The current-limiting hardware can be changed by modifying R107 and the associated circuit in Figure 1.2b.

2.3 MOSFET Selection (Q102)

Only conduction loss and switching loss are considered in selecting suitable MOSFETs. The nomograms in Appendix A.1 can be used to determine suitable MOSFETs using RDS(on) and rise/fall switching times. Actual losses depend on charging time, HVDC voltage and capacitor voltage; however suitable MOSFETs include:

Device	RDS(on)	t_r (nS)	t_f (nS)
IPN60R1K0CEATMA1	1.10	8	13
IPN60R600P7SATMA1	0.60	6	19
IPN60R360P7SATMA1 (fitted)	0.36	7	10

Table 2.3a – Recommended MOSFET for Q102

2.4 Hold-up Circuit (optional) and Capacitor Selection

For applications that require hold up, an optional circuit can be used. The connection marked BULK_EN should be connected as shown in Figure 2.4a.

The circuit ensures that when the HVDC goes below a threshold (determined by the 3 x 2M2 resistor network) a Thyristor will be enabled so that the response to a loss in HVDC potential is controlled by hardware rather than software. This setup can cause an inrush current during initialisation when the HVDC potential is low. To control the Thyristor during initialisation, the PSV-AD-xx includes a means of inhibiting this inrush current.

A suitable capacitance value can be determined by calculating the energy required during the holdup phase, the peak grid voltage, the desired holdup time and load power. The minimum operating voltage of the DC/DC converter is also required to calculate the capacitance. For example, if the required power is 120W and the required holdup time is 12mS, this equates to an energy requirement of 120W x 12mS = 1.44J. Assuming the DC/DC converter can operate from a minimum of 35V, and assuming the grid is at 115V RMS, which equates to $115\sqrt{2}$ V maximum; this gives the required capacitance as
C = 2 x Energy Required / ($Vmax^2 – Vmin^2$) = 2 x 1.44 / (115 x 115 x 2 – 35 x 35) = 115 uF

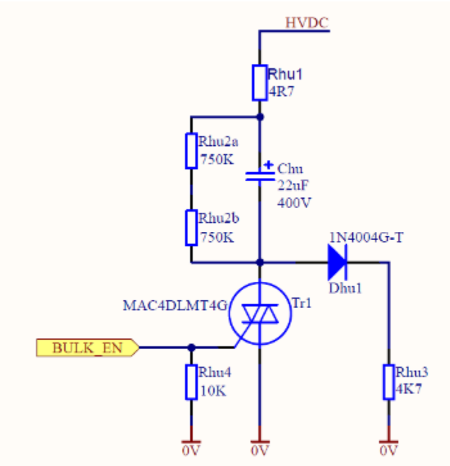

Figure 2.4a - External Components for the PSV-AD-250-DS to Provide System Holdup

2.5 Active Bridge (optional)

The active bridge signals provided by the PSV-AD-xx controller can be used to drive a high-side low-side MOSFET configuration that increases overall efficiency by up to 1.4% (90VAC line input). This is increasingly important at higher power levels and a half active bridge provides efficiency improvement using only two MOSFET’s as shown below (ideal for 150-200W designs). A full active bridge can be implemented with very few additional components (please contact Pulsiv for details).

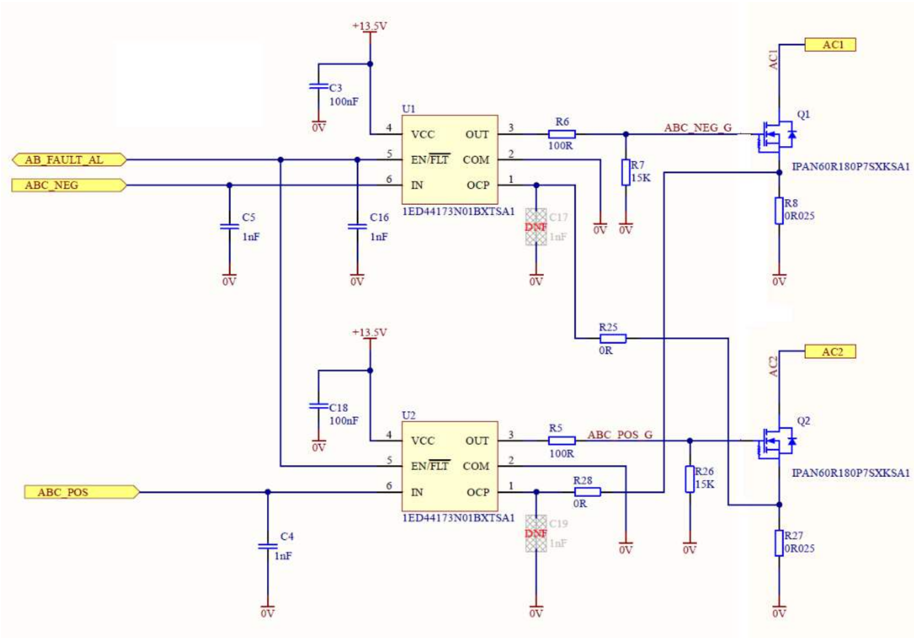

Figure 2.5a - PSV-AD-250-DS Active Bridge Circuit

If Q1 and Q2 are replaced with alternative devices, capacitors C17 and C19 can be fitted if there are noise issues.

The operation of the PSV-AD-xx provides a natural deadtime of approximately 3mS, enabling robust and safe switching to prevent shoot through.

2.6 Power Used

The POWER_USED pin displays real-time power consumption by toggling at a fixed rate.

Our method does not require expensive current measurement techniques, but performs a calculation (Vcap charged)^2 - (Vcap discharged)^2 during each grid cycle, which is directly proportional to the power.

Using the recommended values for C9:
Low power = 0-25% of the rated power = 1.5Hz POWER_USED output frequency
Medium power 26-75% of the rated power = 4Hz POWER_USED output frequency
High power = 76-100% of the rated power= 12Hz POWER_USED output frequenc.

Choosing a different value of C9 to those recommended will require POWER_USED to be characterised.

2.7 Using SECONDARY_PWM

The SECONDARY_PWM output can be used to drive an auxiliary supply for systems that need power when the DC-DC converter is switched off. Please contact Pulsiv for details as the supporting components will depend on specific power requirements.

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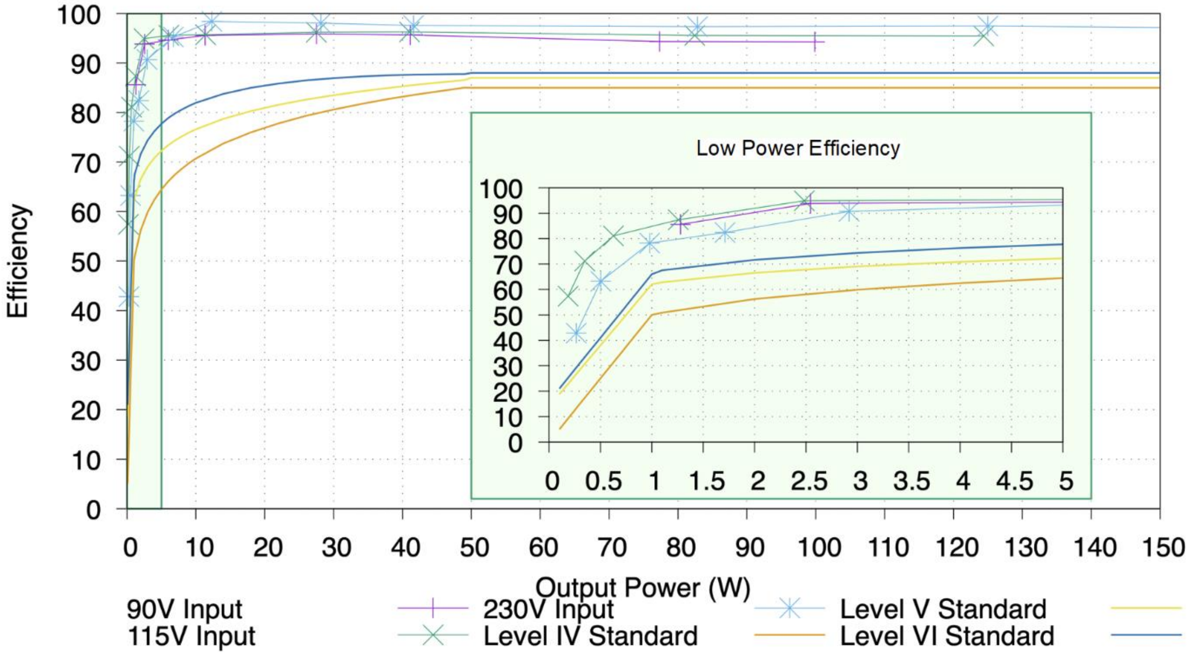
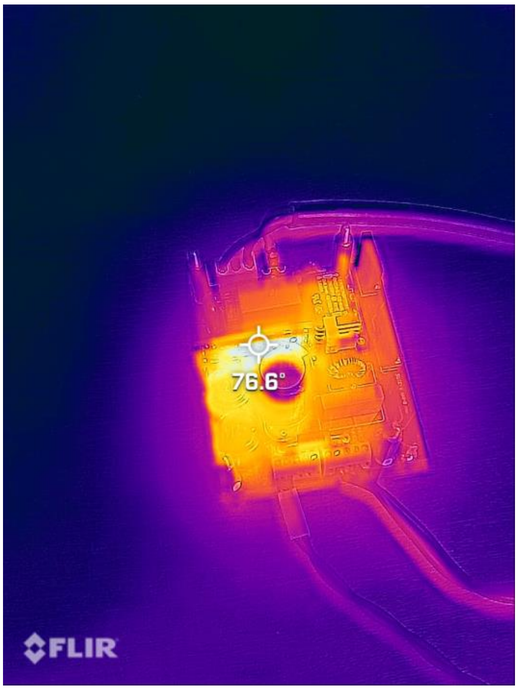
3 Performance Data

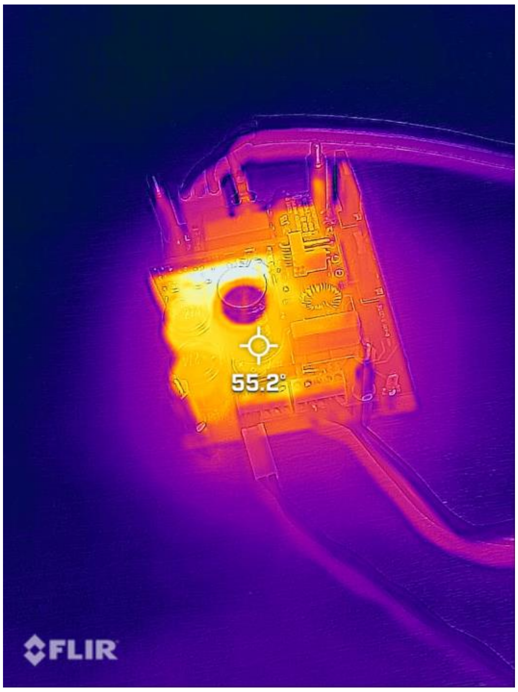
3.1 Efficiency



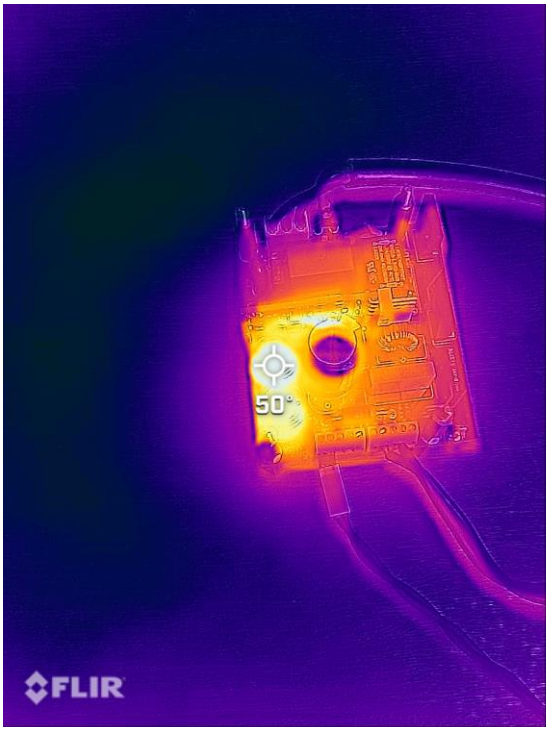
3.2 Thermal Performance

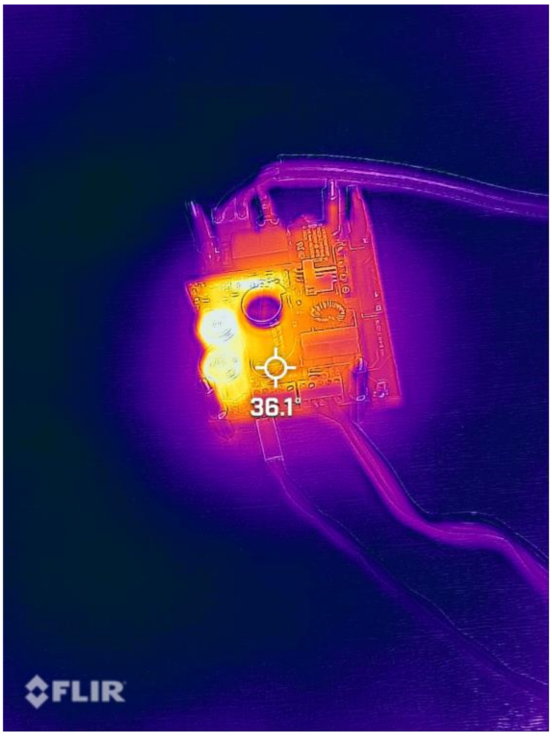
To showcase thermal performance, an image of the PSV-AD250-DS (with active bridge) is shown below for a Flyback load running at 113W with a 115V supply. The hot-spot at 76 Celsius is Q102; which has no heatsink or thermal vias. The calculated loss of Q102 is approximately 1W which has an expected thermal rise of 60 degrees. The capacitor temperature is 55 Celsius.





Running at 113W from a 230V supply, the capacitor temperatures are reduced from 55 Celsius to 36 Celsius and the MOSFET temperature is reduced from 76 Celsius to 50 Celsius. The losses move from the MOSFET to the bobbin chokes. By using lower Rdson MOSFETs or a customised choke, these losses can be reduced and efficiencies increased.





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3.3 Conducted Emissions

CE_Mule_Rev2_PFC_1__based on EN 5011_13-5V_170W_electronic_load

Passed

EMI Test Report

EMI Final Results (1/2)

Rg	Frequency [MHz]	QPK Level [dBµV]	QPK Limit [dBµV]	QPK Margin [dB]	QPK Level [dBµV]	AVG Level [dBµV]	AVG Limit [dBµV]	AVG Margin [dB]	AVG Level [dBµV]	Correction [dB]	Line	Meas. BW [kHz]	Meas. Time [ms]	Time of Meas.
1	0.150	58.08	66.00	7.92						11.00	L1	9.000	2,000.000	11:06:19
1	0.173	59.47	64.84	5.37						11.00	L1	9.000	2,000.000	11:06:23

EMI Final Results (2/2)

Rg	Frequency [MHz]	Source
1	0.150	Critical Points
1	0.173	Critical Points

25/02/2022 / 11:07

1 / 1

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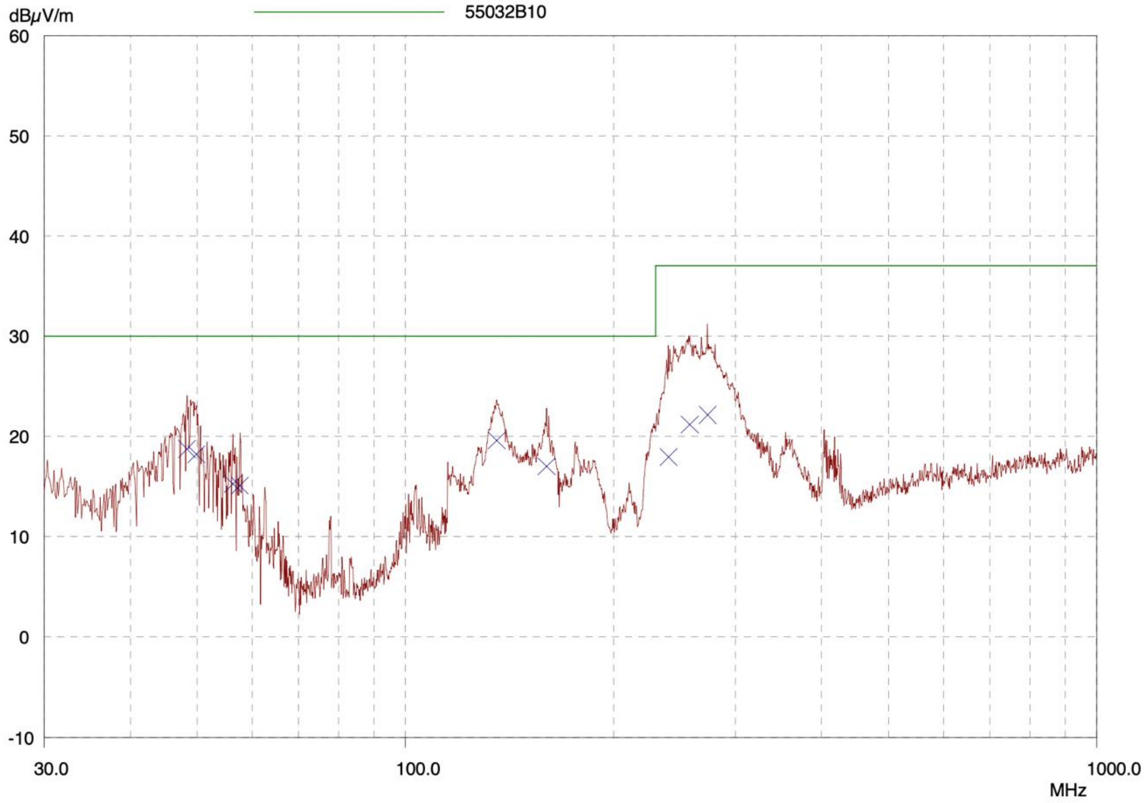
3.4 Radiated Emissions



Scan Settings (1 Range)

Frequencies			Receiver Settings				
Start	Stop	Step	IF BW	Detector	M-Time	Atten	OpRge
30MHz	1000MHz	110kHz	120kHz	PK	20msec	Auto	60dB

Transducer	No.	Start	Stop	Name
5	20	10MHz	1000MHz	CBLB046
	21	10MHz	1000MHz	B108AMP
	22	30MHz	1000MHz	B158_ANT

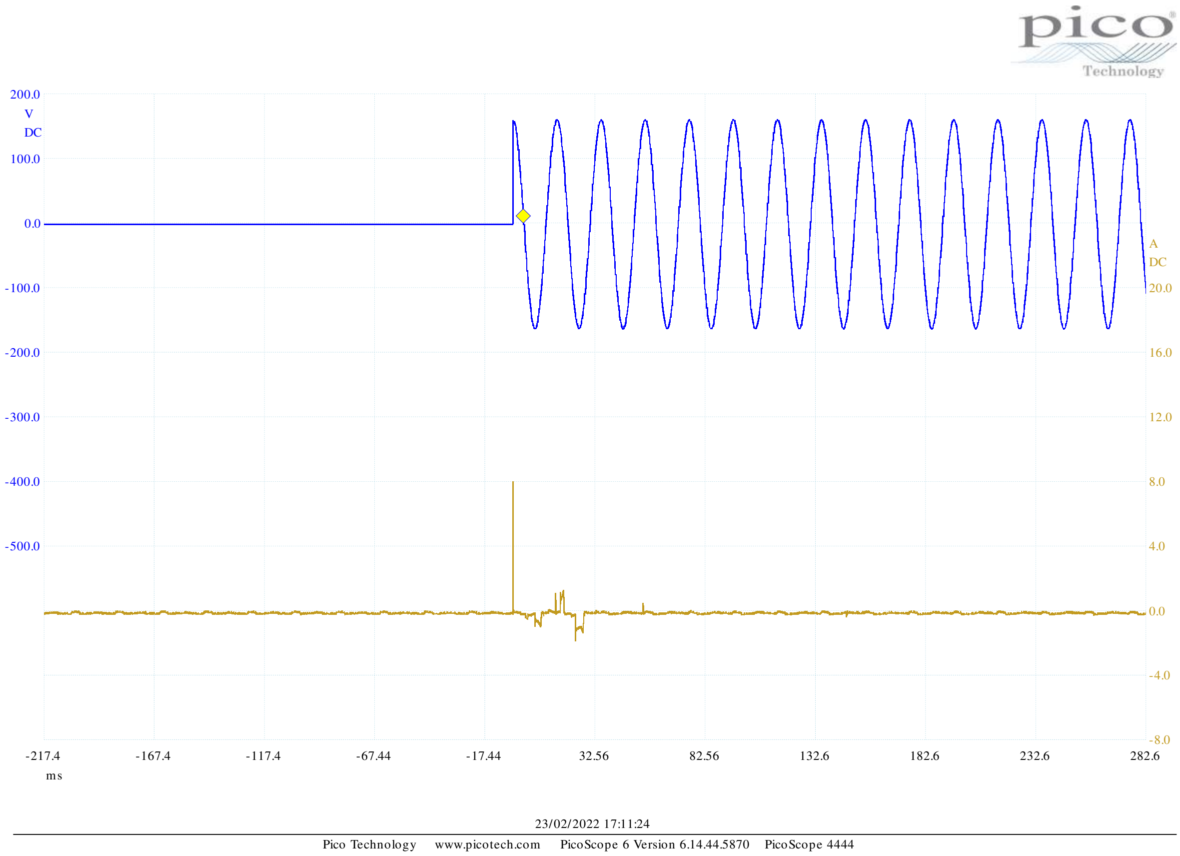
Final Measurement:

Detector:	X QP
Meas Time:	2sec
Subranges:	50
Acc Margin:	25 dB

Final Measurement Results

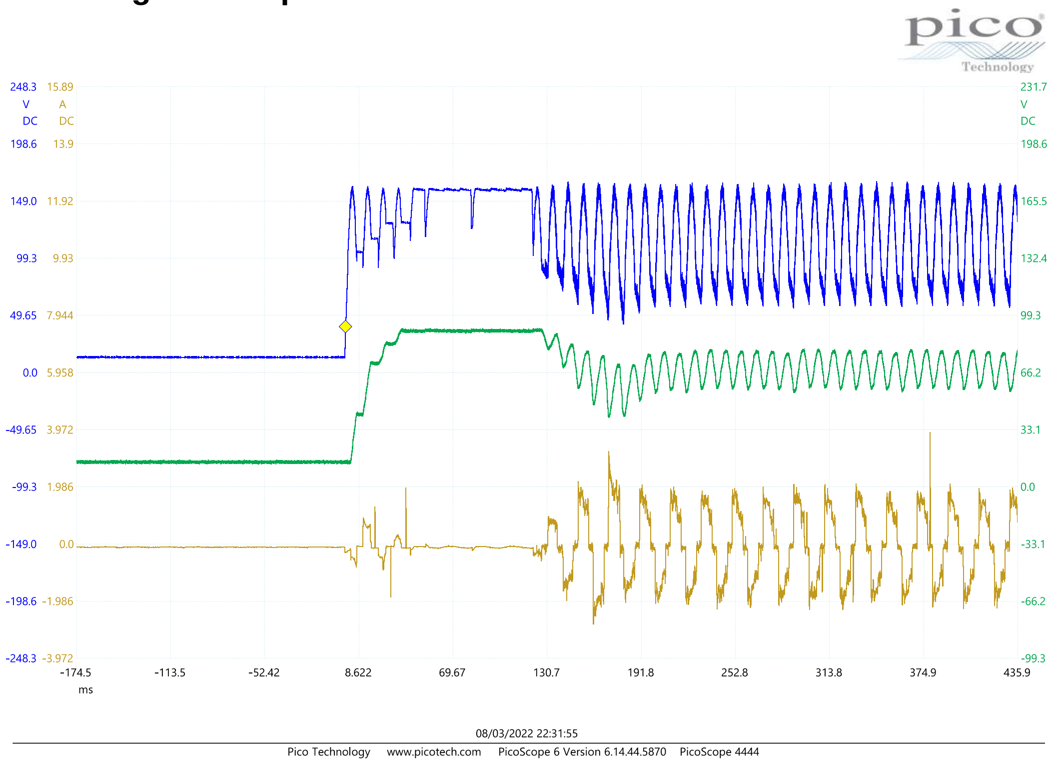
Frequency MHz	QP Level dBµV/m	QP Limit dBµV/m	QP Delta dB
273.32	22.14	37.00	14.86
257.48	21.18	37.00	15.82
135.27	19.60	30.00	10.40
48.26	18.74	30.00	11.26
49.8	18.23	30.00	11.77
239.99	17.97	37.00	19.03
160.02	17.00	30.00	13.00
56.18	15.27	30.00	14.73
57.61	15.11	30.00	14.89

3.5 Inrush Current



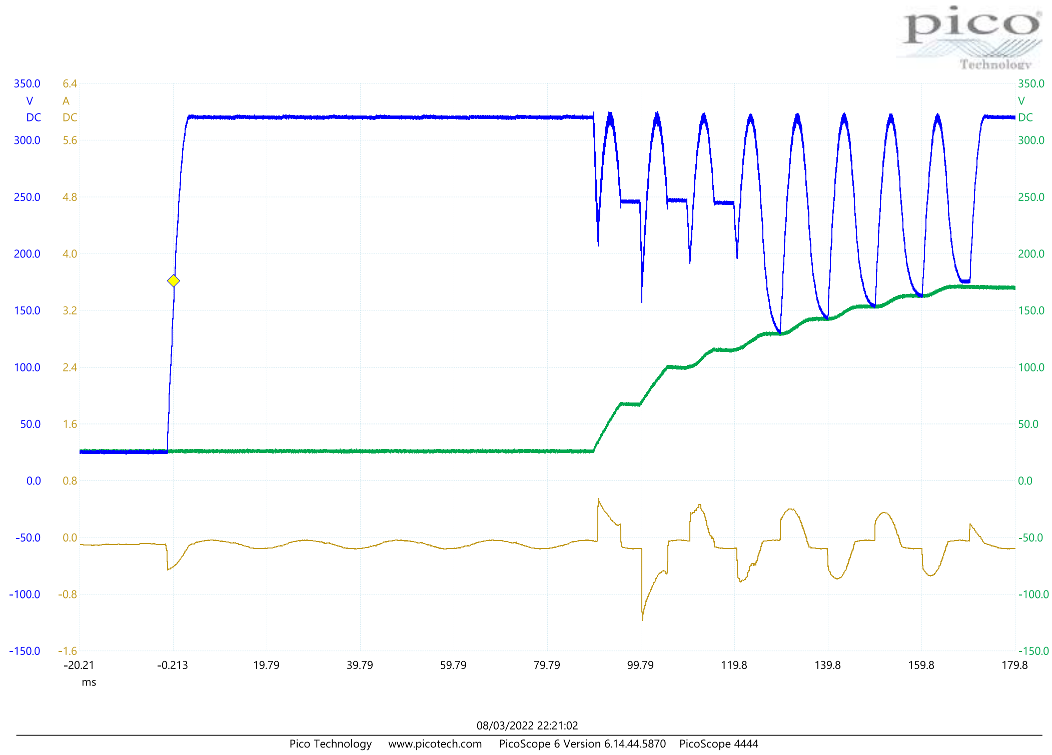
The current spike shown is caused by the X capacitor and the voltage slew rate of the test equipment. It is less than 100uS and does not count towards inrush current as measured using industry standard techniques and guidelines.

3.6 Low Voltage Start-up



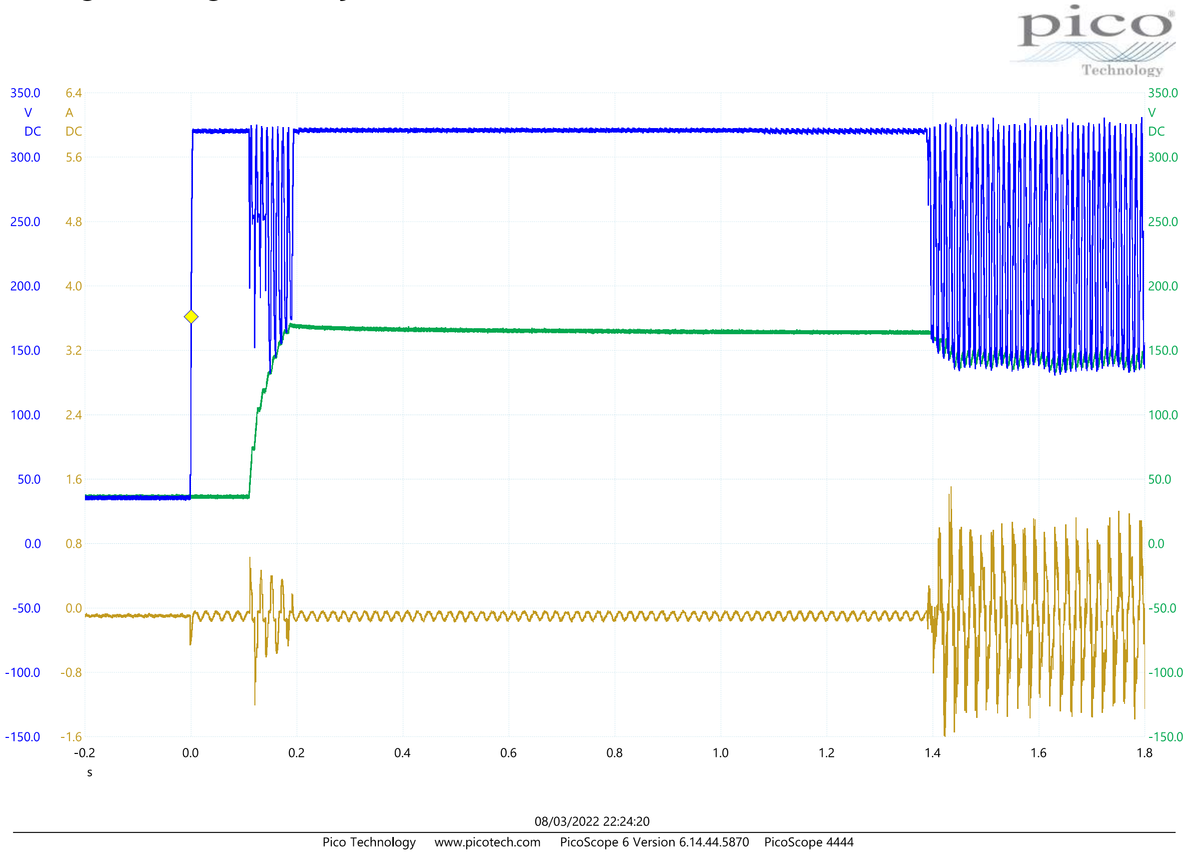
Blue is HVDC; Green is the potential difference on C9 and Brown is the line current

3.7 High Voltage Start-up



Blue is HVDC; Green is the potential difference on C9 and Brown is the line current

3.8 High Voltage Steady State

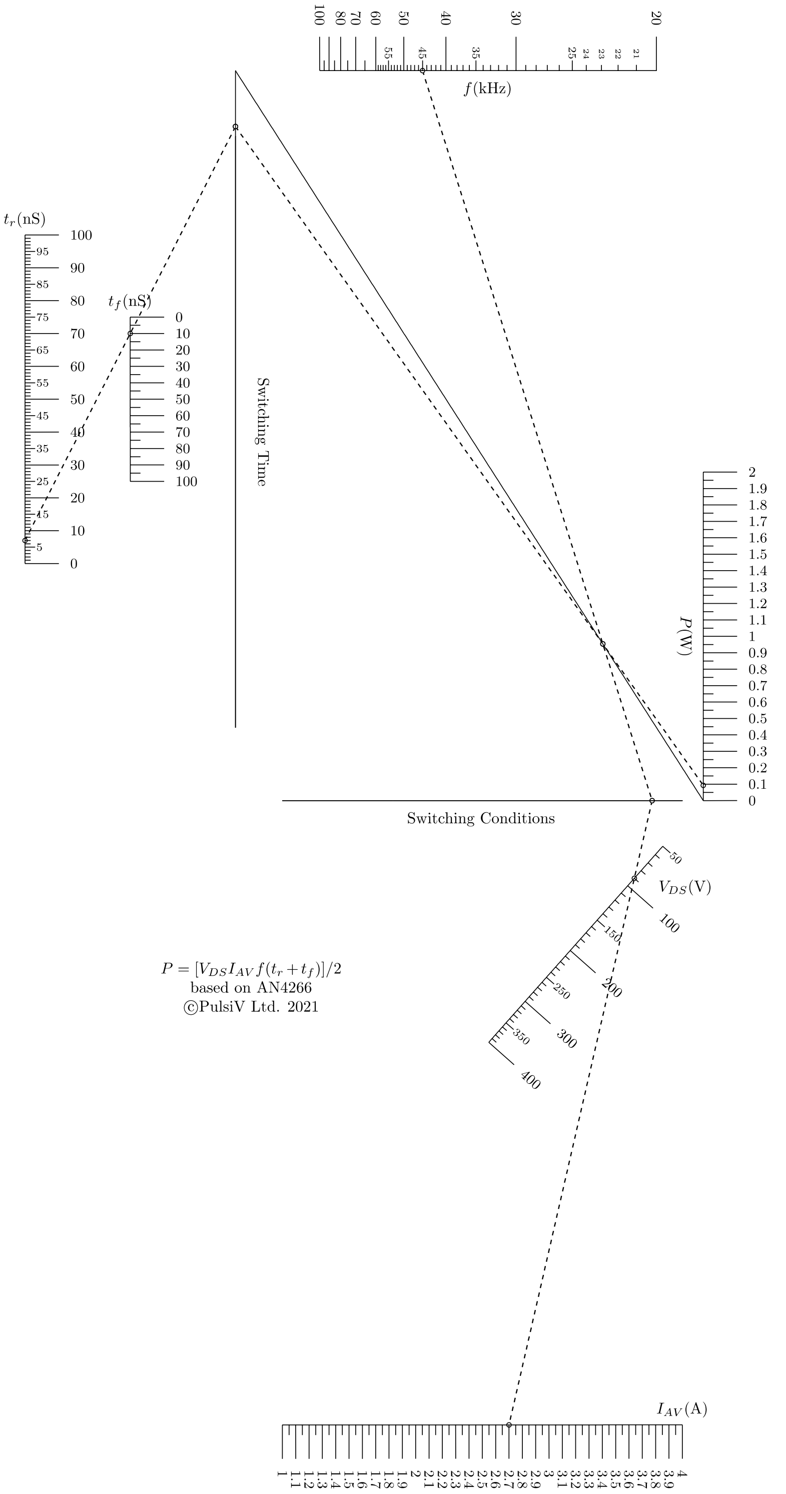


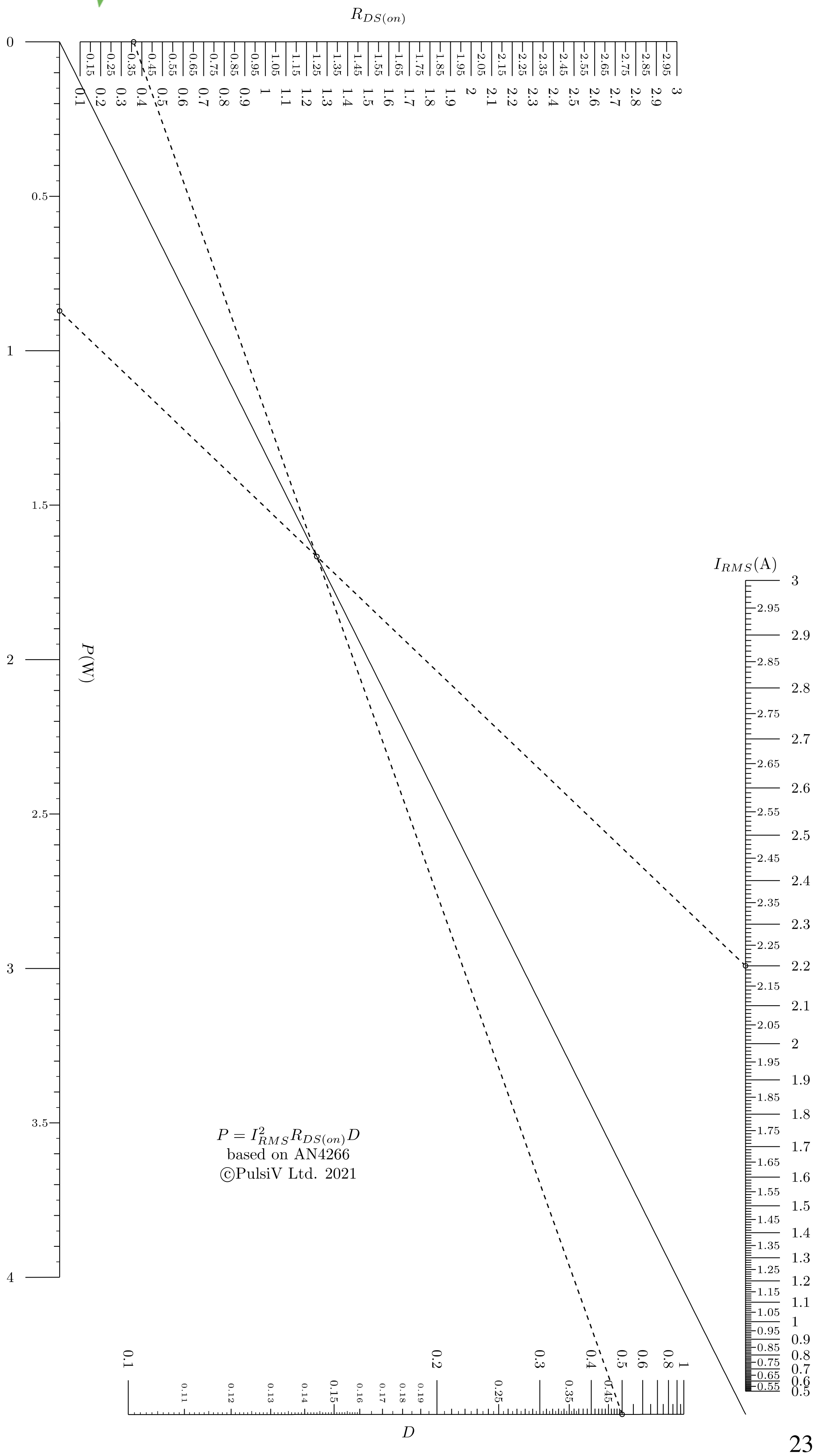
Blue is HVDC; Green is the potential difference on C9 and Brown is the line current

APPENDIX A

Appendix A.1 MOSFET Selection Nomograms

This example shows the losses for MOSFET IPN60R360P7SATMA1.





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