

✓ **54LS/74LS374** 011566  
**OCTAL D-TYPE FLIP-FLOP**  
 (With 3-State Outputs)

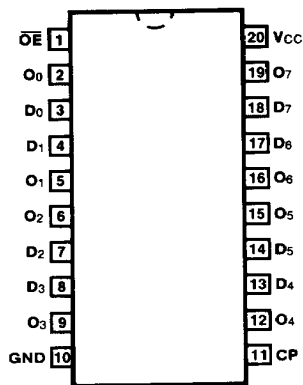
**DESCRIPTION** — The '374 is a high speed, low power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) is common to all flip-flops. The '374 is manufactured using advanced low power Schottky technology and is compatible with all Fairchild TTL families.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**

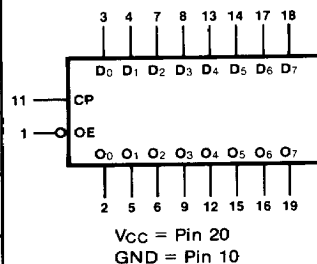
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	74LS374PC		9Z
Ceramic DIP (D)	A	74LS374DC	54LS374DM	4E
Flatpak (F)	A	74LS374FC	54LS374FM	4F

**CONNECTION DIAGRAM**  
PINOUT A



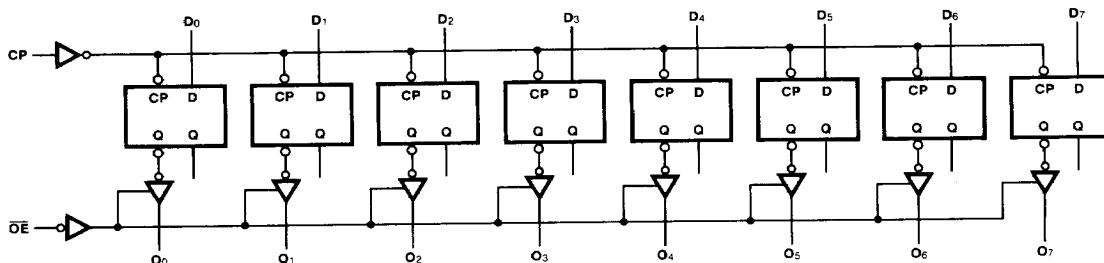
**LOGIC SYMBOL**



**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions



PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D <sub>0</sub> — D <sub>7</sub>	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.25
O <sub>0</sub> — O <sub>7</sub>	3-State Outputs	65/15 (25)/(7.5)

**LOGIC DIAGRAM**



**FUNCTIONAL DESCRIPTION** — The '374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered Clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

**TRUTH TABLE**

INPUTS		OUTPUTS	
D <sub>n</sub>	CP	OE	O <sub>n</sub>
H		L	H
L		L	L
X	X	H	Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I <sub>CC</sub>	Power Supply Current, Outputs OFF		45	mA	V <sub>CC</sub> = Max, D <sub>n</sub> = Gnd OE = 4.5 V

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C <sub>L</sub> = 45 pF			
		Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	35		MHz	Figs. 3-1, 3-8
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>		28	ns	Figs. 3-1, 3-8
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time		28	ns	Figs. 3-3, 3-11, 3-12 R <sub>L</sub> = 667 Ω
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time		20 25	ns	Figs. 3-3, 3-11, 3-12 R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 5 pF

**AC OPERATING REQUIREMENTS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW D <sub>n</sub> to CP	20	20	ns	Fig. 3-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW D <sub>n</sub> to CP	0	0	ns	
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse Width HIGH or LOW	15	15	ns	Fig. 3-8