PHK04P02T

P-channel vertical D-MOS logic level FET

Rev. 02 — 14 December 2010 Product data sheet

1. Product profile

1.1 General description

Logic level P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using vertical D-MOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Suitable for high frequency applications due to fast switching characteristics
- Suitable for logic level gate drive sources
- Suitable for very low gate drive sources voltage

1.3 Applications

- Battery powered applications
- High-speed digital interfaces

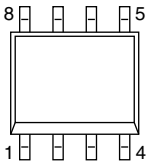
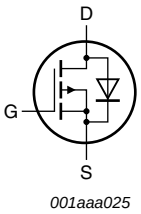
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-	-16	V
I_D	drain current	$T_{sp} = 25$ °C	-	-	-4.66	A
P_{tot}	total power dissipation		-	-	5	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -2.5$ V; $I_D = -1$ A; $T_j = 25$ °C	-	117	150	mΩ
		$V_{GS} = -4.5$ V; $I_D = -1$ A; $T_j = 25$ °C	-	80	120	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = -4.5$ V; $I_D = -1$ A; $V_{DS} = -10$ V; $T_j = 25$ °C	-	1.83	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

SOT96-1 (SO8)

001aaa025

3. Ordering information

Table 3. Ordering information

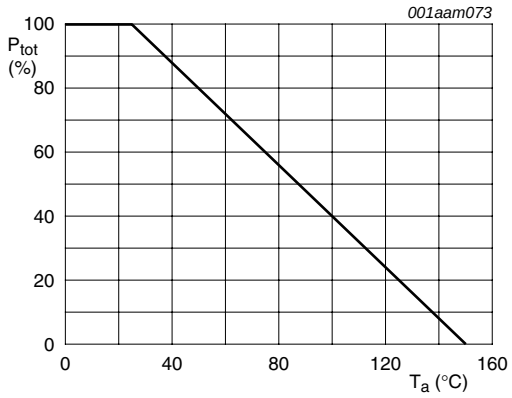
Type number	Package		
	Name	Description	Version
PHK04P02T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

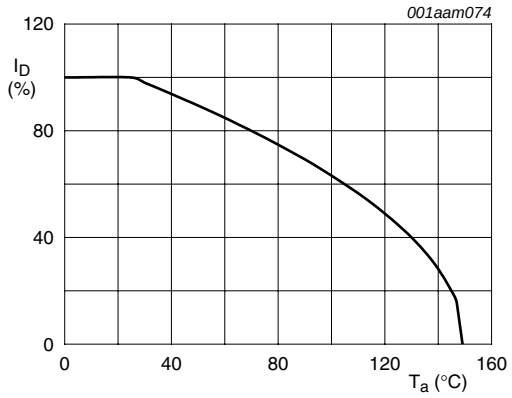
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-16	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ	-	-16	V
V_{GS}	gate-source voltage		-8	8	V
I_D	drain current	T_{sp} = 100 °C	-	-1.87	A
		T_{sp} = 25 °C	-	-4.66	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed	-	-26.4	A
P_{tot}	total power dissipation	T_{sp} = 25 °C	-	5	W
		T_{sp} = 100 °C	-	2	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	T_{sp} = 25 °C	-	-4.66	A
I_{SM}	peak source current	T_{sp} = 25 °C; pulsed; $t_p \leq 5$ s	-	-26	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25\,°C)}} \times 100\,\%$$

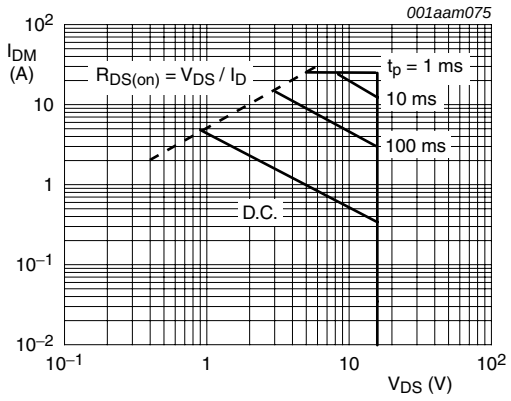
Fig 1. Normalised power dissipation as a function of ambient temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

$V_{GS} \leq -10$ V

Fig 2. Normalized continuous drain current as a function of ambient temperature



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}sp)}$	thermal resistance from junction to solder point	mounted on metal clad substrate	-	25	-	K/W

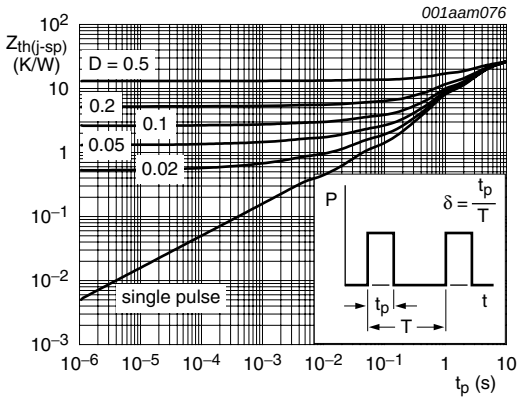
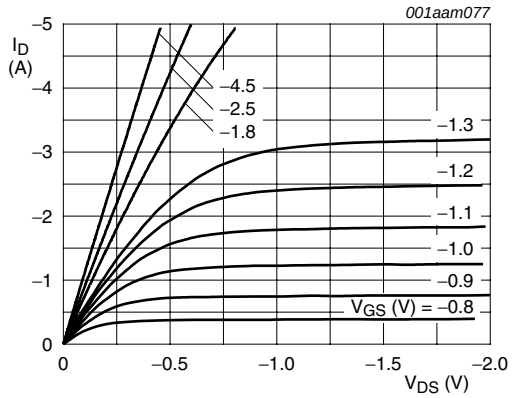


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

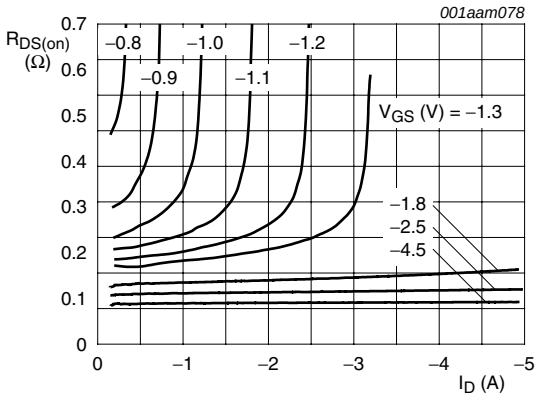
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -10 µA; V_{GS} = 0 V; T_j = 25 °C	-16	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = -1 mA; V_{DS} = V_{GS}; T_j = 25 °C	-0.4	-0.6	-	V
		I_D = -1 mA; V_{DS} = V_{GS}; T_j = 150 °C	-0.1	-	-	V
I_{DSS}	drain leakage current	V_{DS} = -13 V; V_{GS} = 0 V; T_j = 25 °C	-	-50	-100	nA
		V_{DS} = -13 V; V_{GS} = 0 V; T_j = 150 °C	-	-13	-100	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = -2.5 V; I_D = -1 A; T_j = 25 °C	-	117	150	mΩ
		V_{GS} = -2.5 V; I_D = -1 A; T_j = 150 °C	-	175	230	mΩ
		V_{GS} = -1.8 V; I_D = -0.5 A; T_j = 25 °C	-	140	180	mΩ
		V_{GS} = -4.5 V; I_D = -1 A; T_j = 25 °C	-	80	120	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = -1 A; V_{DS} = -10 V; V_{GS} = -4.5 V; T_j = 25 °C	-	7.2	-	nC
Q_{GS}	gate-source charge		-	1.7	-	nC
Q_{GD}	gate-drain charge		-	1.83	-	nC
C_{iss}	input capacitance	V_{DS} = -13 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C	-	528	-	pF
C_{oss}	output capacitance		-	200	-	pF
C_{rss}	reverse transfer capacitance		-	57	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -10 V; R_L = 10 Ω; V_{GS} = -8 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C; I_D = -1 A	-	2	-	ns
t_r	rise time		-	4.5	-	ns
$t_{d(off)}$	turn-off delay time		-	45	-	ns
t_f	fall time		-	20	-	ns
g_{fs}	transfer conductance	V_{DS} = -13 V; I_D = -1 A; T_j = 25 °C	1.5	4.5	-	S
Source-drain diode						
V_{SD}	source-drain voltage	I_S = -0.62 A; V_{GS} = 0 V; T_j = 25 °C	-	-0.62	-1.3	V
t_{rr}	reverse recovery time	I_S = -0.5 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = -12.8 V; T_j = 25 °C	-	75	-	ns
Q_r	recovered charge		-	69	-	nC



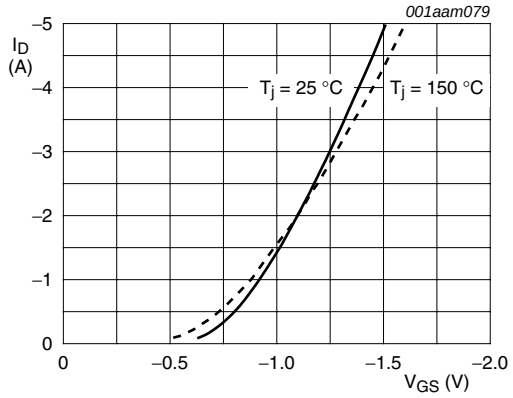
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



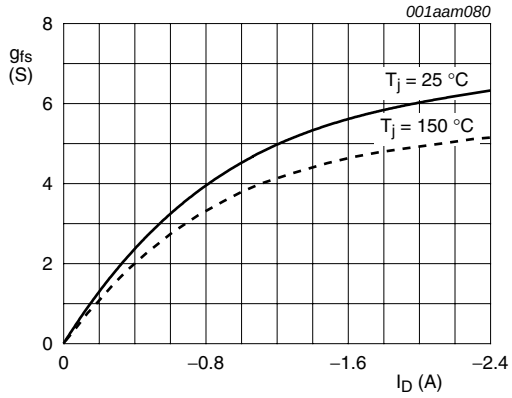
T_j = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



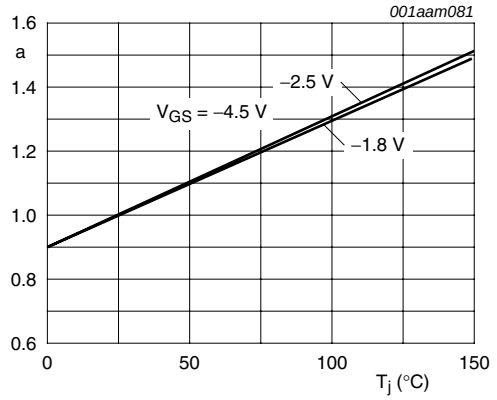
$V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



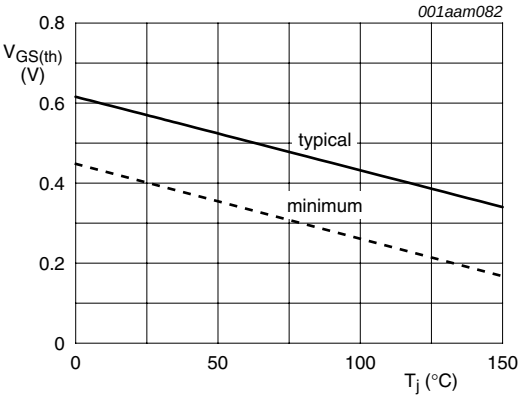
$V_{DS} > I_D \times R_{DSon}$

Fig 8. Forward transconductance as a function of drain current; typical values



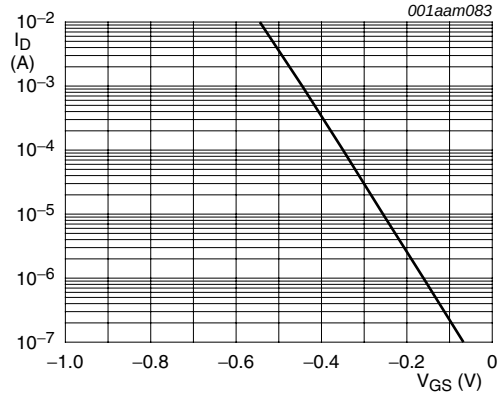
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



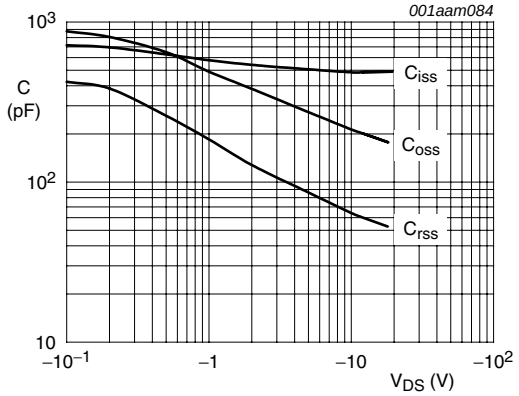
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



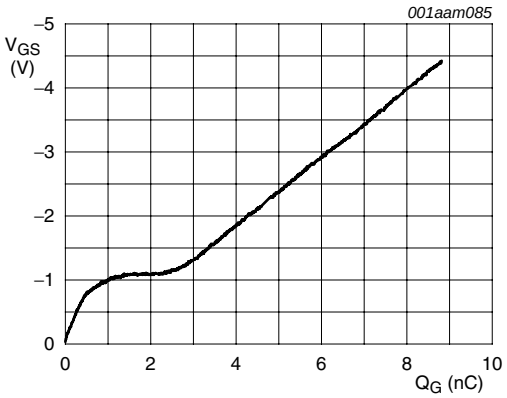
V_{DS} = -5 V; T_j = 25 °C

Fig 11. Sub-threshold drain current as a function of gate-source voltage



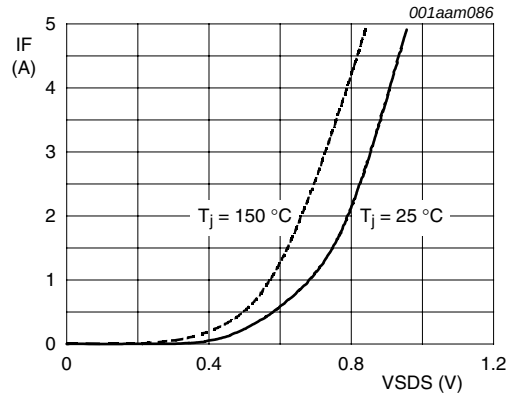
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



T_j = 25 °C; I_D = -1 A

Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values

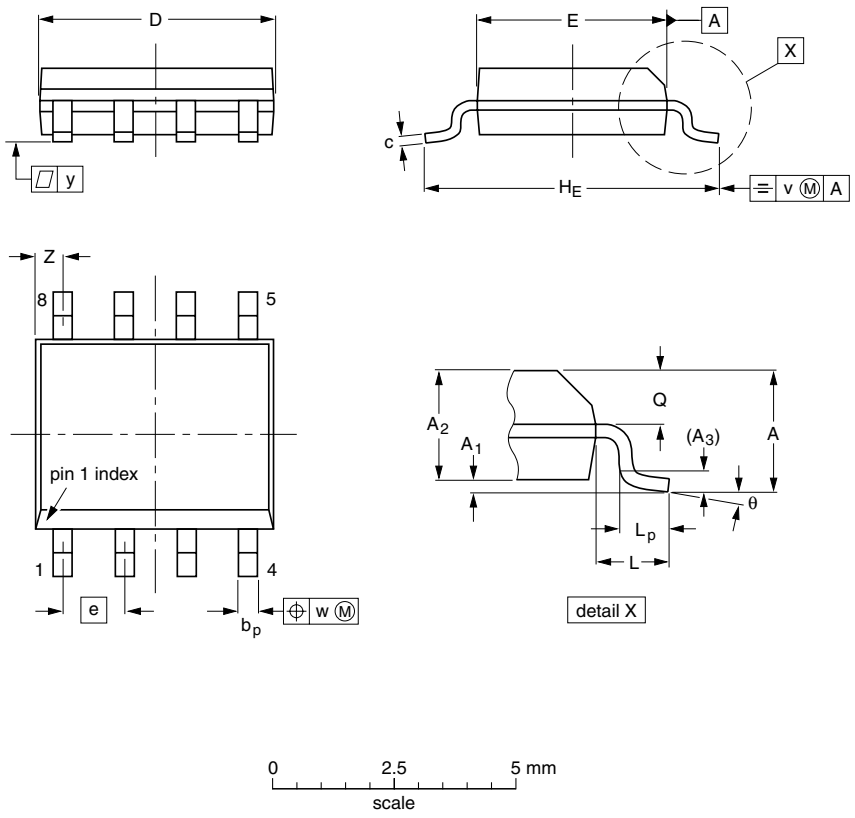


V_{GS} = 0 V

Fig 14. Reverse diode current as a function of reverse diode voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 15. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHK04P02T v.2	20101214	Product data sheet	-	PHK04P02T v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
PHK04P02T v.1	20020501	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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11. Contents

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