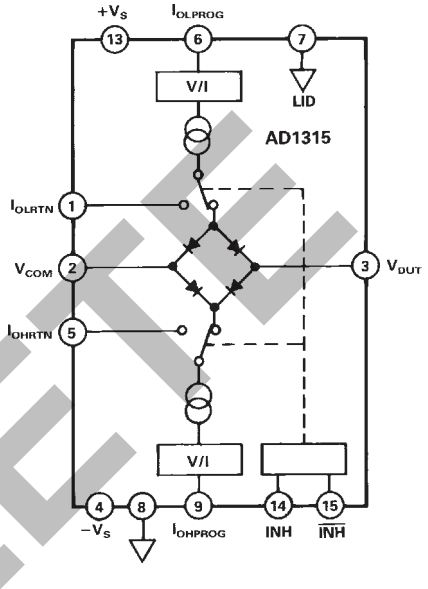
High Speed Active Load with Inhibit Mode

AD1315

FEATURES
+50 mA Voltage Programmable Current Range
1.5 ns Propagation Delay
Inhibit Mode Function
High Speed Differential Inputs for Maximum Flexibility
Hermetically Sealed Small Gull Wing Package
Compatible with AD1321, AD1324 Pin Drivers

APPLICATIONS
Automatic Test Equipment
Semiconductor Test System
Board Level Test System

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1315 is a complete, high speed, current switching load designed for use in linear, digital or mixed signal test systems. By combining a high speed monolithic process with a unique surface mount package, this product attains superb electrical performance while preserving optimum packaging densities in an ultrasmall 16-lead, hermetically sealed gull wing package.

Featuring current programmability of up to +50 mA, the AD1315 is designed to force the device under test to source or sink the programmed I_{OHPROG} and I_{OLPROG} currents. The I_{OH} and I_{OL} currents are determined by applying a corresponding voltage (5 V = 50 mA) to the I_{OH} and I_{OL} pins. The voltage-to-current conversion is performed within the AD1315 thus allowing the current levels to be set by a standard voltage out digital-to-analog converter.

The AD1315's transition from IOH to IOL occurs when the output voltage of the device under test slews above or below the programmed threshold, or commutation voltage. The commutation voltage is programmable from 2 V to +7 V, covering the large spectrum of logic devices while able to support the large current specifications (48 mA) typically associated with line drivers. To test I/O devices, the active load can be switched into a high impedance state (Inhibit mode) electrically removing the active load from the path through the Inhibit mode feature. The active load leakage current in Inhibit is typically 20 nA.

The Inhibit input circuitry is implemented utilizing high speed differential inputs with a common-mode voltage range of 7 volts and a maximum differential voltage of 4 volts. This allows for the direct interface to the precision of differential ECL timing or the simplicity of switching the Active Load from a single ended TTL or CMOS logic source. With switching speeds from IOH or Io~ into Inhibit of less than 1.5 ns, the AD1315 can be electrically removed from the signal path "on-the-fly."

The AD1315 is available in a 16-lead, hermetically sealed gull wing package and is specified to operate over the ambient commercial temperature range from 0°C to +70°C.

REV. A

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AD1315–SPECIFICATIONS

(All measurements made in free air at +25°C. $+V_S$ = +10 V, $-V_S$ = –5.2 V, unless otherwise noted.)

Parameter	AD1315KZ Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
INH to $\overline{\text{INH}}$					
Input Voltage, Any One Input	–3.0		4.0	Volts	
Differential Input Range	0.4	ECL	4.0	Volts	
Bias Current	–2.0	1.0	2.0	mA	
Current Program Voltage Range					
I_{OH}, 0 mA to +50 mA (Sink)[1]	0		+5.0	Volts	
I_{OL}, 0 mA to –50 mA (Source)[1]	0		+5.0	Volts	
Input Resistance		50		kΩ	
I_{OHRTN}, I_{OCRTN} Range[2]	–2.0		+7.0	Volts	
V_{COM}, V_{DUT} Range	–2.0		+7.0	Volts	
I_{OH}, 0 mA to +50 mA	0.5		+7.0	Volts	$V_{DUT} - V_{COM}$ >1 V
I_{OL}, 0 mA to –50 mA	–2.0		+4.0	Volts	$V_{COM} - V_{DUT}$ >1 V
OUTPUT CHARACTERISTICS[3]					
Active (Sink/Source) Mode					
Transfer Function		10		mA/V	See Figure 1
Accuracy					See Figure 1
Linearity Error	–0.12		+0.12	% FSR	
Gain Error	–2.0		+2.0	% FSR	
Offset Error	–1.0		+1.0	mA	
Output Current TC		10		µA/°C	
Inhibit Mode					
Output Capacitance			3.0	pF	
Inhibit Leakage	–200	20	200	nA	
DYNAMIC PERFORMANCE[3]					
Propagation Delay					See Figure 2
$\pm I_{MAX}$ to INHIBIT (t_{PD1})[4]		0.5	1.5	ns	
INHIBIT to $\pm I_{MAX}$ (t_{PD2})[4]		1.5	3.0	ns	
POWER SUPPLIES					
$-V_S$ to $+V_S$ Difference		15.2	15.4	Volts	
Supply Range					
Positive Supply	+9.5	+10	+10.5	Volts	
Negative Supply	–5.45	–5.2	–4.95	Volts	
Current					
Positive Supply[5]	+70[5]	+85	+100	mA	
Negative Supply[5]	–100[5]	–85	–70	mA	
Power Dissipation[6]		1.3	1.54		
PSRR[7]			0.05	%/%	

NOTES

[1]I_{OHPROG}/I_{OLPROG} voltage range may be extended to –100 mV due to a possible 1 mA offset current.

[2]I_{OHRTN}/I_{OLRTN} should be connected to V_{COM} to minimize power dissipation.

[3]V_{DUT} = –2 V to +7 V, C_{TOTAL} = 10 pF, R_{DUT} = 10 Ω. For inhibit leakage tests, V_{DUT} = 0 V to +5.9 V, I_{OH} = –4 mA, I_{OL} = +4 mA, T_{CASE} = +36°C.

[4]Measured from the ECL crossing to the 10% change in the output current.

[5]$I_{PROGRAM}$ = ±50 mA.

[6]Maximum power dissipation with $+V_S$ = +10 V, $-V_S$ = 5.2 V, $I_{PROGRAM}$ 50 mA, $V_{COM} = V_{DUT}$ = 0 V.

[7]For a 1% change in $+V_S$ or V_S, the output current may change a maximum of 0.05% of Full Scale Range (FSR).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage
- $+V_S$ to GND . . . . . +12 V
- $-V_S$ to GND . . . . . –11 V
- Difference from $+V_S$ to $-V_S$ . . . . . 16 V

Inputs
- Difference from INH to $\overline{INH}$ . . . . . 5 V
- INH, $\overline{INH}$ . . . . . $+V_S$ – 13.4 V, $-V_S$ + 11 V
- V_{COM}, V_{DUT} . . . . . $+V_S$ – 13.1 V, $-V_S$ + 13.2 V
- I_{OL}, I_{OH} Program Voltage . . . . . $+V_S$ – 15 V, $-V_S$ + 15 V

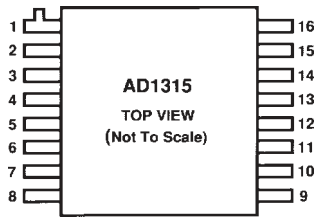
Operating Temperature Range . . . . . 0 to +70°C
Storage Temperature Range . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 20 sec)[2] . . . . . +300°C

Pin No.	Symbol	Function
1	I_{OLRTN}	Logic Low Current Return
2	V_{COM}	Communication Voltage
3	V_{DUT}	Load/Dot Connection
4	$-V_S$	Negative Supply
5	I_{OHRTN}	Logic High Current Return
6	I_{OLPROG}	Logic Low Current Program Voltage
7	LID	Lid Connection (Internal)
8	GND	Ground
9	I_{OHPROG}	Logic High Current Program Voltage
10	N/C	No Connection
11	N/C	No Connection
12	N/C	No Connection
13	$+V_S$	Positive Supply
14	INH	Inhibit
15	$\overline{INH}$	Inhibit
16	N/C	No Connection

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

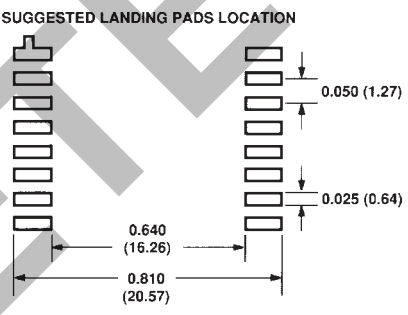
[2]To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in an environment at 24°C, ±5°C (75°F, ±10°F) with relative humidity not to exceed 65%.

CONNECTION DIAGRAM



SUGGESTED PAD LOCATION

Dimensions shown in inches and (mm).



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1315KZ	0 to +70°C	16-Lead Gull Wing	Z-16B

*Z = Leaded Chip Carrier (Ceramic).

DEFINITION OF TERMS

Gain

The measured transconductance.

$$Gain = \frac{I_{OUT}(@\ 5V\ Input) - I_{OUT}(@\ 0.2V\ Input)}{V_{PROG}(@\ 5V) - V_{PROG}(@\ 0.2V)}$$

where:

V_{PROG} values are measured at I_{OL}/I_{OH} PROG

Gain Error

The difference between the measured transconductance and the ideal expressed as a % of full-scale range.

$$Ideal\ Gain = 10\ mA/V$$

$$Gain\ Error = \frac{Ideal\ Gain - Actual\ Gain}{Ideal\ Gain} \times 100$$

Offset Error

Offset Error is measured by setting the I_{OHPROG} or I_{OLPROG} inputs to 0.2 V and measuring I_{OUT}. Since both I_{OH} and I_{OL} outputs are unipolar, this small initial offset of 2 mA must be set to allow for measurement of possible negative offset. With a gain of 10 mA/V, a 0.2 V input should yield an output of ±2 mA. The difference between the observed output and the ideal ±2 mA output is the offset error.

$$Offset\ Error = I_{OUT}\ (@\ 0.2\ V) - Gain \times V_{PROG}\ (@\ 0.2\ V)$$

Linearity Error

The deviation of the transfer function from a straight line defined by Offset and Gain expressed as a % of FSR.

$$I_{OUT}\ (calc) = Gain \times V_{PROG}\ (@\ set\ point) + Offset$$

where:

$set\ point = V_{PROG}$ (from 0.2 V to 5 V)

$$I_{OUT}\ (FSR) = Gain \times V_{PROG}\ (@\ 5\ V) + Offset$$

$$Linearity\ Error\ \frac{I_{OUT}\ (measured) - I_{OUT}\ (calc)}{I_{OUT}\ (FSR)} \times 100$$

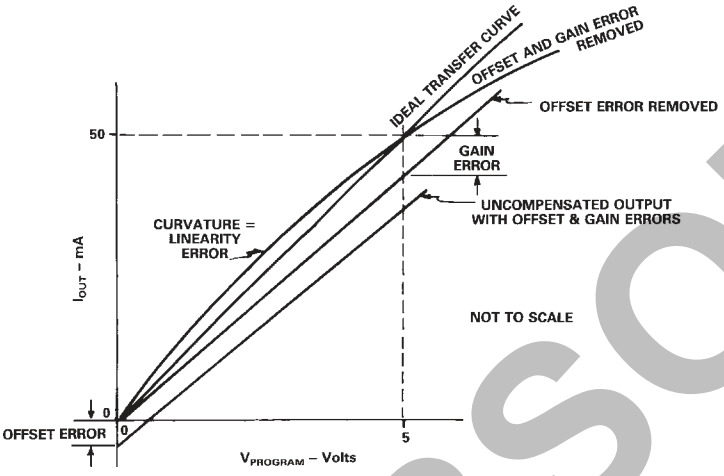


Figure 1. Definition of Terms

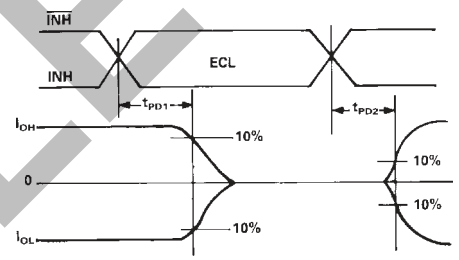


Figure 2. Timing Diagram for Inhibit Transition

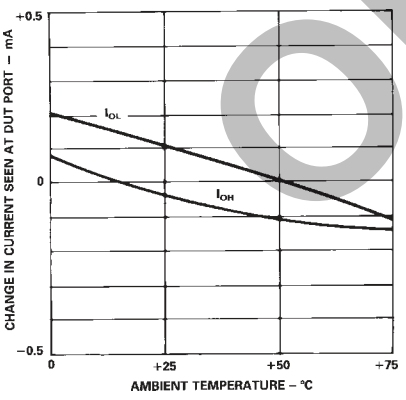


Figure 3. I_{OL}, I_{OH} Offset Current vs. Temperature

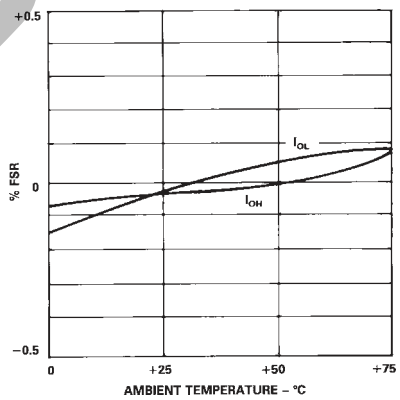


Figure 4. I_{OL}, I_{OH} Gain Error vs. Temperature

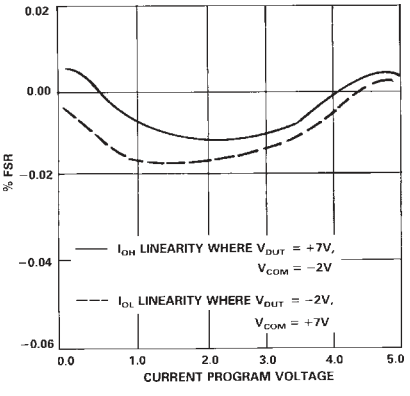


Figure 5. I_{OL}, I_{OH} Linearity Error vs. Current Program Voltage

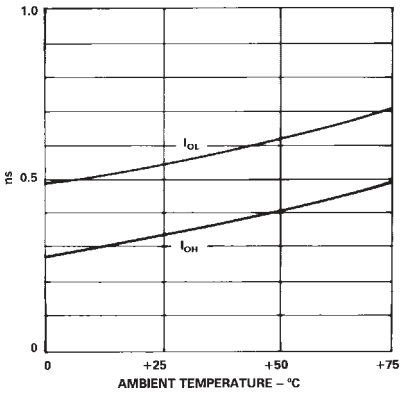


Figure 6. $+I_{MAX}$, $-I_{MAX}$ to Inhibit Propagation Delay vs. Temperature

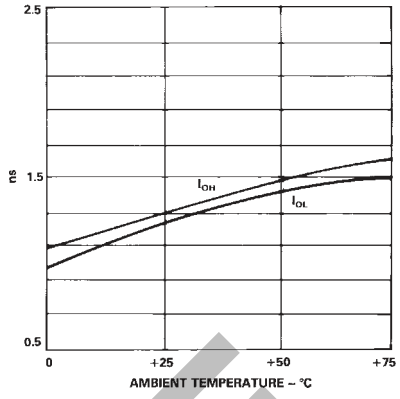


Figure 7. Inhibit to $+I_{MAX}$, $-I_{MAX}$ Propagation Delay vs. Temperature

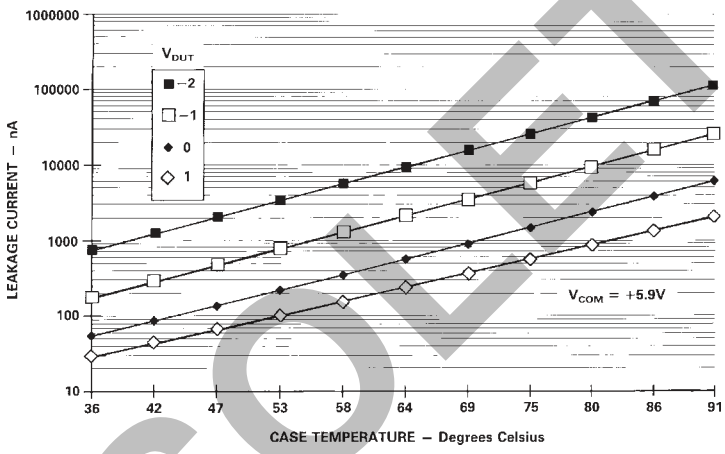


Figure 8. Inhibit Mode Leakage Current vs. Case Temperature

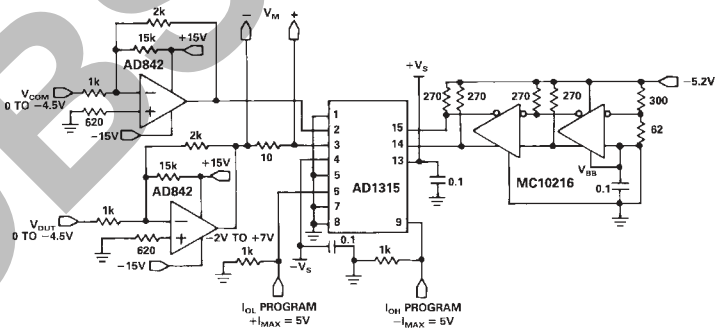


Figure 9. AD1315 DC Test Circuit

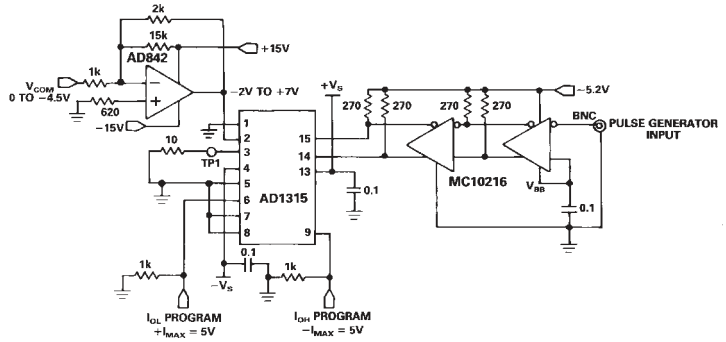


Figure 10. AD1315 Propagation Delay Test Circuit

FUNCTIONAL DESCRIPTION

The AD1315 is a complete high speed active load designed for use in general purpose instrumentation and digital functional test equipment. The function of the active load is to provide independently variable source and sink currents for the device to be tested.

The equivalent circuit for the AD1315 is shown in Figure 11. An active load performs the function of loading the output of the device under test with a programmed I_{OH} or I_{OL}. These currents are independently programmable. V_{COM} is the commutation voltage point at which the load switches from source to sink mode. The active load may also be inhibited, steering current to the I_{OLRTN} and I_{OHRTN} pins, effectively disconnecting it from the test pin.

The AD1315 accepts differential digital signals at its inhibit inputs ensuring precise timing control and high noise immunity. The wide inhibit input voltage range allows for ECL power supplies of –5.2 V and 0 V, –3.2 V and +2 V, and 0 V and +5 V. Where speed and timing accuracy are less important, TTL or CMOS logic levels may be used to toggle the Inhibit inputs of the AD1315. Single ended operation is possible by biasing one of the inputs to approximately +1.3 V for TTL or $V_{CC}/2$ for CMOS. Care should be taken to observe the 4 V maximum allowable input voltage.

The I_{OH} and I_{OL} programming inputs accept 0 V to +5 V analog inputs, corresponding to 0 to 50 mA output currents. The V_{COM} input, which sets the I_{OH}/I_{OL} switch point, may be set anywhere within the input range of –2 V to +7 V.

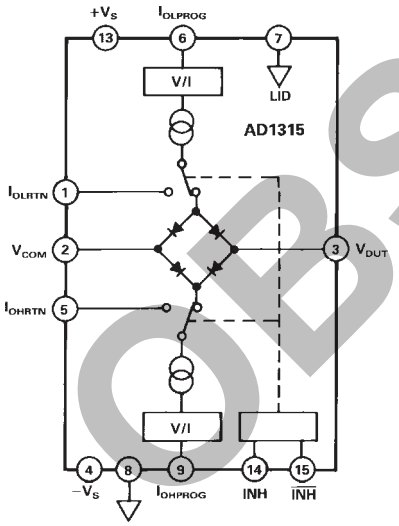


Figure 11. Block Diagram

V_{DUT} VOLTAGE RANGE

In Figure 12, V_{DUT} range, I_{OH} and I_{OL} typical current maximums are plotted versus DUT voltage. In the I_{OH} mode (V_{DUT} higher than V_{COM}), the load will sink 50 mA, until its output starts to saturate at approximately –1.5 V. In the I_{OL} mode (V_{DUT} lower than V_{COM}), the load will source 50 mA until its output starts to saturate at approximately +5.5 V. At +7 V, the source current will be close to zero.

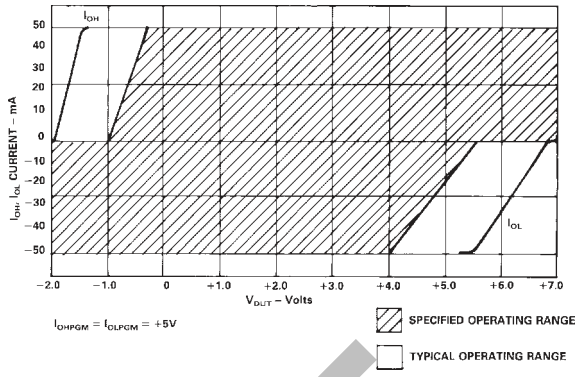


Figure 12. Allowable Current Range for I_{OH}, I_{OL} vs. V_{DUT}

Ideally, the commutation point set at V_{COM} would provide instantaneous current sink/source switching. Because of I/V characteristics of the internal bridge diodes, this is not the case. To guarantee full current switching at the DUT, at least a 1 volt difference between V_{COM} and V_{DUT} must be maintained in steady state conditions. Because of the relatively fast edge rates exhibited by typical logic device outputs, this should not be a problem in normal ATE applications.

INHIBIT MODE LEAKAGE

The AD1315's inhibit-mode leakage current changes with both temperature and bias levels. There are two major contributing effects: transistor reverse-bias collector-base leakage and reverse leakage in the Schottky-diode bridge. Leakage variations with V_{DUT} arise primarily from transistor collector-base leakage, while both effects contribute to leakage current temperature variations. Inhibit-mode leakage is weakly dependent on V_{COM} and decreases slightly as the difference between V_{DUT} and V_{COM} is reduced. Figure 8 shows typical AD1315 inhibit leakage current as a function of V_{DUT} and temperature.

THERMAL CONSIDERATIONS

The AD1315 is provided in a 0.550" × 0.550", 16-lead (bottom brazed) gull wing, surface mount package with a θ_{JC} of 10°C/W (typ). Thermal resistance (case-to-ambient) vs. air flow for the AD1315 in this package is shown in Figure 13. The data presented is for a ZIF socketed device. For PCB mounted devices (w/30 mils clearance) the thermal resistance should be ~3 to 7% lower with air flows below 320 lfm[(1)]. Notice that the improvement in thermal resistance vs. air flow starts to flatten out just above 400 lfm[(2)].

NOTES
[1]lfm is air flow in linear feet/minute.
[2]For convection cooled systems, the minimum recommended airflow is 400 lfm.

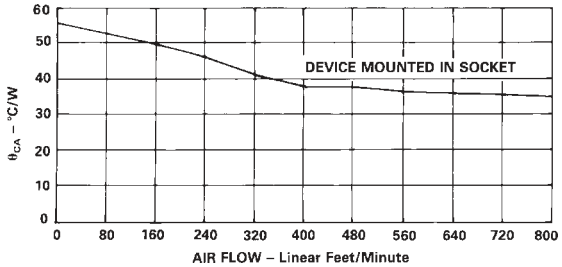


Figure 13. Case-to-Ambient Thermal Resistance vs. Air Flow

APPLICATIONS

The AD1315 has been optimized to function as an active load in an ATE test system. Figure 14 shows a block diagram illustrating the electronics behind a single pin of a high speed digital functional test system with the ability to test I/O pins on logic devices. The AD1315 active load, AD1321 or AD1324 pin driver, AD1317 high speed dual comparator and the AD664 quad 12-bit voltage DAC would comprise the pin electronic portion of the test system. Such a system could operate at 100 MHz with the AD1321 (200 MHz with the AD1324) in a data mode or 50 MHz (100 MHz) in the I/O mode.

The V_{COM} input sets the commutation voltage of the active load. With DUT output voltage above V_{COM}, the load will sink current (I_{OH}). With DUT output voltage below V_{COM}, the load will source current (I_{OL}). Like the I_{OH} and I_{OL} return lines, the V_{COM} must be able to sink or source 50 mA, therefore a standard op amp will not suffice. An op amp with an external complementary output stage or a high power op amp such as the AD842 will work well here. A typical application is shown in Figure 15.

LAYOUT CONSIDERATIONS

I_{OHRTN} and I_{OLRTN} may be connected to any potential between –2 V and +7 V. These return points must be able to source or sink 50 mA, since the I_{OH} and I_{OL} programmed currents are diverted here in the inhibit mode. The RTNs may be connected to a suitable GND. However, to keep transient ground currents to a minimum, they are typically tied to the V_{COM} programming voltage point.

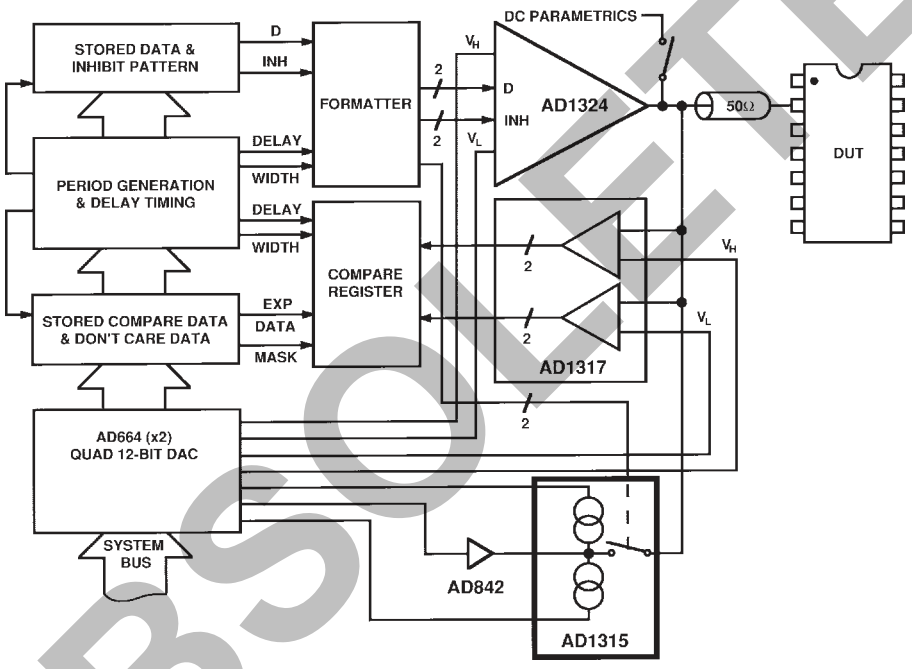


Figure 14. High Speed Digital Test System Block Diagram

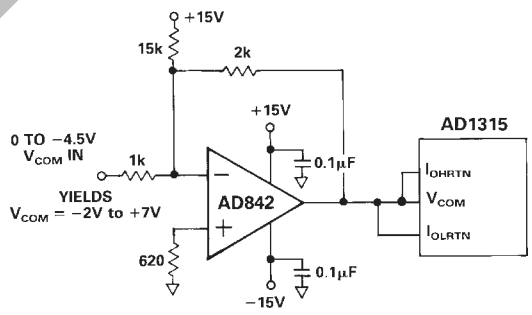


Figure 15. Suggested I_{OHRTN}, I_{OLRTN}, V_{COM} Hookup

EVALUATION BOARD

The AD1315 Evaluation Board allows the designer to easily evaluate the performance of the AD1315 and its suitability for the specific application. The AD1315EB includes a mounted AD1315KZ active load, an ECL input buffer for Inhibit and the oscilloscope probe jacks necessary to properly analyze the true performance of the AD1315KZ. An equipment list is provided in order to minimize variations due to test setups.

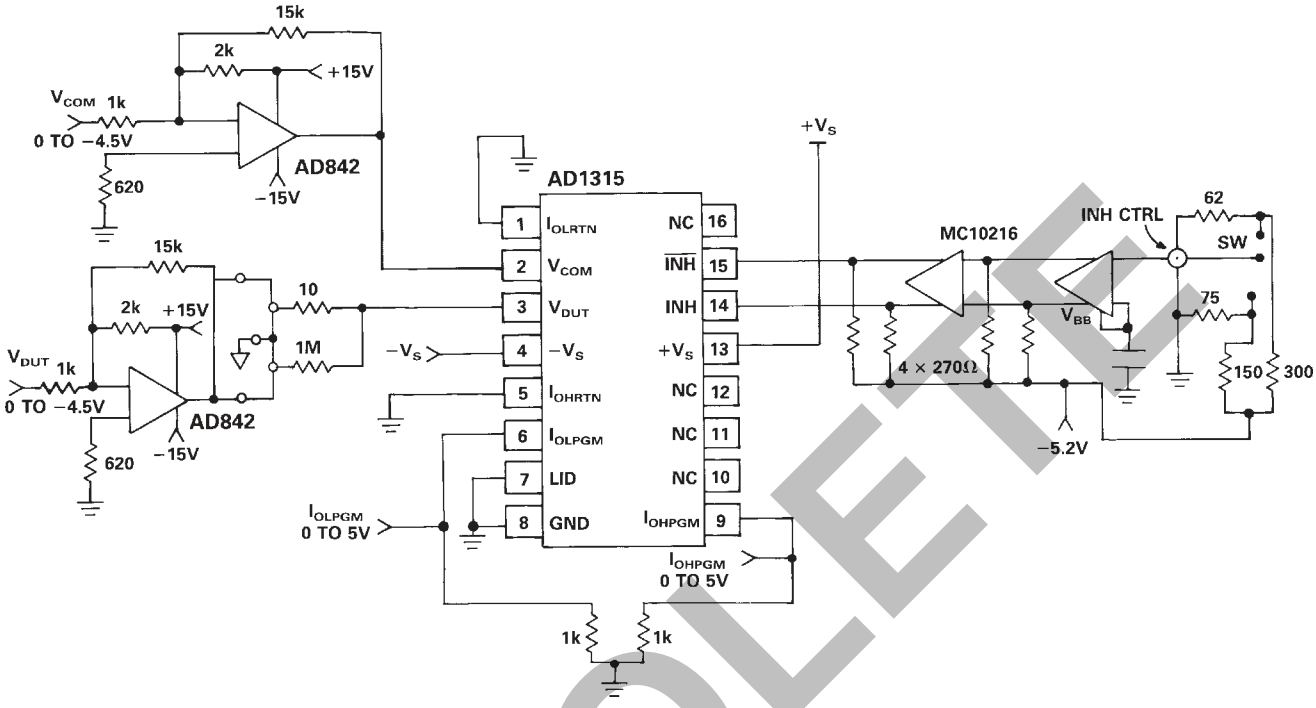
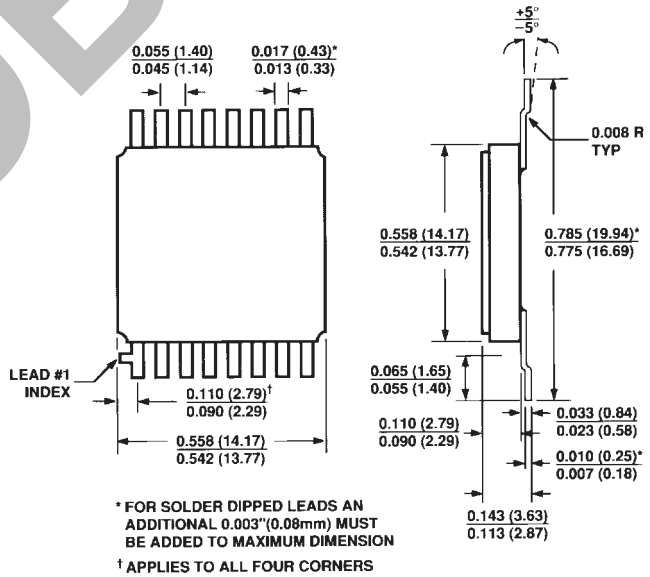


Figure 16. AD1315EB Evaluation Board Circuit

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Gull Wing
(Z-16B)



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