ISL94202EVKIT1Z

Evaluation Kit

UG106
Rev.1.0
Apr 13, 2021

The ISL94202EVKIT1Z is a kit that facilitates testing of the ISL94202 Li-ion battery pack monitor and control ICs. The ISL94202 monitors cell voltage, current, and temperature. It converts the cell voltages, pack current, and temperatures to 12-bit digital values, provides cell balance control, and provides complete stand-alone battery pack operation.

Default stand-alone operation of the ISL94202 can be overridden by an external microcontroller. The PC based Graphical User Interface (GUI) includes functions to monitor stand-alone operation and to demonstrate operation with an external microcontroller.

Specifications

This board has been configured and optimized for the following operating conditions:

- Configurable to 3 to 8 cells, default 3 cells
- Standard cell voltage range 2.699V to 4.250V
- OV/UV delay times 1 and 4 seconds respectively
- CB maximum delta voltage 0.501
- CB maximum/minimum voltage 4.032V and 3.100V

NOTE: Consult programming options for full listing of programmable parameters and ranges.

Key Features

- Status LEDs monitor RGO, EOC, SD, and PSD conditions
- Jumper configuration single or split path applications
- Wakeup push button for "Exit Sleep" control
- FETs off push button for quick all FETs off condition
- Cell balance LEDs for MCB process observation
- PCB layout accommodates "solder braid" addition for high current evaluation
- Software enables real time observation and data collection of 14 analog measurements and 27 digital status indicators

Ordering Information

PART NUMBER	DESCRIPTION
ISL94202EVKIT1Z	Evaluation kit for the ISL94202

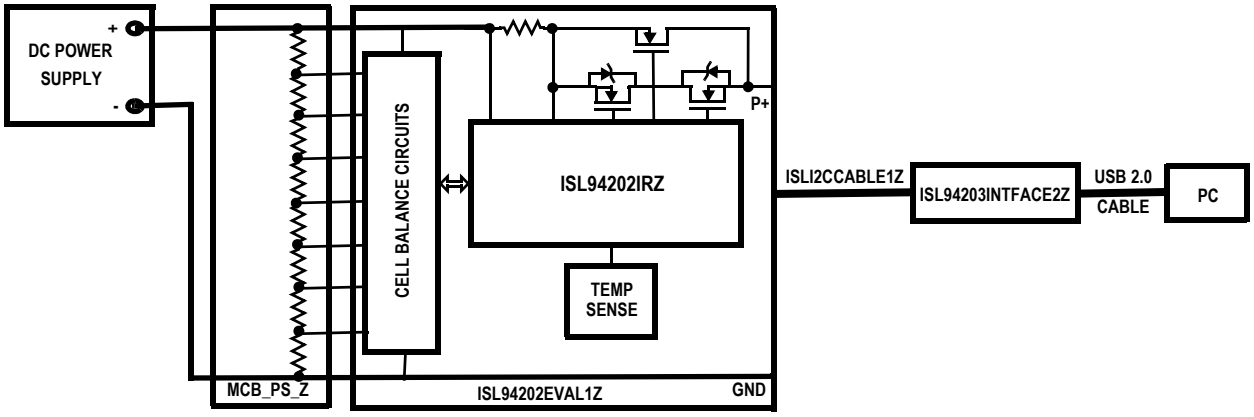


FIGURE 1. BASIC EVALUATION TEST SETUP BLOCK DIAGRAM

What is Inside

The evaluation kit contains:

- ISL94202EVAL1Z evaluation board
- MCB_PS_Z multicell power supply test board
- ISL94202INTFACEKIT1Z USB to I^2C interface kit, includes a PCB and I^2C cable
- USB cable, connects PC to USB-I^2C interface board

What is Needed

The following instruments will be needed to perform testing:

- 30V/1A adjustable power supply
- Wires to connect power supply to MCB_PS_Z board
- Precision multimeter (optional)
- Oscilloscope (optional)
- Cables and wires (optional)

Software Installation

Step 1: Connect the ISLUSBI2C USB to the PC. The board should automatically enumerate in the device control panel under Human Interface Devices. The vendor ID will be 0x09AA and the product ID will be 0x2036. Because it is a HID device, no special driver is needed.

Step 2: Copy the isl94203evkit1z-software.exe program to the PC (any desired location). Double-click to run the installation file. Note you may need to use the “Run as Administrator” option when performing the installation.file.

Quick Hardware Setup Guide

Step 1: Check the jumpers and switches on the board. The board should be configured as follows:

- ADDR jumper set to “0”.
- xT2 Select jumper on either “CELL” or “FET”.
- FET jumpers set for either one path or two path. Start with one path.
- J4 jumper is set to “1 Path”.
  J9 jumper is set to “1 Path”.

Step 2: Connect the power supply to the MCB_PS_Z board. The positive terminal is J5/J11 and the negative terminal is J8/J12. There should be a jumper on JP2/8CELL.

Step 3: Set the power supply voltage to 28V (3.5V per cell). (Optional: check that the voltages at terminal J1 or J3 are 3.5V per cell).

Step 4: Turn off the power to the power supply.

Step 5: Connect the ISL94202 board directly to the MCB_PS_Z board at connector J1. Make sure the board is connected on the ground side of J1 (see Figure 4).

Step 6: Turn on the power to the supply. If no LEDs light, press the “WakeUp” button. Notice that there is one green LED (RGO), indicating the LDO regulator on the ISL94202 is operating.
The voltages at various points should be:
RGO = 2.5V ±3%
VREF = 1.80V ±0.5%

Step 7: Connect the USB port of the PC to the USB port of the ISL94202INTFACEKIT1Z interface board.

Step 8: Connect the I^2C cable from the ISL94202INTFACEKIT1Z board to the ISL94202EVKIT1Z board (J13).

Step 9: Open the ISL94202 GUI software. Use the software to read the cell voltages.

Step 10: Compare the voltages at the board input (use a meter to measure each input voltage, because the MCB_PS_Z board may not accurately divide the voltages into equal 3.5V steps) with the readings provided by the GUI. These voltages should closely match.

Step 11: See other operations described later in this document.

PCB Layout Guidelines

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high performance from your PC board.

- The use of low inductance components, such as chip resistors and chip capacitors, is strongly recommended.
- Minimize signal trace lengths. This is especially true for the VDD, charge pump decoupling, CS1, CS2, and VC0-VC8 inputs. Trace inductance and capacitance can easily affect circuit performance. Vias in the signal lines add inductance at high frequency and should be avoided.
- Match channel-to-channel analog I/O trace lengths and layout symmetry. This is especially true for the CS1 and CS2 lines, since their inputs are normally very low voltage.
- Maximize use of AC decoupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e., no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- When testing, use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.

FIGURE 2. ISL94202EVAL1Z TOP OF BOARD

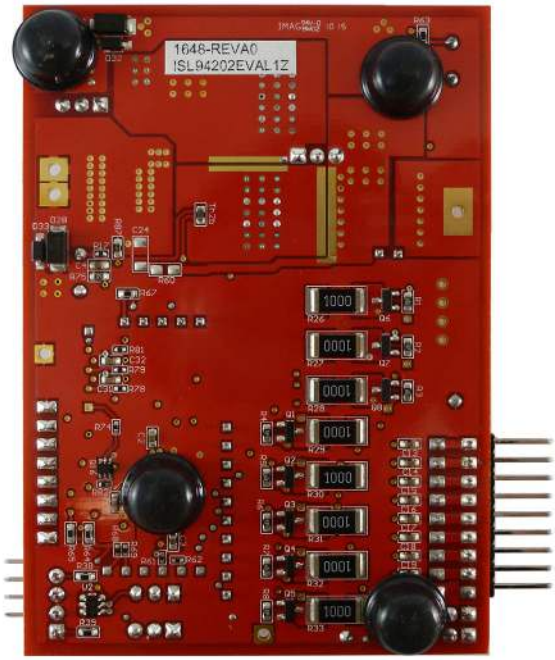


FIGURE 3. ISL94202EVAL1Z BOTTOM OF BOARD

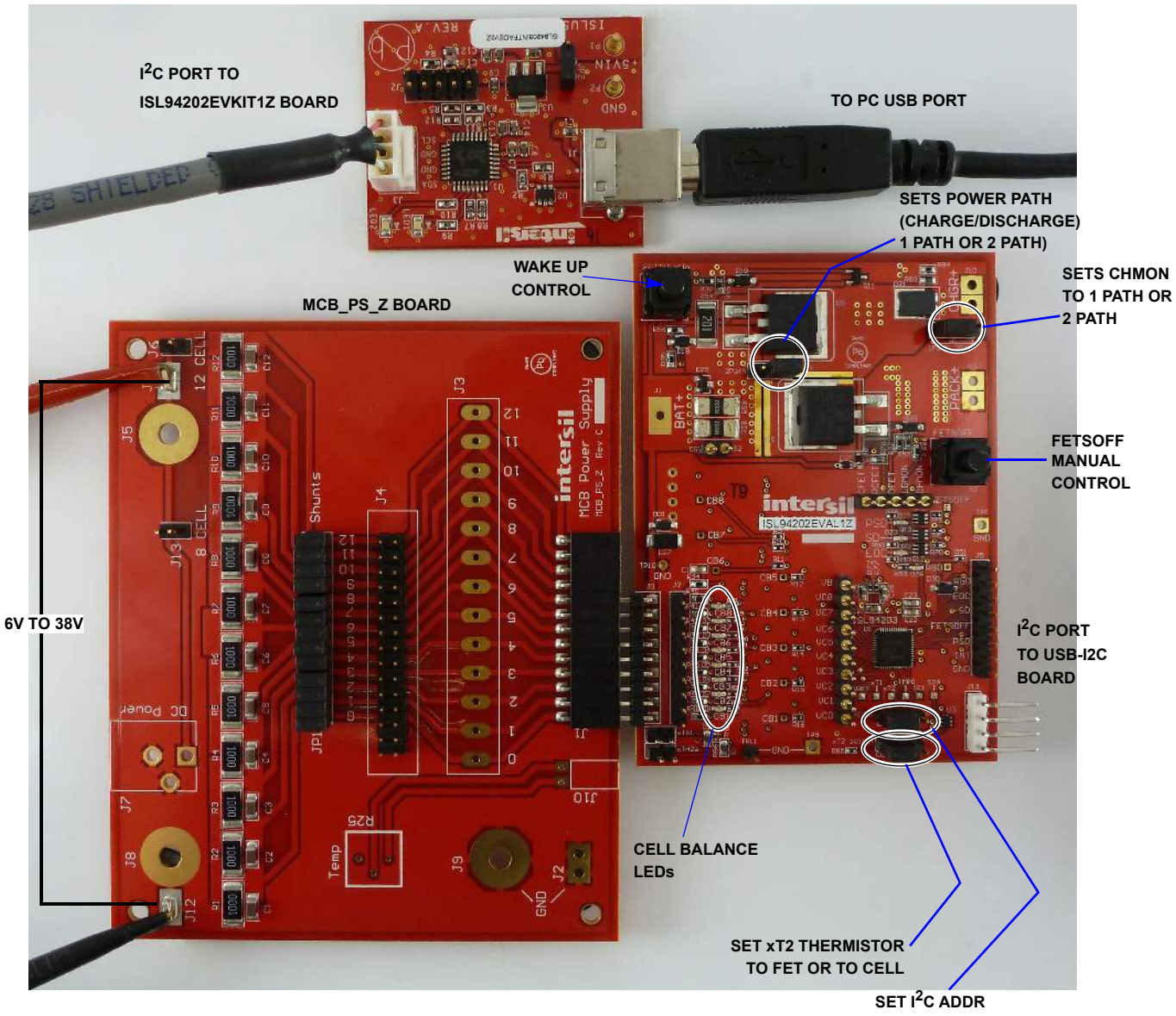


FIGURE 4. ISL94202EVKIT1Z BOARD SETUP

Quick GUI Setup Guide

Step 1: Once the board is powered up and connected to the PC through the USB cable, start the GUI program. Then click on the dropdown box.

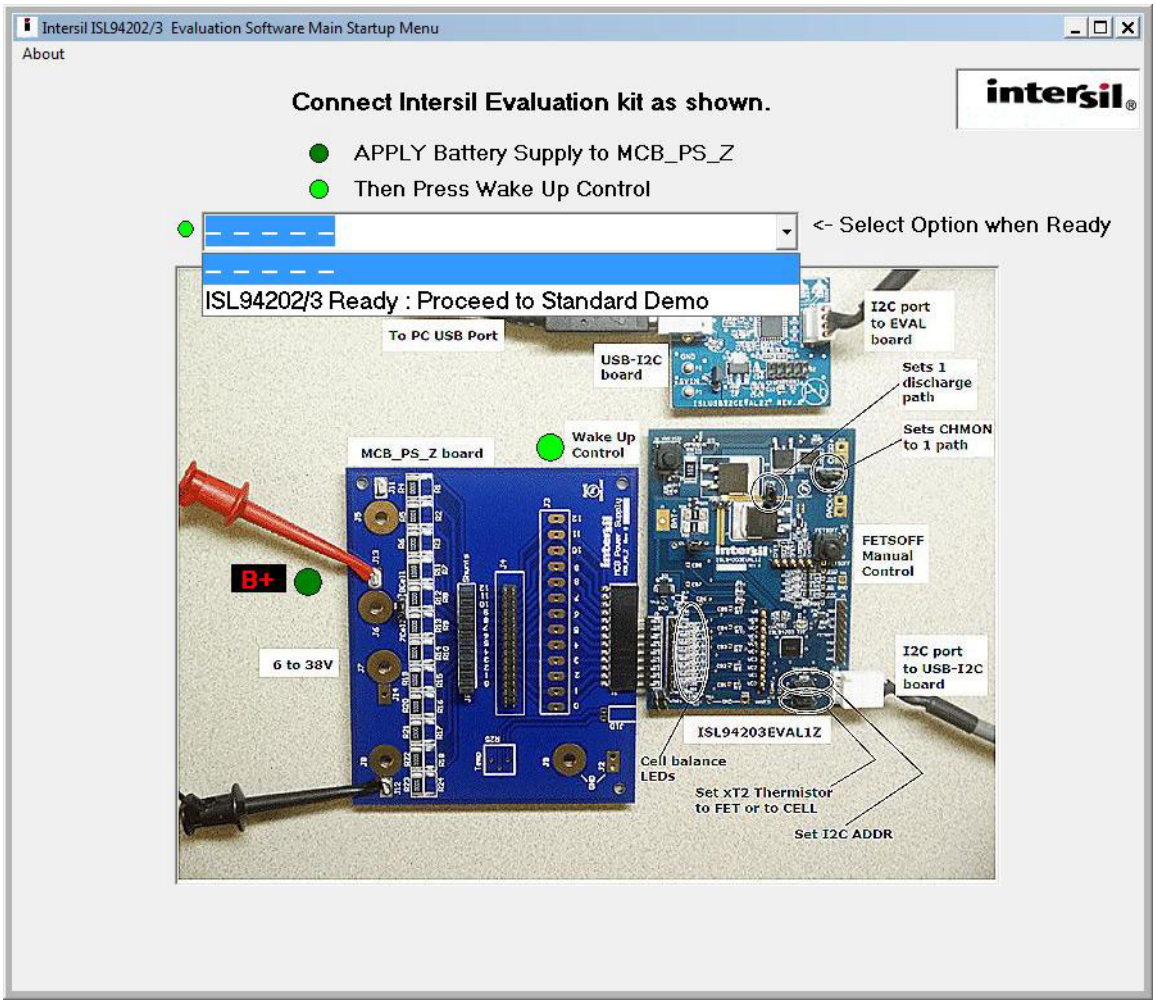


FIGURE 5. MAIN GUI START-UP WINDOW

Step 2: Click on “Read Voltages (Single).” This updates all the cell voltage, temperature and current readings, and updates the status indicators.

Step 3: Click on “Read Pack Settings.” This returns the configuration parameters set in the device.

Step 4: Review the operation of the GUI features in the following sections.

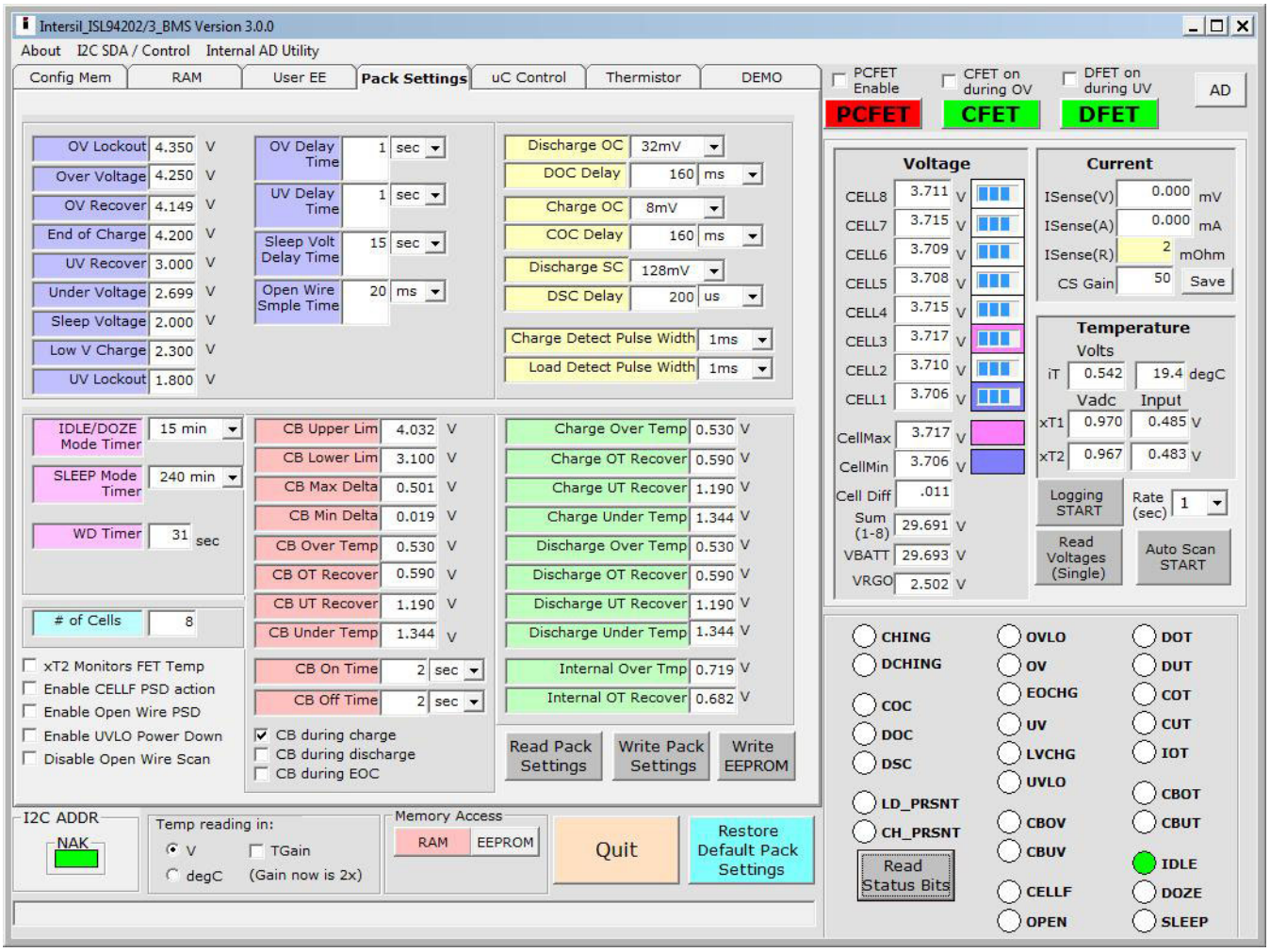


FIGURE 6. MAIN GUI WINDOW SHOWING PACK SETTINGS

Using the GUI

Common Screen

The right side of the GUI shows the status of the ISL94202. At the top are voltage, current, and temperature readings. The bottom are the status bits.

At the bottom of the screen are several controls for temperature settings and memory access.

CELL VOLTAGE SCANS

The voltage readouts (Figure 7) show the values for each cell, plus CELLMAX and CELLMIN values. The CELLMAX and CELLMIN values are returned from the ISL94202 registers. To properly implement this operation, the GUI stops the internal voltage scan of the ISL94202 (using the µCSCAN bit). It then reads the cell voltages and CELLMAX and CELLMIN values and restarts the automatic scan of the device. The values are read asynchronously, so without stopping the scan there is not sufficient time to read all the values prior to the next internal scan. For this reason the CELLMIN and CELLMAX values are often reported from a different scan than the rest of the cell voltages. Also, during the scan, the cell balance operation is stopped. So that the cell balance currents do not cause false readings of the cell voltages due to external voltage drops.

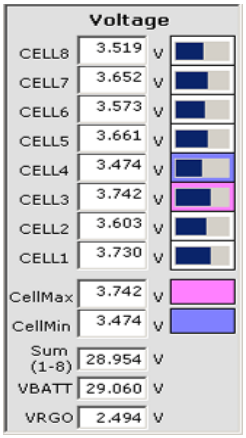


FIGURE 7. VOLTAGE READOUTS

To the right of the cell voltages, there is a graphic indication of the capacity of the cell that is based on the voltage of the cell. In this graphic depiction, the scale shows no bar when the voltage is less than or equal to the undervoltage threshold. It shows 100%, or maximum, when the cell voltage is equal to or greater than the overvoltage threshold. See the overvoltage and undervoltage thresholds in the Pack Settings tab on the left of the screen.

The GUI highlights the specific cells that equal the CELLMAX and CELLMIN voltages. This helps to identify which cells are high or low on quick inspection.

When any cell voltage is lower than the undervoltage level, or higher than the overvoltage level, the background color of that voltage readout changes to red. When the voltage rises above the UV recovery voltage or drops below the OV recovery voltage, the background color returns to white. These color changes are GUI representations of the cell voltage conditions, the actual indication from the device is shown by the UV and OV status indicators (bottom right of the screen). These indicators come directly from the device status bits.

Below the CellMIN and CellMAX readings are three boxes that show additional voltage values. The top box contains the sum of the individual cell readings. The middle box shows the voltage reading of the total battery pack as derived from an internal divide by 16 voltage divider and converted by the ADC. Comparing these two values allows a gross determination if there is a cell voltage failure.

The bottom box shows the voltage of the 2.5V regulator. The regulator voltage is internally divided by 2, then converted by the ADC and multiplied by 2 prior to display.

Pressing the “Read Voltages (Single)” button completes one read of the values in the device (see Figure 8). This includes all of the voltages and the status bits. Between presses of this button, the device continues to scan the voltage, current, and temperature values at the rate of 32ms (or 256ms if in IDLE mode, or 512ms if in DOZE mode).

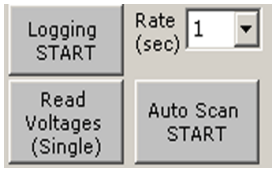


FIGURE 8. MEASURE OPTIONS

Pressing the “Auto Scan START” button starts a repetitive update of the values. The rate of update is set by the “Rate (sec)” dropdown box. As shown, the GUI updates the voltages and status every 1 second. Autoscan is stopped by pressing the autoscan “STOP” button. While the autoscan is operating, all other memory accesses are prohibited. To read the pack settings or change a register value, first stop the automatic scan.

To log the data, press “Logging START” prior to clicking on the “Auto Scan START” button. The data will be stored as a text document in a file location specified by the user. When all data has been captured, stop the auto scan and stop logging.

TEMPERATURE READINGS

To the right of the pack voltage values are the temperature readings (see Figure 9). In the default state, these boxes report the voltage on the temperature inputs. There are two boxes for each temperature.

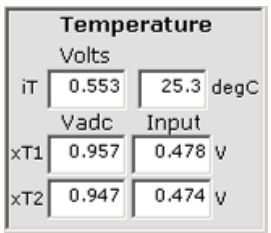


FIGURE 9. TEMPERATURE READINGS

The internal temperature reading (at the top) has two boxes. The left box shows the voltage reading from the internal temperature sensor. This voltage is dependent on the setting of the temperature gain bit (TGAIN). The temperature gain can be

changed using the GUI by clicking the “TGAIN” button in the temperature box in the bottom left of the screen (below the tabs). The box on the right shows the conversion of the internal temperature to °C. This conversion uses Equations 1 and 2:

$$TGAIN = 0 \quad \frac{intTemp(mV)}{1.8527} - 273.15 = ICTemp(°C) \qquad \text{(EQ. 1)}$$

$$TGAIN = 1 \quad \frac{intTemp(mV)}{0.92635} - 273.15 = ICTemp(°C) \qquad \text{(EQ. 2)}$$

For the external temperatures, the left box shows the digital reading from the ADC. The right box shows the applied input voltage. The value on the left is dependent on the setting of the TGAIN bit. If TGAIN = 0, then the temperature input voltage is multiplied by 2 prior to being read by the ADC. If TGAIN = 1, then the temperature input voltage is multiplied by 1. The left box of the external temperature readings simply translates the voltage readout by the ADC. The right box calculates the input voltage, based on the setting of the TGAIN bit.

The temperature readings can also be displayed in °C (see Figure 10). The conversion to °C depends on several items. First is the gain setting, so the actual input voltage is known. Second is the external resistor divider components. Third is the conversion of the thermistor value to °C.

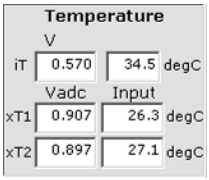


FIGURE 10. TEMPERATURE READINGS DISPLAYED IN °C

The gain setting is important only for determining the voltage applied at the input xTn pin.

Next, the conversion depends on the external resistor divider, and assumes that the external circuit is implemented as shown in the Thermistor tab drawing, Figure 11.

There is a 10k resistor parallel to the thermistor. There are two reasons for this. First, it makes the conversion curve more linear. Second, the thermistor voltage range better matches the default 2 times gain on the temperature input amplifier. The thermistors are from Murata (XH103F). If an external thermistor replaces the thermistors on the board, the conversion can be changed by changing the values in the Thermistor tab of the GUI. The values in the table are the voltages applied to the xTn input pins. The voltage depends on the resistance of the Thermistor at each temperature and the voltage on the TEMPCO pin. The TEMPCO voltage is 2.5V.

Based on calculations, the voltage/temperature curve for this circuit is shown in Figure 12 on page 9. The GUI uses the Thermistor table for this conversion and performs a linear interpolation between points.

For calculations of the external temperature, the Thermistor tab contains a value for the external divider resistor. This can be changed by the user, but not saved.

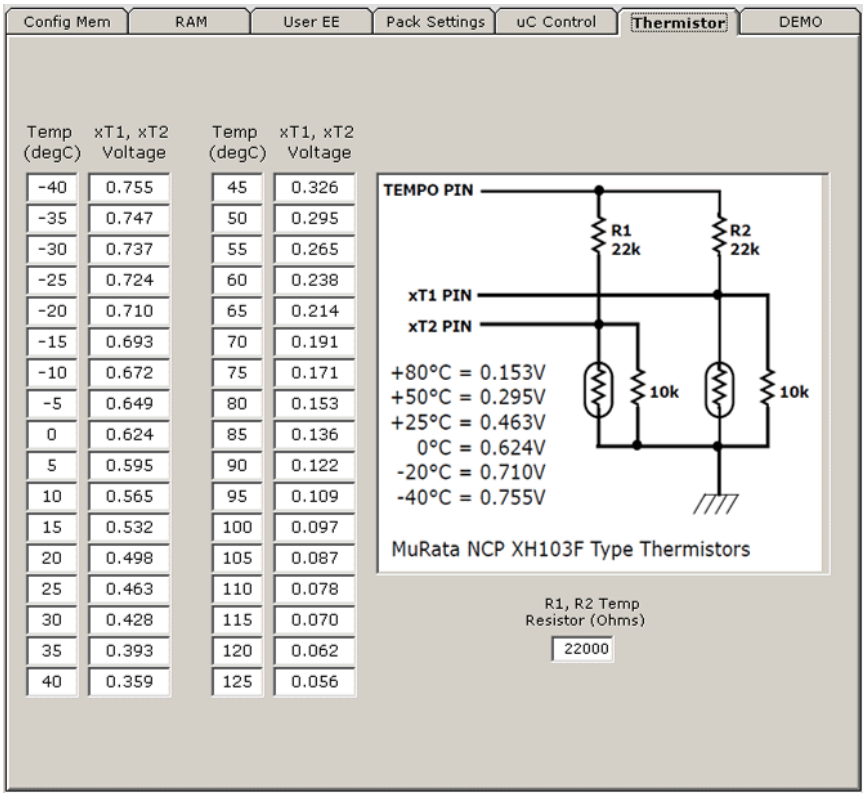


FIGURE 11. ISL94202 GUI THERMISTOR TAB

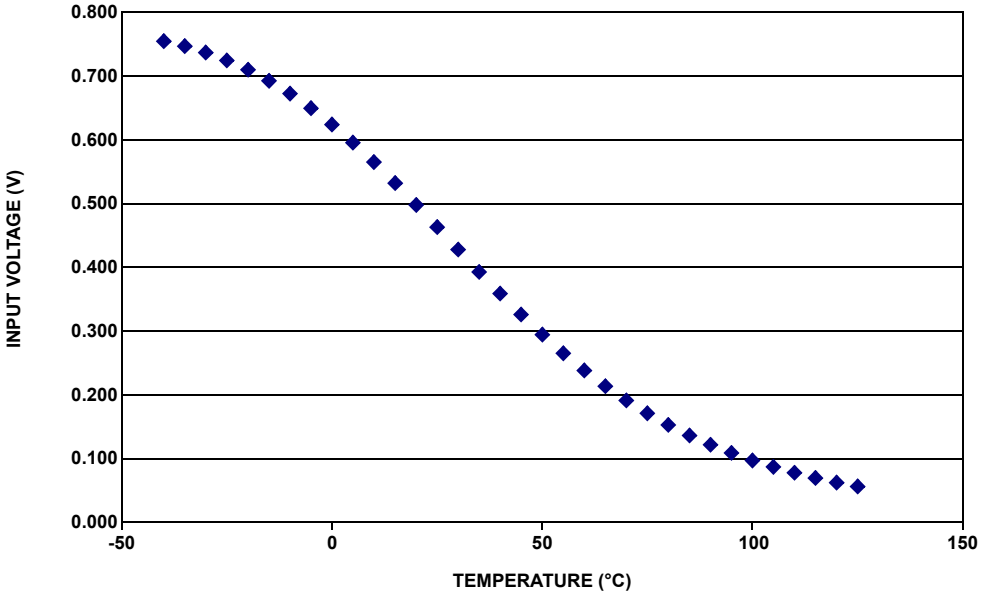


FIGURE 12. VOLTAGE TO TEMPERATURE CONVERSION

CURRENT READINGS

The current readout consists of four boxes (see Figure 13). The top box shows the voltage across the sense resistor, as reported by the device and converted to volts. The next box shows the current reading in milliamps. This value depends on the value of the current resistor, which can be entered into the third current box. The default value is 1Ω, because that is the value on the ISL94202EVKIT1Z board. If the resistor value changes, then this value can be changed in the GUI (but the default cannot be changed in this revision of the GUI). The bottom box simply relates the current amplifier gain setting in the device. In automatic scans, there is an automatic gain control. The gain setting is most useful when forcing a current read by the GUI.

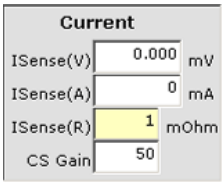


FIGURE 13. CURRENT READOUT

STATUS BITS

The status indicators on the lower right of the GUI screen (see Figure 14) reflect the status of the bits in the device. If an indicator is red, it shows a fault or out-of-bounds condition. If an indicator is green, it is showing an operating condition, such as current direction or power mode.

The status indicators are automatically updated when doing a voltage read operation. However, refreshing only the status bits is much quicker. So, clicking the “Read Status bits” updates only the status.

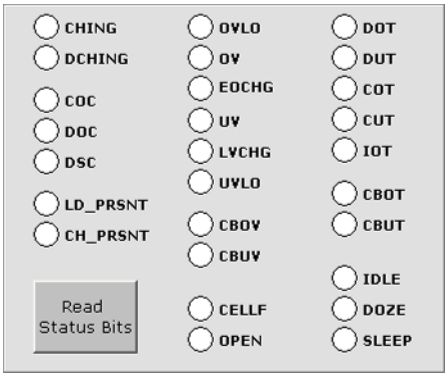


FIGURE 14. STATUS INDICATORS

FET INDICATORS

Above the voltage readings are the FET indicators (see Figure 15). These show the status of the PCFET, CFET, and DFET control bits. If the bit is “1” indicating that the FET should be on, the indicator is green. If the bit is “0” indicating that the FET should be off, then the indicator is red.

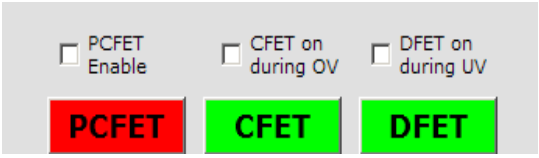


FIGURE 15. FET INDICATORS

The FET indicators are more than just readouts. Clicking on the indicators can also set or clear the bits to turn on or turn off the FETs. However, the GUI does not have control over the FETs when the device is operating in stand-alone mode. Controlling the FETs through the GUI requires that the µCFET bit is set first. This bit is set or reset using the “µC Controls FET” button in the µC Control Tab.

Above the FET control bits are some controls to change the operation of the device. These controls are “PCFET enable”, “CFET on during OV”, and “DFET on during UV”.

Setting the “PCFET enable” to active causes the PCFET to turn on, instead of the CFET, when the voltage is below the Low V Charge threshold voltage (see the Pack Settings tab).

Setting the “CFET on during OV” to active means that the charge FET will turn on when there is an overvoltage condition, if the device detects a discharge current. This reduces heat generated in the CFET during discharge, which is more important when there is a single charge/discharge path configuration.

Similarly, setting the DFET on during UV to active means that the discharge FET will turn on when there is an undervoltage condition, if the device detects a charge current. This reduces heat generated in the DFET during charge, which is more important when there is a single charge/discharge path configuration.

OTHER MAIN SCREEN CONTROLS

Communication to the device requires an I^2C bus. The I^2C bus uses a Slave byte to determine the specific device on bus that is being addressed. In the GUI, this is set by the “I^2C Addr” box (see Figure 16), which is located in the lower left of the screen. By default, the Slave Byte is 50H (0101 000x), which addresses the device having the ADDR pin pulled low. In a cascade configuration (or an application that does not need current sense or FET control, where the ADDR pin is tied high,) write the I^2C Address as 52.

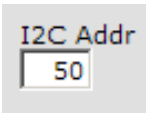


FIGURE 16. I^2C ADDRESS BOX

Temperature measurement options are selected in this box (Figure 17) below the tabs. The pack settings and temperature outputs can be shown as either volts or °C. Changing the setting initiates a voltage scan and an update of the Pack Settings. The calculations are made in the GUI as described in previous. The device simply maintains the voltage value associated with the temperature.

FIGURE 17. TEMPERATURE MEASUREMENT OPTIONS

This box also has the selection for the TGAIN bit. Clicking on the TGAIN box changes the TGAIN bit in the device, updates all of the RAM settings for temperature limits and initiates an update of the Pack Settings tab. It does not do a voltage scan. The caption shows the current status of the temperature gain. Figure 17 indicates that the temperature gain is set to 2 times.

Access to EEPROM requires an access control bit to be set prior to a read or write operation. In all of the screens where a button initiates multiple read or write operations, the memory access is automatically set to the correct access code and automatically reverts to RAM access. However, for individual memory read or write, it may be necessary to change the access code. These buttons allow this access code change. Simply click on the desired memory area button, prior to the actual read or write operation.

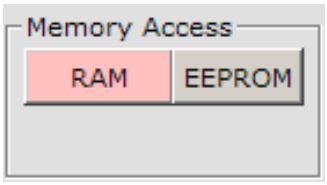


FIGURE 18. MEMORY ACCESS

The ISL94202 Internal AD Utility screen enables the user to view and record AD readings in real time. By using the I^2C interface, the GUI enables a user to select any of the internal Mux channels and view/capture the results in real time.

To bring up the AD form, click on the “Internal AD Utility” selection on the menu bar of the main form.

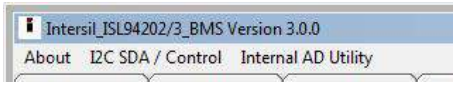


FIGURE 19. INTERNAL AD UTILITY LOCATION

When first loaded, the new form will appear as in Figure 20 on page 11.

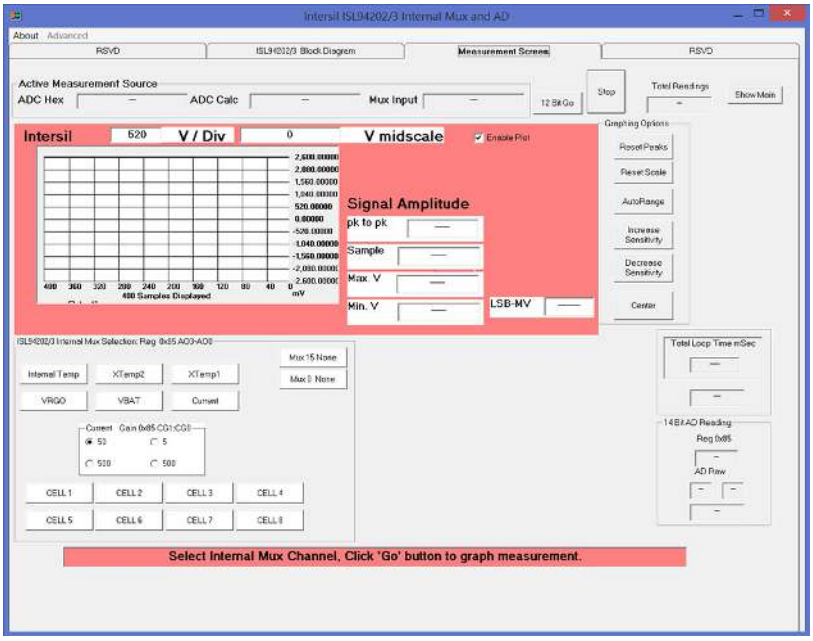


FIGURE 20. INTERNAL MUX AND AD FORM

An important first step is to select an internal Mux Channel that is going to be measured. By making a selection (clicking on a Mux selection button, see Figure 21), data collection/graphing will automatically start and after a few seconds, “Auto Range” will take place.

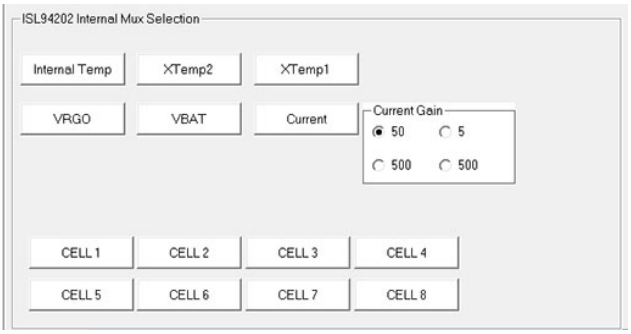


FIGURE 21. MUX SELECTION BUTTONS

Essentially, clicking in the frame selection selects the value written to register 0x85. The user can consult the datasheet for specifics related to each Mux Input connection.

BIT/ ADDR	7	6	5	4	3	2	1	0
85 (R/$\overline{W}$)	Analog MUX control bits Voltage monitored by ADC when microcontroller overrides the internal scan operation.							
	Current Gain Setting Current gain set when current is monitored by ADC. Only used when microcontroller overrides the internal scan.							
	ADC Conversion Start							
	Reserved	ADCSTRT	CG1	CG0	AO3	AO2	AO1	AO0
		Ext µC sets this bit to 1 to start a conversion	**CG1 0 Gain** 0 0 x50 0 1 x5 1 0 x500 1 1 x500		**AO3 2 1 0** 0 0 0 0 OFF 0 0 0 1 VC1 0 0 1 0 VC2 0 0 1 1 VC3 0 1 0 0 VC4 0 1 0 1 VC5 0 1 1 0 VC6 0 1 1 1 VC7		**AO3 2 1 0** 1 0 0 0 VC8 1 0 0 1 Pack current 1 0 1 0 VBAT/16 1 0 1 1 RGO/2 1 1 0 0 xT1 1 1 0 1 xT2 1 1 1 0 iT 1 1 1 1 OFF	

FIGURE 22. REGISTER 0x85

A real-time display of the register contents is displayed in Figure 23.

FIGURE 23. REGISTER CONTENT

Therefore, this selection programs the “MUX” blocks connected to the input of the internal AD.

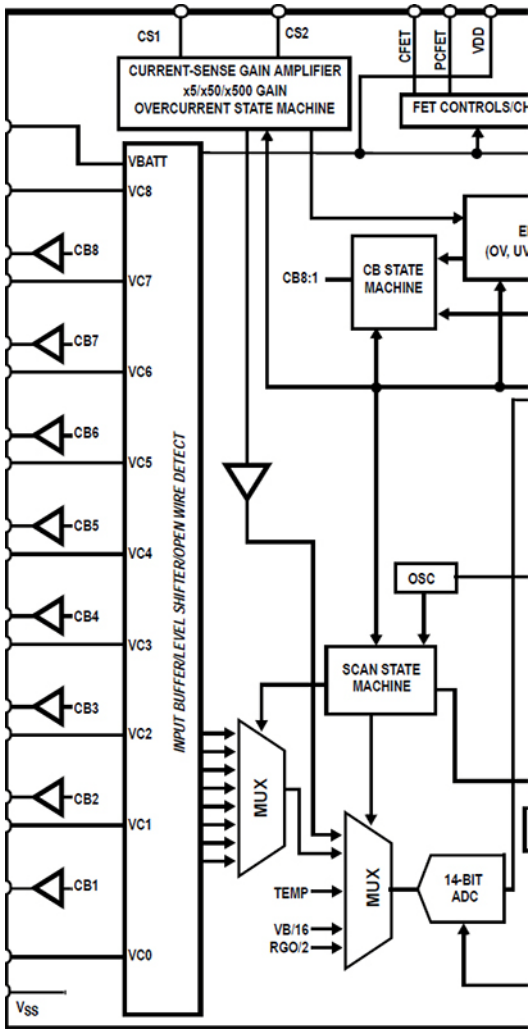


FIGURE 24. ANALOG MUX

MAIN AD FORM TOOLS

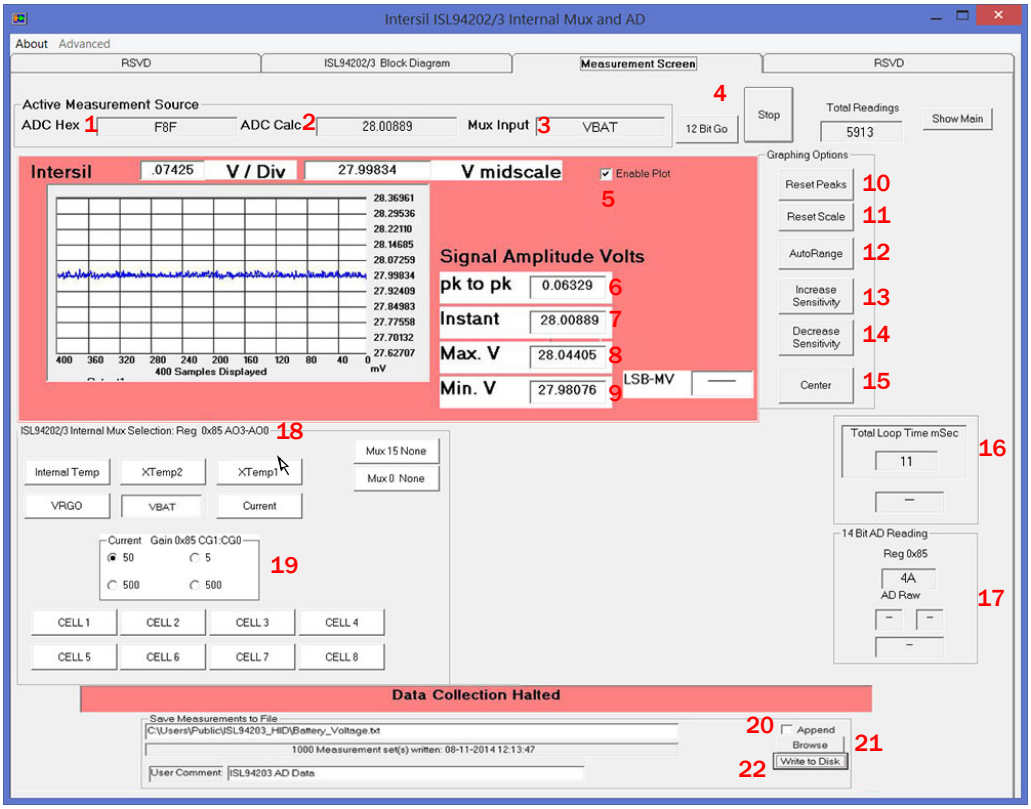
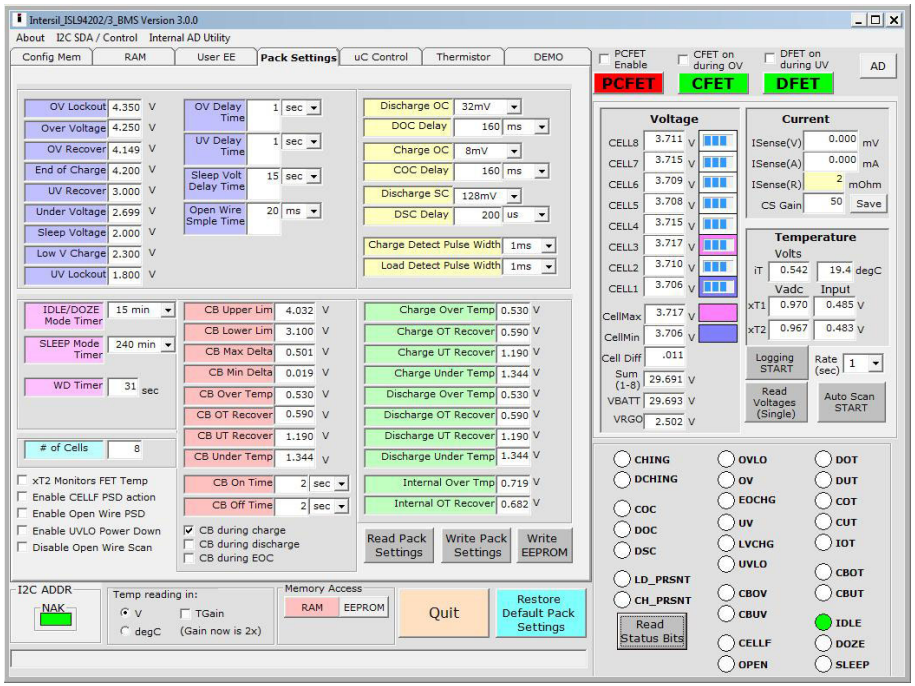
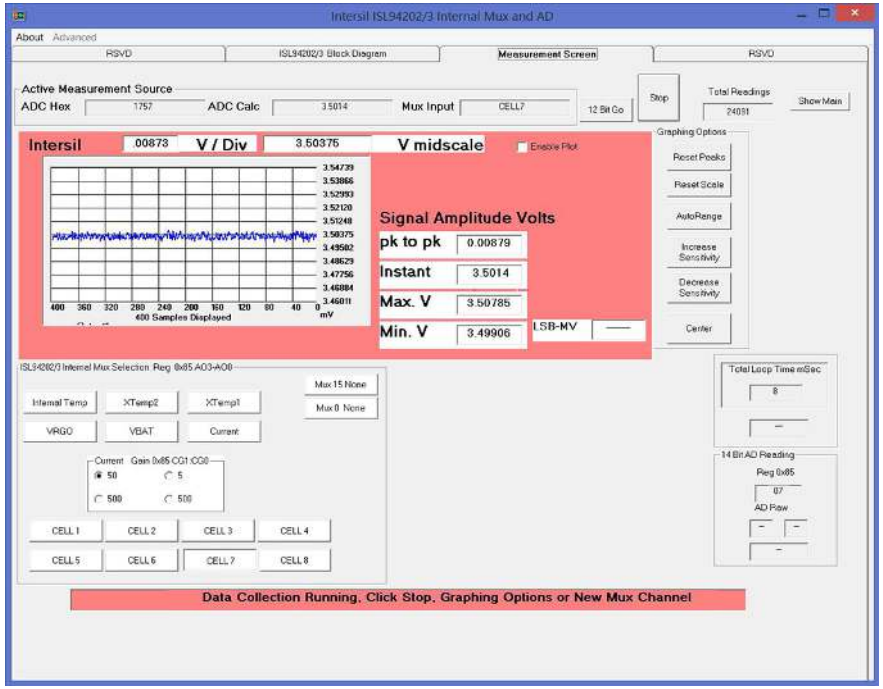


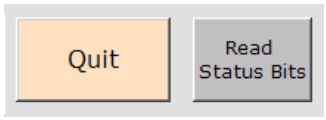
FIGURE 25. MEASUREMENT SCREEN

1. Actual Dual Byte Hex value of AD reading
2. Calculated value based on channel selected
3. Active channel being measured
4. GO Starts and STOP ends data collection. Click “Stop” to save collected readings to file.
5. Enable Plot, speeds up data collection by disabling real-time graphing
6. Highest reading – lowest reading
7. Display of most recent reading
8. Peak/Maximum value recorded
9. Minimum value recorded
10. Clears items 6, 8, 9
11. Resets graphing scale to max default
12. Recalculate Maximum and Minimum values of graphing area
13. Decreases volts per division (visual only does not affect collected readings)
14. Increase voltages per division (visual only does not affect collected readings)
15. Recenters midrange scale and moves graphing range
16. Actual time in milliseconds to capture and graph a measurement
17. Hex value of Mux control register
18. Internal Mux selection
19. PGA gain selected when making a current measurement
20. Checking will append latest collection of readings to a file
21. Browse to directory location where captured readings will be saved
22. Perform actual write operation

The Internal AD Utility form is a separated form that can be closed or minimized independent of the main screen (see Figure 26 on page 14).







To quit the program, click on "Quit".

FIGURE 26. INTERNAL AD UTILITY

Tab Controls

ISL94202 Memory Access

RAM

The ISL94202 has two main memory areas, RAM and Configuration Memory. The RAM area contains the transient values, such as cell voltages, status bits, and microcontroller override conditions. The RAM registers relate to the part of the GUI already described, and the GUI reads and writes these registers as needed. The user also has direct access to the RAM memory through the RAM tab. See Figure 27.

To update the values in the GUI with the values in the ISL94202, press the “Read All RAM” button. The display now shows the hex values of the RAM registers. Alternatively, each individual location can be updated by clicking on the “R” to the right of the register location.

There are only six registers that can be changed by the user. These are addresses 84H to 89H. These locations have a “W” next to the register. To change the register contents, write a new hex value in the desired location and press the “W” button (or the “Write All RAM” button). Until a write occurs, the contents of the ISL94202 RAM are not changed.

As shown in Figure 27, hovering the mouse pointer over the address of a register returns a description of the register. Also, the registers are color coded to match the datasheet and to group like registers. For example, in Figure 27, registers 80H to 84H are cyan color. These are the status registers. Also, registers 8EH through ABH are blue. These registers hold the voltage readings for the cells, current, and temperature.

When pressing the “Read All RAM” or “Write All RAM” buttons, the color of the button changes and the caption changes to “Busy”. During this time the GUI is performing the specified operation and other operations are prohibited until the read or write completes and the color and caption return to normal. This sequence occurs on all controls.

The main screen shows the “real world” contents of the ISL94202 registers, converting hex values to volts, current, or temperature and indicating individual status bits. The GUI performs this update when the “Read Voltages (Single)” or automatic scan executes. The update operation begins with a Read All RAM operation. This brings in values from the ISL94202 (see Figure 28 on page 16). The GUI then converts the hex values in RAM to the proper voltage, current, or temperature value.

The GUI controls for the writable RAM registers are located in the µC Control tab. These tab operations will be discussed in more detail in the following sections.

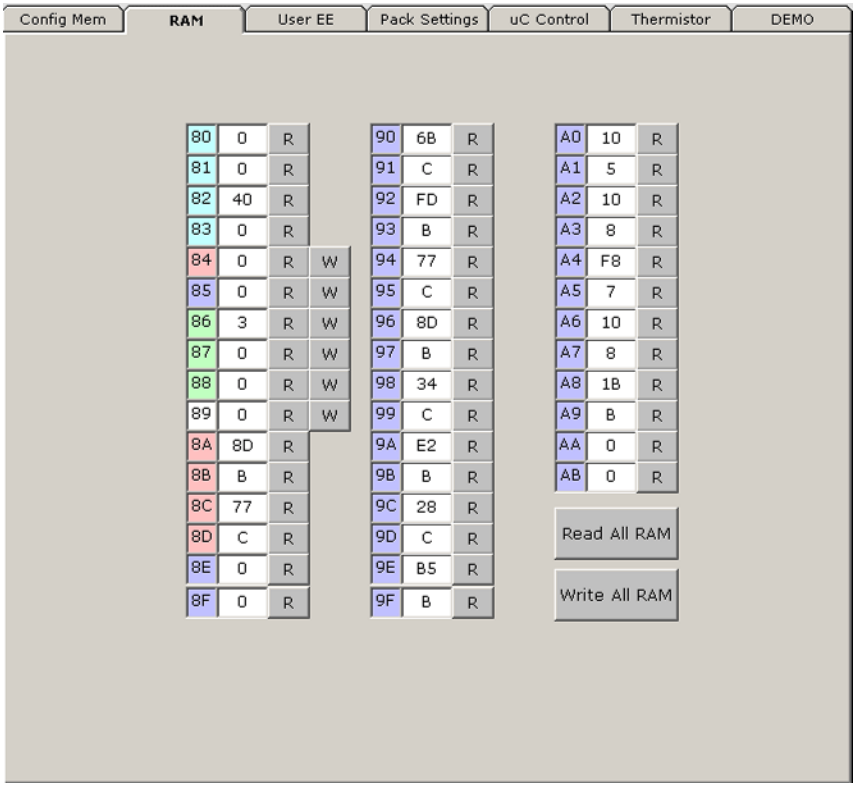
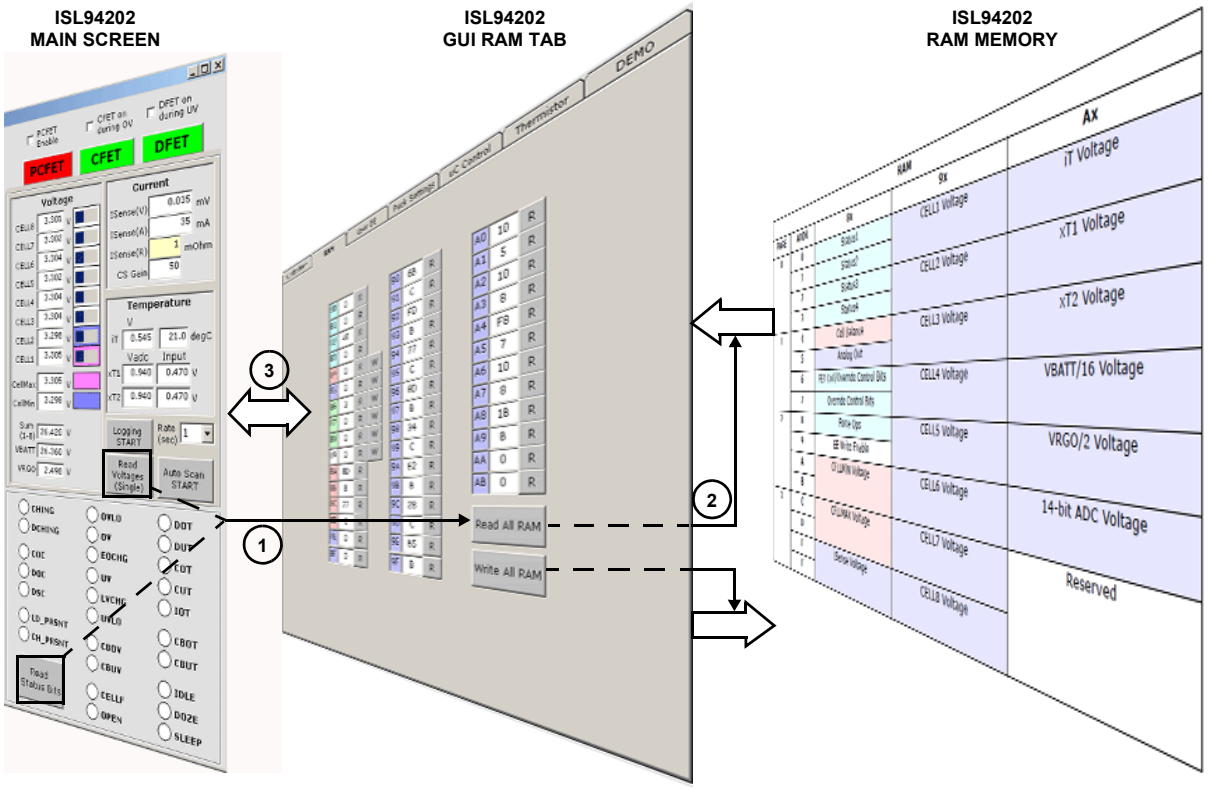


FIGURE 27. ISL94202 GUI RAM ACCESS TAB



NOTE: "Read Voltages (Single)" or "Read Status Bits" operation execution steps are numbered. "Write All RAM" writes to the ISL94202 RAM memory, then updates the Main Screen.

FIGURE 28. ISL94202 GUI RAM UPDATE OPERATION (READ OPERATION NUMBERED)

CONFIGURATION MEMORY

The Configuration Memory consists of two parts, the EEPROM cells and Configuration RAM. On power-up, the contents of the EEPROM is copied to the Configuration RAM. The device operates out of Configuration RAM.

Reading and writing the EEPROM does not automatically go through the Configuration RAM. Writes made to the EEPROM locations will go into effect when the device power cycles or when the EEPROM contents are read from the EEPROM and rewritten to the Configuration RAM.

In the normal course of developing an application, a change is made to the Configuration RAM, which changes the operation of the device. For example, changing the overvoltage setting in the Configuration RAM changes the voltage at which the device detects a fault condition. However, the value has not yet changed in the EEPROM, so a power cycle returns the old OV threshold. To make the value permanent requires that the value also be written to the EEPROM.

The EEPROM tab (see Figure 29) of the GUI shows only one set of registers. This could be the values read from the Configuration RAM or from the EEPROM. Which values it displays is dependent on the access code. The access code is set in Register 89H, but the GUI automatically sets this bit when the “Read EEPROM” or “Write EEPROM” buttons are pressed. The Access code is also settable by clicking the Memory Access button as described previously.

To write to individual bytes of the RAM part of the Configuration Memory, set the “RAM Access” in the Memory access box. Each byte in RAM can be written separately.

Writing to individual bytes to the EEPROM part of the Configuration Memory is limited. Each EEPROM write needs to write all four bytes on a page. For this reason, the GUI has a different (larger) button for writing to EEPROM. As previously mentioned, in order to write to a page of EEPROM, it is necessary to set the “EEPROM Access” in the Memory access box prior to the write.

As with the RAM tab, hovering over an address box brings up a dialog showing a simple description of the register contents. Also, the various registers are color coded as shown in the datasheet and are grouped by function.

The EEPROM tab has three other buttons. The first is a “Load Factory Default” button, which fills the GUI EEPROM locations with the factory default values (as defined at the time of the GUI release) and lets the user recover to a known good operating point. Again, use of this button simply fills the GUI registers. To change the operation of the device or the contents of the EEPROM requires a separate write for each memory location.

The other two buttons are “Save User Default to File” and “Load User Default from File.” These commands allow the user Configuration Memory to be saved and recalled. The values saved are locations 0H through 4BH.

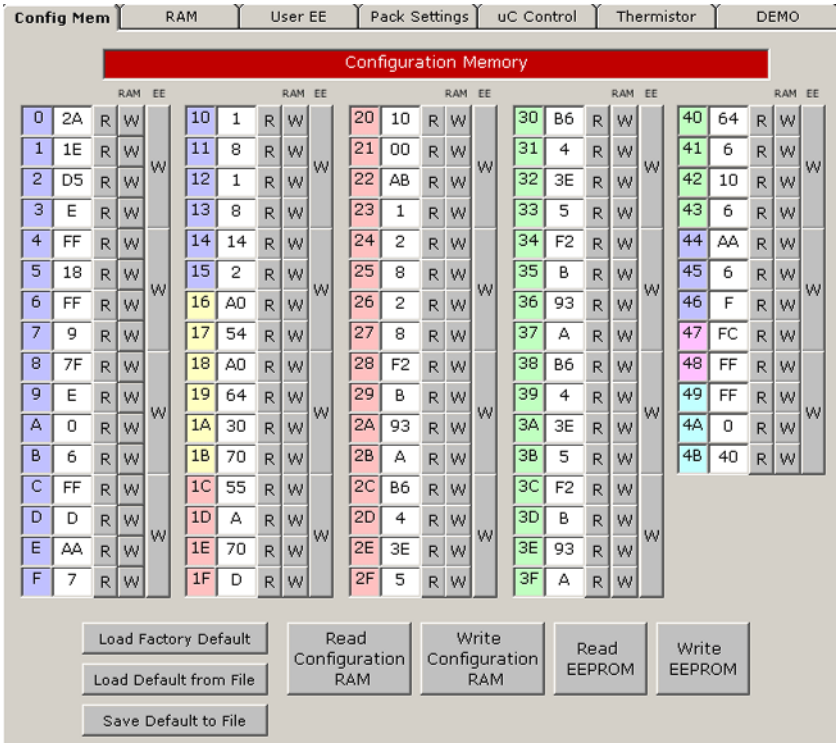


FIGURE 29. ISL94202 GUI - EEPROM ACCESS TAB

USER MEMORY

The user memory area is different from the Configuration memory. The user memory does not have a RAM component, so all reads and writes are to the EEPROM only. Also, the device ships with the user memory cleared. So, an initial read from user memory reads 0.

Using the Load User Factory Default tells the GUI to put the software revision number in the GUI locations for the user memory. The user can keep these values or load other data in the GUI boxes. To write the data to the ISL94202 User EEPROM requires individual writes (click the “EEPROM Memory Access” first) or a write all, using the “Write User EE” button (this automatically sets the EEPROM Access bit).

The User EE tab also includes a Load Default from File and a Save User Default to File. These buttons load and save User EE data at addresses 50H to 57H only.

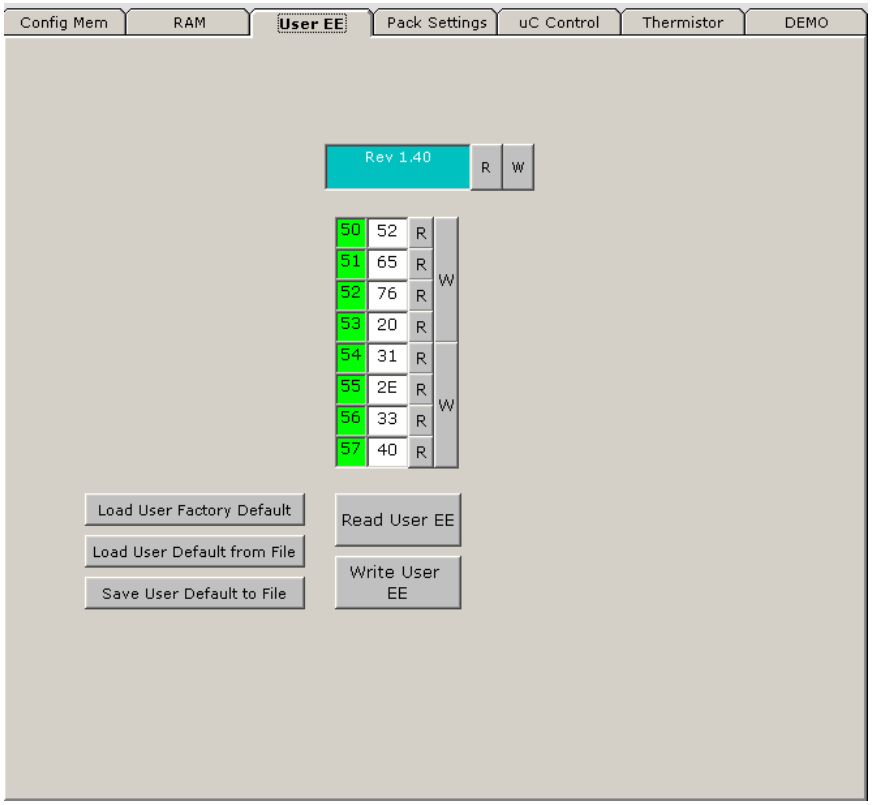


FIGURE 30. ISL94202 GUI - USER EEPROM TAB

PACK SETTINGS TAB

The Pack Settings tab (see Figure 31) provides access to the contents of the Configuration RAM, but with “real world” values. This provides an easier way to program the operation of the pack and to monitor the present settings. Values in the Pack Settings tab are saved in the GUI. When a “Read Pack Settings” button is pressed, the value is read from the device and loaded into the Configuration RAM tab of the GUI. The GUI then takes the contents of the Configuration RAM, calculates the real world value, and writes it to the Pack Settings tab.

When a value is changed in the Pack Settings tab, nothing happens until a “Write Pack Settings” button is pressed. The GUI then takes the value in the Pack Settings tab, converts the value to hex, and writes the new value to the Configuration RAM tab in the GUI. These values are then written from the GUI to the RAM part of the device Configuration memory. If a value is changed in the GUI, but no write button is pressed, then the device is not updated with the new value.

As soon as the Write Pack operation completes, the ISL94202 begins operating with the new parameters.

The Pack Settings tab also includes a “Write EEPROM” button. This is a convenience, since it does the same function as the button in the EEPROM Tab. However, in the Pack Settings tab, it is necessary to do a “Write Pack Settings” operation prior to doing the “Write EEPROM”. Otherwise, the EEPROM would not get the latest values from the Configuration Memory RAM to write to EEPROM. This is because the “Write EEPROM” writes values from the GUI Config Mem tab to the device and the values in the GUI Config Mem tab are not updated until execution of the “Write Pack Settings” operation.

Figure 32 on page 20 shows a graphical representation of the operation of the Pack Settings tab operation, the GUI EEPROM tab and the ISL94202 internal registers.

The memory operations of the Pack Settings tab was previously described. The next section covers some additional details about the calculations and use of the values shown in the Pack Settings tab.

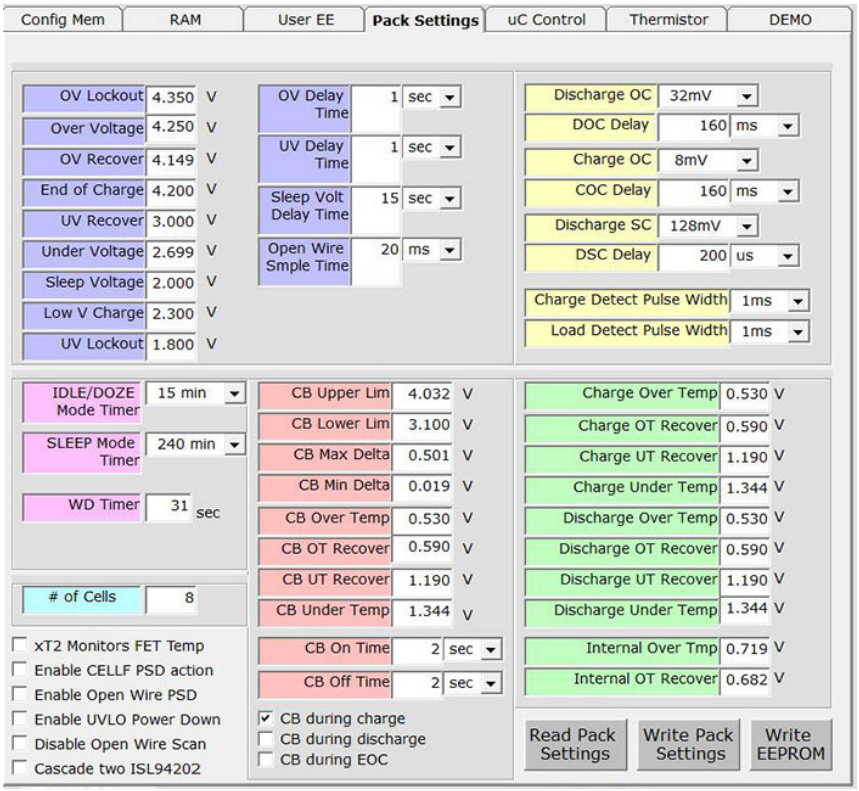


FIGURE 31. ISL94202 GUI - PACK SETTINGS TAB

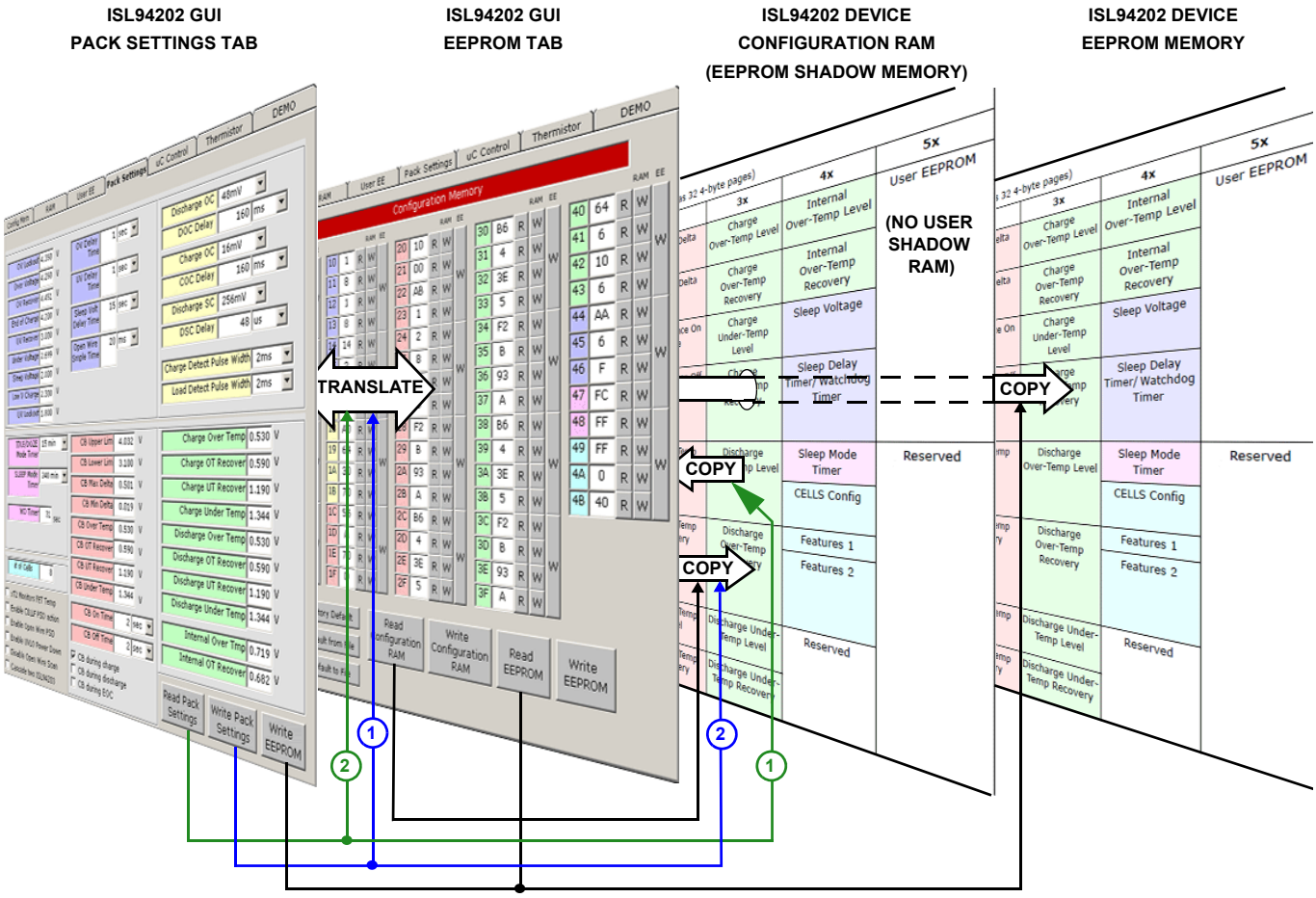


FIGURE 32. ISL94202 GUI PACK SETTINGS TAB MEMORY OPERATIONS

VOLTAGE LIMITS

The upper left section of the Pack Settings tab contains the voltage thresholds and delay times (see Figure 33). The voltages can be set from 0V to 4.8V. A negative number loads 0 and a value greater than 4.8V loads 4.8V. The timer values for OV Delay, UV Delay, and Open Wire Sample Time can be between 0 and 1023. The timer value for Sleep Voltage Delay time can be between 0 and 512.

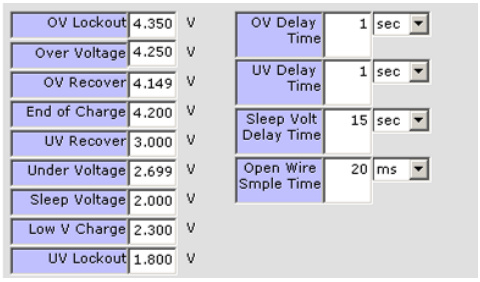


FIGURE 33. VOLTAGE THRESHOLDS AND DELAY TIMES

Normally, the OV Lockout threshold is greater than the Overvoltage threshold and the UV Lockout threshold is lower than the Undervoltage threshold. The reason for this is based on the definition of the values. Reaching the overvoltage and undervoltage thresholds causes the respective power FETs to turn off, but the pack continues to operate normally. However, if the voltage of any cell reaches the UVLO or OVLO thresholds, then something is very wrong with the pack or the charger. Reaching the OVLO threshold causes the device to set a pack shutdown (PSD) bit. This can be used to blow a fuse to disable the pack. Reaching the UVLO threshold indicates that one or more cells are much below their lower limit, so the device powers down to remove as much load as possible from the cells.

The End-of-Charge threshold is usually lower than the overvoltage threshold. When a cell reaches the overvoltage threshold, the end-of-charge output (EOC pin) can turn off the charger. If the voltage continues to rise, then there is something wrong with the charger, so the overvoltage indication turns off the charger current from within the pack.

Alternatively, the EOC limit can be used for cell balancing to specify a level where balancing is to begin. In this case, when any cell reaches the End-of-Charge threshold, all cells that are higher than *CELLMIN + CB MIN Delta* start to balance. Balancing continues until all cells are below the EOC Threshold -117mV.

The sleep voltage, along with the sleep voltage timer determine if the cells drop below a sleep threshold. If so, the power FETs turn off and the device enters a sleep mode. The device wakes from a sleep mode by the connection of a load or a charger to the pack.

The “Low V Charge” threshold is used when the Precharge FET is enabled. The low voltage charge threshold is the level where the charge FET turns on instead of the precharge FET. When the cell voltages are below the Low V charge level, the precharge FET is on. When the cell voltages are greater than the Low V charge level, then the charge FET is on.

CURRENT LIMITS

To the right of the voltage settings are the current limits for discharge overcurrent, charge overcurrent, and discharge short-circuit events (see Figure 34). The delay time values can be 0 to 1023 microseconds, milliseconds, seconds or minutes. Care should be taken when setting the range of these timers. The threshold levels are selected via drop down boxes and set the overcurrent level by setting the voltage expected across the sense resistor.

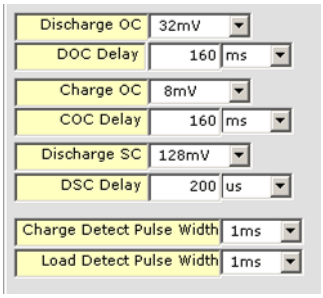


FIGURE 34. CURRENT LIMITS

Also in this selection is the setting for the duration of the charge and load pulse widths. When the power FETs turn off in response to an overcurrent event, the ISL94202 starts looking for the release of the load or charger. It does this by periodically sourcing or sinking a current to the load or from the charger. The duration of the pulse width might need to be changed, depending on the load or charger capacitance, since the detection circuit is attempting to pull the voltage at the terminals to some intermediate state. If the load or charger is off, but there is a large capacitance still connected to the terminals, a short pulse width will take longer to detect the removal. The ISL94202 allows detection pulse widths from 1ms to 16ms.

TIMERS

Below the voltage settings are some timer controls. The upper box specifies the amount of time the device spends in normal mode (with no measured current) before entering into IDLE as well as the time the device spends in IDLE before entering the DOZE mode. The Sleep mode timer specifies how long the device remains in DOZE mode (with no measured current) before going to sleep. Detection of any current returns the part to the normal operating mode.

FIGURE 35. TIMER CONTROLS

The WD Timer setting is used with µC override operations. When the µC sets any condition that overrides internal operation, the WD timer starts. The WDT is reset by any valid reception of an I^2C slave byte. If there are no valid communications before the WDT times out, then the ISL94202 turns off all FETs and waits for a valid command.

NUMBER OF CELLS

The "# of Cells" box (Figure 36) specifies the number of cells connected to the pack. The number in the box can be lower than the number of cells connected to the pack. This value is a direct representation of the number of cells, it is not the value stored in memory. The GUI translates the number of cells value to the proper code for the device, as specified in Table 1.

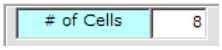


FIGURE 36. NUMBER OF CELLS BOX

When the board first powers up, the "# of Cells" is set to 3. This causes some of the cells to show 0V in a Voltage Scan. This is because the cells are skipped in the scan. If there are more cells connected, change the setting, write the values to the pack, then write the values to EEPROM.

The reason for the default value of 3 in the "# of Cells" box is that, if the number in the box is greater than the number of cells connected to the pack, when the ISL94202 first powers up it reads a cell input as 0V. The ISL94202 thinks that this is a cell failure, so does not complete its power up sequence. This is part of the protection mechanisms of the part. If the value written to the EEPROM is higher than the number of cells connected and the device powers down, then it will not power up properly. It will be necessary to connect the programmed number of cells (or more) so the device powers up. Then the EEPROM value can be reset.

For the proper connections of fewer than eight cells, see Table 1. When using the evaluation board with fewer than eight cells, connect the unused cell inputs at the board connection. It is not necessary to remove any components on the board (see Figure 57 on page 33).

TABLE 1. ISL94202 CELL CONFIGURATION

CELLS VALUE	NUMBER OF CELLS
10000011	3 Cells connected, C1, C2, C8
11000011	4 Cells connected, C1, C2, C7, C8
11000111	5 Cells connected, C1, C2, C3, C7, C8
11100111	6 Cells connected, C1, C2, C3, C6, C7, C8
11101111	7 Cells connected, C1, C2, C3, C4, C6, C7, C8
11111111	8 Cells connected, All cells connected

NOTE: Only these combinations are acceptable. Any other combination will prevent any FET from turning on.

CELL BALANCE LIMITS

Figure 37 contains the settings for cell balancing, which is the next box to the right. The voltage limits that can be set in the GUI are fixed at 0 and 4.8V. There are no limits to the temperature settings. The temperature values are limited by the GUI from 0 to 1.8V (voltage setting) or -40°C to +125°C (temperature setting).

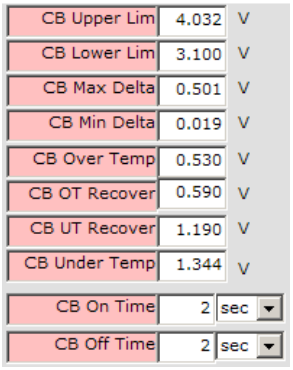


FIGURE 37. CELL BALANCING LIMITS

The CB lower limit and CB upper limit define the boundaries of the cell voltage operation (except in EOC balancing). If ALL cell voltages exceed the limits, then balancing stops. Balancing starts again when ALL cell voltages drop back within the specified limits plus a hysteresis. For example, if the CB upper limit is set to 4.0V, then balancing stops when all cell voltages exceed 4.0V. Balancing resumes when all cell voltages drop below 3.883V.

CB Max Delta specifies the maximum difference between the CELLMAX and CELLMIN values. When this happens, it implies that there is something wrong with the cells or connections. When cell voltages exceed the CB Max Delta limits, the CELLF flag is set. This can cause the PSD pin to active (optional), which can shut down the pack. The CELLF indication also starts the open wire detection operation.

The CB over- and under-temperature settings specify the temperature range over which the cell balance operates. If the external temperature sensors show that the temperature is out of bounds, then cell balance stops.

The CBON and CBOFF times specify how long the cell balance is on and off. These timers are mainly used for thermal control to manage the heat dissipated by the cell balance resistors.

TEMPERATURE LIMITS

On the lower right of the Pack Settings tab are the pack temperature limit settings. There are temperature limits for charge and discharge as well as temperature recovery levels for each limit. These limits refer to the ADC converted value of the temperature sensor inputs, so they are affected by the TGAIN bit. The GUI limits values in these locations from 0 to 1.8V (voltage setting) or -40°C to +125°C (temperature setting).

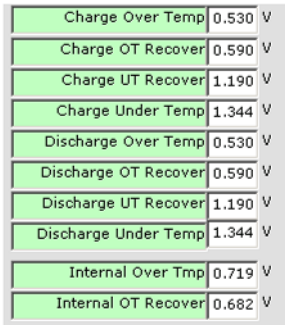


FIGURE 38. PACK TEMPERATURE LIMIT SETTINGS

When the TGAIN bit changes from “0” to “1” or “1” to “0”, the GUI rewrites the values of the temperature limits in the EEPROM tab (based on the temperature input amplifier gain) and sends these new values to the ISL94202. The GUI also updates the Pack Settings Information. The Pack Settings tab temperature limits do not change if they are shown in °C, but the value in the device does change. This is because the calculations for the temperature settings in °C includes the setting of the TGAIN bit.

PACK OPTIONS

In the lower left of the Pack Setting tab are various option controls (see Figure 39).

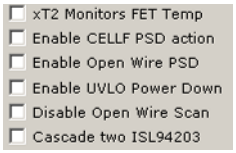


FIGURE 39. OPTION CONTROLS

Setting the “xT2 Monitors FET Temp” to “1” tells the device to treat the xT2 input as a FET temperature, not a cell temperature. With this bit set, an over-temperature on the xT2 input does not stop cell balancing, it only turns off the power FET.

- The “Enable CELLF PSD action”, when set to “1”, causes the PSD bit to be set when the device detects a condition that sets the CELLF bit.
- The “Enable Open Wire PSD” bit, when set to “1”, causes the PSD bit to be set when the device detects an open wire condition.
- The “Enable UVLO Power Down”, when set to “1”, causes the device to power down when it detects an undervoltage lockout condition.
- The “Disable Open Wire Scan” bit, when set to “1”, turns off the open wire scan operation.
- The “Cascade two ISL94202” bit, when set causes the device to operate in cascade mode - as determined by the ADDR input. When the ADDR input is tied to RGO, then the part thinks that it is the lower device, so it turns off the current sense circuits and does not drive the FETs. When the ADDR is tied to VSS, then it thinks it is the upper device, so it keeps the current sense circuit on and controls the power FETs. The ADDR bit also changes the I^2C slave byte address.

CELL BALANCE ENABLE

Part of the Cell balance settings are the Cell Balance controls for charge, discharge, or end-of-charge balancing (see Figure 40).

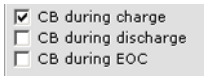


FIGURE 40. CELL BALANCE CONTROLS

- If “CB during charge” is checked, then the device activates cell balancing if charge current is detected and all other conditions are within limits. If there is no current or there is discharge current, then the device does not balance.
- If “CB during discharge” is checked, then the device activates cell balancing if discharge current is detected and all other conditions are within limits. If there is no current or there is a charge current, then the device does not balance.
- If the “CB during EOC” is checked, then the device ignores the current detection and balances only based on the end-of-charge condition (as long as all other conditions are with limits). With this option selected, cell balancing is enabled when any cell reaches the end-of-charge threshold. Balancing continues as long as any cell is greater than the EOC threshold minus 117mV.

While cell balancing is enabled, in any mode, balancing is turned on for any cell whose voltage is more than *CELLMIN + CB Min Delta* volts.

µC Control Tab

The µC Control tab provides a mechanism for the GUI to override the internal operation of the device. An external microcontroller would use similar techniques to provide different functionality to the pack than is offered by the built-in automatic operations. The options available on the µC Control tab are shown in Figure 41 on page 24.

POWER CONTROL

The mode of operation of the device is controlled by these check boxes (see Figure 42 on page 24). Clicking any box puts the device into that mode of operation. Clicking on “None” removes any forcing condition. The µC Control features does not allow the device to be placed back into normal operation. For example, once the device enters IDLE mode, it can be placed in DOZE mode, returned to IDLE mode, put to sleep, or set to power down, but it can only return to a normal scan operation if it detects current flow in the pack. The GUI also offers a demo mode that forces a current indication, so that can be used to return to normal mode.

It is not necessary to override any internal operation to change the operating mode.

INDIVIDUAL VOLTAGE MONITORING

The GUI or an external µC can force a read of any voltage available from the internal MUX. This includes cell voltages, pack current and voltage, and temperatures. It is not necessary to override any internal function to use this measurement.

To use this feature, select the voltage to be measured and click the “W” button. The “R” button reads the status of the AO3:AO0 bits, but a write operation sets the bits for the desired voltage and sets the ADCSTRT bit needed to start the internal conversion operation. The resulting voltage shows in the box at the right (see Figure 43). This is a 14-bit hex value. This value then needs to be converted to voltage, current, or temperature.

When measuring the current, the gain of the amplifier can be manually set prior to the ADC read by using the drop down box and “W” button on the top line.

The GUI allows the repetitive capture of any single voltage or all voltages. For a single voltage capture, the desired voltage is selected by the Monitor Voltage box (see Figure 44). The number of samples is specified and the “Sample Voltages” button is pressed. This brings up a dialog box asking for the file name for the data to be stored. The GUI then captures the specified number of samples and stores the data to the file. This is a tab delimited file that can be imported into Excel.

Between the Sample All Voltages and Sample Single Voltage buttons is a progress indicator showing the ongoing data capture.

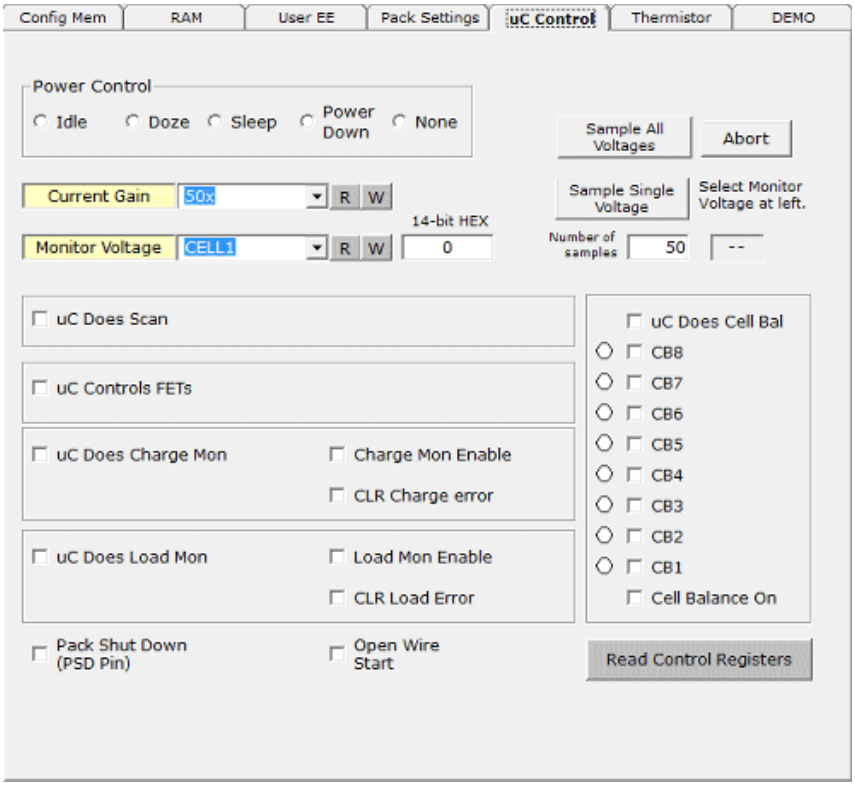


FIGURE 41. ISL94202 GUI - µC CONTROL TAB

FIGURE 42. MODE OF OPERATION

FIGURE 43. MONITOR VOLTAGE SELECTION

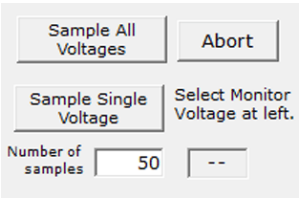


FIGURE 44. MONITOR VOLTAGE BOX

MICROCONTROLLER DOES...

The next set of controls (Figure 45) allows the GUI (or microcontroller) to take over several functions of the device. The most general is the “µC Does Scan” box. When checked, the device stops scanning the cells, which effectively stops automatic operation. When this box is checked, cell voltages are scanned by the external µC, OV, and UV voltages and must be manually compared with limits. Cell balance must be controlled externally. The only function maintained internally during a µCSCAN operation is the overcurrent/short-circuit monitoring. These continue to be automatically monitored.

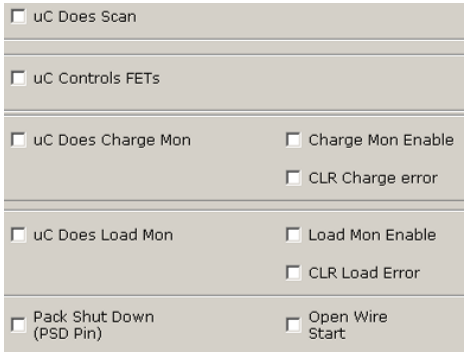


FIGURE 45. MCU CONTROL OPTIONS

The “µC Controls FETs” operation gives the GUI or external µC control over the FETs. With this box unchecked, the ISL94202 has exclusive control over the FETs. It is not possible to change the FETs from the outside. When the box is checked, the FETs are only controlled by the GUI or an external µC.

The “µC Does Charge Mon” bit overrides the internal charger monitor function. When overridden, the GUI or an external µC can turn on the charger monitor current and detection hardware by setting the “Charge Mon Enable.” The GUI or external µC then needs to monitor the CH_PRSNT bit to detect if there is a charger present. If the charger is removed following an overcurrent condition, then the GUI/µC needs to reset the charge error bit by clicking on “CLR Charge Error”.

The “µC Does Load Mon” bit overrides the internal load monitor function. When overridden, the GUI or an external µC can turn on the load monitor current and detection hardware by setting the “Load Mon Enable.” The GUI or external µC then needs to monitor the LD_PRSNT bit to detect if there is a load present. If the load is removed following an overcurrent condition, then the GUI/µC needs to reset the load error bit by clicking on “CLR Load Error”.

All of these operations start the Watchdog timer. If communications with the device stop for more than the Watchdog time-out period, then the device resets the override bits and waits for a valid communication. When a valid communication is received, the device resumes normal, default operation.

The “Pack Shut Down” control is a direct control of the PSD pin. The “Open Wire Start” is a manual open wire start operation. This open wire scan does not need to first wait for a CELLF condition.

µC CELL BALANCE

The GUI/µC can manually control the cell balance operation, overriding the internal automatic balancing. Set the “µC Does Cell Bal” bit and the “Cell Balance On” bit. Then check any, or all, of the individual cell balance bits to activate the cell balance outputs (see Figure 46).

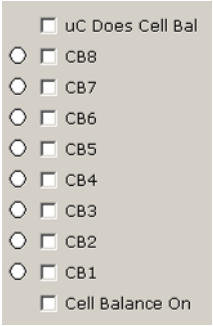


FIGURE 46. CELL BALANCE

However, before the balancing outputs turn on, all other conditions for balancing must be met. There can be no error conditions and if balancing is selected during charge, then there must be a charge current before the cell balance outputs turn on. During a µC controlled cell balance operation the CBON and CBOFF timers are not used.

Once the “µC Does Cell Bal” is set, the Watchdog timer starts and communications must happen within the watchdog time out period. If there is an interruption in the communications, then the µCCBAL bit is reset and the device waits for a valid communication. When a valid communication is received, the device resumes normal, default operation.

The indicators to the left of the control boxes indicates which cells are to be balanced. If proper balancing conditions are not met, the indicators are off. If the cells should be balancing, the indicators are on. If the LEDs on the board are not on at the same time as the indicators in the GUI, then there could be a hardware problem.

When clicking the Read Control Registers button (Figure 47), the status of all of the override bits are updated.

FIGURE 47. READ CONTROL REGISTER BUTTON

DEMO Tab

The last tab in the GUI offers some demonstration controls, see Figure 48. This allows the user to test some items without connecting a real charger or load to the system. This is useful in simulating current flow and overcurrent errors.

The controls available in this tab are test modes only. They set the various bits in the device, but do not actually create the condition. However, by setting the bits in the device, the device responds as if the condition occurred. For example, forcing the charge current direction bit forces the device back into normal operating mode and enables balancing (if balancing is enabled during charge).

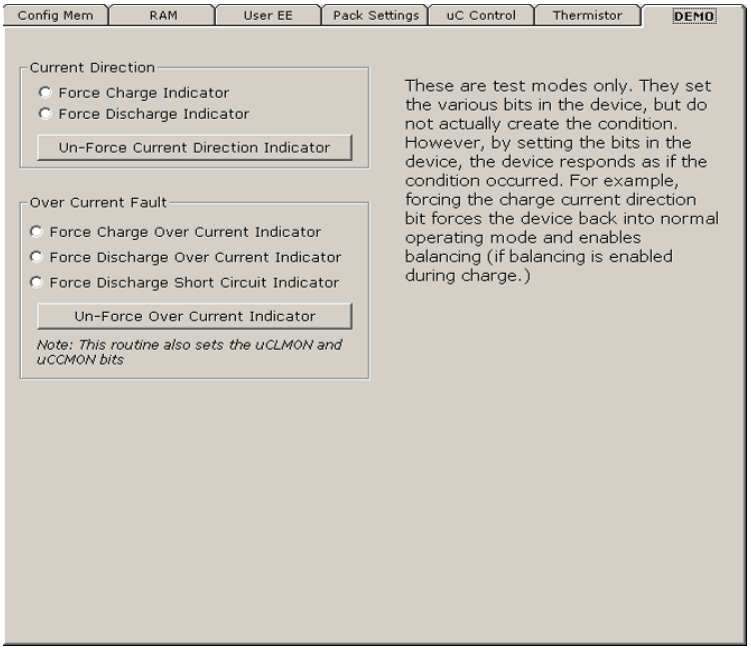


FIGURE 48. ISL94202 GUI - DEMO TAB

CURRENT DIRECTION DEMO

The “Force Charge Indicator” or “Force Discharge Indicator” controls force the device to indicate a charge or discharge condition (see Figure 49). This is not a real condition, for example, the current readout shows no current flow. However, the device responds as if there is a current.

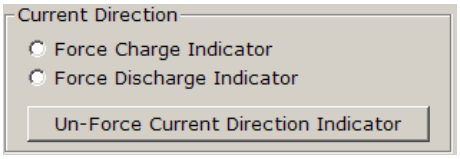


FIGURE 49. CURRENT DIRECTION

While in either of these demo modes, the device will not respond to real overcurrent or short circuit conditions.

To clear the conditions, click on the “Un-force Current Direction Indicator” button.

OVERCURRENT DEMO

To simulate any of the overcurrent or short circuit conditions, use the Overcurrent Fault demo options (see Figure 50). The “Force Charge Overcurrent Condition” sets the COC bit and the device responds as if that condition exists. In order to better view the operation, the GUI sets the µCLMON and µCCMON bits so the recovery conditions are controlled manually. Without the µCCMON and µCLMON bits set, the device will do the following:

- The test bit indicates to the device that there is an overcurrent condition.
- The device sees that there is no current, so starts the LDMON or CHMON operation.
- The device sees that there is no load and no charger, so it clears the fault condition.
- The device immediately sees the test mode fault condition, so it again responds as if there is fault.
- The device continues to “oscillate” between these modes, because the demo condition is not real.

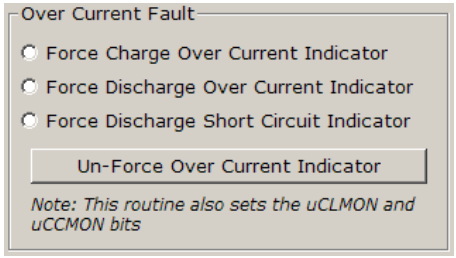


FIGURE 50. OVERCURRENT FAULT DEMO OPTIONS

To get a better understanding of the operation, connect a potentiometer to the load output. Make sure that the minimum resistance on the potentiometer is about 1kΩ. This is not so low that it is damaged when the FETs are on, but is low enough to detect a load. Now, force a discharge overcurrent condition. (Look at the SD LED on the PCB, it should be on continuously). Use the µC Control tab to clear the µC Load Monitor bit. Now, the device detects the overcurrent (from the test bit). It sees that there is no current, so it starts the load monitor. Because of the potentiometer, it sees that there is a load, so the fault condition remains in effect and the SD LED remains on. By gradually increasing the resistance on the potentiometer, the device will reach the point where the device detects that the load is removed. At this point, the SD LED will resume the “oscillations” as it detects the load clearing and sees the demo fault.

ISL94202EVKIT1Z Hardware Design

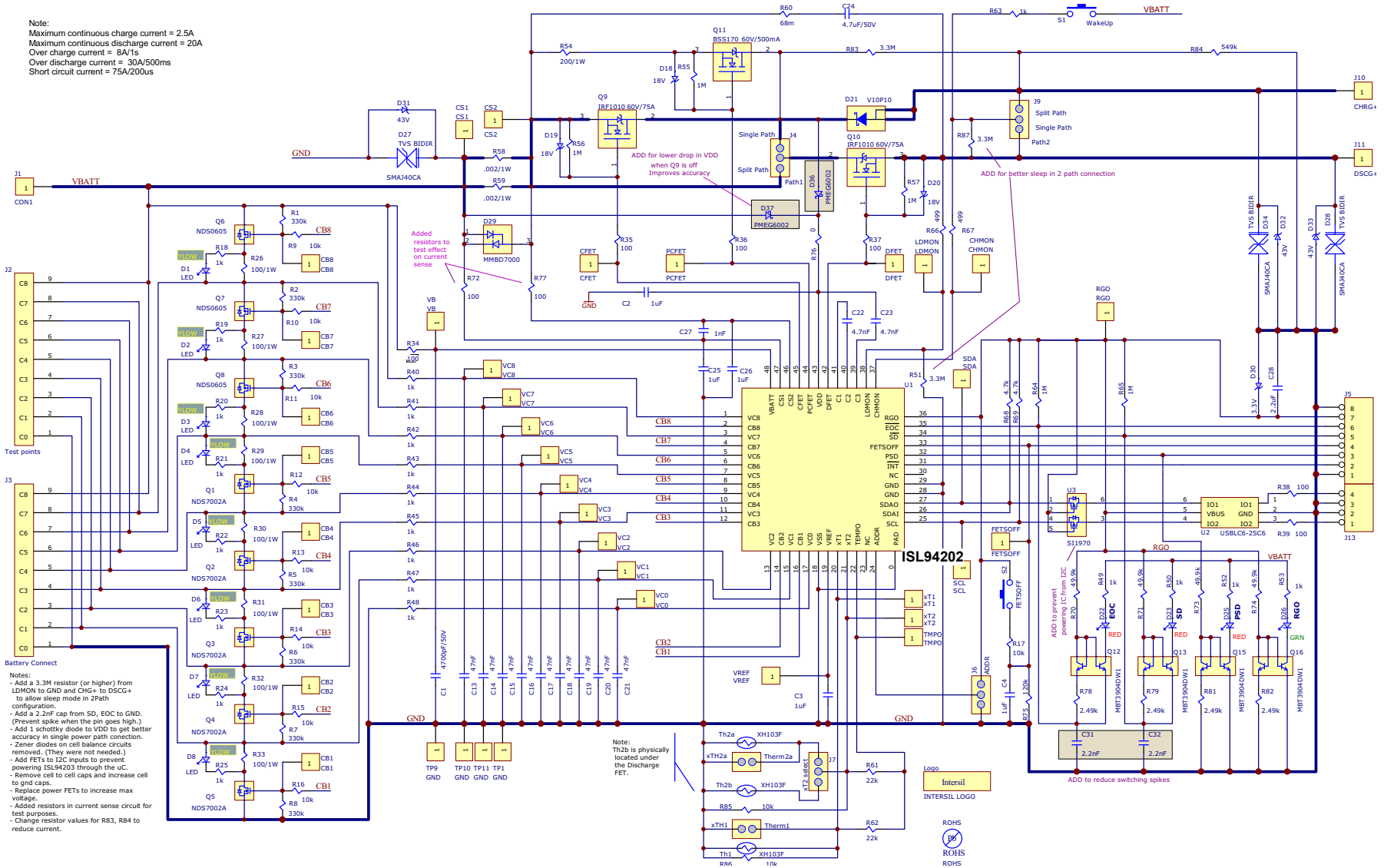


FIGURE 51. ISL94202EVKIT1Z HARDWARE DESIGN

Bill of Materials

QTY	UNIT	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	MANUFACTURER PART
9	ea.	C13-C21	CAP, SMD, 0603, 47nF, 100V, 10%, X7R, ROHS	VENKEL	C0603X7R101-473KNE
3	ea.	C2, C25, C26	CAP, SMD, 0603, 1µF, 50V, 10%, X5R, ROHS	TDK	C1608X5R1H105K
3	ea.	C1, C22, C23	CAP, SMD, 0603, 4700pF, 100V, 10%, X7R, ROHS	VENKEL	C0603X7R101-472KNE
1	ea.	C27	CAP, SMD, 0603, 1000pF, 16V, 10%, X7R, ROHS	VENKEL	C0603X7R160102KNE
1	ea.	C28	CAP, SMD, 0603, 2.2µF, 10V, 10%, X7R, ROHS	MURATA	GRM188R71A225KE15D
2	ea.	C3, C4	CAP, SMD, 0603, 1.0µF, 10V, 10%, X7R, ROHS	AVX	0603ZC105KAT2A
2	ea.	C31, C32	CAP, SMD, 0603, 2.2nF, 100V, 10%, X7R, ROHS	VENKEL	C0603X7R101-222KNE
3	ea.	D18-D20	DIODE-ZENER, SMD, 2P, SOD-123, 18V, 500mW, ROHS	DIODES INC.	MMSZ5248B-7-F-T
8	ea.	D1-D8	LED-SMART, SMD, 0603, YELLOW, 1.8V, 2mA, 587nm, 7.9mcd, ROHS	OSRAM	LY L29K-J1K2-26-Z
1	ea.	D21	DIODE-RECTIFIER, SMD, SMPC, 100V, 10A, ROHS	VISHAY	V10P10-M3/86A
3	ea.	D22-D23, D25	LED-SMART, SMD, 0603, 2P, RED, 1.8V, 2mA, 630nm, 4.5mcd, ROHS	OSRAM	LSL29K-G1J2-1-0-2-R18-Z
1	ea.	D26	LED-SMART, SMD, 0603, GREEN, 1.7V, 2mA, 570nm, 3.9mcd, ROHS	OSRAM	LGL29K-G2J1-24-Z
3	ea.	D27, D28, D34	DIODE-TVS, BIDIRECTIONAL, SMD, 2P, SMA, 40V, 400W, ROHS	DIODES, INC.	SMAJ40CA-13-F
1	ea.	D29	DIODE-DUAL, SWT, SMD, SOT23, 100V, 2A, 350mW, ROHS	DIODES INC.	MMBD7000HS-7-F
1	ea.	D30	DIODE-ZENER, SMD, 2P, SOD-123, 3.3V, 500mW, ROHS	DIODES, INC.	BZT52C3V3-7-F
3	ea.	D31, D33, D32	DIODE-ZENER, SMD, SOD-123, 43V, 410mW, ROHS	DIODES, INC.	BZT52C43-7-F
1	ea.	D35	Diode Schottky, SOD323		
2	ea.	D36, D37	Diode, Schottky, SOD523		
1	ea.	Q11	TRANSIST-MOS, N-CHANNEL, SMD, DPAK, 40V, 9A, ROHS	FAIRCHILD	FDD8451
4	ea.	Q12, Q13, Q15, Q16	TRANSISTOR-DUAL NPN, SMD, 6P, SOT363, 40V, 200mA, ROHS	DIODES, INC.	MMDT3904-7-F
5	ea.	Q1-Q5	TRANSISTOR-MOS, N-CHANNEL, SMD, SOT23, 60V, 280mA, ROHS	FAIRCHILD	NDS7002A
3	ea.	Q6-Q8	TRANSISTOR, P-CHANNEL, SMD, SOT23, -60V, -180mA, ROHS	FAIRCHILD	NDS0605
2	ea.	Q9, Q10	TRANSISTOR-MOS, N-CHANNEL, SMD, D2PAK, 40V, 75A, ROHS	NXP SEMICONDUCTOR	PHB101NQ04T
12	ea.	R18-R25, R49, R50, R52, R53	RES, SMD, 0402, 1k, 1/16W, 1%, TF, ROHS	VENKEL	CR0402-16W-102JT
8	ea.	R1-R8	RES, SMD, 0603, 330k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-07330KL
8	ea.	R26 - R33	RES, SMD, 2512, 100Ω, 1W, 1%, TF, ROHS	VISHAY/DALE	CRCW2512100RFKEG
10	ea.	R40-R48, R63	RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF1001V
7	ea.	R34-R39	RES, SMD, 0603, 100Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1000FT
1	ea.	R54	RES, SMD, 2512, 200, 1W, 5%, TF, ROHS	VENKEL	CR2512-1W-201JT
5	ea.	R55-R57, R64, R65	RES, SMD, 0603, 1M, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF1004V
2	ea.	R58, R59	RES, SMD, 2512, 002Ω, 1W, 1%, TF, ROHS	PANASONIC	ERJ-M1WTF2M0U
2	ea.	R61, R62	RES, SMD, 0402, 22k, 1/16W, 1%, TF, ROHS	VENKEL	CR0402-16W-223JT
2	ea.	R66, R67	RES, SMD, 0603, 499Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-4990FT
2	ea.	R68, R69	RES, SMD, 0402, 4.7k, 1/16W, 1%, TF, ROHS	VENKEL	CR0402-16W-4701FT
5	ea.	R70-R74	RES, SMD, 0402, 49.9k, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ-2RKF4992

Bill of Materials (Continued)

QTY	UNIT	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	MANUFACTURER PART
1	ea.	R75	RES, SMD, 0603, 120k, 1/10W, 1%, TF, ROHS	VISHAY/DALE	CRCW0603120KFKEA
1	ea.	R76	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL	CR0603-10W-000T
1	ea.	R77	RES, SMD, 0402, 0Ω, 1/16W, 5%, TF, ROHS	VENKEL	CR0402-16W-00T
4	ea.	R78, R79, R81, R82	RES, SMD, 0402, 2.49k, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ-2RKF2491V
2	ea.	R83, R87	RES, SMD, 0603, 3.3M, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF3304V
1	ea.	R84	RES, SMD, 0603, 550k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-5503FT
11	ea.	R9-R17, R85, R86	RES, SMD, 0402, 10k, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ-2RKF1002X
2	ea.	S1, S2	SWITCH-TACTILE, PUSH, TH, 8x8mm, SPST, 12V, 50mA, ROHS	OMRON	B3WN-6002
3	ea.	Th1, TH2a, TH2b	THERMISTOR, SMD, 0603, 10k, 1/10W, 5%, B VALUE = 3375-3345K, ROHS	PANASONIC	ERT-J1VG103JA
1	ea.	U1	IC-MULTI-CELL, LI-ION MONITOR, 48P, QFN, 6x6, ROHS	INTERSIL	ISL94202IRTZ
1	ea.	U2	IC-TVS, ESD PROTECTOR, SMD, 6P, SOT-23-6L, 3pF, 6V, ROHS	ST MICROELECTRONICS	USBLC6-2SC6
1	ea.		PWB-PCB, ISL94202EVKIT1Z, REVD, ROHS		
CONNECTORS/HEADERS					
1	ea.	J13	CONN-HEADER, 4PIN, 2.54mm, RIGHT-ANGLE, ROHS	MOLEX	22-05-2041
1	ea.	J3	CONN-HEADER, 1x9, FLAT BRK-AWAY, 2.54mm, R/A, ROHS	MOLEX	22-28-8091
1	ea.	TP11	CONN-HEADER, 1x1, BREAKAWAY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
4	ea.	1Path, 2Path, xTH1, xTH2a	CONN-HEADER, 1x2, BRKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
3	ea.	ADDR, J7, J9	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
1	ea.	J5	CONN-HEADER, 1x8, BRKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
1	ea.	J2	CONN-HDR, 1x9, BRKAWY 1x36, 2.54mm, ST, ROHS	BERG/FCI	68000-236
1	ea.	CS1, CS2	CONN-HEADER, 1x2, BRKAWY 1x64, 2.54mm, 0.195x0.118, ROHS	MILL-MAX	800-10-064-10-001000
1	ea.	CHMON, LDMON, PCFET, CFET, DFET	CONN-HEADER, 1x5, BRKAWY 1x64, 2.54mm, 0.195x0.118, ROHS	MILL-MAX	800-10-064-10-001000
1	ea.	VB, VC0-VC8	CONN-HDR, 1x10, BRKAWY 1x64, 2.54mm, 0.195x0.118, ROHS	MILL-MAX	800-10-064-10-001000
DO NOT POPULATE					
0	ea.	C24	CAP, SMD, 1206, ROHS		
0	ea.	R60	RES, SMD, 0805, 68mΩ, ROHS		
0	ea.	J1, J10, J11	DO NOT POPULATE		
0	ea.	TP1, TP9, TP10	DO NOT POPULATE		
0	ea.	CB1-CB8	CONN-HEADER, 1x1, BRKAWY 1x64, 2.54mm, 0.195x0.118, ROHS	MILL-MAX	800-10-064-10-001000
0	ea.	SCL, SDA, TMPO, VREF, xT1, xT2	CONN-HEADER, 1x3, BRKAWY 1x64, 2.54mm, 0.195x0.118, ROHS	MILL-MAX	800-10-064-10-001000
0	ea.	FETSOFF, PSD, INT, SD, EOC, RGO	CONN-HEADER, 1x6, BRKAWY 1x64, 2.54mm, 0.195x0.118, ROHS	MILL-MAX	800-10-064-10-001000

Layout

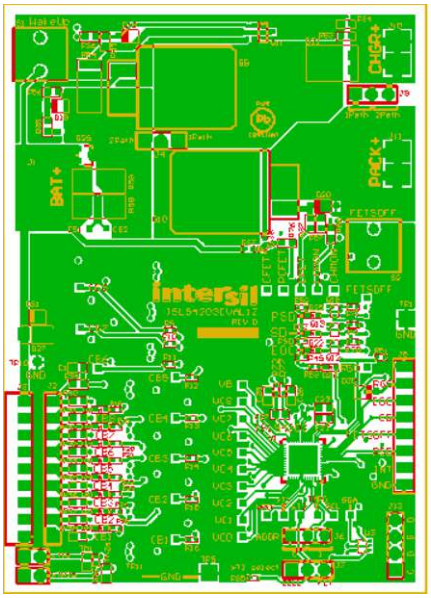


FIGURE 52. TOP LAYER

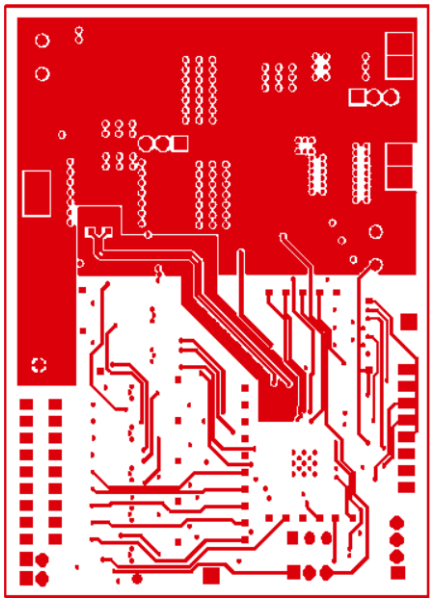


FIGURE 53. MIDDLE LAYER 1

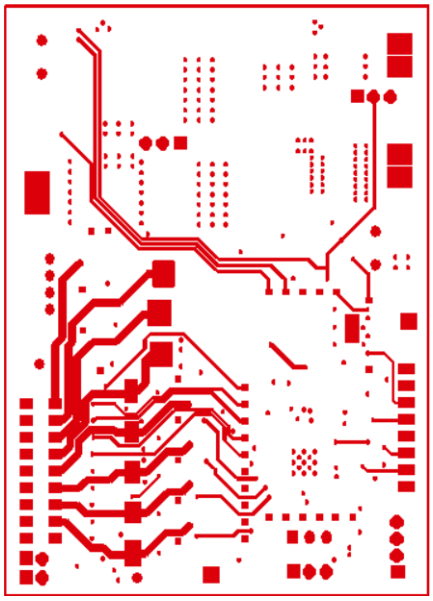


FIGURE 54. MIDDLE LAYER 2

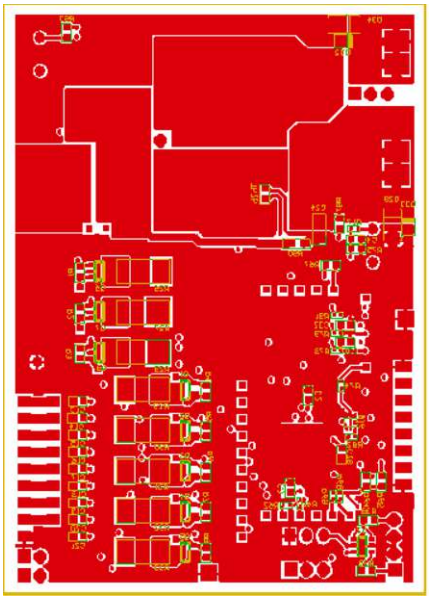


FIGURE 55. BOTTOM LAYER

Hardware Overview

The hardware design follows recommendations in the datasheet. However, this section provides some additional guidelines and explanations.

Jumpers

There are three user selectable options on the ISL94202EVKIT1Z board.

ADDR

This jumper selects the I^2C address. Normally, this jumper connects to the “0” position. With the jumper set to the “1” position, the GUI I^2C address value must be changed to “52.”

XT2 SELECT

There are three external thermistors on the board. There are two near the battery connectors. These can be used to monitor the battery cells (connect external thermistors to connectors xTh1 or xTH2a and remove the on-board thermistors Th1 and Th2a). There is a third resistor located under the discharge power FET.

The xT2Select jumper allows the ISL94202 to monitor either the Th2a thermistor near the battery terminals (CELL position) or the Th2b thermistor under the power FET (FET position). When monitoring the FET thermistor, you might want to check the “xT2 Monitors FET” box in the GUI (see “Pack Options” on page 23).

POWER FET CONFIGURATION

The board allows for both a single charge/discharge path and a separate charge/discharge path. Configuring the options requires two jumpers. For a single path, connect a shunt on the “1 Path” aide of J4. Also, connect a shunt on the “1 Path” side of jumper J9. In this configuration both charge and discharge connections of the pack connect to the DSCG+ pin.

For the separate charge and discharge path, connect a shunt on J4 and J9 on the “2 Path” side of each. In this configuration, discharge is on the DSCG+ pin and charge is on the CHRG+ pin.

If the plan is to test the board with significant amounts of current, then replace the shunt with some soldered braided wire to complete the circuit. In this way the board should be able to handle a discharge current of 20A and charge current of 2.5A.

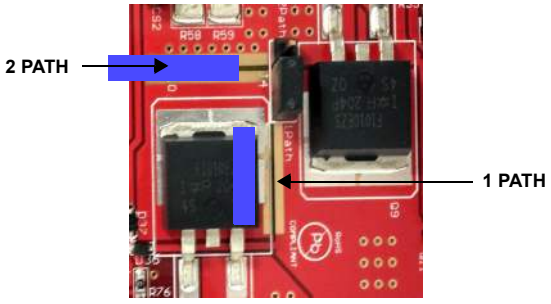


FIGURE 56. SOLDER JUMPERS FOR HIGHER CURRENT

AFE

The analog front end of the ISL94202 adds external cell balancing components. The cell balance output from each cell balance pin is a constant current of about 25µA. This generates about 8.25V across the 330k resistor between the gate and source of the balancing transistor. If a balance FET with lower gate voltage requirements is desired, reduce the value of the gate resistor.

The evaluation board uses 100Ω cell balance resistors, so it balances about 40mA of current. The board also includes LEDs on each cell balance circuit to indicate when the cell balance is active.

The cell input filters consist of a 1k resistor, a 4.7nF capacitor to ground, and a 10nF capacitor cell-to-cell. These can be changed to suit the application, but the following guidelines should be considered.

- The 1k resistor can be reduced, but this makes the part more susceptible to input currents during hot plug of the battery cells. A smaller input resistor would also require higher value capacitors to ground to maintain the same filter. Higher value resistors on the upper cells would be higher cost.
- The 1k resistor can be increased. The limit relates to the accuracy of measurement. In the worst case conditions, there is a difference of about 2µA of bias current on the inputs. The ISL94202 is factory calibrated assuming an input 1k resistor. An extra 1k input resistor can generate up to 2mV of error. Larger input resistors increase this error.
- The capacitors from each input to ground provide a better filter than the capacitors across each input. However, differences in capacitors on adjacent inputs could result in some voltage errors on the input. Both capacitors to ground and capacitors across inputs are provided on the board, but the application may not need both.
- Larger input capacitors can affect the open wire detection circuit. If larger capacitors are used and the open wire circuit does not seem to detect the open condition, increase the “Open Wire Sample Time” timer value in the GUI.

Protection Circuits

The board contains several protection components that should be on any application.

- There should be diodes on VBATT, DSCG+, and CHRG+ to GND to prevent negative voltages on the pins of the ISL94202. The schematics show the use of 43V Zener diodes, so the inputs are also protected against high voltage transients.
- The board provides transient voltage suppressors on the pack pins to help minimize problems with ESD on the board.
- There is a protection device (USBLC6) on the I^2C inputs to minimize damage due to ESD on the I^2C connector. While this component helps protect against ESD, it is also a problem for the board. Since this component has internal diodes between the I2C pins and the RGO power pin, connecting the I^2C interface to an externally powered µC before the ISL94202 powers up prevents proper power-up of the ISL94202. If there is a hardwired connection between the µC and the evaluation board, U2 can be removed from the board and replaced with jumpers across Pins 1 to 6 and 3 to 4. This will allow the µC to power up before the ISL94202 powers up.
- Back to back diodes are connected across the current sense inputs to prevent excessive differential voltage across these pins.

Push Buttons

The board provides two push buttons for ease of use and evaluation purposes. These are not required in an application.

- The wake up push button simulates the connection of a pack to a charger. It does this by connecting the CHRG+ pin to VDD using a 1k series resistor. The device sees this as a charger connection. The ISL94202 can also be wakened by momentarily connecting a resistor from the DSCG+ pin to GND. Use a 2k resistor to minimize current when the power FETs turn on. During manufacture of the battery pack, the finished pack can be connected to a charger, or the wake up switch can be included on an external jig to power up the board prior to final programming.
- The FETSOFF pin connects directly to the FETSOFF input of the ISL94202. When pressed, the power FETs and cell balance FETs turn off. Normally in a system, this input would connect to a µC or an external control source. If FETSOFF connects off the board, add a 3V Zener diode to GND to prevent glitches on this input from going too high or negative.

LED Indicators

There are four LED indicators on the board. The LEDs are not required in a real application, they are used here to provide quick monitoring of the system. The LEDs are RGO (Green), EOC (Red), SD (Red), and PSD (Red).

The LED indicator circuits use current mirrors to drive the LEDs. There are several reasons for this.

- The ISL94202 RGO regulator output voltage is 2.5V (2.25V to 2.75V). Because of this voltage and range, it is difficult to directly drive LEDs that have a forward voltage drop of 1.8V to 2.3V while controlling current to acceptable levels.
- When directly driving the LEDs from the RGO output using a current-limiting resistor, small variations in the supply voltage result in large changes in LED brightness.
- If the LEDs connect direct to the RGO output, the four LEDs would pull at least 5mA from the RGO output. While this is within the capability of the RGO, it could lead to some internal heating of the die. Since this board is for evaluation, and an actual application would not normally have the LEDs, an indirect approach to powering the LEDs was adopted.

The current mirrors use a resistor on one side to provide a “current gain.” The LEDs are each driven with ~ 1mA of current from VBATT, but the drain from the RGO output is only ~ 40µA.

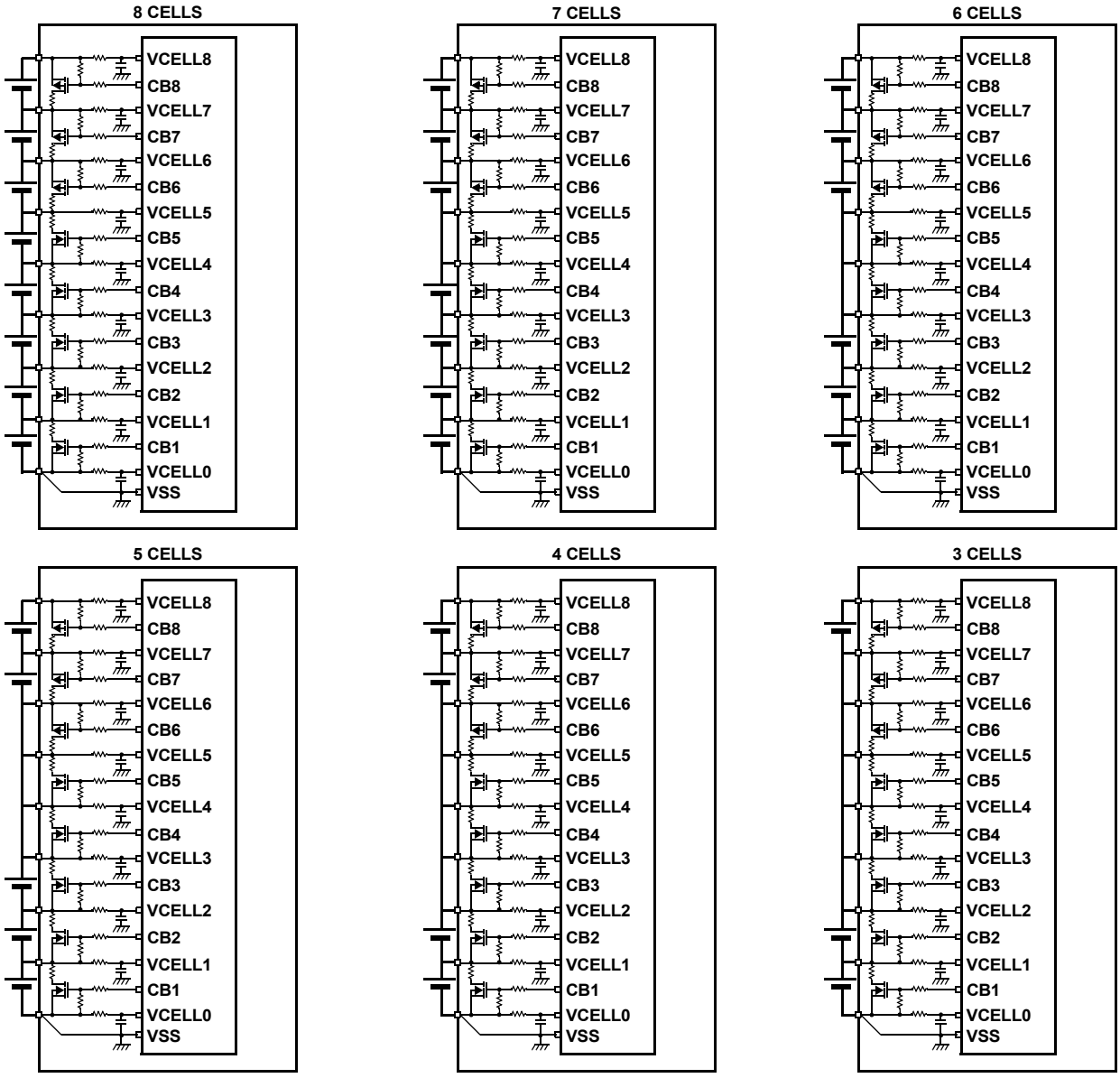


FIGURE 57. BATTERY CONNECTION OPTIONS USING THE ISL94202EVKIT1Z BOARD

Errata/Q&A

1. When I power the board, the device does not power up correctly. It looks like it is in sleep mode.

   Before applying power to the evaluation board, disconnect the I^2C cable. Once the board is powered, connect the I^2C interface. The reason for this is that U2 on the board has internal protection diodes from the I^2C traces to RGO. When SCL and SDA pull up externally to 3.3V, the ISL94202 is partially powered, so it does not complete its power-up cycle.

2. Cell measurement accuracy does not match the specifications in the datasheet.

   There are some other potential reasons for inaccurate readings.

   - The source of measurement should have a low output impedance. A string of resistors that sets the input voltages, like the Intersil MCB_PS_Z board, can have small changes in the input voltage as the ISL94202 samples each cell. Later models of the MCB_PS_Z board will have 10µF capacitors across each input. These capacitors should minimize sampling errors.
   - The ADC reading should be compared with the voltage on the PCB before the input resistors (at J2). If the voltages are compared with DVM readings at the battery pack where there is a long cable, then there should be separate wires for GND and VC0 and for VC8 and VBAT. The reason for this is that the VBAT and GND leads will carry perhaps a lot of current, so there may be voltage drops across the wires. The VC0 and VC8 terminals are “Kelvin” connections that do not carry much current. Cell voltage measurements are based on VC0 and VC8, not GND and VBAT.
   - Soldering the board to the PCB can change the stresses on the package from what they were during device calibration. This can change the value of the voltage reference, which changes the ADC converted value. This does not affect the relative voltage readings. If there is an external µC, then an offset can be added to the µC to correct for solder induced stresses.

3. I changed the “Pack Settings” tab such that the “CB during EOC” button is checked. But after power cycling the part, the “CB during EOC” is no longer checked and the part is not balancing during End-of-Charge.

   - After clicking on any of the option bits in the “Pack Settings” tab or on the main screen (above the FET control indicators), it is necessary to do a “Write EEPROM” either on the “Pack Settings” tab or the “Config Mem” tab. Without this write operation the change only resides in the ISL94202 Configuration RAM space.

4. When I repeatedly read the EEPROM memory in the configuration tab, the communications lock up.

   - There was a problem with the old GUI code. The best solution is to get the new Win7/8 code. This new code does not have this problem. Until then, the best way to clear this, without removing the battery from the board, is to remove the I^2C cable and use a jumper to momentarily connect and release the SCL line to VSS (it is pulled up by a resistor). This creates a clock pulse. Do this up to nine times to clear the ISL94202 port. Then reconnect the I^2C cable.

FET Gate Drive Rise/Fall Characteristics

Verify basic digital logic, analog interface, level shifters, and charge pump operation.

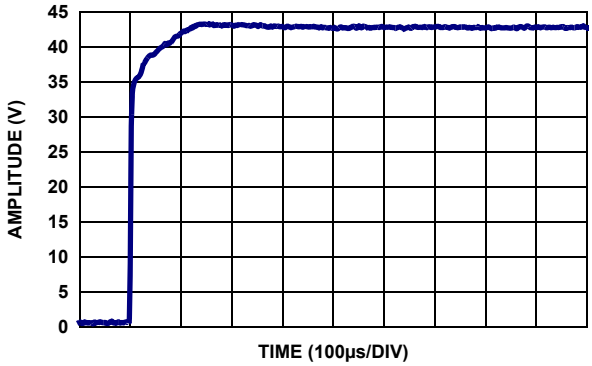


FIGURE 58. DFET RISE

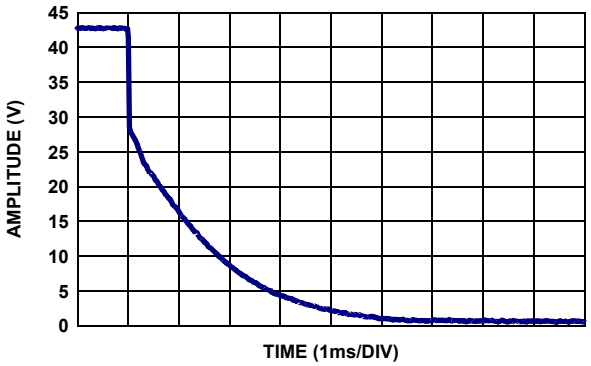


FIGURE 59. DFET FALL

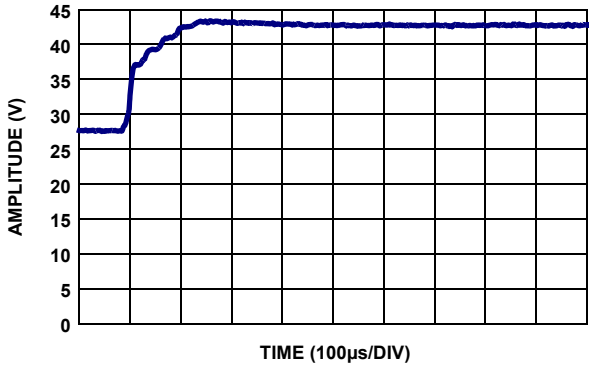


FIGURE 60. CFET RISE

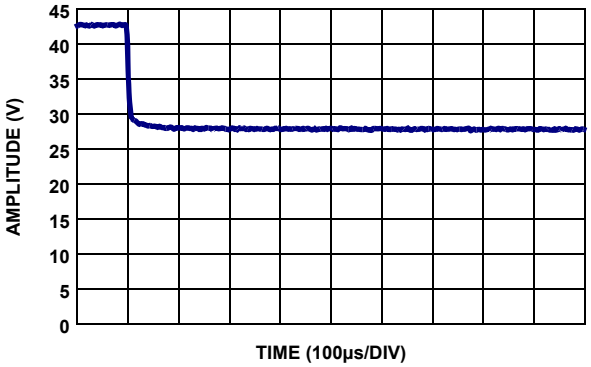


FIGURE 61. CFET FALL

Revision History

REVISION	DATE	DESCRIPTION
1.0	Apr 13, 2021	Updated Figure 56 by correcting labels.
0.0	Feb 10, 2017	Initial release.

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