



**High-Speed CMOS  
16Kx4 SRAM  
with Common I/O**

**QS8888A  
Preliminary**

**FEATURES/BENEFITS**

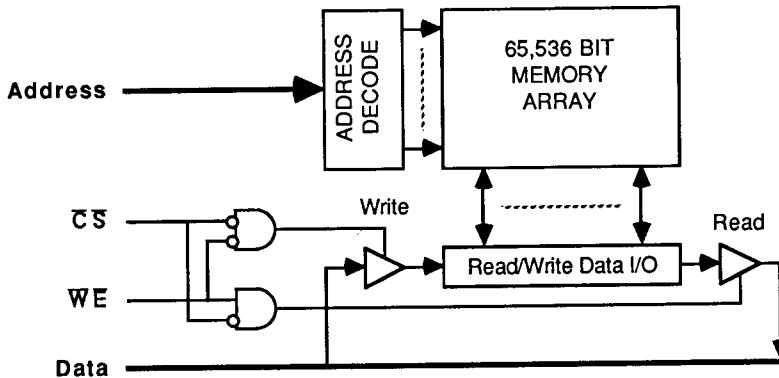
- 8ns/10ns/12ns/15ns Commercial
- 10/12ns/15ns/20ns Military
- TTL compatible I/O
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- Ideal for reliable, dense memory systems
- Available in DIP, SOJ, LCC
- 6-Transistor cell for high reliability
- Low Standby current
- JEDEC standard pinout

2

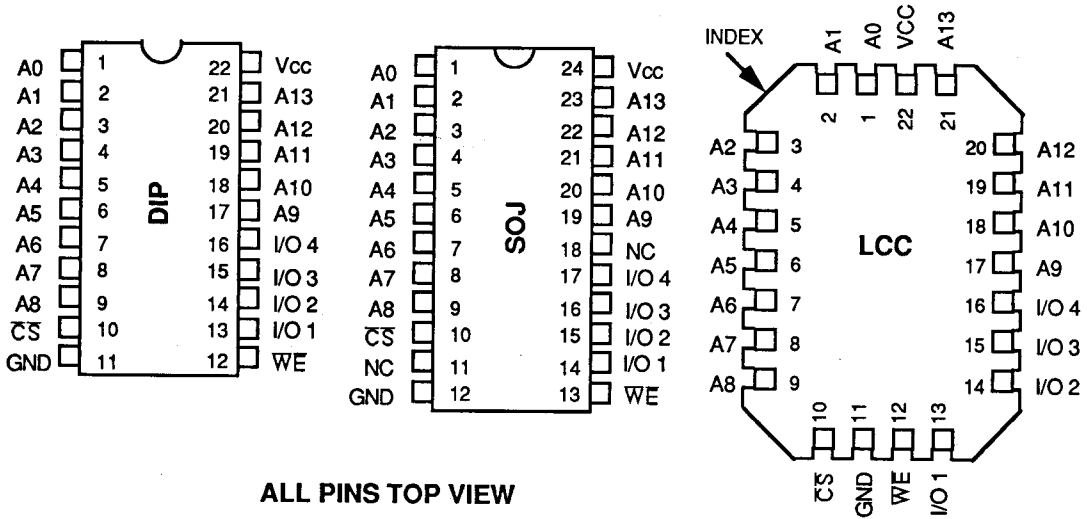
**DESCRIPTION**

The QS8888A is a high-speed 64K SRAM organized as 16Kx4. It is manufactured in a high-performance CMOS process, and it based on a 6-transistor cell design for high reliability and radiation tolerance. The high-speed access times of the QS8888A make it useful for cache data RAM, cache tag RAM, high-speed scratchpad memories, and look-up tables. Low operating power and excellent latch-up and ESD protection are provided. The QS8888A is offered in a variety of packages.

**FUNCTIONAL BLOCK DIAGRAM**



**PIN CONFIGURATIONS**



**ALL PINS TOP VIEW**

**PIN DESCRIPTION**

Pin Name	I/O	Function
A	I	Address
I/O1 - I/O4	I/O	Data
$\overline{CS}$	I	Chip Select
WE	I	Write Enable

**FUNCTION TABLE**

$\overline{CS}$	WE	I/O	Power	Function
H	X	High Z	Standby	Deselect
L	H	Data Out	Active	Read
L	L	Data In	Active	Write

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage to Ground..... -0.5V to +7.0V  
 DC Output Voltage  $V_O$  ..... -0.5V to  $V_{CC} + 0.5V$   
 DC Input Voltage  $V_I$  ..... -0.5V to  $V_{CC} + 0.5V$   
 AC Input Voltage (for a pulse width  $\leq 20$  ns)..... -3.0V  
 DC Output Current Max. sink current/pin..... 50 mA  
 DC Output Current Max. source current/pin..... 30 mA  
 TBIAS Temperature Under Bias, COM..... -65° to +125°C  
 TSTG Storage Temperature, COM..... -65° to +125°C  
 TBIAS Temperature Under Bias, MIL..... -65° to +135°C  
 TSTG Storage Temperature, MIL..... -65° to +155°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

**RECOMMENDED OPERATING RANGES**

Parameter		Commercial		Military		Units
		Min	Max	Min	Max	
Ta	Ambient Operating Temperature	0	70	-55	125	deg
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
Vcc	Supply voltage (8 ns coml. only)	4.75	5.25			V

**CAPACITANCE**

Ta=+25°C, f=1 MHz

Name	Description	Package	Typ	Max	Unit
Cin	Input Capacitance Vin = 0 V	PDIP	3	6	pF
		SOJ	2.5	5	pF
Cout	Output Capacitance Vout = 0 V	PDIP		7	pF
		SOJ		7	pF

Note: Capacitance is measured at characterization but not tested at final production.

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
Ii	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	μA
Io	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

**Notes:**

1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

**POWER SUPPLY CHARACTERISTICS**

Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-8		-10		-12		15		-20		Unit
		C	M	C	M	C	M	C	M	C	M	
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	160	145	165	135	155	125	145	120	140		mA
I <sub>sb</sub>	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX	70	60	70	60	70	60	70	60	70		
I <sub>sb1</sub>	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc	20	15	20	15	20	15	20	15	20		

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

See Read Timing Diagrams. All values in nanoseconds.

Symbol	Parameter	-8		-10		-12		-15		-20	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
<b>READ</b>											
t <sub>RC</sub>	Read Cycle Time (1)		8		10		12		15		19
t <sub>AA</sub>	Address Access Time		8		10		12		15		19
t <sub>ACS</sub>	Chip Select Access Time		8		10		12		15		19
t <sub>OH</sub>	Output Hold from Address Change	1.5		2		2		2		3	
t <sub>LZ</sub>	Chip Select to Output in Low Z (2)	1.5		2		2		2		2	
t <sub>HZ</sub>	Chip Select to Output in High Z (2,3)		4		5		5		7		8
t <sub>PU</sub>	Chip Select to Power Up Time (2)	0		0		0		0		0	
t <sub>PD</sub>	Chip Select to Power Down Time (2)		8		10		12		15		19

**Notes:**

- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.

2

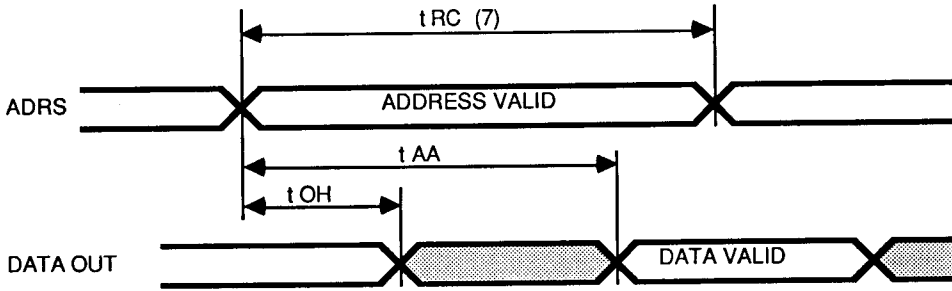
**QS8888A**

Symbol	Parameter	-8		-10		-12		-15		-20	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
<b>WRITE</b>											
t WC	Write Cycle Time (1)	8		10		12		15		19	
t CW	Chip Select Valid to End of Write	7		8		10		13		17	
t AW	Address Valid to End of Write	7		8		10		13		17	
t AS	Address Setup Time	0		0		0		0		0	
t WP	Write Pulse width	7		8		10		12		16	
t WR	Write Recovery Time	0		0		0		0		0	
t DW	Data Valid to End of Write	4		5		6		8		10	
t DH	Data Hold Time	0		0		0		0		0	
t WZ	Write Enable to Output in High Z (2,3)		4		4		5		6		7
t OW	Output Active from End of Write (2)	1.5		2		2		2		2	

**Notes:**

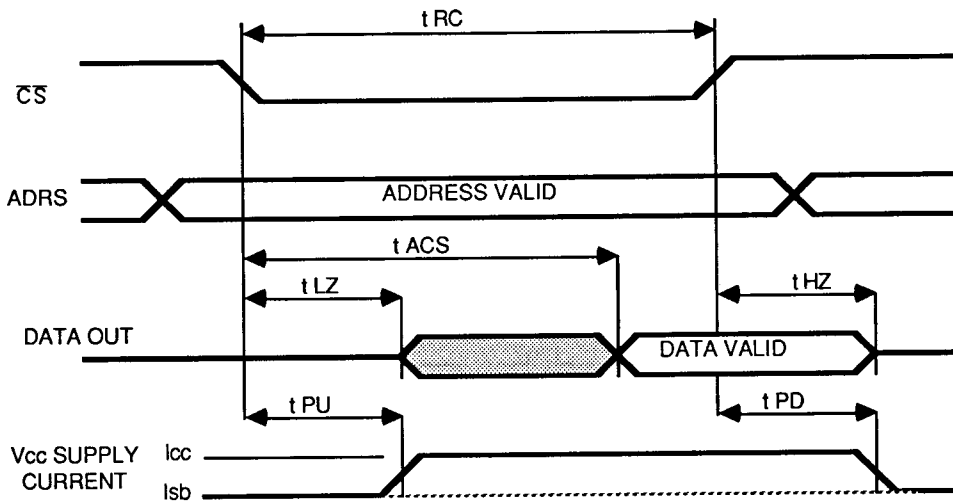
- 1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- 2) This parameter is guaranteed by design but not tested.
- 3) Transition to Hi-Z is measured  $\pm 200$  mV change from the prior steady state voltage.

**TIMING WAVEFORMS - READ CYCLE NO. 1 (4, 5)**



2

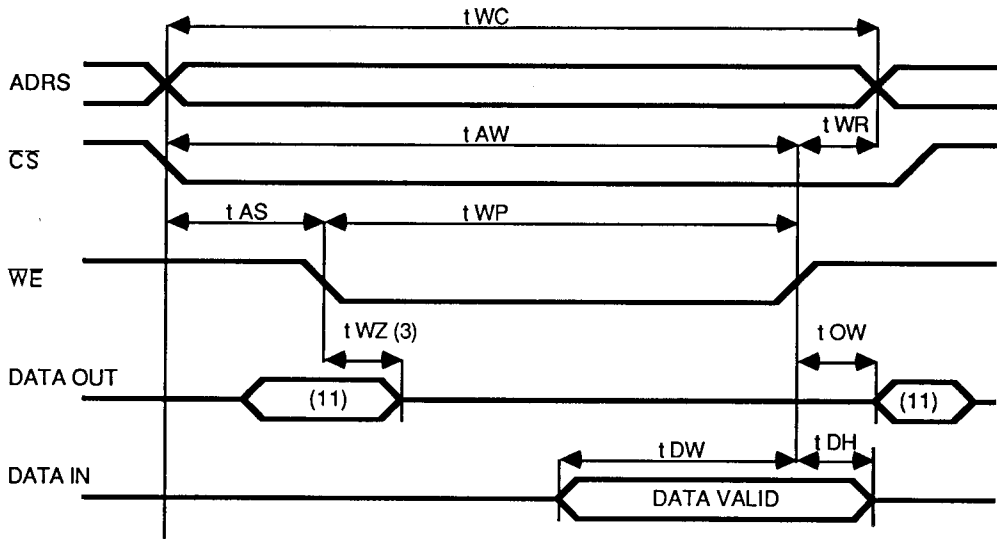
**TIMING WAVEFORMS - READ CYCLE NO. 2 (4,6)**



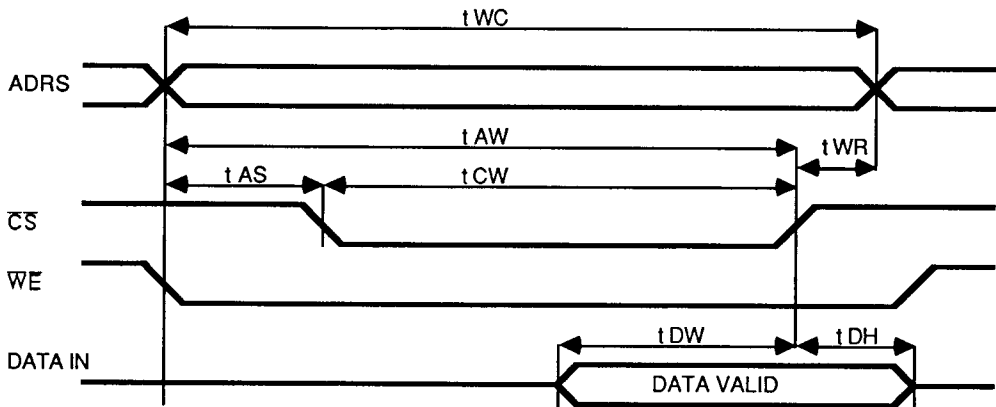
Notes:

4.  $\overline{WE}$  is high for Read cycle.
5.  $\overline{CS}$  is low for Read cycle #1.
6. Address is valid to or coincident with  $\overline{CS}$  transition time for Read Cycle #2.
7. All read timings are referenced from the last valid address to the first transitioning address.

**TIMING WAVEFORMS-WRITE CYCLE No. 1 (8,9,10 WE controlled timing)**



**TIMING WAVEFORMS-WRITE CYCLE No. 2 (8,9,10,12 CS controlled timing)**



**Notes:**

8. WE or CS must be high during address transitions.
9. A write occurs during the overlap of a low CS and a low WE.
10.  $t_{WR}$  is measured from the earlier of CS and WE going high to end of the write cycle.
11. During this period the I/O pins are in the output state and input signals must not be applied.
12. If the CS low transition occurs simultaneously with or after the WE low transition, the output remains in the high impedance state.