3.3 VOLT ZERO DELAY, LOW SKEW BUFFER

ICS671-03

Description

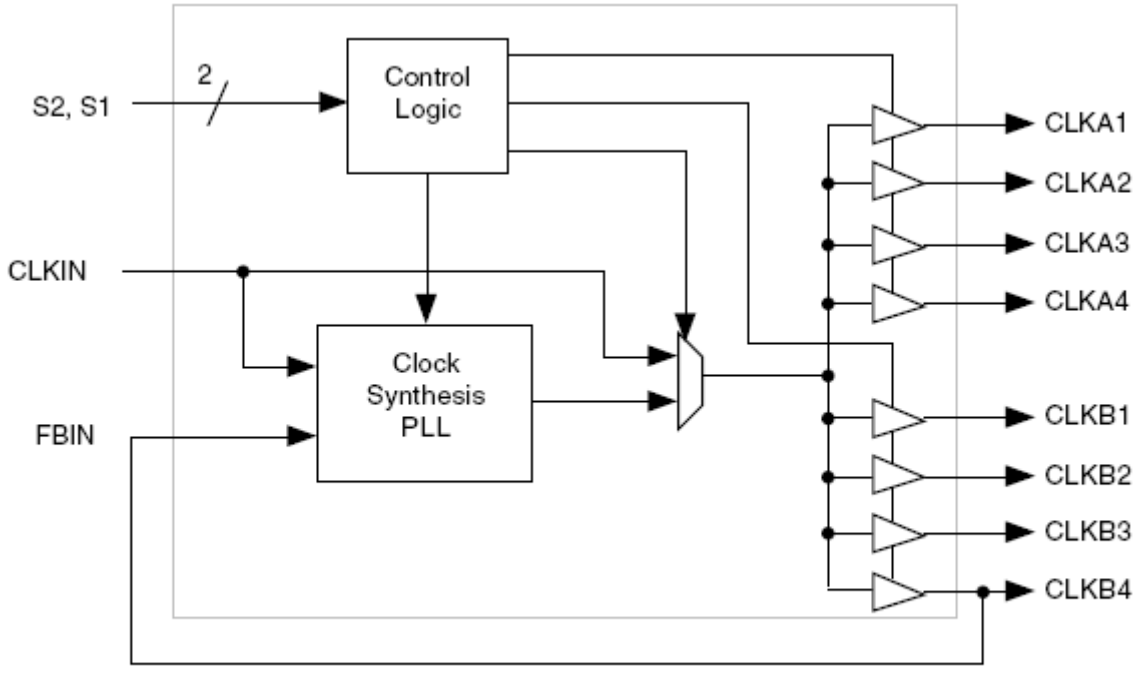
The ICS671-03 is a low phase noise, high speed PLL based, 8 output, low skew zero delay buffer. Based on IDT's proprietary low jitter Phase Locked Loop (PLL) techniques, the device provides eight low skew outputs at speeds up to 133 MHz at 3.3 V. The outputs can be generated from the PLL (for zero delay), or directly from the input (for testing), and can be set to tri-state mode or to stop at a low level. For normal operation as a zero delay buffer, any output clock is tied to the FBIN pin.

Features

- Packaged in 16 pin narrow (150 mil) SOIC
- Clock outputs from 10 to 133 MHz
- Zero input-output delay
- Eight low-skew (<200 ps) outputs
- Device-to-device skew <700 ps
- Low jitter (<200 ps)
- Full CMOS outputs with 25 mA output drive capability at TTL levels
- 5 V tolerant FBIN and CLKIN pins
- Tri-state mode for board-level testing
- Advanced, low power, sub-micron CMOS process
- 3.3 V operating voltage
- Industrial temperature range of -40 to 85 °C
- Available in RoHS compliant (Pb free) package

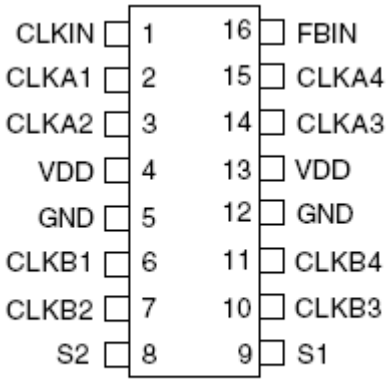
NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



Feedback is shown from CLKB4 for illustration, but may come from any output.

Pin Assignment



16 pin narrow (150 mil) SOIC

Output Clock Mode Select Table

S2	S1	CLKA1:A4	CLKB1:B4	A & B Source	PLL Status
0	0	Tri-state (note 1)	Tri-state (note 1)	PLL	ON
0	1	Stopped Low	Stopped Low	None	OFF
1	0	Running	Running	CLKIN (note 2)	OFF
1	1	Running	Running	PLL	ON

Note 1: Outputs are in high impedance state with weak pulldowns.

Note 2: Buffer mode only; not zero delay between input and output.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Clock Input (5 V tolerant).
2, 3, 14, 15	CLKA1:A4	Output	Clock Outputs A1:A4. See above table. Outputs have weak pulldown resistors.
4, 13	VDD	Power	Power supply. Connect both pins to 3.3 V.
5, 12	GND	Power	Connect to ground.
6, 7, 10, 11	CLKB1:B4	Output	Clock Outputs B1:B4. See above table. Outputs have weak pulldown resistors.
8	S2	Input	Select input 2. See table above. Internal pull-up.
9	S1	Input	Select input 1. See table above. Internal pull-up.
16	FBIN	Input	Feedback Input. Connect to any output under normal operation (5 V tolerant).

Note: Outputs have a weak internal pull-down when in tri-state mode.

External Components

The ICS671-03 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01µF should be connected between VDD and GND on pins 4 and 5, and VDD and GND on pins 13 and 12, as close to the device as possible. A series termination resistor of 33 Ω may be used close to each clock output pin to reduce reflections.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD and GND, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS671-03. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS671-03. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD (referenced to GND)	-0.5 V to 7 V
Inputs and Clock Outputs (referenced to GND)	-0.5 V to VDD+0.5 V
CLKIN and FBIN Inputs	-0.5 V to 5.5 V
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C
Ambient Operating Temperature	-40 to +85 ° C
Electrostatic Discharge (MIL-STD-883)	2000 V min.

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.00		3.60	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -8 mA	VDD-0.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Operating Supply Current	IDD	No load, S2=1, S1=1, Note 1			70	mA
Power Down Supply Current	IDD	CLKIN=0, S2=0, S1=0		1.3		mA
		CLKIN=0, Note 2		1.3		mA
Short Circuit Current	I_{OS}	Each output		±50		mA
Input Capacitance	C_{IN}	S2, S1, FBIN		5		pF

Note 1: With CLKIN = 100 MHz, FBIN to CLKA4, all outputs at 100 MHz.

Note 2: When there is no clock signal present at CLKIN, the ICS671-03 will enter a power down mode. The PLL is stopped and the outputs are tri-state.

AC Electrical Characteristics

CycleUnless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{IN}	See table on page 2	10		133	MHz
Output Clock Frequency		See table on page 2	10		133	MHz
Output Rise Time	t_R	20% to 80%, CL=30 pF			1.5	ns
Output Fall Time	t_F	80% to 20%, CL=30 pF			1.25	ns
Output Clock Duty Cycle		At VDD/2	45	50	55	%
Device to Device Skew, equally loaded		Rising edges at VDD/2			700	ps
Output to Output Skew, equally loaded		Rising edges at VDD/2			200	ps
Input to Output Skew, FBIN to CLKA4, S1=1, S0=1		Rising edges at VDD/2, Note 1			±250	ps
Maximum Absolute Jitter				130		ps
Cycle to Cycle Jitter, 30 pF loads					300	ps
PLL Lock Time		Note 2			1.0	ms

Note 1: With CLKIN = 100 MHz, FBIN to CLKA4, all outputs at 100 MHz.

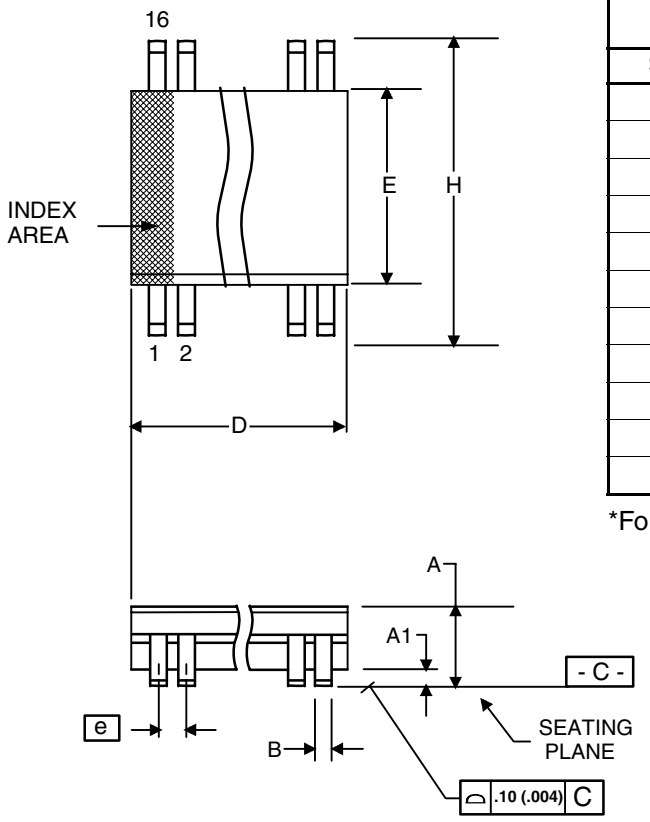
Note 2: With VDD at a steady state, and valid clocks at CLKIN and FBIN.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	9.80	10.00	.3859	.3937
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
671M-03I*	ICS671M-03I	Tubes	16-pin SOIC	-40 to 85° C
671M-03IT*	ICS671M-03I	Tape and Reel	16-pin SOIC	-40 to 85° C
671M-03ILF	671M-03ILF	Tubes	16-pin SOIC	-40 to 85° C
671M-03ILFT	671M-03ILF	Tape and Reel	16-pin SOIC	-40 to 85° C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
B		11/27/06	Added LF ordering information.
C		11/04/09	Added EOL note for non-green parts.

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