MOTOROLA

BCD To Seven Segment Decoder/Driver With Open Collector Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/30704

Military 54LS47

AVAILABLE AS:

1) JAN: JM38510/30704BXA
2) SMD: 7604501
3) 883: 54LS47/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

The LSTTL/MSI 54LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth table. Output configurations of the 'LS47 are designed to withstand the relatively high voltages required for 7-segment indicators.

These outputs will withstand 15 V with a maximum reverse current of 250 µA. Indicator segments requiring up to 24 mA of current may be driven directly from the 54LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The 54LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time when the BI/RBO node is a HIGH level. This device also contains an overriding blanking input (BI) which is used to control the lamp intensity or to inhibit the outputs.

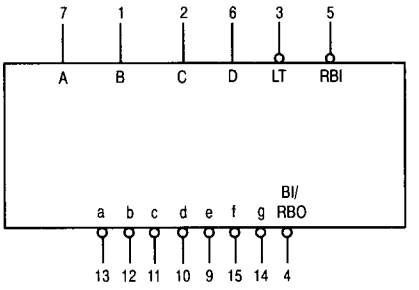
- Lamp Intensity Modulation Capability
- Open Collector Output
- Lamp Test Provision
- Leading/Trailing Zero Suppression
- Input Clamp Diodes Limit High-Speed Termination Effect

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
B	1	1	2	V_{CC}
C	2	2	3	V_{CC}
LT	3	3	4	V_{CC}
RBO	4	4	5	V_{CC}
RBI	5	5	7	V_{CC}
D	6	6	8	V_{CC}
A	7	7	9	V_{CC}
GND	8	8	10	GND
e	9	9	12	V_{OH}
d	10	10	13	V_{OH}
c	11	11	14	V_{OH}
b	12	12	15	V_{OH}
a	13	13	17	V_{OH}
g	14	14	18	V_{OH}
f	15	15	19	V_{OH}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

LOGIC SYMBOL



Pin Names		Loading (Note a) HIGH	LOW
A-D	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{RBI}$	Ripple Blanking Input	0.5 U.L.	0.25 U.L.
$\overline{LT}$	Lamp Test Input	0.5 U.L.	0.25 U.L.
$\overline{BI/RBO}$	Blanking Input or Ripple Blanking Output	0.5 U.L. 1.2 U.L.	0.75 U.L. 2.0 U.L.
$\overline{a}$, to $\overline{g}$	Outputs	Open Collector	15(7.5) U.L.

NOTES:
a. One TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

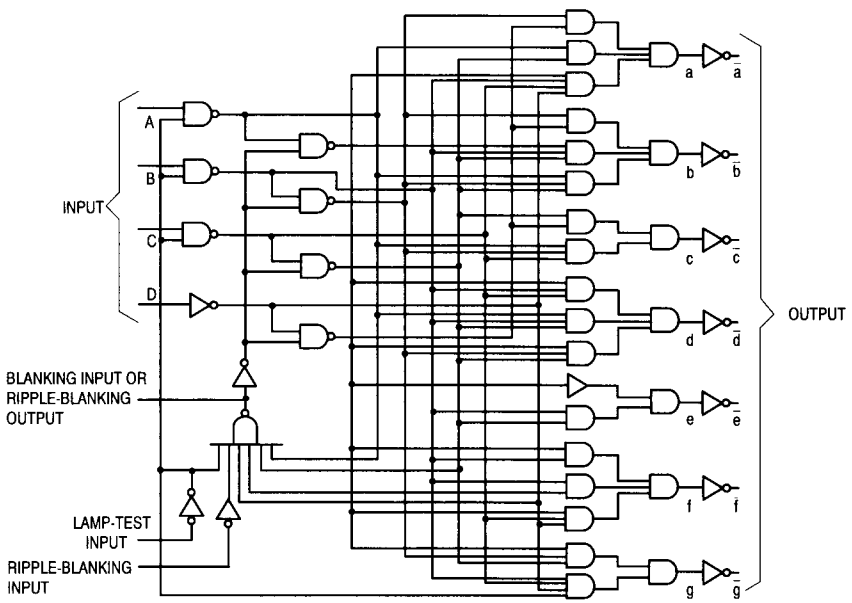
54LS47
TRUTH TABLE

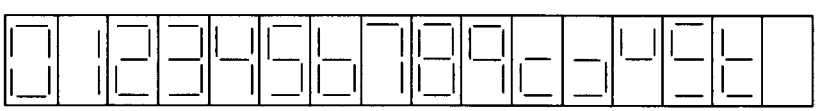
	Inputs							Outputs							
DECIMAL OR FUNCTION	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	NOTE
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

H = HIGH Voltage Levels
L = LOW Voltage Levels
X = Immaterial

REFERENCE NOTES A THROUGH D ON PAGE 5-50

LOGIC DIAGRAM





NUMERICAL DESIGNATIONS-RESULTANT DISPLAYS

NOTES:

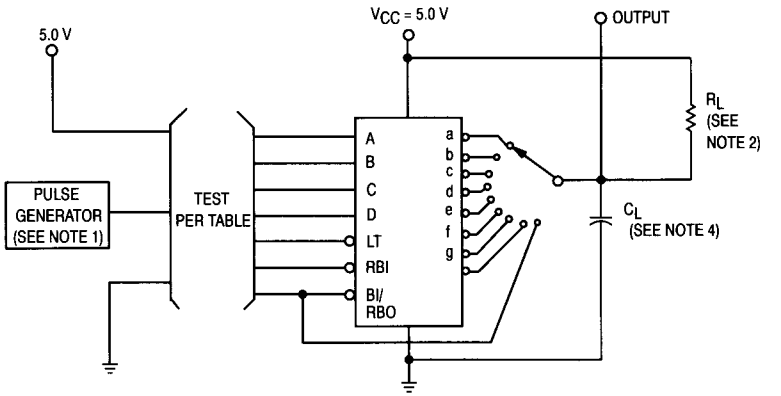
A. $\overline{BI/RBO}$ is wire-AND logic serving as blanking input (BI) and/or ripple blanking output ($\overline{RBO}$). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

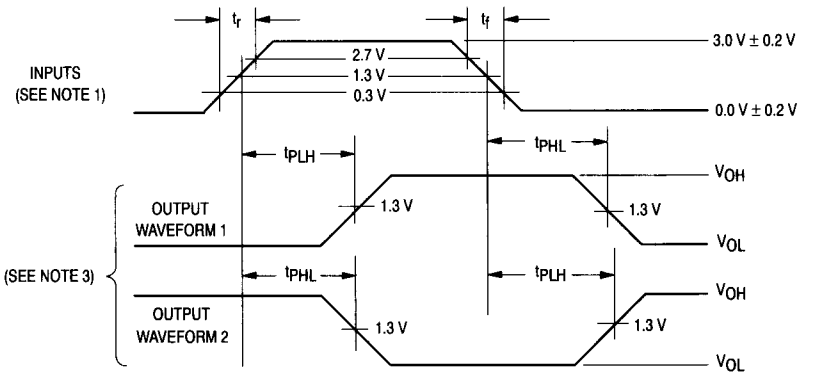
B. When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.

C. When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).

D. When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

TEST CIRCUIT AND WAVEFORM





NOTES:

1. The input pulse generator has the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, PRR ≤ 1.0 MHz, and $Z_{OUT} = 50\ \Omega$.
2. $R_L = 665\ \Omega \pm 10\%$.
3. Input-output waveform combination in accordance with truth table.
4. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance.
5. Voltage measurements are to be made with respect to network ground terminal.
6. The limits specified for $C_L = 15$ pF are guaranteed but not tested.
7. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = − 50 µA, V_{IH} = 2.0 V (LT, RBI) other inputs = 0.7 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, V_{IN} = 0.7 V (LT), other inputs are Don't Cares.
$V_{OL(RBO)}$	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 1.6 mA, V_{IN} = 2.0 V (LT), other inputs = 0.7 V.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are GND.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5 5 V, other inputs are GND.
I_{IL}	Logical "0" Input Current	− 0.1	− 0.34	− 0.1	− 0.34	− 0.1	− 0.34	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs = 5.5 V.
$I_{IL(LT,RBI)}$	Logical "0" Input Current	− 0.11	− 0.35	− 0.11	− 0.35	− 0.11	− 0.35	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs = 5.5 V.
$I_{IL(RBO)}$	Logical "0" Input Current	− 0.36	− 1.37	− 0.36	− 1.37	− 0.36	− 1.37	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs = 5.5 V.
I_{CEX}	Open Collector Input Current		250		250		250	µA	V_{CC} = 5.5 V, V_{IN} = 2.0 V (LT), other inputs = 0.7 V, V_{OUT} = 15 V.
I_{CC}	Power Supply Current Off		13		13		13	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.5 V, and V_{INH} = 2.4 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay/ Data-Output High-Low	5.0 —	105 100	5.0 —	158 125	5.0 —	158 125	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 665 Ω. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH1} t_{PLH1}	Propagation Delay/ Data-Output Low-High	5.0 —	105 100	5.0 —	158 125	5.0 —	158 125	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 665 Ω. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL2} t_{PHL2}	Propagation Delay/ Data-Output High-Low	5.0 —	105 100	5.0 —	158 125	5.0 —	158 125	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 665 Ω. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH2} t_{PLH2}	Propagation Delay/ Data-Output Low-High	5.0 —	105 100	5.0 —	158 125	5.0 —	158 125	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 665 Ω. V_{CC} = 5.0 V, C_L = 15 pF.

5