F0109

Dual Path Ultra-Low Noise Amplifier 650MHz to 1000MHz

The F0109 is a dual-path 650MHz to 1GHz high gain/ultra-low noise amplifier used in receiver applications.

The F0109 LNA is operated as a *balanced amplifier* where the inputs and outputs are combined using external 90° couplers and provides 18dB of typical gain with 0.5dB of typical noise figure and 40dBm OIP3 performance. The device uses a single 5V supply and 115mA typical of total I_{CC}.

The F0109 is packaged in a 4 × 4 mm, 16-VFQFPN with 50Ω single-ended RF input and output impedances for ease of integration into the signal path.

Competitive Advantage

- Ultra-low noise performance of 0.5dB over wide bandwidths improves receiver sensitivity
- High gain and linearity

Features

- RF range: 650MHz to 1000MHz
  - F0110: 1500MHz to 2300MHz
  - F0111: 2500MHz to 2700MHz
- 18dB typical gain at 850MHz
- 0.5dB typical NF at 850MHz
- 40dBm typical OIP3 at 850MHz
- 50Ω single-ended input/output impedances
- +5V power supply
- I_{CC} = 58mA per channel
- Independent channel standby modes for power savings
- 1.8V logic standby control
- Operating temperature (T_{EP}) range: -40°C to +105°C
- 4 × 4 mm, 16-VFQFPN package

Applications

- 3G, 4G, 5G wireless infrastructure
- Public safety infrastructure
- General purpose RF

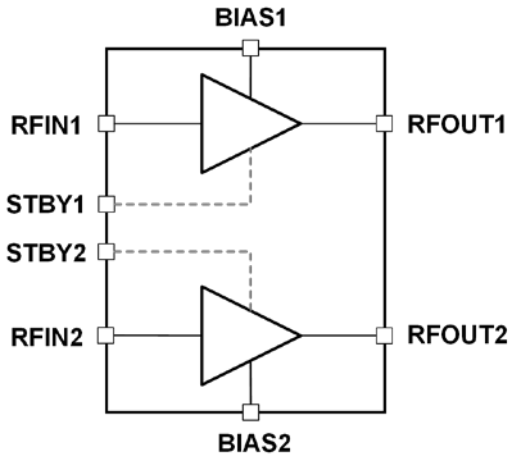

Figure 1. Block Diagram

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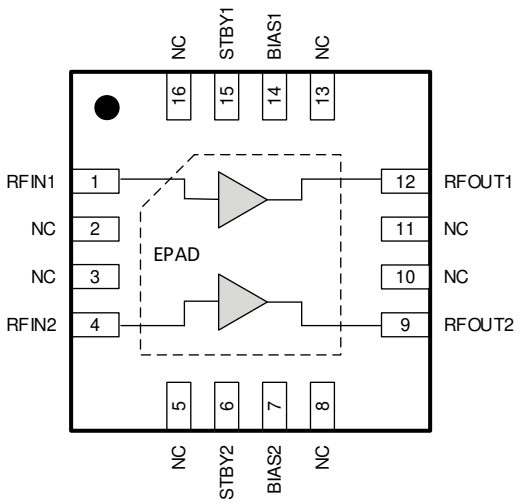
1. Pin Information

1.1 Pin Assignments



4 × 4 × 0.75 mm 16-VFQFPN Package
Top View

1.2 Pin Descriptions

Number	Name	Description
1	RFIN1	Path 1 RF input. Must use external DC block. DC block is also a tuning element and must be close to the pin for best RF performance.
4	RFIN2	Path 2 RF input. Must use external DC block. DC block is also a tuning element and must be close to the pin for best RF performance.
2, 3, 5, 8, 10, 11, 13, 16	NC	No internal connection. These pins can be left unconnected, or connected to ground (highly recommended). Use a via as close to the pin as possible if grounded.
6	STBY2	Standby pin for path 2. With Logic LOW applied to this pin (or if the pin is left unconnected), the amplifier on path 2 is powered ON. With Logic HIGH applied to this pin, the path 2 amplifier is Powered OFF and the path is in Standby mode. Pin is 1.8V logic compatible.
7	BIAS2	Path 2 voltage control.
9	RFOUT2	Path 2 RF output internally matched to 50Ω. An external pull-up inductor to a common V_{CC} is required to bias the amplifier. Must use an external DC block after the pull-up inductor. DC block is also a tuning element and must be close to the pin for best RF performance.
12	RFOUT1	Path 1 RF output internally matched to 50Ω. An external pull-up inductor to a common V_{CC} is required to bias the amplifier. Must use an external DC block after the pull-up inductor. DC block is also a tuning element and must be close to the pin for best RF performance.
14	BIAS1	Path 1 voltage control.
15	STBY1	Standby pin for path 1. With Logic LOW applied to this pin (or if the pin is left unconnected), the amplifier on path 1 is powered ON. With Logic HIGH applied to this pin, the path 1 amplifier is Powered OFF and the path is in Standby mode. Pin is 1.8V logic compatible.
–	EPAD	Exposed paddle. Internally connected to ground. Solder this exposed paddle to a Printed Circuit Board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

2. Specifications

2.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F0109 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions can affect device reliability.

Parameter	Symbol	Minimum	Maximum	Unit
V_{CC} to GND	V_{CC}	-0.3	+ 6.0	V
STBY1, STBY2	V_{CTL}	-0.3	+5.25	V
RFIN1, RFIN2 externally applied DC voltage	V_{RFIN}	- 0.3	+ 0.3	V
RFOUT1, RFOUT2 externally applied DC voltage	V_{RFOUT}	- 0.3	+ 6.0	V
ON STATE: RF CW Input Power (RFIN1, RFIN2) applied for 2 hours max. V_{CC} = 5V, T_{EP} = 105˚C, input / output VSWR < 2:1 based on a 50Ω system. [a]	$P_{MAX\_IN\_ON}$		20	dBm
OFF STATE: RF CW Input Power (RFIN1, RFIN2) applied for 2 hours max. V_{CC} = 5V, T_{EP} = 105˚C, input / output VSWR < 2:1 based on a 50Ω system. [a]	$P_{MAX\_IN\_OFF}$		20	dBm
Storage Temperature Range	T_{STOR}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		500	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}		500	V

[a] Exposure to these maximum RF levels can result in significantly higher I_{CC} current draw because of overdriving the amplifier stages.

2.2 Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Voltage [a]	V_{CC}		4.75		5.25	V
Operating Temperature Range	T_{EP}	Exposed paddle	-40		+105	°C
Junction Temperature	T_J				160	°C
RF Frequency Range	F_{RF}		650		1000	MHz
Maximum Operating RF Input Power to RFIN1, RFIN2 [b]	P_{MAX}				+5	dBm
RF Source Impedances	Z_{RFI}	Single-ended		50		Ω
RF Load Impedances	Z_{RFO}	Single-ended		50		Ω

[a] Functional voltage operating range. Device is designed to function with any supply voltage ≥ 4.75V, although performance may be degraded when operated outside the recommended voltage range.

[b] CW power over operating temperature, operating voltage, and operating frequency range. Input/output VSWR < 2:1.

2.3 Electrical Specifications

2.3.1. General

See the F0109 Typical Application Circuit. Specifications apply when operated as a dual RX LNA with V_{CC} = +5.0V, f_{RF} = 850MHz, T_{EP} = +25°C, STBY1 = STBY2 = Logic LOW, Z_S = Z_L = 50Ω, P_{OUT} = +5dBm/tone for two-tone parameters, two-tone spacing = 1MHz, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Logic Input High Threshold	V_{IH}		***1.17*** [a]		Lower of (V_{CC}, 5.25)	V
Logic Input Low Threshold	V_{IL}		-0.3		***0.63***	V
Logic Current High Threshold	I_{IH}		***5***		***250***	µA
Logic Current Low Threshold	I_{IL}		***-20***		***50***	µA
Quiescent Current	I_{CC_Q}	Single path		58	***80***	mA
		Both paths		115	***160***	mA
Standby Current	I_{CC_STBY}	STBY1 = STBY2 = HIGH		5	***15***	mA
Standby Switching Time	T_{ON}	50% STBY control to within 0.1dB of the on-state final gain value and 1 degree of final phase value		840		ns
	T_{OFF}	50% STBY control to I_{CC} < 10mA		250		ns

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

2.3.2. RF (Balanced Configuration) (0.65GHz to 1GHz) Performance

See the F0109 Typical Application Circuit. Specifications apply when operated as a dual RX LNA with V_{CC} = +5.0V, f_{RF} = 850MHz, T_{EP} = +25°C, STBY1 = STBY2 = Logic LOW, Z_S = Z_L = 50Ω, P_{OUT} = +5dBm/tone for two-tone parameters, two-tone spacing = 1MHz, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
RF Input Return Loss	RL_{IN}			23		dB
RF Output Return Loss	RL_{OUT}			21		dB
Gain	G		***16***	18	***20.5***	dB
Gain Flatness	G_{FLAT}	f_{RF} = 650MHz – 1000MHz Flatness referenced to Gain at band center		-1.4/+1.8		dB
Gain Variation over Temperature	G_{TEMP}	T_{EPAD} = -40°C to 105°C		-0.3/+0.4		dB
Reverse Isolation	ISO			27		dB
STBY Mode Gain	G_{STBY}			-25		dB
Noise Figure	NF	De-embedded to the input pin of the Hybrid Coupler		0.5	0.7	dB
Output IP3	OIP3	P_{OUT} = 5dBm/tone, Δf = 1MHz	37	40		dBm
Output P1dB	OP1dB		20	24		dBm
Stability	K	K-Factor V_{CC} = 4.75V – 5.25V T_{EP} = -40°C – 105°C f_{RF} = 10MHz – 20GHz	1			

[a] Specifications in the minimum/maximum columns that are shown in bold italics are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization using external matching BOM optimizing for 0.65GHz to 1.0GHz.

2.4 Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance.	θ_{JA}	95.6	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	$\theta_{JC\text{-}BOT}$	23.6	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

3. Typical Operating Conditions (TOC)

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- V_{CC} = 5.0V
- STBY = LOW
- f_{RF} = 850MHz
- $Z_L = Z_S$ = 50Ω single-ended
- P_{OUT} = 5dBm/tone (Two-tone parameters)
- 1MHz tone spacing
- 650MHz – 1000MHz tune specific application circuit
- All temperatures are referenced to the exposed paddle
- Evaluation Kit traces and connector losses are de-embedded

3.1 Typical Performance Characteristics

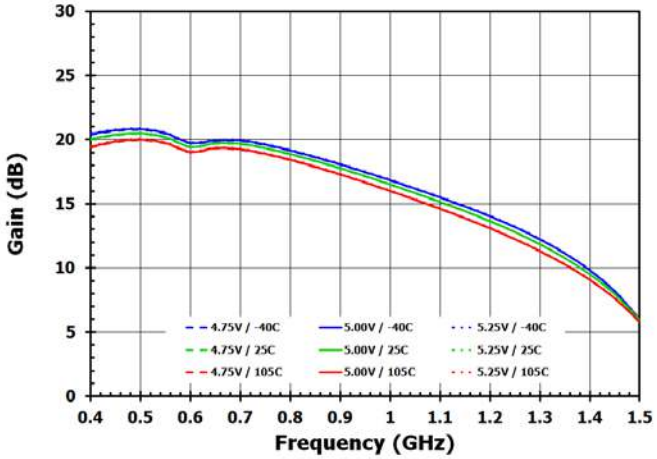


Figure 2. Gain

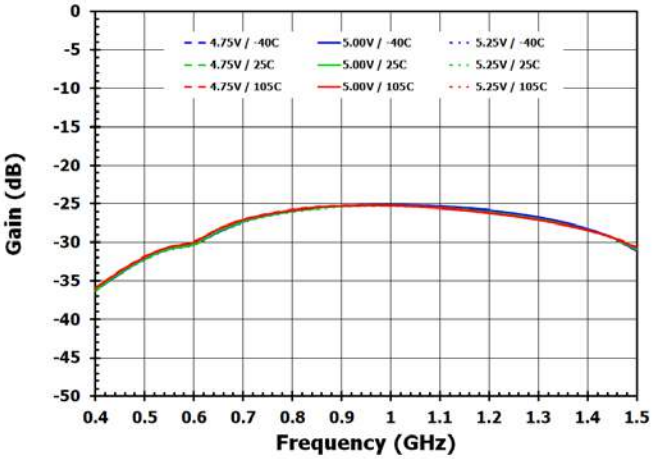


Figure 3. STBY Mode Gain

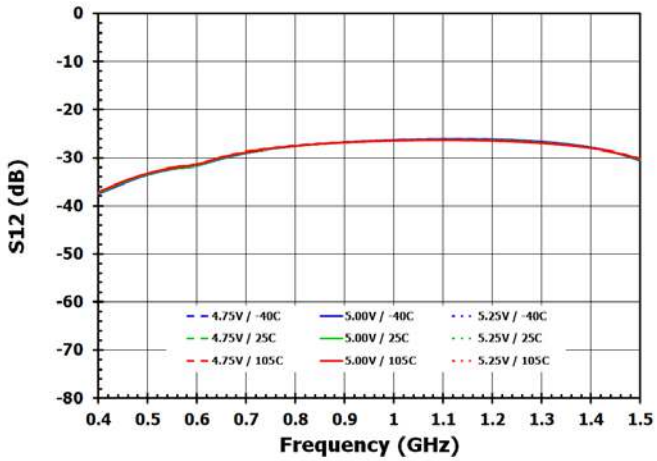


Figure 4. Reverse Isolation

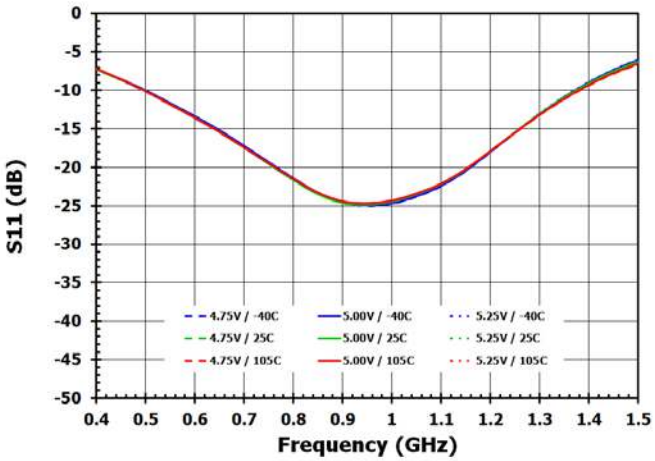


Figure 5. Input Return Loss

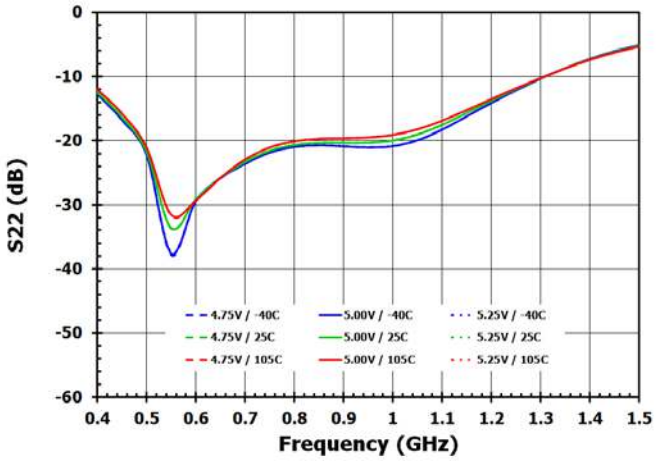


Figure 6. Output Return Loss

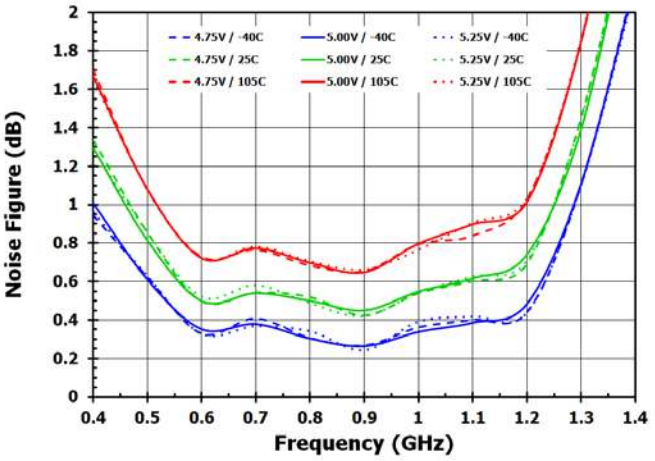


Figure 7. Noise Figure

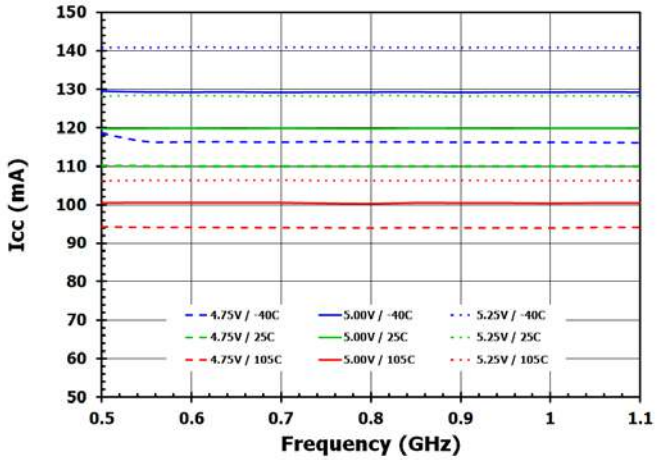


Figure 8. DC Current (I_{CC}) Vs Frequency

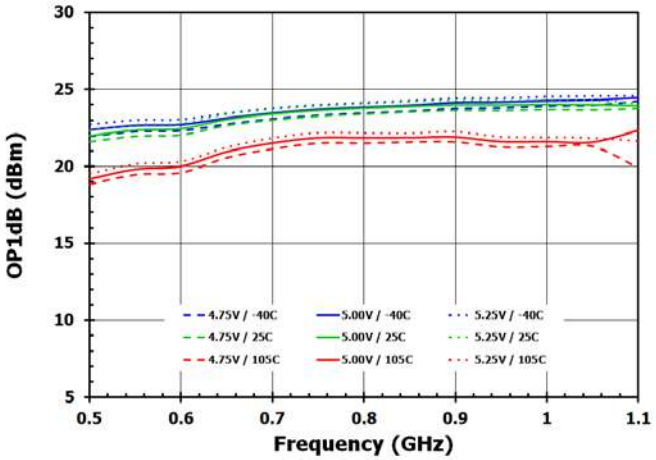


Figure 9. OP1dB

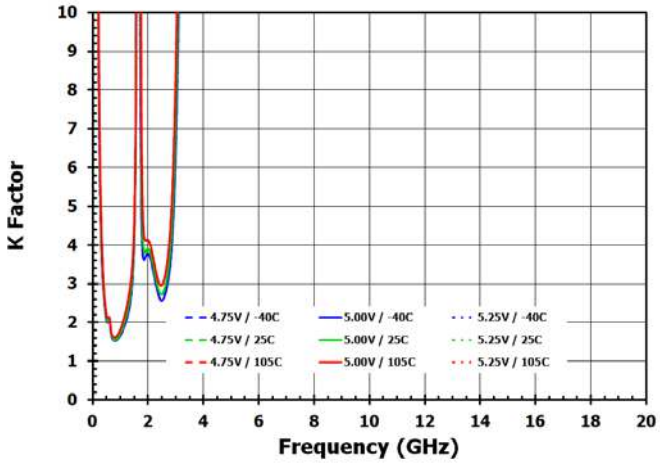


Figure 10. K Factor

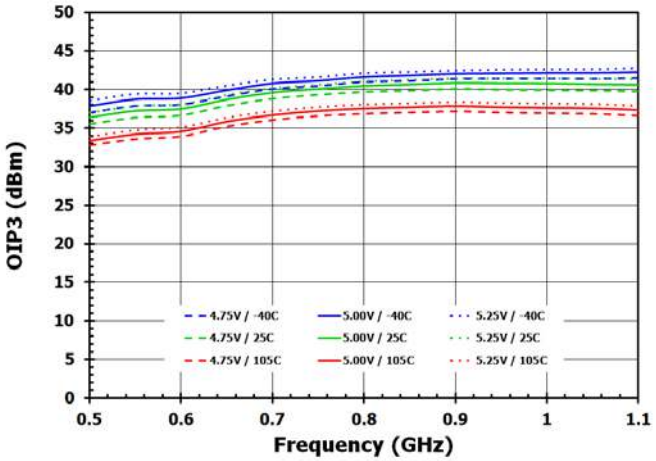


Figure 11: OIP3

4. Functional Description

4.1 Programming

The F0109 uses two dedicated control pins (STBY1 and STBY2) to place each respective signal path into its standby mode. The following section provide specific details on the functionality of each pin.

4.2 STBY Mode Programming

The F0109 allows for the independent shutdown of each signal path. Simply apply the logic shown in Table 1 below to control paths 1 and 2, respectively.

Table 1. STBY Mode Truth Table

Path	Pin	Logic	Path Power State
1	15/STBY1	Low	Path 1 Power On
		High	Path 1 Standby
2	6/STBY2	Low	Path 2 Power On
		High	Path 2 Standby

5. Evaluation Kit Information

5.1 Evaluation Kit Pictures

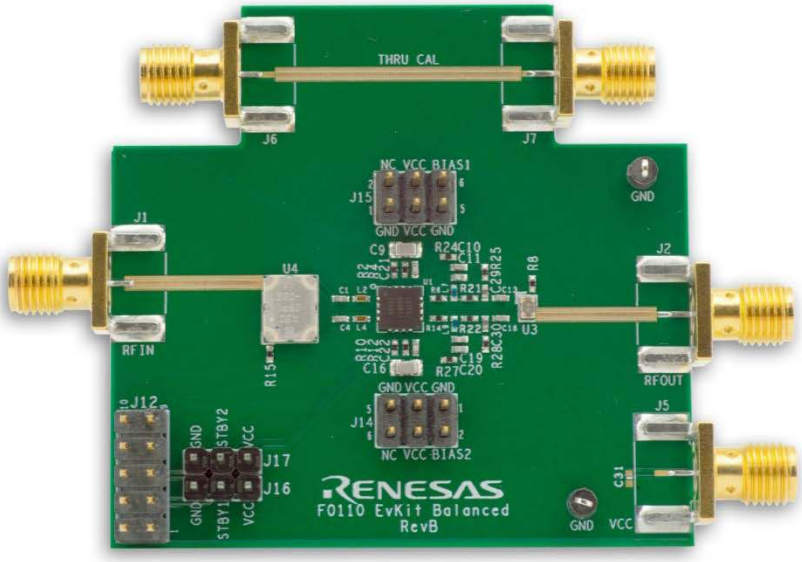


Figure 12. Top View

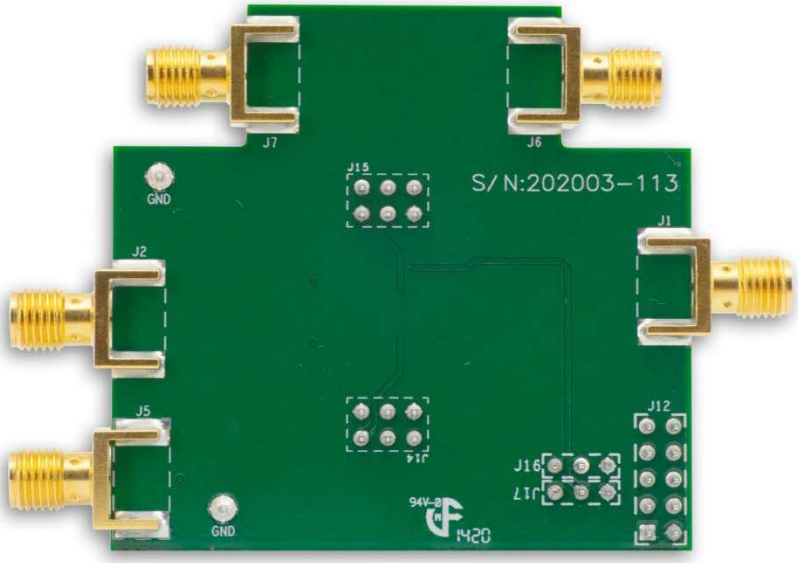


Figure 13. Bottom View

5.2 Evaluation Kit Schematic

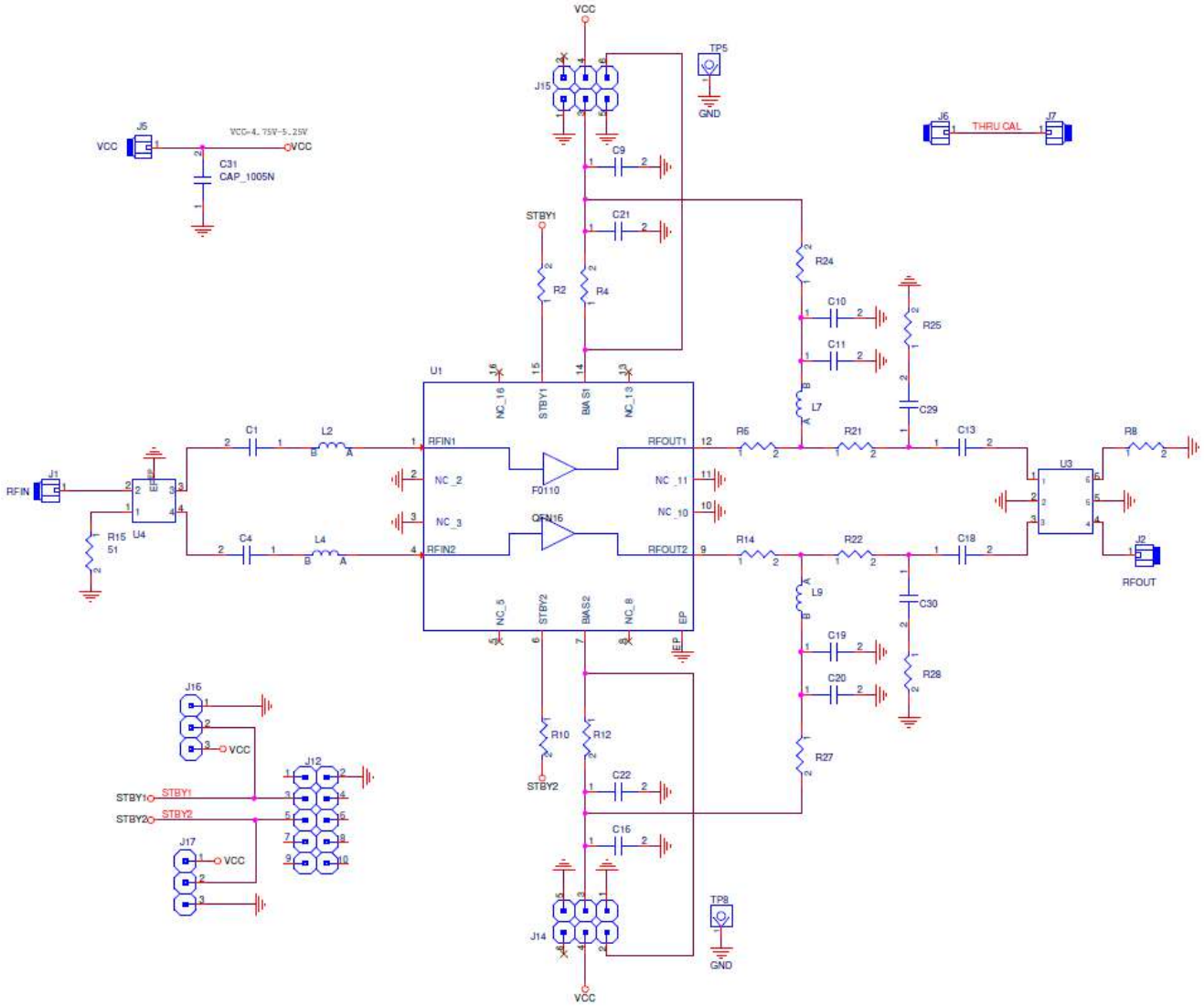


Figure 14. Electrical Schematic

Table 2. Bill of Materials (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1, C4, C13, C18	4	51pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H510J	Murata
C21, C22, C11, C19	4	100pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	Murata
C9, C16	2	10,000pF ±10% 50V Ceramic Capacitor X7R (0805)	GRM216R71H103KA	Murata
C10, C20	2	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	Murata
C29, C30	2	1.2pF ±0.05pF, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H1R2W	Murata
L2, L4	2	1.2nH ±5%, Inductor (0402)	LQP15MN1N2B02	Murata
L7, L9	2	12nH ±5%,Inductor 0402	0402CT-12NXJR	Coilcraft
R8, R15	2	51Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF51R0X	Panasonic
R4, R12	2	806Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF8060X	Panasonic
R2, R6, R10, R14, R21, R22	6	0Ω Resistors (0402)	ERJ-2GE0R00X	Panasonic
R24, R25, R27, R28	4	0Ω Resistors (0402)	ERJ-2GE0R00X	Panasonic
U4	1	Hybrid Coupler	X3C09P1-03S	Anaren
U3	1	Hybrid Coupler	C0810J5003AHF	Anaren
U1	1	F0109	Renesas	Renesas
J14, J15	2	CONN HEADER VERT DBL 3 X 2 POS GOLD		3M
J12	1	CONN HEADER VERT DBL 5 X 2 POS GOLD	961210-6404-AR	3M
J17, J18		CONN HEADER VERT DBL 3 X 1 POS GOLD		3M
J1, J2, J5, J6, J7	5	Edge Launch SMA (0.375inch pitch ground tab) (50Ω)	142-0701-851	Emerson Johnson
	1	Printed Circuit Board (Rev B)	Renesas	Renesas
C31	1	DNP		

5.3 Evaluation Kit Operation

5.3.1. Power Supply Setup

Set up a power supply in the voltage range of 4.75V to 5.25V with the power supply output disabled. The voltage can be applied using one of the following connections:

- Directly to the J5 SMA and connecting Pins 3 and 4 together on both J14 and J15.
- Directly to Pin 3 on both J14 and J15.

5.3.2. Power-On Procedure

Set up the voltage supplies, and Evaluation Board as described in the Power Supply Setup section and Enable the V_{CC} supply. Make sure the correct logic voltage is applied to the STBY pins on each path as defined in Table 1.

5.3.3. Power-Off Procedure

Disable the V_{CC} supply.

6. Application Information

The F0109 has been optimized for use in high performance RF applications ranging from 0.65GHz to 1GHz.

6.1 Power Supplies

Use a common V_{CC} power supply for all pins requiring DC power. Bypass all supply pins with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change, or transients should have a slew rate smaller than 1V/20µs. In addition, keep all control pins at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

6.2 Startup Condition

At device power-up, both channels default to the power state as determined by the logic present on the STBY1 and STBY2 pins.

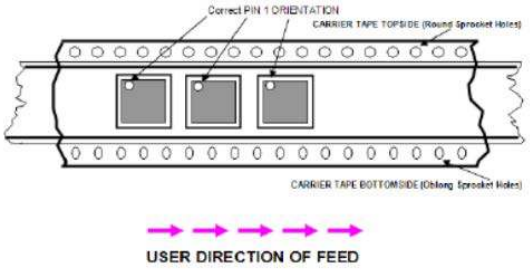
7. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

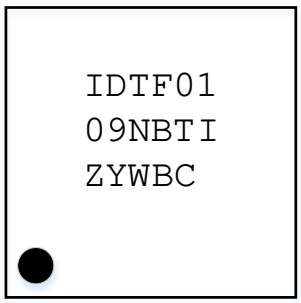
8. Ordering Information

Part Number	Package Description	MSL Rating	Carrier type	Temp. Range
F0109NBTI	4 × 4 × 0.75 mm 16-VFQFPN	1	Tray	-40° to +105°C
F0109NBTI8	4 × 4 × 0.75 mm 16-VFQFPN	1	Tape and Reel	-40° to +105°C
F0109EVB	Evaluation Board			

Table 3. Pin1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
BTI8	Quadrant 1 (EIA-481-C)	

9. Marking Diagram



- Lines 1 and 2 are the part number.
- Line 2:
  - “NBT” is for package code.
  - “I” is for Industrial grade.
- Line 3:
  - “Z” is for die version.
  - “YW” are for year and week that the part was assembled.
  - “BC” is for assembly lot number

10. Revision History

Revision	Date	Description
1.03	Jan 13, 2022	• Added Tape and Reel Information (Table 3).
1.02	Aug 11, 2021	• Modified the pin descriptions of 2, 3, 10, 11 to NC, and updated the relevant pin map and symbol in schematic to NC (see Pin Information). • Completed other minor changes.
1.01	Oct 14, 2020	Updated RF Performance table and Typical Performance Characteristics.
1.00	Aug 28, 2020	Initial release.

16-VFQFPN, Package Outline Drawing

4.0 x 4.0 x 0.75 mm Body,0.65mm Pitch,Epad 2.50 x 2.50 mm

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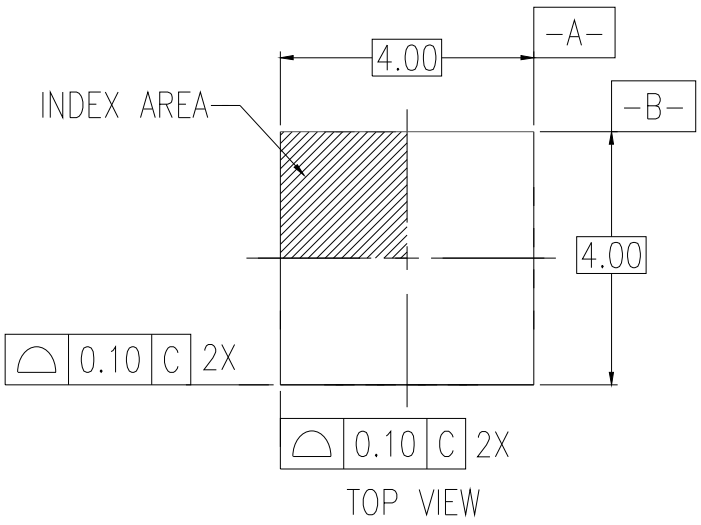
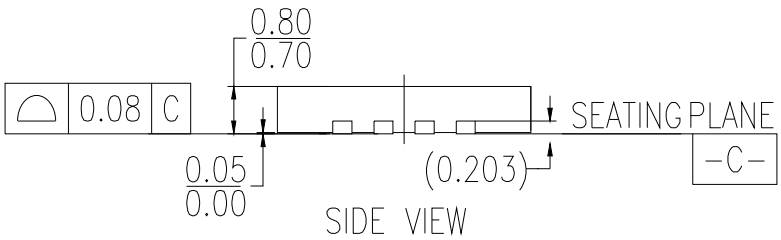
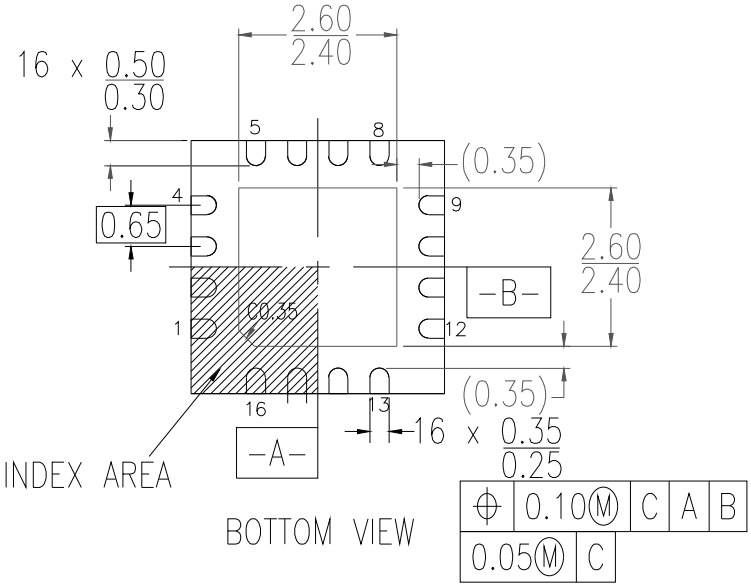


TOP VIEW



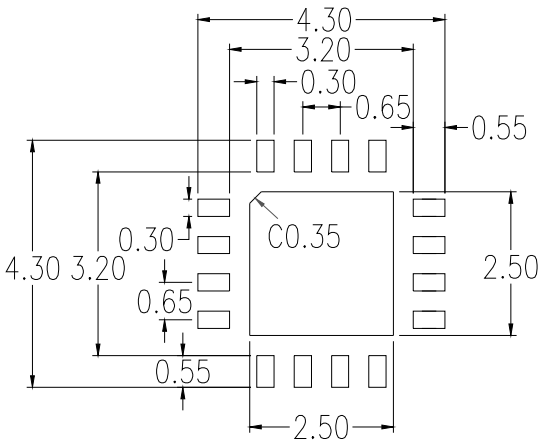
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS IN MM.
2. THE DIMENSION AND TOLERANCING MEET ASME Y-14.5M-1994



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS IN MM.ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS IVIEW ON PCB.
3. LAND PATTERN RECOMMENDATION AS PER IPC-7351B.
   GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
June 13, 2021	Rev 01	Coplanarity change and update to Renesas Logo
May 06, 2019	Rev 00	Initial Release

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