

# HIGH POWER SP4T SWITCH GaAs MMIC

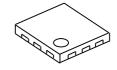
#### ■ GENERAL DESCRIPTION

The NJG1684ME2 is a GaAs SP4T switch MMIC suitable for LTE/UMTS/CDMA/GSM applications.

The NJG1684ME2 features very low insertion loss, high isolation and excellent linearity performance down to 1.8V control voltage at high frequency up to 2.7GHz. In addition, this switch is able to handle high power signals.

The NJG1684ME2 has ESD protection devices to achieve excellent ESD performances. No DC Blocking capacitors are required for all RF ports unless DC is biased externally. And the ultra small & ultra thin EQFN12-E2 package is adopted.

#### PACKAGE OUTLINE



NJG1684ME2

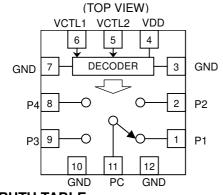
#### ■ APPLICATIONS

LTE, UMTS, CDMA, GSM applications Post PA Switching, Antenna Switching and Bands Switching applications General Purpose Switching applications

#### ■ FEATURES

- Low voltage logic control V<sub>CTL(H)</sub>=1.8V typ. V<sub>DD</sub>=2.7V typ. • Low voltage operation Low distortion IIP3=+70dBm typ. @f=829+849MHz, P<sub>IN</sub>=24dBm IIP3=+69dBm typ. @f=1870+1910MHz, P<sub>IN</sub>=24dBm 2nd harmonics=-80dBc typ. @f=0.9GHz, PIN=35dBm 3rd harmonics=-77dBc typ. @f=0.9GHz, PIN=35dBm 0.25dB typ. @f=0.9GHz, PIN=35dBm, VDD=2.7V Low insertion loss 0.30dB typ. @f=1.9GHz, PIN=33dBm, VDD=2.7V 0.35dB typ. @f=2.7GHz, PIN=27dBm, VDD=2.7V 36dBm min.
- P-0 1dB
- Ultra small & ultra thin package EQFN12-E2 (Package size: 1.8 x 1.8 x 0.397mm)
- RoHS compliant and Halogen Free, MSL1

#### ■ PIN CONFIGURATION



Pin connection 1. P1 7. GND 8. P4 2. P2 3. GND 9. P3 4. VDD 10. GND 5. VCTL2 11. PC 6. VCTL1 12. GND Exposed PAD: GND

#### ■ TRUTH TABLE

"H"=V <sub>CTL(H)</sub> , "L"=V <sub>CTL(L)</sub>			
VCTL1	VCTL2	Path	
L	L	PC-P1	
Н	L	PC-P2	
L	Н	PC-P3	
Н	Н	PC-P4	

NOTE: Please note that any information on this catalog will be subject to change.

#### ■ ABSOLUTE MAXIMUM RATINGS

 $T_a=+25^{\circ}C, Z_s=Z_l=500hm$ SYMBOL RATINGS UNITS PARAMETER CONDITIONS V<sub>DD</sub> =2.7V, V<sub>CTL</sub>=0/1.8V **RF Input Power**  $\mathsf{P}_{\mathsf{IN}}$ 37 dBm V Supply Voltage  $V_{\text{DD}}$ VDD terminal 5.0 **Control Voltage**  $V_{\text{CTL}}$ VCTL1, VCTL2 terminal 5.0 ٧ Four-layer FR4 PCB with through-hole 1200 **Power Dissipation**  $P_{D}$ mW (101.5x114.5mm), Tj=150°C °C Operating Temp. Topr -40~+85 °C Storage Temp. -55~+150 T<sub>stg</sub>

#### ■ ELECTRICAL CHARACTERISTICS 1 (DC)

(General conditions:  $T_a=+25^{\circ}C$ ,  $Z_s=Z_I=50$  ohm,  $V_{DD}=2.7V$ ,  $V_{CTL(H)}=1.8V$ ,  $V_{CTL(L)}=0V$ , with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{DD}$	VDD Terminal	2.375	2.7	5.0	V
Operating Current	I <sub>DD</sub>	No RF input	-	180	400	μA
Control Voltage (LOW)	V <sub>CTL(L)</sub>	VCTL1, VCTL2 Terminal	0	-	0.45	V
Control Voltage (HIGH)	V <sub>CTL(H)</sub>	VCTL1, VCTL2 Terminal	1.35	1.8	5.0	v
Control Current	Ictl	V <sub>CTL(H)</sub> =1.8V	-	4	10	μA

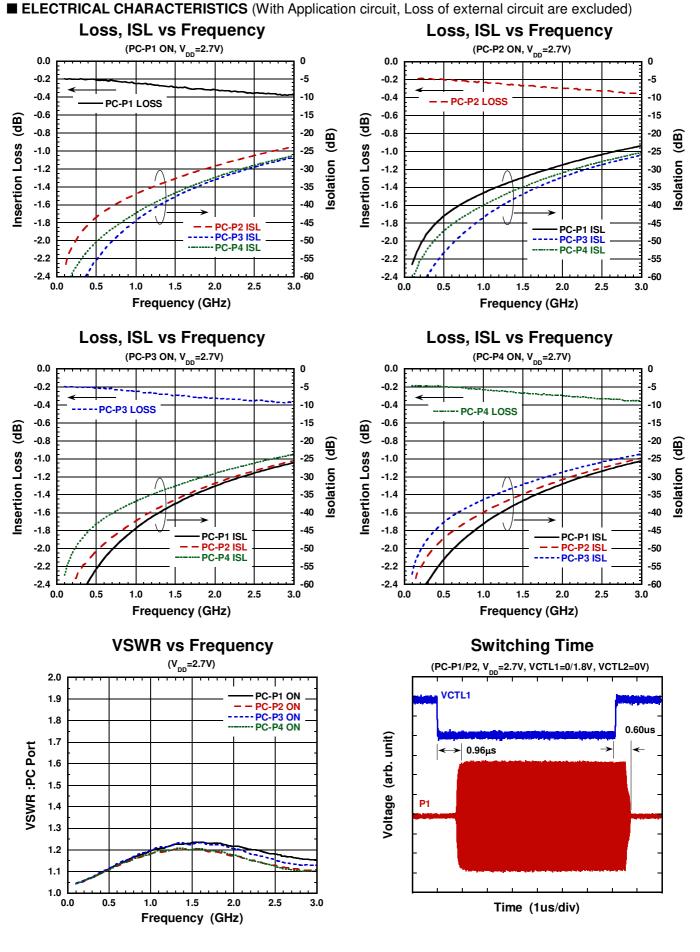
# NJG1684ME2

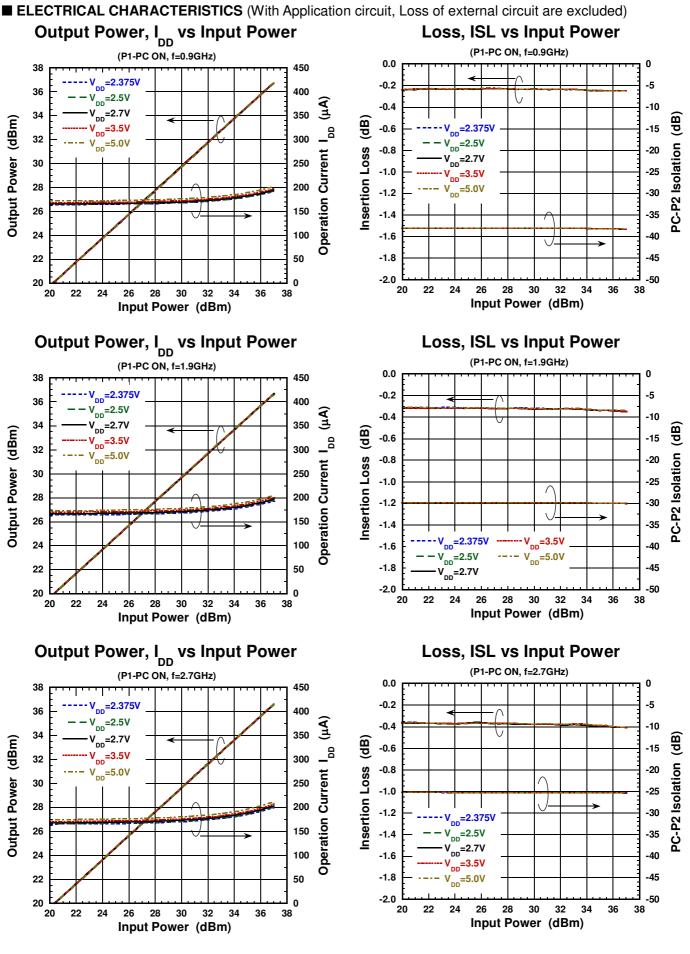
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss 1	LOSS1	f=0.9GHz, P <sub>IN</sub> =35dBm	-	0.25	0.40	dB
Insertion Loss 2	LOSS2	f=1.9GHz, P <sub>IN</sub> =33dBm	-	0.30	0.45	dB
Insertion Loss 3	LOSS3	f=2.7GHz, P <sub>IN</sub> =27dBm	-	0.35	0.50	dB
Isolation 1	ISL1	f=0.9GHz, P <sub>IN</sub> =35dBm	30	37	-	dB
Isolation 2	ISL2	f=1.9GHz, P <sub>IN</sub> =33dBm	25	29	-	dB
Isolation 3	ISL3	f=2.7GHz, P <sub>IN</sub> =27dBm	22	25	-	dB
Input Power at 0.1dB Compression Point	P-0.1dB	f=0.9GHz, 1.9GHz, 2.7GHz	36	-	-	dBm
2nd Harmonics 1	2fo(1)	f=0.9GHz, P <sub>IN</sub> =35dBm	-	-80	-70	dBc
2nd Harmonics 2	2fo(2)	f=1.9GHz, P <sub>IN</sub> =33dBm	-	-80	-70	dBc
2nd Harmonics 3	2fo(3)	f=2.7GHz, P <sub>IN</sub> =27dBm	-	-90	-70	dBc
3rd Harmonics 1	3fo(1)	f=0.9GHz, P <sub>IN</sub> =35dBm	-	-77	-70	dBc
3rd Harmonics 2	3fo(2)	f=1.9GHz, P <sub>IN</sub> =33dBm	-	-77	-70	dBc
3rd Harmonics 3	3fo(3)	f=2.7GHz, P <sub>IN</sub> =27dBm	-	-90	-70	dBc
Input 3 <sup>rd</sup> order intercept point1	IIP3(1)	f=829+849MHz, P <sub>IN</sub> =24dBm each *1	+65	+70	-	dBm
Input 3 <sup>rd</sup> order intercept point2	IIP3(2)	f=1870+1910MHz, P <sub>IN</sub> =24dBm each *1 +63 +69		+69	-	dBm
VSWR	VSWR	R On-state ports, f=2.7GHz - 1.2		1.4		
Switching time	Tsw	50% V <sub>CTL</sub> to 10/90% RF	-	1.0	5.0	μS

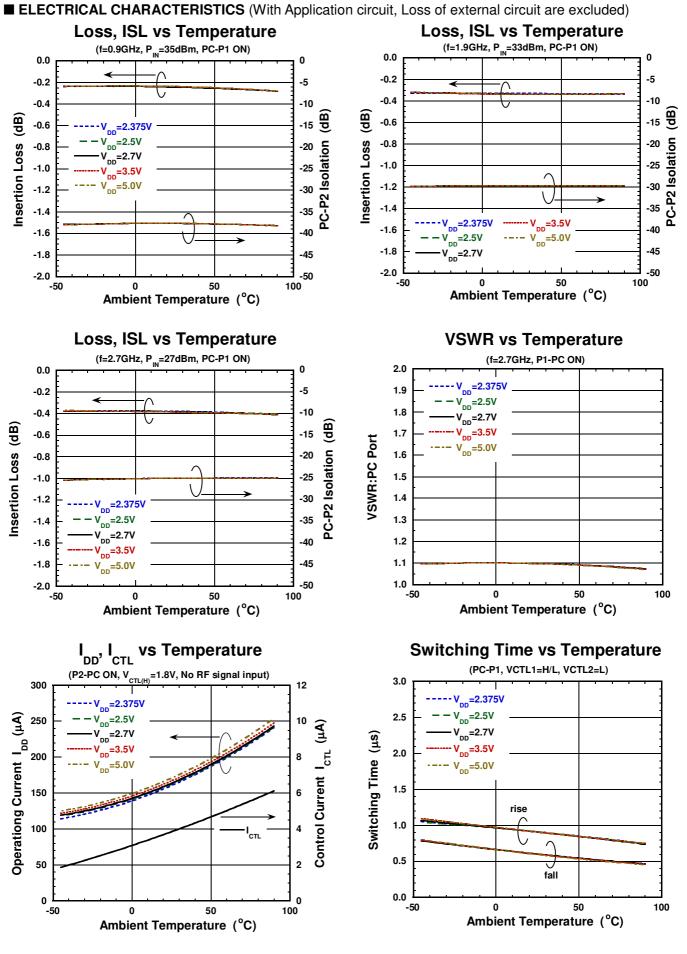
\*1: IIP3 are defined by the following equations. IIP3=(3 x Pout-IM3)/2+LOSS

#### ■ TERMINAL INFORMATION

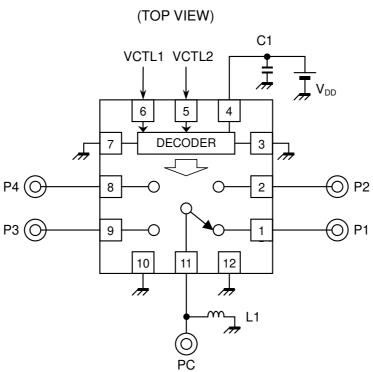
No.	SYMBOL	DESCRIPTION		
1	P1	RF transmitting/receiving port.		
2	P2	RF transmitting/receiving port.		
3	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.		
4	VDD	Positive voltage supply terminal. The positive voltage (+2.375~+5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.		
5	VCTL2	Control signal input terminal. This terminal is set to High-Level (+1.35~+5.0V) or Low-Level (0~+0.45V).		
6	VCTL1	Control signal input terminal. This terminal is set to High-Level (+1.35~+5.0V) or Low-Level (0~+0.45V).		
7	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.		
8	P4	RF transmitting/receiving port.		
9	P3	RF transmitting/receiving port.		
10	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.		
11	PC	RF transmitting/receiving port. Please connect an inductor with GND terminal for ESD protection.		
12	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.		
Exposed Pad	GND	Ground terminal.		







#### ■ APPLICATION CIRCUIT



#### PRECAUTIONS

[1] The Inductor L1 is required for enhancing ESD protection level.

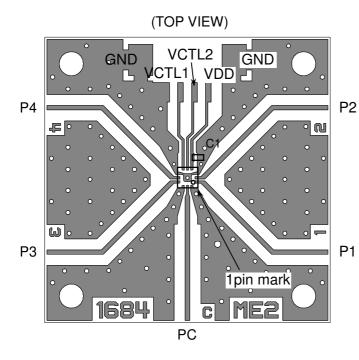
[2] All RF terminals are biased DC GND level.

[3] No DC block capacitors are required for RF ports unless DC is biased externally.

#### ■ PARTS LIST

No.	Parameters	Note
C1	1000pF	MURATA (GRM15)
L1	68nH	TAIYO-YUDEN (HK1005)

### PCB LAYOUT

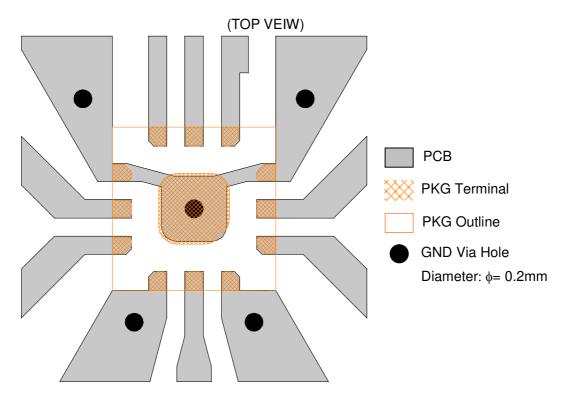


FR-4, t=0.2mm
1005
0.4mm
26 x 26mm

Losses of PCB and connectors, Ta=+25°C

Frequency (GHz)	Loss (dB)
0.9	0.27
1.9	0.50
2.7	0.61

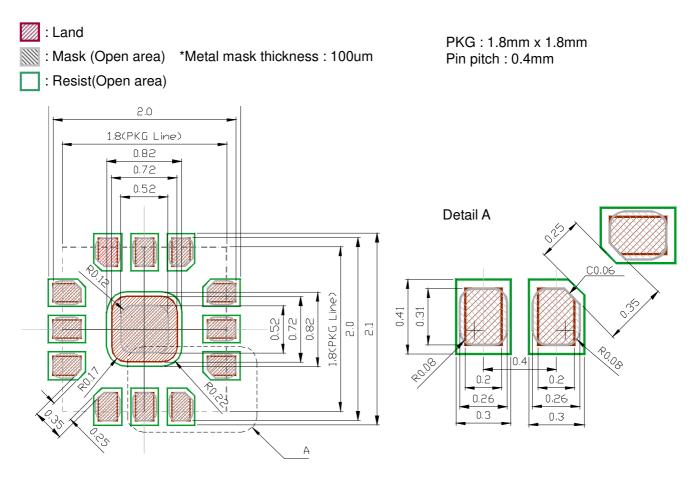
#### <PCB LAYOUT GUIDELINE>



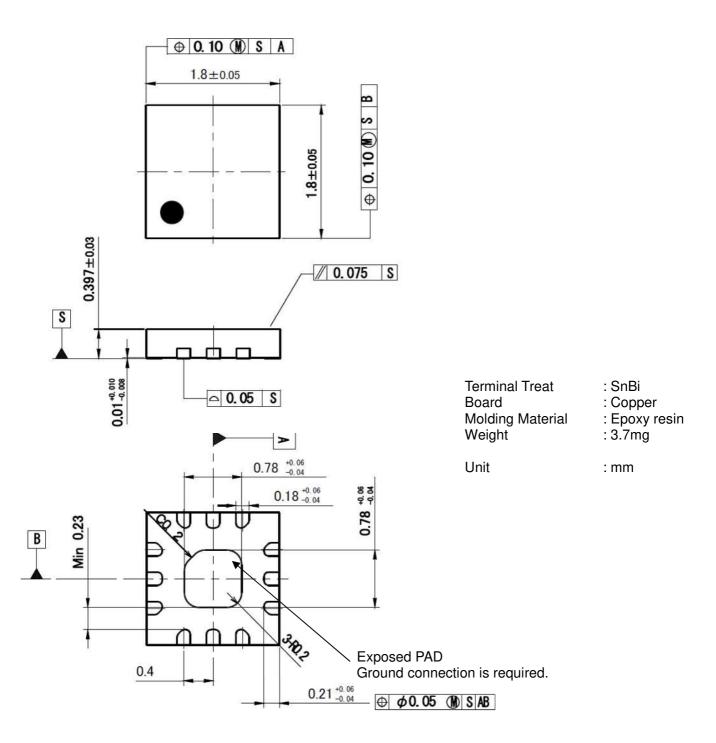
#### ■ PRECAUTIONS

- [1] No DC block capacitors are required for RF ports unless DC is biased externally. When the other device is biased at certain voltage and connected to the NJG1684ME2, a DC block capacitor is required between the device and the switch IC. This is because the each RF port of NJG1684ME2 is biased at 0 V (GND).
- [2] For good RF performance, all GND terminals must be connected to PCB ground plane of substrate, and via-holes for GND should be placed near the IC.
- [3] For good RF performance, through-holes for GND should be placed close to the GND pin 6 and pin 13. One of the ways to do this is to place a via-hole at the TAB pad under this IC.

### ■ RECOMMENDED FOOTPRINT PATTERN (EQFN12-E2 PACKAGE Reference)



#### ■ PACKAGE OUTLINE (EQFN12-E2)



#### Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

[CAUTION]

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  - Equipment Used in the Deep Sea
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  - Combustion equipment

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- 7. The products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this datasheet. Failure to employ the products in the proper applications can lead to deterioration, destruction or failure of the products. We shall not be responsible for any bodily injury, fires or accident, property damage or any consequential damages resulting from misuse or misapplication of the products.
- 8. Quality Warranty
  - 8-1. Quality Warranty Period

In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.

8-2. Quality Warranty Remedies

When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.

- Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
- 8-3. Remedies after Quality Warranty Period

With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.

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- 10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
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- 12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
- 13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.



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