Motor Driver IC Series for Printers

Three-phase Brushless Motor pre-driver for Paper Feed Use

BA6680FS, BD6761FS, BD6762FV

●**Description**

This product is a motor predriver for high-side/low-side N-channel MOS-FET with a built-in boost (step-up) driver. BA6680FS and BD6761FS are controlled by the external servo signal. The BD6762FV incorporates a servo circuit (Speed discriminator + PLL servo).

●**Features**

1) Predriver for high-side/low-side N-channel MOS-FET
2) Built-in boost (step-up) circuit
3) Built-in FG and hysteresis amplifiers
4) Built-in current limit circuit
5) Built-in thermal shutdown circuit
6) Built-in forward/reverse rotation switching circuit (BD6761FS, FD6762FV)
7) Built-in short brake circuit (BD6761FS, BD6762FV)
8) Built-in low voltage protection circuit (BD6761FS, BD6762FV)
9) Built-in speed lock detection circuit (BD6762FV)
10) Built-in motor lock protection circuit (BD6762FV)
11) Built-in start-stop circuit (BD6762FV)
12) Built-in servo circuit (Speed discriminator + PLL) (BD6762FV)
13) Built-in frequency multiplication circuit (BD6762FV)
14) 120°, direct PWM drive (BA6680FS)
15) 180°, direct PWM drive (BD6761FS)
16) 120°, slope switchable direct PWM drive (BD6762FV)

●**Applications**

Main paper feed motor for laser printer and PPC

●**Absolute maximum ratings** (Ta=25℃)

Parameter	Symbol	Limit			Unit
		BA6680FS	BD6761FS	BD6762FV	
Applied voltage	VCC	36	36	36	V
Applied voltage	VG	36	36	36	V
Pin input voltage	Vin	VREG	VREG	VREG	V
Power dissipation	Pd	950(※1)	950(※1)	1100(※2)	mW
Operating temperature range	T_{OPR}	-25～+75	-35～+75	-25～+75	℃
Storage temperature range	T_{STG}	-40～+150	-40～+150	-40～+150	℃
Junction temperature	Tjmax	150	150	150	℃

※1 Reduced by 7.6 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

※2 Reduced by 8.8 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

●**Product lineup**

	BA6680FS	BD6761FS	BD6762FV	Unit
Power supply voltage (VCC)	16~28	16~28	16~28	V
Drive type	120°	180°	120° / 120° slope	—
Servo	No	No	Yes	—

●**Electrical Characteristics**

BA6680FS (Unless otherwise specified, Ta=25°C, VCC=25.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Overall						
Circuit current	ICC	11.7	15.7	19.7	mA	
VREG voltage	VREG	5.4	5.9	6.4	V	IVREG=-1mA
Hall amp						
Input bias current	IHA	-3.0	-0.7	–	μA	
In-phase input voltage range	VHAR	1.0	–	4.9	V	
Minimum input level	VINH	50	–	–	mVpp	
Hysteresis level	VHYS	10	20	30	mV	
PWM						
High output voltage	VHPCFE	3.8	4.3	4.8	V	
Low output voltage	VLPCFE	1.9	2.3	2.7	V	
Oscillating frequency (reference values)	FCFE	12.0	15.5	19.0	kHz	Rfe=50kΩ, Cfe=100pF
Pref. input current: High	IPREFH	–	0.05	1	μA	
Pref. input current: Low	IPREFL	-1	0	–	μA	
PWM on duty relative error	DPWM	-1.5	0	1.5	%	Rfe=50kΩ, Cfe=100pF
FG amp						
Input bias current	IBFG	-1	–	1	μA	
Input offset voltage	VBFG	-10	–	10	mV	
High output voltage	VHFG	4.5	5.0	–	V	IHFGOUT=-2mA
Low output voltage	VLFG	–	1.0	1.5	V	ILFGOUT=2mA
Low FGs output voltage	VLFGS	–	0.1	0.3	V	ILFGSOUT=3mA
Open loop gain	GVFG	45	54	–	dB	
Bias voltage	VBIASFG	2.7	3.0	3.3	V	
Hysteresis width	VHYS	100	180	250	mV	
ACC and DEC						
High ACC input current	IACCH	–	0	1	μA	ACC=5V
Low ACC input current	IACCL	-3.0	-0.5	–	μA	ACC=0V
High DEC input current	IDECH	–	0	1	μA	DEC=5V
Low DEC input current	IDECL	-3.0	-0.5	–	μA	DEC=0V
Accelerating current	ISS	147	210	273	μA	RCP=13.5kΩ
Decelerating current	ISO	-286	-220	-154	μA	RCP=13.5kΩ
High-level ACC input	VIHACC	2.0	–	–	V	
Low-level ACC input	VILACC	–	–	0.8	V	
High-level DEC input	VIHDEC	2.0	–	–	V	
Low-level DEC input	VILDEC	–	–	0.8	V	
Current limit						
Current detection voltage	VCL	0.342	0.38	0.418	V	
High-side output						
High-side voltage	VHG	Vcc+6	Vcc+7	Vcc+8	V	
Pull-down resistor	RHD	70	100	130	kΩ	
Low-side output						
Low-side voltage	VLG	9.5	10.5	11.5	V	
Pull-up resistor	RLU	14	20	26	kΩ	
Charge pump oscillator						
Oscillating frequency	FOSC	65	95	125	kHz	OSC=100pF
Charge pump voltage	VG	Vcc+6	Vcc+7	Vcc+8	V	

BD6761FS (Unless otherwise specified, Ta=25°C, VCC=24.0V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Overall						
Circuit current	ICC	10	15	20	mA	
VREG voltage	VREG	5.5	6	6.5	V	IVREG=-1mA
Hall amp						
Input bias current	IHA	–	0.7	3.0	uA	
In-phase input voltage range	VHAR	1.5	–	4.1	V	
Input level	VINH	30	–	250	mVpp	Single-phase Hall amplitude
PWM						
High CFE voltage	VHPCFE	3.0	3.5	4.0	V	
Low CFE voltage	VLPCFE	2.1	2.5	2.9	V	
CFE oscillating frequency	FCFE	12	15	18	kHz	RFE=50kΩ, CFE=1000pF
PWM on duty offset	DPWM	-1.5	0	1.5	%	
Torque amplifier						
High CPOUT input current	ICPOUTH	–	0	1	uA	
Low CPOUT input current	ICPOUTL	-1	0	–	uA	
Current limit						
Current detection voltage 1	VCL1	0.391	0.435	0.479	V	For current sense amplifier
Current detection voltage 2	VCL2	0.432	0.480	0.528	V	For current limit comparator
VCL2-VCL1	ΔVCL	40	45	50	mV	
FG Amp						
Input bias current	IBFG	-1	–	1	uA	
Input offset voltage	VBFG	-10	–	10	mV	
High output voltage	VHFG	4.5	5.0	VREG	V	IHFGOUT=-0.75mA
Low output voltage	VLFG	–	1.0	1.5	V	ILFGOUT=2mA
Low FGS output voltage	VLFGS	–	0.1	0.3	V	ILFGSOUT=3mA
Open loop gain	GVFG	45	54	–	dB	f=3kHz
Bias voltage	VBIASFG	2.7	3.0	3.3	V	
Hysteresis width	VHYS	100	180	250	mV	
F/R						
High input current	IFRL	30	60	90	uA	F/R=6V
Low input current	IFRH	-10	0	10	uA	F/R=0V
High input level	VIHFR	2.2	–	VREG	V	Reverse rotation
Low input level	VILFR	0	–	0.8	V	Forward rotation
ACC and DEC						
High ACC input current	IACCH	30	60	90	uA	ACC=6V
Low ACC input current	IACCL	-10	0	10	uA	ACC=0V
High DEC input current	IDECH	30	60	90	uA	DEC=6V
Low DEC input current	IDECL	-10	0	10	uA	DEC=0V
Accelerating current	ISS	-260	-200	-140	uA	RCP=13.5kΩ, ACC=L
Decelerating current	ISO	140	200	260	uA	RCP=13.5kΩ, DEC=L
High ACC input level	VIHACC	2.2	–	VREG	V	
Low ACC input level	VILACC	0	–	0.8	V	
High DEC input level	VIHDEC	2.2	–	VREG	V	
Low DEC input level	VILDEC	0	–	0.8	V	
High-side output						
High-side voltage	VHG	Vcc+5	Vcc+6	Vcc+7	V	
Pull-down resistor	RHD	70	100	130	kΩ	
Low-side output						
Low-side voltage	VLG	9.5	10.5	11.5	V	
Pull-down resistor	RLD	70	100	130	kΩ	
Booster						
Boost voltage	VG	Vcc+5	Vcc+6	Vcc+7	V	
CP1 oscillating frequency	FCP1	35	62.5	85	kHz	

BD6762FV (Unless otherwise specified, Ta=25°C, VCC=24V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Overall						
Circuit current 1	ICCS	5.1	7.6	10.2	mA	ST/SP=OPEN
Circuit current 2	ICC	10	17	25	mA	ST/SP=GND
VREG voltage	VREG	4.5	5	5.5	V	IVREG=-1mA
Low voltage protection level	VUVON	9.5	11.5	13.5	V	
Low voltage protection hysteresis level	VUVHYS	0.4	0.5	0.6	V	
Hall amp						
Input bias current	IBH	–	1	3	μA	
In-phase input voltage range	VHAR	0	–	3	V	
Input level	VINH	50	–	–	mVp-p	
PWM						
High CFE voltage	VCFEH	2.6	2.9	3.2	V	
Low CFE voltage	VCFEL	1.2	1.4	1.6	V	
CFE oscillating frequency	FCFE	13	16	19	kHz	RFE=20K, CFE=1000pF
REF voltage	VRFE	0.75	0.95	1.15	V	
FG amp						
Input bias current	IFGM	-1	–	1	μA	
Input offset voltage	VFGOF	-10	–	10	mV	
High output voltage	VFGOH	3.5	4.0	–	V	I=-0.5mA
Low output voltage	VFGOL	–	1.0	1.5	V	I=0.5mA
Low FGS output voltage	VFGSL	–	0.1	0.3	V	I=2mA
Open loop gain	GFG	45	54	–	dB	f=3kHz
Bias voltage	VBFG	2.25	2.50	2.75	V	
Hysteresis width	VFGHYS	100	180	250	mV	
Integration amp						
Di clamp voltage 1	VDI1	1.5	2.1	2.7	V	INTIN=0.1mA
Di clamp voltage 2	VDI2	0.5	0.7	0.9	V	INTOUT=0.1mA
Bias voltage	VBERR	2.25	2.50	2.75	V	INTIN=INTOUT
Speed discriminator						
High output voltage	VDOH	VREG-0.3	VREG-0.1	–	V	I=-0.1mA
Low output voltage	VDOL	–	0.1	0.3	V	I=0.1mA
PLL						
High output voltage	VPOH	VREG-0.45	VREG-0.15	–	V	I=-0.1mA
Low output voltage	VPOL	–	0.15	0.45	V	I=0.1mA
Lock detection						
Low output voltage	VLDL	–	0.15	0.3	V	I=2mA
Lock protection						
CLK cycle for protection circuit	TLP	13	20	27	msec	LP=0.1μF
VCO						
CLK input frequency range	FCLK	0.2	–	2.5	kHz	Designed value (VCO alone)
High-level CLK input voltage	VCKH	2.2	–	VREG	V	
Low-level CLK input voltage	VCKL	0	–	0.8	V	
High-level CLK input current	ICKH	-10	–	10	μA	
Low-level CLK input current	ICKL	-140	-100	-60	μA	

BD6762FV (Unless otherwise specified, Ta=25°C, VCC=24 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Start/Stop						
High-level ST/SP input voltage	VSTH	2.2	–	VREG	V	STOP
Low-level ST/SP input voltage	VSTL	0	–	0.8	V	START
High-level ST/SP input current	ISTH	-10	0	10	μA	
Low-level ST/SP input current	ISTL	-70	-50	-30	μA	
Forward rotation/Reverse rotation						
High-level FR input voltage	VFRH	2.2	–	VREG	V	Reverse rotation
Low-level FR input voltage	VFRL	0	–	0.8	V	Forward rotation
High-level FR input current	IFRH	-10	0	10	μA	
Low-level FR input current	IFRL	-70	-50	-30	μA	
120°/Slope switching						
High-level 120/slope input voltage	VANH	2.2	–	VREG	V	120°
Low-level 120/slope input voltage	VANL	0	–	0.8	V	120° slope
High-level 120/slope input current	IANH	-10	0	10	μA	
Low-level 120/slope input current	IANL	-70	-50	-30	μA	
Short brake						
High-level SB input voltage	VSBH	2.2	–	VREG	V	Short brake operation
Low-level SB input voltage	VSBL	0	–	0.8	V	Short brake clear
High-level SB input current	ISBH	-10	0	10	μA	
Low-level SB input current	ISBL	-70	-50	-30	μA	
Current limit						
Current detection voltage	VCL	0.23	0.26	0.29	V	
Booster						
CP1 oscillating frequency	FCP1	75	125	175	kHz	
VG step-up voltage	VG	VCC+5.7	VCC+6.7	VCC+7.7	V	
High-side output						
High output voltage 1	VHHG1	VCC+5.8	VCC+6.8	VCC+7.8	V	VG=31V
High output voltage 2	VHHG2	VCC+3.8	VCC+4.8	VCC+5.8	V	Io=-1mA
Low output voltage 1	VHLG1	–	0.1	0.3	V	
Low output voltage 2	VHLG2	–	0.5	1.0	V	Io=5mA
Clamp voltage	VHCL	10	11	12	V	
Low-side output						
High output voltage 1	VLHG1	9.8	10.8	11.8	V	
High output voltage 2	VLHG2	9.0	10.0	11.0	V	Io=-5mA
Low output voltage 1	VLLG1	–	0.1	0.3	V	
Low output voltage 2	VLLG2	–	0.3	0.5	V	Io=5mA

●**Reference Data**

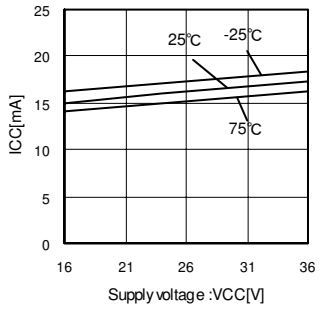


Fig.1 Circuit current (BA6680FS)

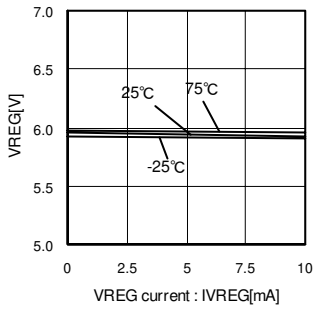


Fig.2 VREG Voltage (BA6680FS)

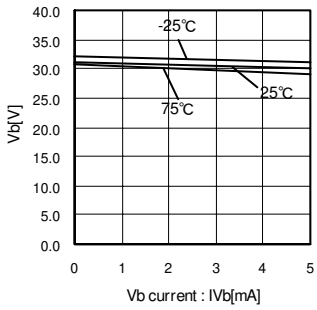


Fig.3 Vb Voltage (BA6680FS)

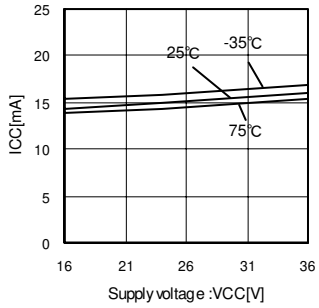


Fig.4 Circuit current (BD6761FS)

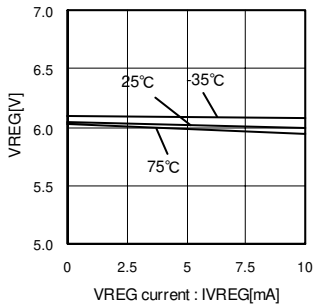


Fig. 5 VREG Voltage (BD6761FS)

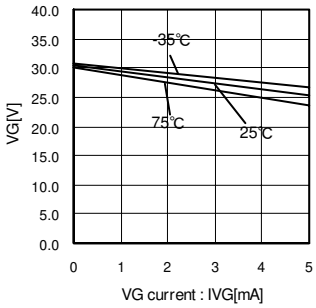


Fig. 6 VG Voltage (BD6761FS)

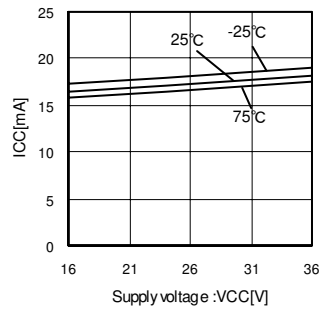


Fig.7 Circuit current (BD6762FV)

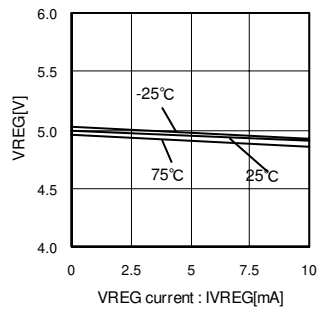


Fig.8 VREG Voltage (BD6762FV)

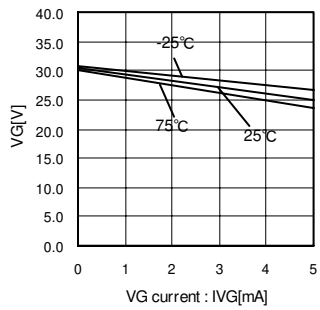


Fig.9 VG Voltage (BD6762FV)

●**Power dissipation reduction**

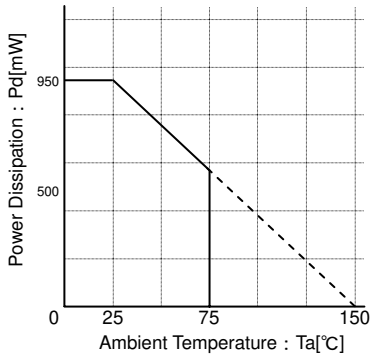


Fig.10 BA6680FS and BD6761FS Power Dissipation Reduction

Reduced by 7.6 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

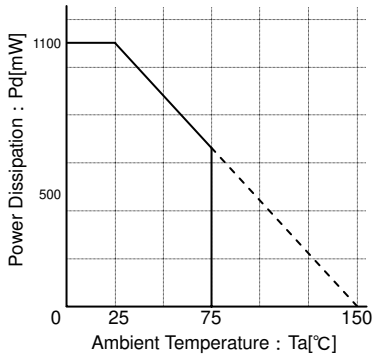


Fig.11 BD6762FV Power Dissipation Reduction

Reduced by 8.8 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

●Block diagram, Application circuit diagram, and Pin function

1)BA6680FS

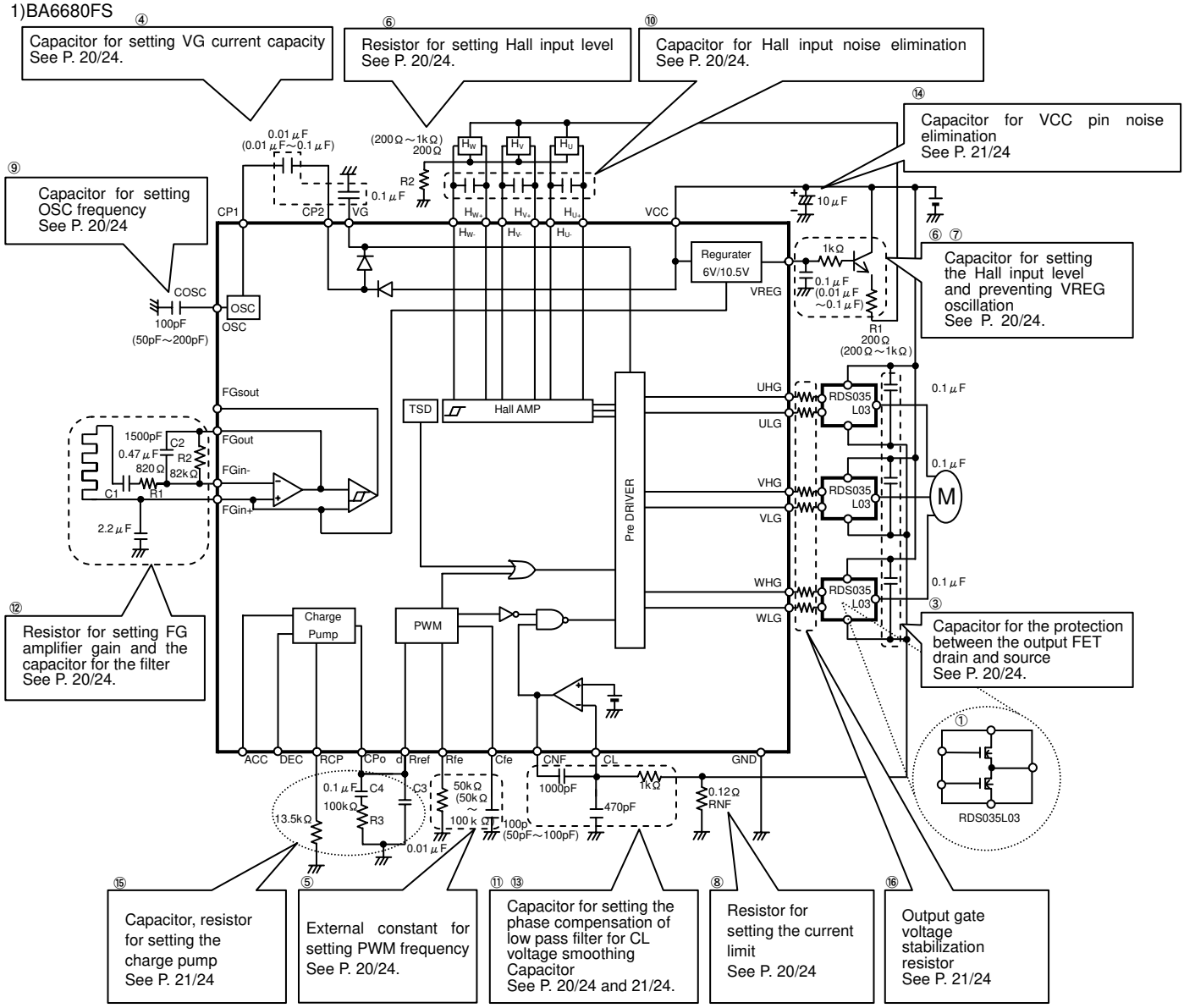


Fig. 12 BD6680FS Block Diagram

BA6680FS pin function

No.	Pin name	Function	No.	Pin name	Function
1	GND	GND pin	17	HV+	Hall signal input pin
2	CL	Limit pin	18	HV-	Hall signal input pin
3	UHG	U-phase high-side FET gate pin	19	HW+	Hall signal input pin
4	ULG	U-phase low-side FET gate pin	20	HW-	Hall signal input pin
5	VHG	V-phase high-side FET gate pin	21	FGin+	FG input + pin
6	VLG	V-phase low-side FET gate pin	22	FGin-	FG input - pin
7	WHG	W-phase high-side FET gate pin	23	FGout	FG output pin
8	WLG	W-phase low-side FET gate pin	24	FGsout	FGs output pin
9	VCC	VCC pin	25	DEC	Deceleration signal input pin
10	OSC	Oscillator pin	26	ACC	Acceleration signal input pin
11	VG	Boost pin	27	RCP	CPout current control pin
12	CP2	CP2 pin	28	CPout	Charge pump output pin
13	CP1	CP1 pin	29	Pref	PWM control signal input pin
14	VREG	VREG pin	30	Rfe	Cfe current control pin
15	HU+	Hall signal input pin	31	Cfe	PWM frequency control pin
16	HU-	Hall signal input pin	32	CNF	Phase compensation pin

2)BD6761FS

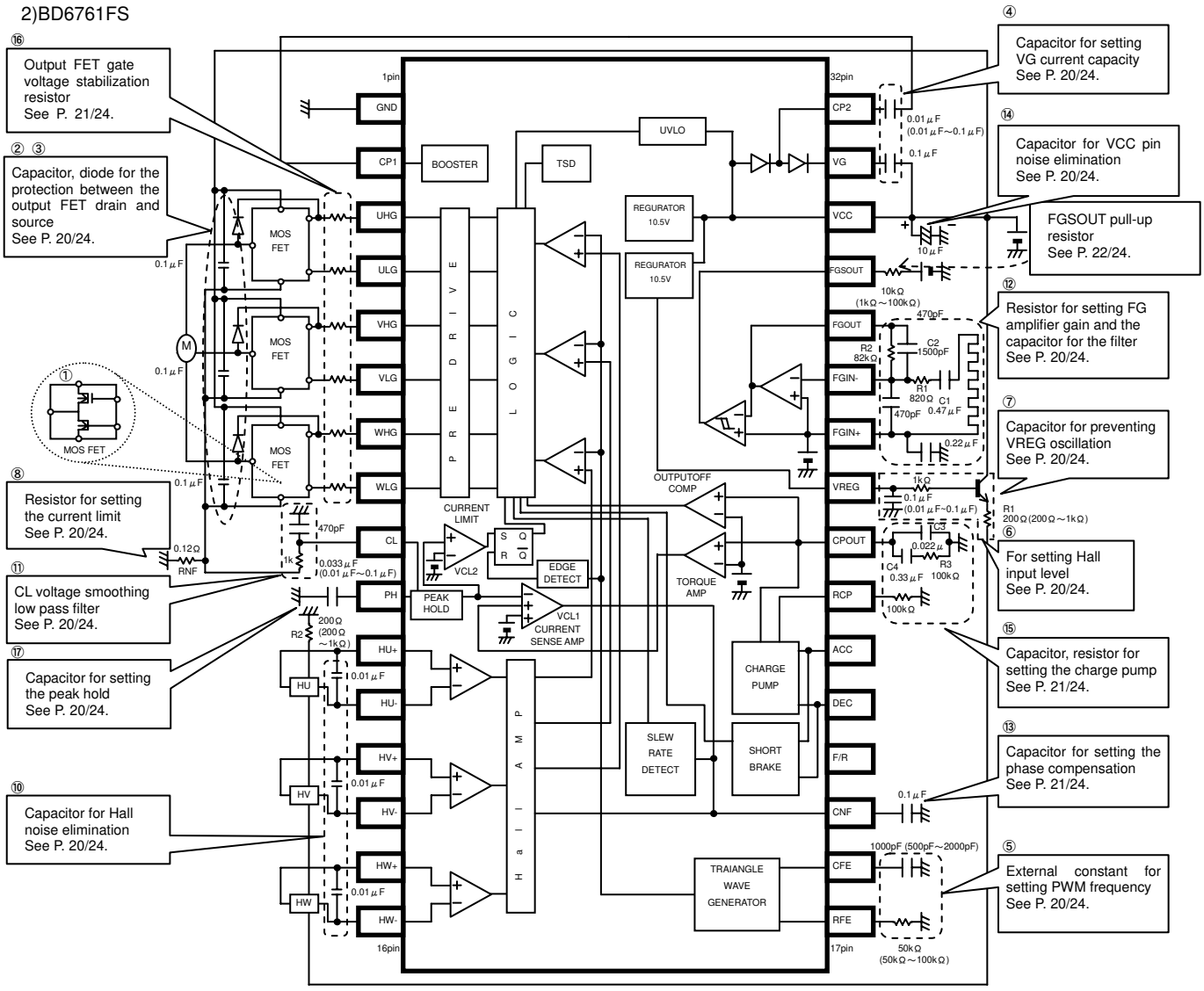


Fig.13 BD6761FS Block Diagram

BD6761FS pin function

No.	Pin name	Function	No.	Pin name	Function
1	GND	GND pin	17	RFE	CFE current control pin
2	CP1	CP1 pin	18	CFE	PWM frequency control pin
3	UHG	U-phase high-side FET gate pin	19	CNF	Phase compensation pin
4	ULG	U-phase low-side FET gate pin	20	F/R	Forward/reverse rotation switching pin
5	VHG	V-phase high-side FET gate pin	21	DEC	Deceleration signal input pin
6	VLG	V-phase low-side FET gate pin	22	ACC	Acceleration signal input pin
7	WHG	W-phase high-side FET gate pin	23	RCP	CPOUT current control pin
8	WLG	W-phase low-side FET gate pin	24	CPOUT	Charge pump output / Torque control signal input pin
9	CL	Motor current detection pin			
10	PH	Peak hold pin	25	VREG	VREG pin
11	HU+	Hall signal input pin	26	FGIN+	FG input + pin
12	HU-	Hall signal input pin	27	FGIN-	FG input - pin
13	HV+	Hall signal input pin	28	FGOUT	FG output pin
14	HV-	Hall signal input pin	29	FGSOUT	FGS output pin
15	HW+	Hall signal input pin	30	VCC	VCC pin
16	HW-	Hall signal input pin	31	VG	Boost pin
			32	CP2	CP2 pin

3)BD6762FV

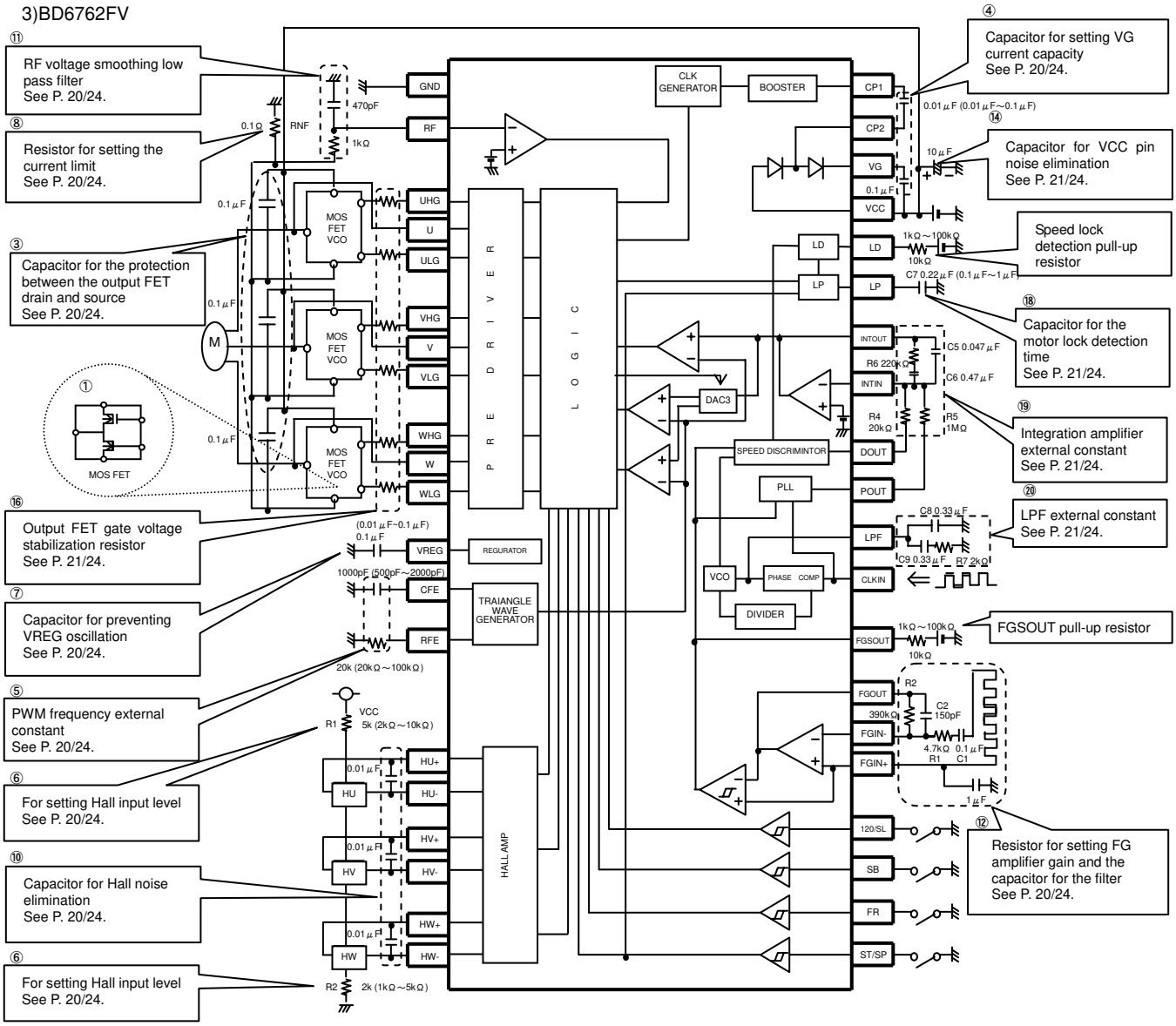


Fig.14 BD6762FV Block Diagram

BD6762FV pin function

No.	Pin name	Function	No.	Pin name	Function
1	GND	GND pin	21	ST/SP	Start/Stop pin
2	RF	Motor current detection pin	22	FR	Forward/reverse rotation switching pin
3	UHG	U-phase high-side FET gate pin	23	SB	Short brake pin
4	U	Protection pin for U-phase high-side FET GS breakdown voltage	24	120/SL	120°/slope switching pin
5	ULG	U-phase low-side FET gate pin	25	FGIN+	FG amplifier input + pin
6	VHG	V-phase high-side FET gate pin	26	FGIN-	FG amplifier input - pin
7	V	Protection pin for V-phase high-side FET GS breakdown voltage	27	FGOUT	FG amplifier output pin
8	VLG	V-phase low-side FET gate pin	28	FGSOUT	FGS output pin
9	WHG	W-phase high-side FET gate pin	29	CLKIN	Reference CLK input pin
10	W	Protection pin for W-phase high side FET GS breakdown voltage	30	LPF	VCO system loop filter connection pin
11	WLG	W-phase low-side FET gate pin	31	POUT	PLL output pin
12	VREG	Internal power supply 5 V output pin	32	DOUT	Speed discriminator output pin
13	CFE	PWM frequency control pin	33	INTIN	Integration amplifier input pin
14	RFE	CEF charge/discharge current control pin	34	INTOUT	Integration amplifier output pin
15	HU+	Hall signal input pin	35	LP	Motor lock protection time setting pin
16	HU-	Hall signal input pin	36	LD	Motor rotation number lock detection pin
17	HV+	Hall signal input pin	37	VCC	VCC pin
18	HV-	Hall signal input pin	38	VG	Step-up voltage output pin
19	HW+	Hall signal input pin	39	CP2	Capacitor connection pin (to CP1)
20	HW-	Hall signal input pin	40	CP1	Capacitor connection pin (to CP2)

●I/O Logic

1)BA6680FS

	Input conditions						Output state					
							High-side FET gate voltage			Low-side FET gate voltage		
Pin No.	15	16	17	18	19	20	3	5	7	4	6	8
	HU+	HU-	HV+	HV-	HW+	HW-	UHG	VHG	WHG	ULG	VLG	WLG
Condition 1	L	M	L	M	H	M	L	H	L	L	L	H
Condition 2	L	M	H	M	H	M	H	L	L	L	L	H
Condition 3	L	M	H	M	L	M	H	L	L	L	H	L
Condition 4	H	M	H	M	L	M	L	L	H	L	H	L
Condition 5	H	M	L	M	L	M	L	L	H	H	L	L
Condition 6	H	M	L	M	H	M	L	H	L	H	L	L

＜Input conditions＞ ＜Output criteria＞

Hall input voltage High-side FET gate voltage

H : 1.3V L≦1 V, VG-1V≦H

M : 1.2V Low-side FET gate voltage

L : 1.1V L≦1 V, 9 V≦H

2)BD6761FS

Forward rotation (F/R=Low)

	Input conditions			Output state					
Pin No.	15	17	19	3	5	7	4	6	8
	HU+	HV+	HW+	UHG	VHG	WHG	ULG	VLG	WLG
Condition 1	L	M	H	H	H	L	L	L	H
Condition 2	L	H	H	H	PWM	L	L	PWM	H
Condition 3	L	H	M	H	L	L	L	H	H
Condition 4	L	H	L	H	L	PWM	L	H	PWM
Condition 5	M	H	L	H	L	H	L	H	L
Condition 6	H	H	L	PWM	L	H	PWM	H	L
Condition 7	H	M	L	L	L	H	H	H	L
Condition 8	H	L	L	L	PWM	H	H	PWM	L
Condition 9	H	L	M	L	H	H	H	L	L
Condition 10	H	L	H	L	H	PWM	H	L	PWM
Condition 11	M	L	H	L	H	L	H	L	H
Condition 12	L	L	H	PWM	H	L	PWM	L	H

Reverse rotation (F/R=High)

	Input conditions			Output state					
Pin No.	15	17	19	3	5	7	4	6	8
	HU+	HV+	HW+	UHG	VHG	WHG	ULG	VLG	WLG
Condition 1	L	M	H	L	L	H	H	H	L
Condition 2	L	H	H	L	PWM	H	H	PWM	L
Condition 3	L	H	M	L	H	H	H	L	L
Condition 4	L	H	L	L	H	PWM	H	L	PWM
Condition 5	M	H	L	L	H	L	H	L	H
Condition 6	H	H	L	PWM	H	L	PWM	L	H
Condition 7	H	M	L	H	H	L	L	L	H
Condition 8	H	L	L	H	PWM	L	L	PWM	H
Condition 9	H	L	M	H	L	L	L	H	H
Condition 10	H	L	H	H	L	PWM	L	H	PWM
Condition 11	M	L	H	H	L	H	L	H	L
Condition 12	L	L	H	PWM	L	H	PWM	H	L

＜Input conditions＞ ＜Output criteria＞

Hall input voltage High-side FET gate voltage

H: 3.05V L≦1V, VG-1V≦H

M: 3.0V Low-side FET gate voltage

L: 2.95V L≦1V, 9 V≦H

ACC, DEC

	Input conditions		Output state	
Pin No.	21	22	24	Short brake
	DEC	ACC	CPOUT	
Condition 1	H	H	OPEN	OFF
Condition 2	H	L	H	OFF
Condition 3	L	H	L	OFF
Condition 4	L	L	L	ON

＜Input conditions＞

ACC, DEC input conditions

H：2.2V

L：0.8V

＜Output criteria＞

○CPOUT

RCP=13.5kΩ, CPOUT=3V

High: Current outflow more than 140μA from CPOUT pin

Low: Current inflow more than 140μA to CPOUT pin

OPEN: CPOUT pin current -10μA≦ICPOUT≦10μA

○Short brake function

On state

High-side FET gate voltage≦1V

Low-side FET gate voltage≧9V

3)BD6762FV

Forward rotation (F/R=Low), 120° (120/SL=High)

	Input conditions			Output state								
				High-side gate			Low-side gate			Output		
Pin No.	15	17	19	3	6	9	5	8	11	4	7	10
	HU+	HV+	HW+	UHG	VHG	WHG	ULG	VLG	WLG	U	V	W
Condition 1	L	L	H	L	H	L	L	L	H	M	H	L
Condition 2	H	L	H	L	H	L	H	L	L	L	H	M
Condition 3	H	L	L	L	L	H	H	L	L	L	M	H
Condition 4	H	H	L	L	L	H	L	H	L	M	L	H
Condition 5	L	H	L	H	L	L	L	H	L	H	L	M
Condition 6	L	H	H	H	L	L	L	L	H	H	M	L

Reverse rotation (F/R=High), 120° (120/SL=High)

	Input condition			Output state								
				High-side gate			Low-side gate			Output		
Pin No.	15	17	19	3	6	9	5	8	11	4	7	10
	HU+	HV+	HW+	UHG	VHG	WHG	ULG	VLG	WLG	U	V	W
Condition 1	L	L	H	L	L	H	L	H	L	M	L	H
Condition 2	H	L	H	H	L	L	L	H	L	H	L	M
Condition 3	H	L	L	H	L	L	L	L	H	H	M	L
Condition 4	H	H	L	L	H	L	L	L	H	M	H	L
Condition 5	L	H	L	L	H	L	H	L	L	L	H	M
Condition 6	L	H	H	L	L	H	H	L	L	L	M	H

ST/SP	Mode
OPEN or High	Standby
L	Operating mode

＜Input condition＞

Hall input voltage H : 2.0V
M : 1.5V
L : 1.0V

HU-, HV-, HW- : M

＜Output criteria＞

High-side FET gate voltage : L≦output (U, V, W) + 1V, VG - 1V≦H

Low-side FET gate voltage : L≦1V, 9V≦H

●**Timing chart**

1)BA6680FS

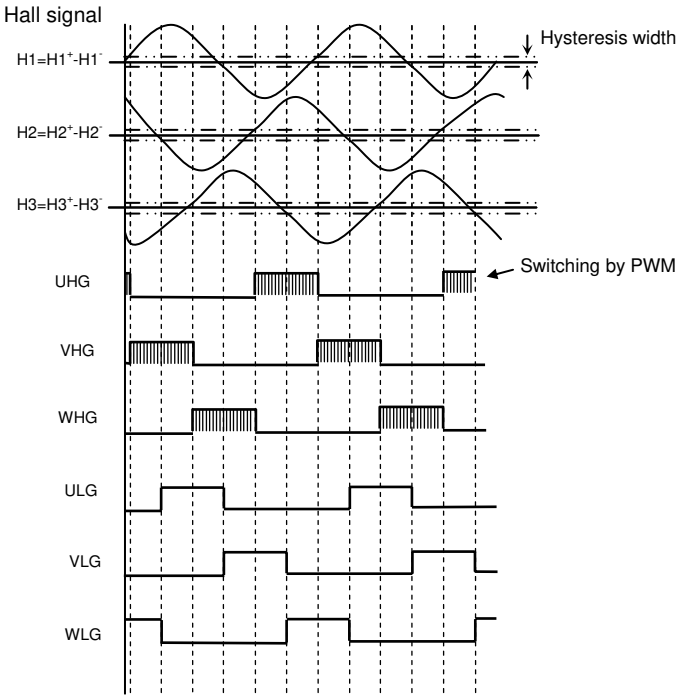


Fig.15 BA6680FS I/O Timing Chart

2)BD6761FS

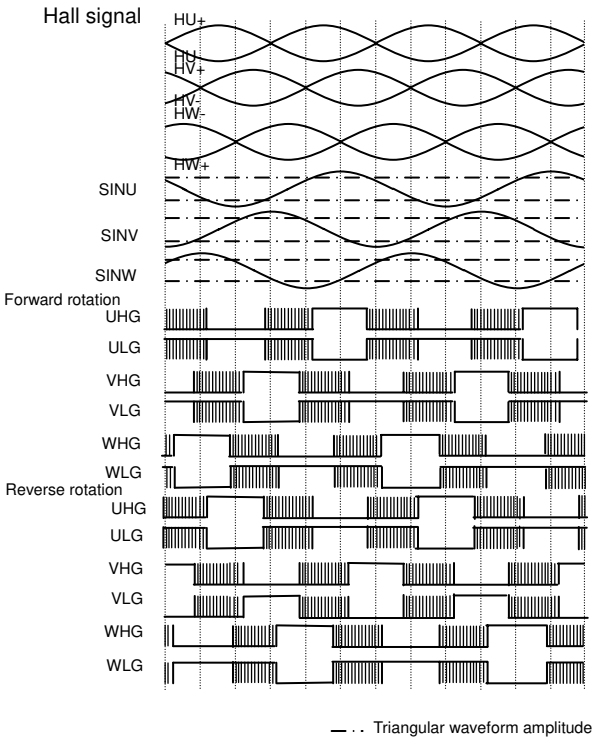


Fig.16 BD6761FS I/O Timing Chart

SINU, SINV, and SINW are the internal IC signals synthesized by the Hall amplifier.

3)BD6762FV

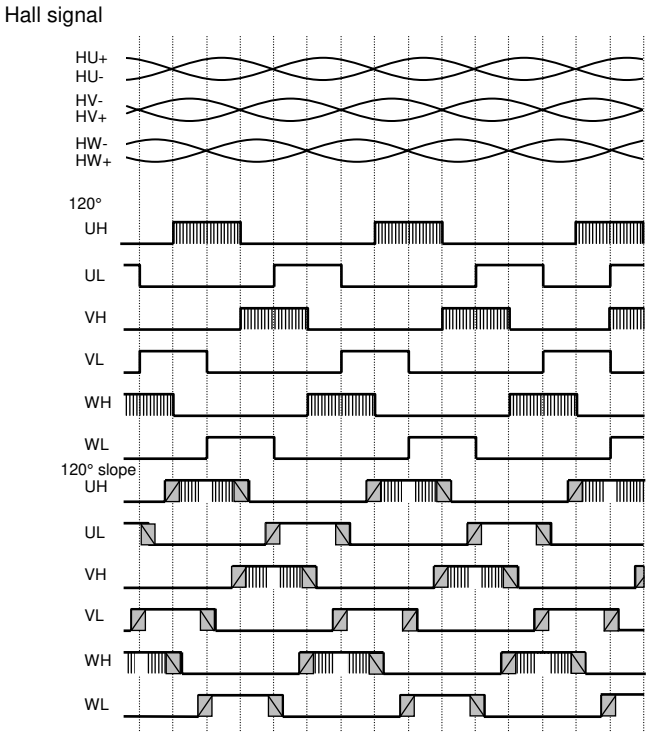
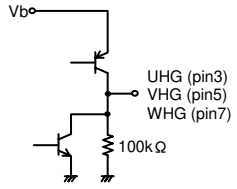


Fig.17 BD6762FV I/O Timing Chart

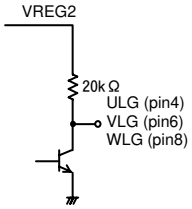
●I/O Circuit diagram

1)BA6680FS

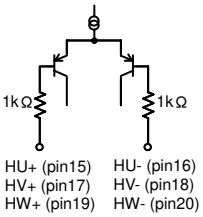
○High-side gate



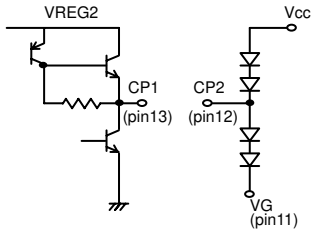
○Low- side gate



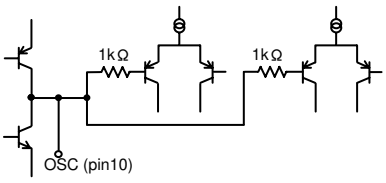
○Hall input



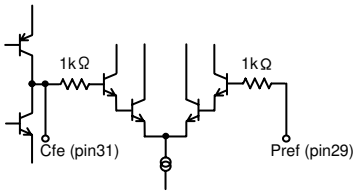
○Booster



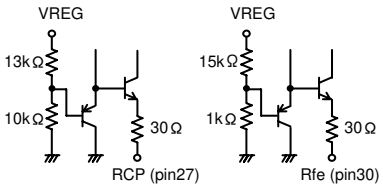
○OSC



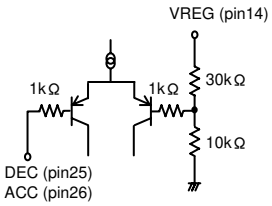
○PWM comparator



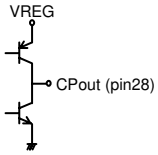
○RC, Rfe pins



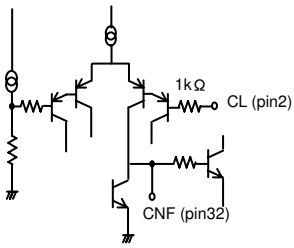
○ACC, DEC pins



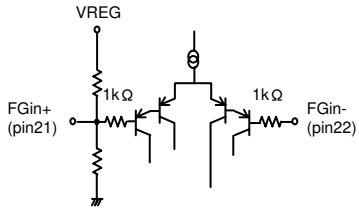
○CPout pin



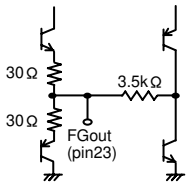
○Current limit



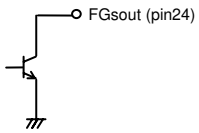
○FG amplifier input



○FG amplifier output

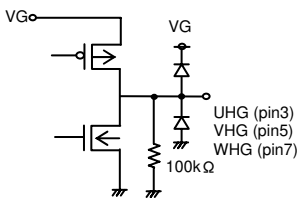


○FGsout pin

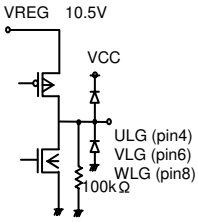


2)BD6761FS

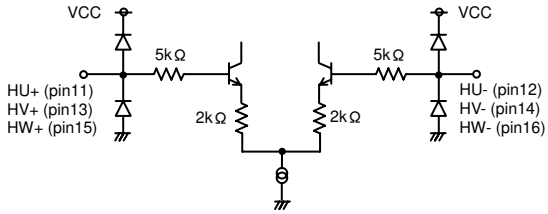
○High-side gate



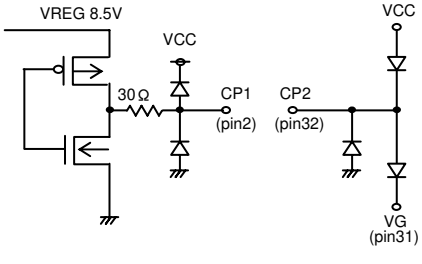
○Low-side gate



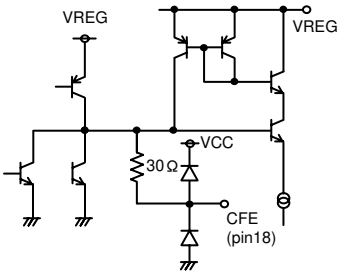
○Hall input



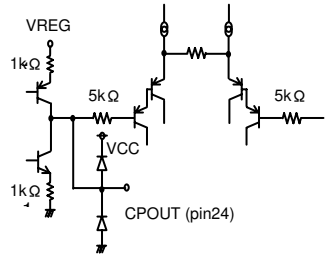
○Booster



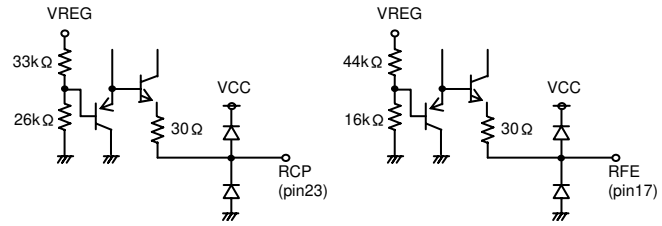
○CFE pin



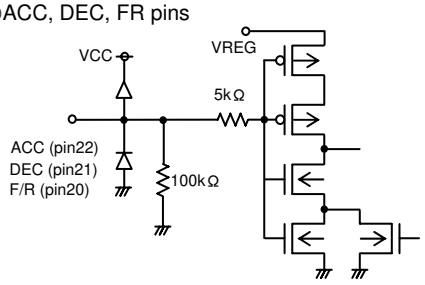
○CPOUT pin



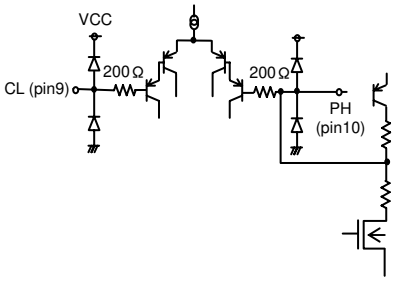
○RCP, RFE pins



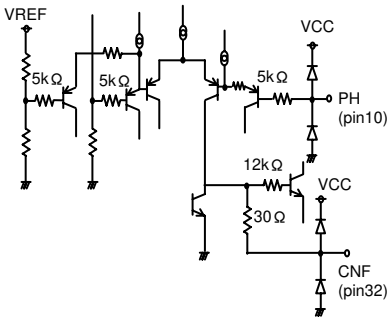
○ACC, DEC, FR pins



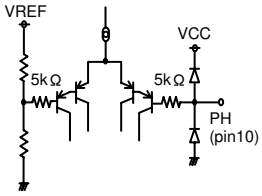
○Peak hold



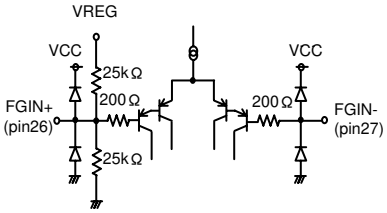
○Current sense amplifier



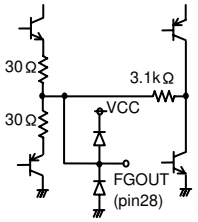
○Current limit



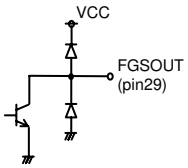
○FG amplifier input



○FG amplifier output

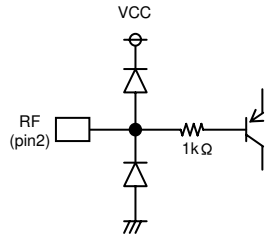


○FGSOUT pin

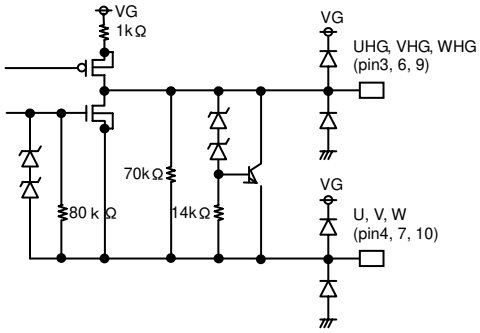


3)BD6762FV

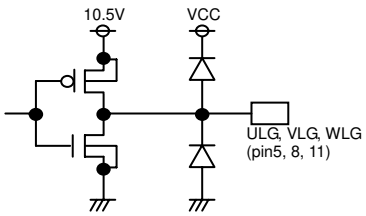
○RF pin



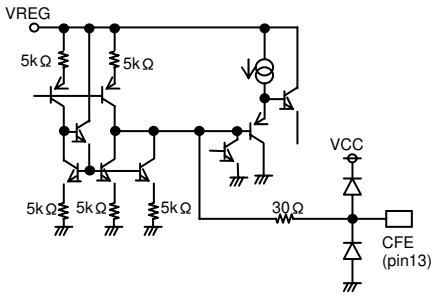
○UHG, VHG, WHG, U, V, W pins



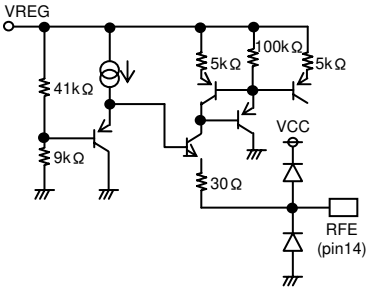
○ULG, VLG, WLG pins



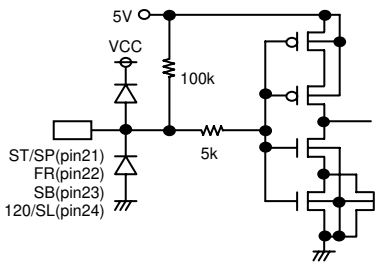
○CFE pin



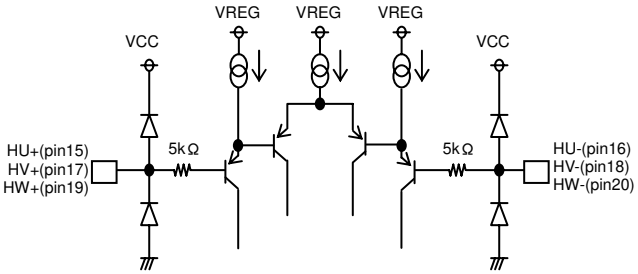
○RFE pin



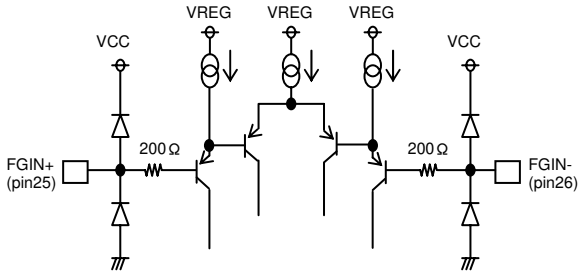
○ST/SP, FR, SB, 120/SL



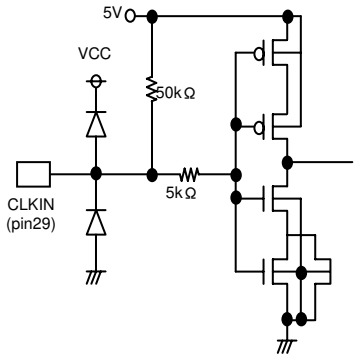
○ HU+, HV+, HW+, HU-, HV-, HW- pins



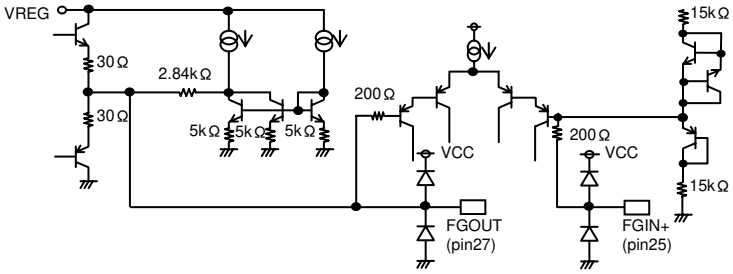
○FGIN+, FGIN- pins



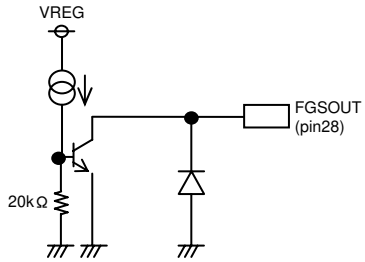
○CLKIN



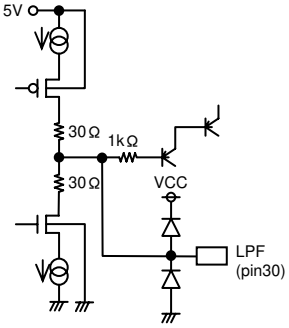
○FGIN+, FGOUT pins



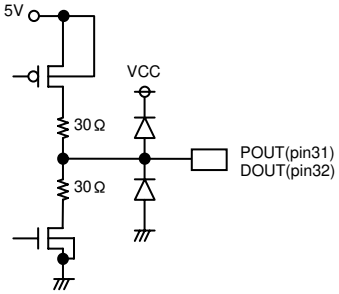
○ FGSOUT pin



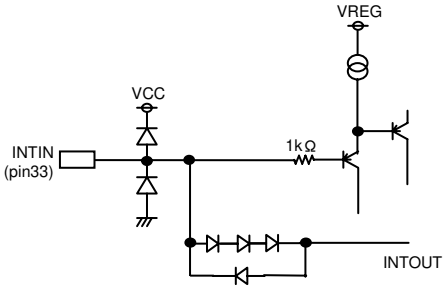
○LPF pin



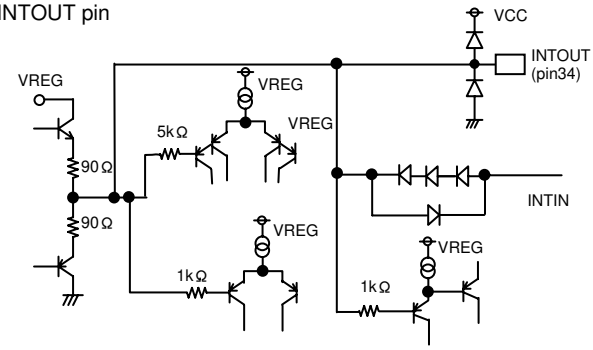
○POUT, DOUT pins



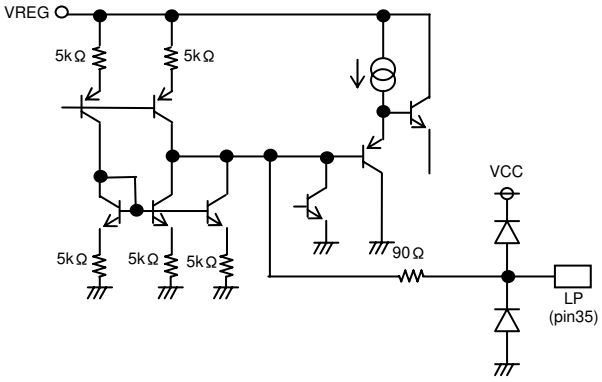
○ INTIN pin



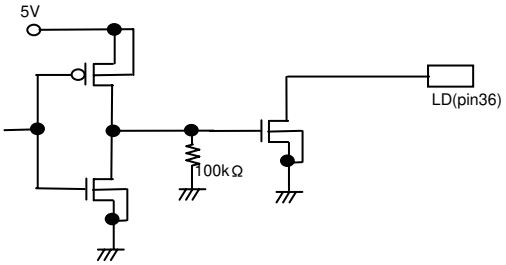
○INTOUT pin



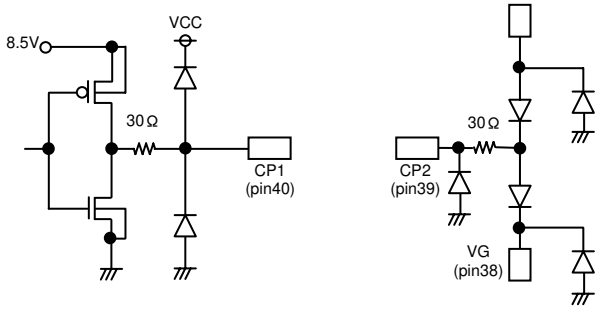
○LP pin



○LD pin



○ VG, CP2, CP1 pins



●IC Operation

1) Hall input and output

The hall amplifier shapes the hall input signal to generate the drive signal.

This drive signal is amplified in the predriver block and the gate voltage is output for N-channel MOS FET.

2) PWM operation

PWM oscillating frequency is determined by the triangular waveform frequency which is set by the external constant.

This triangular waveform voltage and the listed voltage in the following chart are compared to perform PWM drive.

	Rfe, RFE	Cfe, CFE	Cfe, CFE pin charge/discharge current I	Frequency (Typ.)	Comparison voltage
BA6680FS	50kΩ	100pF	0.4V/R	15.5kHz	Pref
BD6761FS	50kΩ	1000pF	1.6V/R	16.5kHz	Drive signal shaped by the hall amplifier
BD6762FV	20kΩ	1000pF	VRFE/R	16kHz	Integration amplifier output pin voltage

3) Boost circuit (step-up circuit) (common)

BA6680FS generates the triangular waveform by connecting a capacitor (COSC = 100pF: Frequency = 95 kHz) between the OSC and GND pins. BD6761FS (Frequency = 62.5 kHz) and BD6762FV (Frequency = 125 kHz) generate the triangular waveform by the internal free-run oscillator and the rectangular waveform at CP1. When a capacitor is connected between CP1 and CP2, and VG and GND, the step-up voltage is generated at VG pin. In this case, set VCC so that VG does not exceed the absolute maximum ratings (36 V).

	Triangular waveform oscillating frequency	Charge pump voltage (VG pin voltage)
BA6680FS	95kHz(COSC=100pF)	VCC+7V
BD6761FS	62.5 kHz	VCC+6V
BD6762FV	125 kHz	VCC+6.7V

4) FG amplifier (common)

Set the FG amplifier gain so that the FGOUT pin is within the range of high and low output voltage and the amplitude is higher than the hysteresis width (250 mV: max) of the HYS amplifier.

FGSOUT pin is an open collector which requires a resistor to the supply line. Voltage higher than 36 V must not be applied to the FGSOUT pin.

5) ACC, DEC circuits (BA6680FS、BD6761FS)

When a resistor is connected to the RCP pin and the low voltage is input to the ACC pin, the current flows out from the CPOUT pin. When the low signal is input to the DEC pin, the current flows in to the CPOUT pin. Furthermore, when the ACC pin and DEC pin both set to low, the current flows in to the CPOUT pin. This current can be converted to the voltage by connecting a filter between the CPOUT and GND pins.

The voltage generated at the CPOUT pin controls the PWM's on-duty and maintains the constant motor rotation by inputting the controlled signal to ACC and DEC pins.

6) Current limit operation

The CL voltage (BA6680FS, BD6761FS) and RF voltage (BD6762FV) become the current limit voltage and the current limit circuit limits PWM on_dutty. It also turns off the current limit circuit (current limit clear) at the peak of PWM triangular waveform and makes the current flow again. Output current Iomax at this time are shown in the table.

	Current limit current
BA6680FS	Iomax=0.38/RNF [A]
BA6761FS	Iomax=0.48/RNF [A]
BA6762FV	Iomax=0.26/RNF [A]

7) Preventing low-side and high-side switch overlapping (BD6761FS, BD6762FV)

When the low-side gate voltage becomes high while the high-side gate voltage is low, or vice versa, a prevention delay time is provided with t=3.2 μs (TYP value). When the input capacity of external FET is C and the gate connection resistor is R, set R to satisfy the following equation:

$$C \leqq \frac{1.8\mu}{10 \times (24 + R)}$$

Note: Confirm by testing on the actual system.

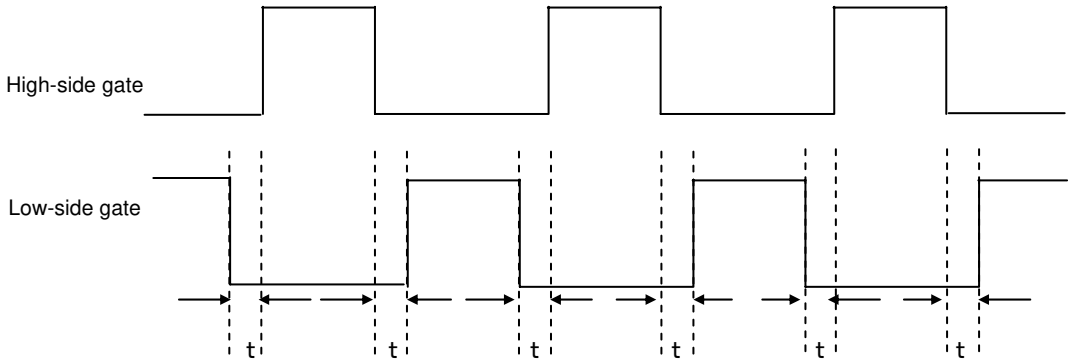


Fig.18 High/Low-side Simultaneous On Prevention Timing Chart

8) Short brake (BD6761FS and BD6762FV)

BD6761FS operates the short brake action with the ACC and DEC pins set to low, while BD6762FV does so with the SB pin set to OPEN or high. At the time of short brake, the high-side gate is turned off and the low-side is turned on. At the time of short brake operating, the current flows to the output FET, which is set by the motor's counter electromotive voltage and coil impedance. Since this current does not flows through the overcurrent protection (current limit) detection resistor, the overcurrent protection does not operate as the IC operates. Therefore, the current must not exceed the output FET rating.

9) Forward/reverse rotation circuit (BD6761FS and BD6762FV)

Forward /reverse rotation of motor can be switched according to the FR pin input conditions. Logics of the hall input and output conditions according to the FR pin input conditions are shown in the I/O conditions table (P.12/24). If the FR pin is switched during the motor rotation, when the prevention circuit in the IC operates, the feed through current does not flow. However, since the motor current flows toward the power source due to the electromotive force, the voltage may be raised if the power source does not have the power supply voltage absorption ability. Examine the capacitor characteristics between the power supply and ground sufficiently. Power supply voltage and step-up voltage must not exceed the absolute maximum ratings. When the physical measures are taken, such as increasing the capacitor value which is connected between the power supply and ground, characteristics must be monitored prior to use.

10) Start/stop circuit (BD6762FV)

When the ST/SP pin is in the sate of OPEN or high, IC is on standby. In standby mode, some circuit operations are turned off to reduce the current consumption.

When the ST/SP pin is in the state of low, the IC operates.

11) Low voltage protection circuit (BD6761FS and BD6762FV)

An IC with a built-in low voltage protection circuit. When VCC becomes lower than 11.5 V (Typ.), the high-side and low-side gates are both turned off and turn the coil off. Protection off voltage is 12.0 V (Typ.) and hysteresis width is 0.5 V (Typ.).

Since the motor locking protection detection circuit operates in BD6762FV during the low voltage protection operation, if the low voltage protection operating time becomes longer than the motor locking protection detection time, the operation moves to the motor locking protection operation after the low voltage protection operation.

12) Built-in 120° slope PWM logic (BD6762FV)

It is possible to perform 120° drive by setting 120/SL pin to OPEN or making high. 120° slope drive is possible by setting the 120/SL pin to OPEN or making high. Low noise design is realized by reducing the electromagnetic sound generated at the time of phase switching by means of gradually changing the output PWM on-duty during 120° slope energization. However, at the time of startup or the hall input frequency is lower than about 3 Hz (Typ. value), it becomes 120° drive. When the hall input frequency is more than about 3 Hz (Typ. value) and the rise of hall U-phase is detected 7 times, it switches to the 120° slope drive.

13) Servo circuit (BD6762FV)

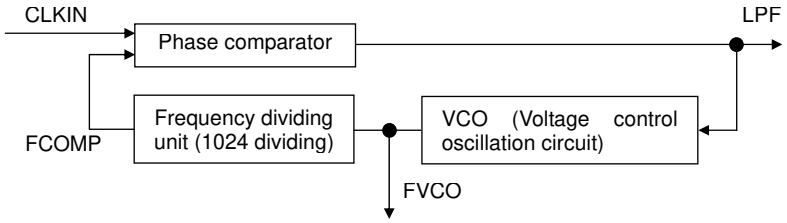
・Frequency multiplication circuit (Dividing period) (BD6762FV)

An IC with a built-in the frequency multiplication circuit.

Servo circuit is composed of the feedback loop as shown in the diagram and flows in/out the current (22μA: Typ.) to the LPF pin (30 pin) by detecting the phase difference between the CLKIN pin (29 pin) and the frequency dividing unit output FCOMP. The phase difference signal output to the LPF pin (30 pin) is smoothed by the filter which is connected at the IC external of the LPF pin (30 pin) and this voltage is input to the VCO (Voltage control oscillation circuit) to determine the frequency for the internal signal FVCO. Since the dividing ratio of this frequency dividing unit is set to 1024, the relation of:

FVCO[Hz]=1024・FCOMP[Hz] ,

can be obtained. The FCOMP and CLKIN have the same frequency according to the feedback loop as shown in the following diagram. Therefore the multiplied frequency of 1024 times of FCOMP or CLKIN is acquired as the FVCO frequency.



・Speed discriminator (BD6762FV)

The FGSOUT signal (28 pin), which detects the motor rotation speed and the reference clock in the IC, are compared and the acceleration/deceleration signal is output to the DOUT pin (32 pin). Reference clock is the signal (FVCO) that the CLKIN signal (29 pin) is multiplied by 1024. When the FG period is short to the reference clock period, it is determined that the motor revolution speed is too fast and the difference from the reference clock period is output to the DOUT pin as the deceleration command. When the FG period is long, the difference is output as an accelerating command.

・PLL (BD6762FV)

Phases of the FGSOUT (28 pin) signal, which detected the motor revolution speed and the CLKIN (29 pin) input from the external are compared, and if the FG phase leads to CLKIN (28 pin), the difference is output as the deceleration command. If the FG phase lags, the difference is output as the acceleration command.

・Integration amplifier (BD6762FV)

Speed error of the reference clock, which is obtained in the speed discriminator block and the FG signal, and the phase difference signal of the CLKIN acquired in PLL block and the FG are integrated together and smoothed to become the DC voltage. This smoothed signal determines the PWM on-duty.

14) Speed lock detection circuit (BD6762FV)

When the motor speed is within ±6.25% range to the CLKIN signal (29 pin), L is output to the LD pin (36 pin) output.

Since the LD pin (36 pin) has the open/drain output format, use as it is pulled up to the power supply with the resistor (100kΩ). At this time, pay attention so that the voltage more than 36 V is not applied to the LD pin.

15) Motor locking protection (BD6762FV)

The motor locking protection circuit determines when the motor is in the locking condition. When the motor speed is not in the lock range (preset value: ±6.25%) and the motor locking detection time T_{LP} elapsed, the high-side and low-side output gates are both turned off.

Motor locking protection can be cleared by making the condition Low, after setting the ST/SP pin or the SB pin to OPEN or making high. Motor locking detection time T_{LP} is determined by the capacitor C7 which is connected to the LP pin and the count number CLP (preset value: 96) of the internal counter.

$$T_{LP}=2\times10^{5}\times C7\times CLP \quad [S]$$

●**Selecting application components**

Design method	Design example
①Output FET This IC is the predriver for high-side and low-side N-channel MOS FET drive. Select the FET with the required current capacity to drive the motor.	Recommended FET RDS035L03 (A)
②Diodes (BD67861FS) Diodes are required to protect between the gate and source of output FET.	Recommended diode 1SS355 Insert the diode in the direction from high-side FET source to the gate side (in the forward direction).
③Protection capacitor between the output FET drain and source Check the operation so that the voltage between the output FET drain and source does not exceed the absolute maximum ratings due to the fluctuation of VCC at the time of PWM driving and then set the value.	A value of 0.01μ to 0.1μF is recommended. A value of 0.1μF is appropriate for the capacitance. Insert the capacitor between the output FET drain and source. (Position at the close point to FET as much as possible.)
④VB current capacitance capacitor Current capacity from VG changes according to the capacitance to be connected. However, if the capacitance is too large, the following action is delayed when VCC starts up, and the magnitude relation becomes VCC > VG. Typically, should be VCC < VG and the large current may flow in internal block circuits and result in damaging the circuits. When VG is directly supplied from the external block without using the internal circuits, disconnect the capacitor between CP1 and CP2, and connect the 20kΩ resistor (for noise reduction) between CP1 and ground to use.	A value of 0.01μF is appropriate for the capacitor between CP1 and CP2 (A value of 0.01μF 0.1μF is recommended.) A value of 0.1μF is appropriate for the capacitor between VG and VCC.
⑤PWM frequency PWM frequency can be adjusted by the capacitance and resistance to connect. When the frequency is high, the heat generation increases due to switching loss. When the frequency is low, it enters audible range. Check the operation with the actual product and determine the constant.	The following constants are appropriate: BA6680FS Cfe=100pF, Rfe=50kΩ, fo=15.5kHz(TYP.) BD6761FS Cfe=1000pF, Rfe=50kΩ, fo=16.5kHz(TYP.) BD6762FV Cfe=1000pF, Rfe=20kΩ, fo=16.0kHz(TYP.)
⑥Hall input level The current value to feed to the hall element changes by changing the resistance and the amplitude level of hall element. Amplitude level increases when the resistance value is chosen smaller by considering the noise affect. Pay attention to the hall input voltage range. BA6680FS (1.0V to 4.9V), BD6761FS (1.5V to 4.1V) and BD6762FV (0V to 3V)	Connect to the transistor base via 1kΩ resistor (base current limit) from the VREG pin. Connect the transistor collector to VCC, the emitter to the hall element via R1. Connect the ground side of hall element to the ground via R2. A value of 200Ω to 1kΩ is recommended. A value of 200Ω is appropriate. When connecting to the VCC side directly with R1, values of R1=5kΩ and R2=2kΩ are appropriate.
⑦VREG VREG which is the internal voltage output pin drives the circuits in IC. Connect the capacitor to stabilize it.	A value of 0.01μF to 0.1μF is recommended. A value of 0.1μ is appropriate.
⑧Current limit The current flowing to FET can be controlled by setting the resistance value. Determine the constant according to the motor specifications.	Following equation shows the current value: BA6680FS Iomax=0.38/RNF [A] BD6761FS Iomax=0.48/RNF [A] BD6762FV Iomax=0.26/RNF [A]
⑨OSC frequency (BA6680FS) Triangular waveform is formed by the capacitance to connect.	A value of C=100pF and Frequency=95kHz (Typ.) is appropriate.
⑩Hall input noise Insert capacitors between the hall phases in order to eliminate the hall input noise due to the effect by the pattern routing design.	A value of 0.01μF is appropriate for the capacitor to be installed between the hall phases. A value of 0.01μF to 0.1μF is recommended.
⑪CL (RF) voltage smoothing low pass filter Smooth the CL (RF) voltage which has PWM noise through the low pass filter.	A value of C = 470pF and R=1kΩ is appropriate for the low pass filter. For the external constant, since the impedance is high, make sure to design the pattern with the shortest circuit route so that the circuit is hard to be affected by noise.
⑫FG AMP constant setting FG AMP gain: GFG is the ratio of R1 and R2 calculated by the following equation: GFG=20log R2/R1 [dB] Set up the gain so that the FGOUT amplitude is large enough to the hysteresis level of the hysteresis comparator and it cannot be clamped by the high and low output voltages (VFGOH and VFGOL).	R1 and C1 form a high pass filter and R2 and C2 form a low pass filter. Each cut off frequency; f_{MPF} and f_{LPF} is determined by the following equation: $f_{MPF}=1/2\pi R1C1$, $f_{LPF}=1/2\pi R2C2$ Set the value so that the main signal from PG by the motor is not attenuated but the unnecessary noise.

Design method	Design example
⑬Phase compensation capacitor (BA6680FS, BD6761FS) Phase compensation is performed in the output of the CS amplifier. The capacitance value should be selected according to the servo constant, and proper motor operation should be confirmed. When the capacitance is large, the I/O response becomes bad. When it is small, the output can easily oscillate.	A value of 0.001 μF to 0.1 μF is recommended. A value of 0.001 μF is appropriate for BA6680FS. A value of 0.1 μF is appropriate for BD6761FS.
⑭VCC pin Set up the capacitance for the stabilization and noise reduction on the power line.	A value of value 1 μF to 10 μF is recommended. A value of 10 μF is appropriate.
⑮Charge pump filter (BA6680FS) Filter composed of C3, C4 and R3 smoothes the current pulses output from the CPOUT pin and converts it to DC. This impedance Z is shown by the following equation: $Z = R3 \times \frac{C4}{C3+C4} \times \frac{S+\omega_2}{S\left(1+\frac{S}{\omega_1}\right)}$ When the pole frequency is set to fP1 and fP2, they are: $fP1=\omega_1/2\pi=1/2\pi(C3//C4)R3$ $fP2=\omega_2/2\pi=1/2\pi C4R3$	Recommended values: C3: 0.01 μF to 0.1 μF; a value of 0.01 μF is appropriate. C4: 0.033 μF to 0.33 μF; a value of 0.1 μF is appropriate. R3 : 30kΩ to 300kΩ; a value of 100kΩ is appropriate.
⑯Output FET gate voltage stabilization resistor When the noise is generated at the time of external MOSFET on/off, due to the rise and fall speed of the IC output, insert the resistor between the IC output and external MOSFET gate.	Establish R so that the simultaneous on prevention time does not exceeded as shown in #7. Output simultaneous on prevention circuit in P.17/24 Operating Explanation. A value of R = 0Ω is appropriate.
⑰Peak hold setting capacitor (BD6761FS) Charges the peak hold on the voltage at the current detection pin CL.	A value of 0.33 μF is appropriate.
⑱Motor locking detection time setting capacitor (BD6762FV) Motor locking detection time T_{LP} is determined by the capacitor C7 which is connected to the LP pin and the count number CLP (Preset value: 96) of the internal counter. The T_{LP} is shown by the following equation: $TLP=2\times10^5\times C7\times96$	A value of 0.22 μF is appropriate.
⑲Integration amplifier constant setting (BD6762FV) Speed discriminator side current value ID is shown by $\lvert I_D \rvert = 2.5/R4$ and the PLL side current value IP is shown by $\lvert I_P \rvert = 2.5/R5$. Therefore, the current I_{IN} which flows in the integration AMP input pin INTIN is shown by $I_{IN}=I_D+I_P$. The larger the I_{IN} is, the higher the integration amplifier gain becomes. Gains of the speed discriminator and PLL can be set by adjusting R4 and R5. Gain G is shown by the following equation: $G = \frac{R6}{R4 // R5} \times \frac{C6}{C5+C6} \times \frac{S+\omega_2}{S\left(1+\frac{S}{\omega_1}\right)}$ When the pole frequency is set to fP1 and fP2, they are: $fP1=\omega_1/2\pi=1/2\pi(C5//C6)\times R6$ $fP2=\omega_2/2\pi=1/2\pi C6R6$	Recommended values: R4: 10kΩ to 40kΩ; a value of 20 kΩ is appropriate. R5: 300kΩ to 3MΩ; a value of 1 MΩ is appropriate. R6: 100kΩ to 500kΩ; a value of 220 kΩ is appropriate. C5: 0.01 μF to 0.1 μF; a value of 0.047 μF is appropriate. C6: 0.033 μF to 1.0 μF; a value of 0.47 μF is appropriate.
⑳LPF external constant (BD6762FV) Filter composed of C8, C9 and R7 smoothes the current pulses output from the LPF pin and converts it to DC. This impedance Z is shown by the following equation: $Z = R7 \times \frac{C9}{C8+C9} \times \frac{S+\omega_2}{S\left(1+\frac{S}{\omega_1}\right)}$ When the pole frequency is set to fP1 and fP2, they are: $fP1=\omega_1/2\pi=1/2\pi(C8//C9)R7$ $fP2=\omega_2/2\pi=1/2\pi C9R7$	Recommended values: C8: 0.1 μF to 0.6 μF; a value of 0.33 μF is appropriate. C9: 0.1 μF to 0.6 μF; a value of 0.33 μF is appropriate. R7: 0.5kΩ to 10kΩ; a value of 2kΩ is appropriate.

※Setting values in these materials are only for reference. Actual set may change its characteristics due to the board layout, wiring and components each type uses. Please perform the sufficient verification using the actual product for the field operation.

●Operation Notes

1. Absolute maximum ratings

   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Connecting the power supply connector backward

   Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines.
   An external direction diode can be added.

3. Power supply lines

   Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, note that capacitance characteristic values are reduced at low temperatures.

4. GND voltage

   The potential of GND pin must be minimum potential in all operating conditions.

5. Thermal design

   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6. Inter-pin shorts and mounting errors

   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7. Operation in a strong electromagnetic field

   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8. ASO

   When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9. Thermal shutdown circuit

   The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD on temperature [°C] (Typ.)	Hysteresis temperature [°C] (Typ.)
BA6680FS	175	25
BD6761FS	175	35
BD6762FV	175	23

10. PWM drive

    Voltage between the output FET drain and source may exceed the absolute maximum ratings due to the fluctuation of VCC at the time of PWM driving. If there is the threat of this problem, it is recommended to take physical countermeasures for safety such as inserting the capacitor between the VCC pin of FET and the detection resistor pin.

11. Testing on application boards

    When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

12. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

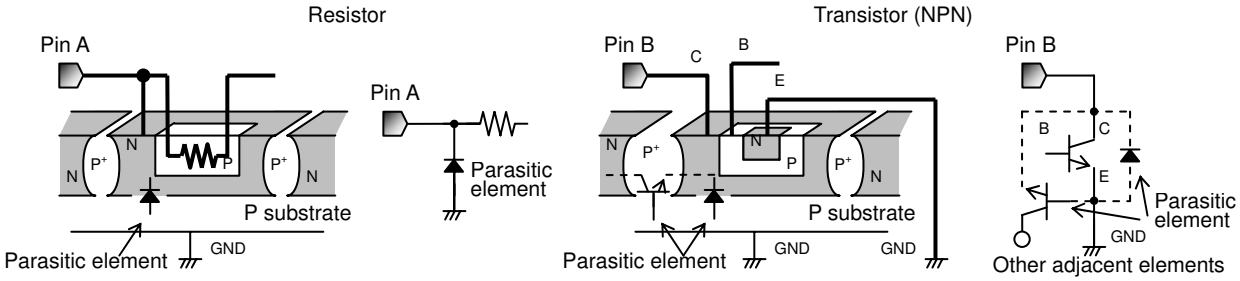


Fig.31 Example of IC structure

13. Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

●**Selecting a model name when ordering**

B	A	6	6	8	0	F	S	–	E	2

ROHM model name

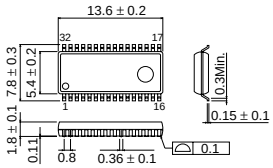
Part number

Package type
FS=SSOP-A32
FV=SSOP-B40

Taping type
E2=Reel-wound embossed taping

SSOP-A32

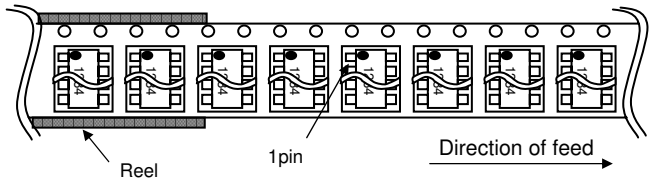
<Dimension>



(Unit:mm)

<Tape and Reel information>

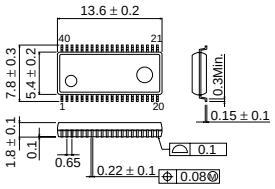
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

SSOP-B40

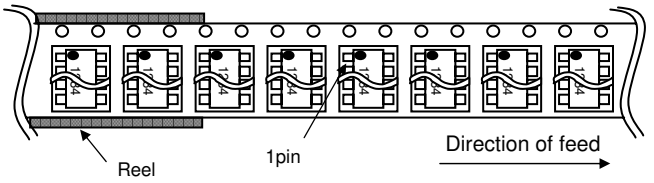
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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