DATA SHEET

# SKY87222: Dual Step-Down DC-DC Converter

## Applications

- Wi-Fi systems
- Access points
- Laptops/ultra-books

## Features

- $V_{IN}$ range: 2.7 V to 5.0 V
- OUT1: fixed 1.8 V at 500 mA
- OUT2: adjustable from 0.6 V to 3.3 V at 1.5 A
- 1.2 MHz switching frequency
- 92% peak efficiency (OUT1)
- 80% light load efficiency
- EN and Power Good for power sequencing
- Cycle-by-cycle over-current protection
- Over-temperature protection
- Control loop stabilization with low ESR ceramic capacitors
- Internal soft start
- –40 °C to 85 °C operating temperature range.
- Low profile QFN (17-pin, 2.0 mm × 2.5 mm) package (MSL1, 260 ºC per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

## Description

The SKY87222 is a dual, 1.2 MHz, Constant On-time (COT) synchronous step-down DC-DC converter. The SKY87222 provides a fixed output voltage of 1.8 V and an adjustable output voltage from 0.6 V to 3.3 V from input voltage ranging from 2.7 V to 5.0 V. The SKY87222 provides excellent line and load regulation along with high light load efficiency.

The Constant On-time control allows for easy loop stabilization with minimal external components while providing fast transient response. Power sequencing is available via EN pins along with a Power Good pin.

The SKY87222 has cycle-by-cycle current limit and thermal shutdown to protect against fault conditions.

The SKY87222 is available in a Pb-free, low-profile, 17-pin 2.0 mm × 2.5 mm Quad Flat No-Lead (QFN) package, and rated over the –40 °C to 85 °C temperature range.

A typical application circuit is shown in Figure 1. The pin configurations are shown in Figure 2. Pin assignments and pin descriptions are provided in Table 1.

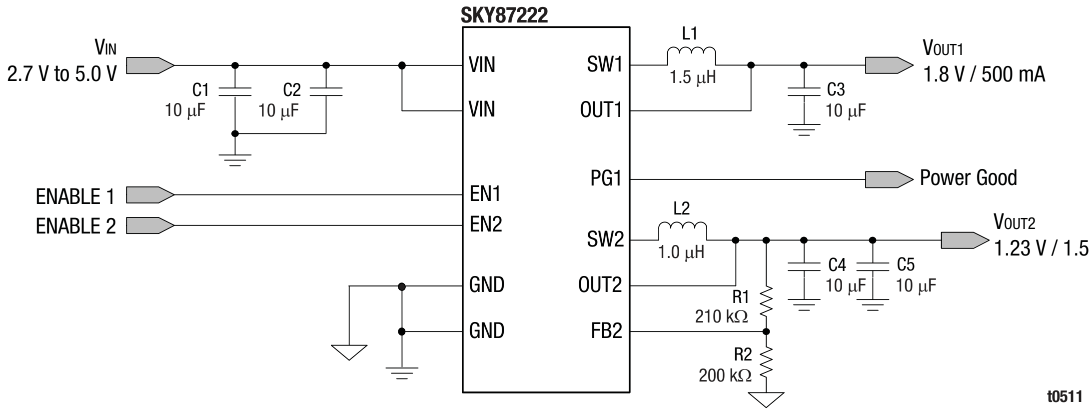



**Figure 1. SKY87222 Typical Application Circuit**

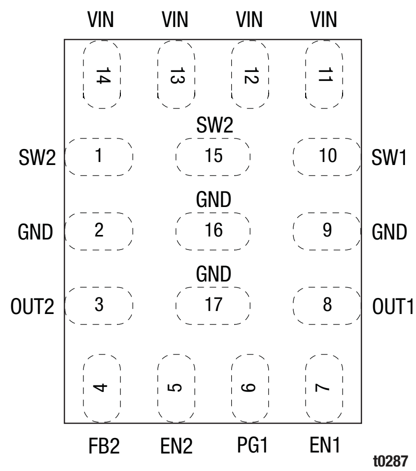



**Figure 2. SKY87222 Pinout – 17-Pin, 2.0 mm × 2.5 mm QFN (Top View)**

**Table 1. SKY87222 Pin Descriptions**

| Pin | Name | I/O | Description |
|---|---|---|---|
| 1, 15 | SW2 | O | Switch node for buck converter 2. Internally connected to an NMOS switch to GND and a PMOS switch to VIN. The SW2 pin is high impedance when EN2 is low. Connect to the inductor for the buck converter 2. |
| 2, 16 | GND | - | Power ground for buck converter 2. |
| 3 | OUT2 | I | Output sense pin for buck converter 2. |
| 4 | FB2 | I | Feedback voltage pin for buck converter 2. Adjust the output voltage of buck converter 2 according to the ratio of the feedback resistors. |
| 5 | EN2 | I | Buck converter 2 Enable. Active high enable input. Connect to VIN or a logic high for normal operation. Connect to GND or a logic low for shutdown mode. |
| 6 | PG1 | O | Power Good pin for buck converter 1. Open drain with internal pull up resistor. |
| 7 | EN1 | I | Buck converter 1 Enable. Active high enable input. Connect to VIN or logic high for normal operation. Connect to GND or a logic low for shutdown mode. |
| 8 | OUT1 | I | Output sense pin for buck converter 1. |
| 9, 17 | GND | - | Power ground for buck converter 1. |
| 10 | SW1 | O | Switch node for buck converter 1. Internally connected to an NMOS switch to GND and a PMOS switch to VIN. The SW1 pin is high impedance when EN1 is low. Connect to the inductor for buck converter 1. |
| 11, 12, 13, 14 | VIN | I | Power supply pins for the buck converter 1 and the buck converter 2. Note VIN must be connected to the same supply source. |

## Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY87222 are provided inTable 2, the thermal information is listed in Table 3, and electrical specifications are provided in Table 4. Typical performance characteristics of the SKY87222 are shown in Figures 3 through 45.

**Table 2. SKY87222 Absolute Maximum Ratings (Note 1)**

| Parameter | Symbol | Minimum | Maximum | Units |
|---|---|---|---|---|
| VIN to GND | $V_{IN}$ | –0.3 | +5.5 | V |
| GND (pins 9, 17) to GND (pins 2, 16) | $V_{GND}$ | –0.3 | +0.3 | V |
| SW1 to GND (pins 9, 17), SW2 to GND (pins 2, 16) | $V_{SW1}$, $V_{SW2}$ | –0.3 | $V_{IN}$ + 0.3 | V |
| OUT1, OUT2, FB2, PG1, EN1, EN2 to GND | $V_{OUT1}$, $V_{OUT2}$, $V_{FB2}$, $V_{PG1}$, $V_{EN1}$, $V_{EN2}$ | –0.3 | +5.5 | V |
| Maximum continuous current for SW1 | $I_{SW1(MAX)}$ | | 500 | mA |
| Maximum continuous current for SW2 | $I_{SW2(MAX)}$ | | 1500 | mA |
| Junction operating temperature | $T_J$ | –40 | +150 | ºC |
| Storage temperature | $T_S$ | –65 | +150 | ºC |
| Maximum soldering temperature (at leads, 10 seconds) | $T_{LEAD}$ | | 260 | ºC |

**Note 1:** Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed may result in permanent damage to the device.

**Table 3. SKY87222 Thermal Information**

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Thermal resistance, junction to ambient (Note 1, Note 2) | $\theta_{JA}$ | 72 | ºC/W |
| Maximum power dissipation (at 25 °C) | $P_D$ | 1.7 | W |

**Note 1:** Mounted on an FR4 board. Two-layer, 1 ounce copper.

**Note 2:** The thermal resistance is measured in accordance with EIA/JESD 51 series.

***CAUTION:*** *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

**Table 4. SKY87222 Electrical Specifications (1 of 2) (Note 1)**
**($V_{OUT1}$ = 1.8 V, $V_{OUT2}$ = 1.23 V, $V_{IN}$ = 3.3 V, $V_{EN1}$ = $V_{EN2}$ = 3.3 V, C1 = C2 = 10 μF, C3 = 10 μF, C4 = C5 = 10 μF, L1 = 1.5 μH, L2 = 1.0 μH, R1 = 210 kΩ, R2 = 200 kΩ, $T_A$ = –40 °C to +85°C, Typical Values are at $T_A$ = 25 °C, Unless Otherwise Noted)**

| Parameter | Symbol | Test Condition | Min | Typical | Max | Units |
|---|---|---|---|---|---|---|
| ***Operation*** | | | | | | |
| Operating input voltage | $V_{IN}$ | | 2.7 | | 5.0 | V |
| Input under-voltage lockout | $V_{IN\_UVLO}$ | $V_{IN}$ rising | 2.3 | 2.5 | 2.7 | V |
| | | Hysteresis | | 400 | | mV |
| Quiescent supply current | $I_Q$ | Both step-down converters enabled, No load, no switching | | 80 | | μA |
| | | OUT1 enabled, No load, no switching. $V_{EN1}$ =3.3 V, $V_{EN2}$ = 0 V, $V_{OUT1}$ = 1.95 V | | 60 | | μA |
| | | OUT2 enabled, No load, no switching. $V_{EN2}$ = 3.3 V, $V_{EN1}$ = 0 V, $V_{FB2}$ = 0.63 V | | 60 | | μA |
| Shutdown supply current | $I_{SHDN}$ | $V_{IN}$ = 5.0 V, $V_{EN1}$ = $V_{EN2}$ = 0 V | | | 1 | μA |
| ***Step-Down Converter 1*** | | | | | | |
| Output voltage (Note 2) | $V_{OUT1\_REG}$ | $I_{OUT1}$ = 10 mA | | 1.800 | | V |
| | | Voltage accuracy, $V_{IN}$ = 3.0 V to 3.6 V $I_{OUT1}$ = 100 mA to 500 mA | –3 | | +3 | % |
| Load regulation | $\Delta V_{OUT}/\Delta I_{OUT}$ | $I_{OUT1}$ = 100 mA to 500 mA, $V_{IN}$ = 3.3 V, $V_{OUT1}$ = 1.8 V | | 0.005 | | %/mA |
| Line regulation | $\Delta V_{OUT}/\Delta V_{IN}$ | $I_{OUT1}$ = 400 mA, $V_{IN}$ = 3.0 V to 3.6 V, $V_{OUT1}$ = 1.8 V | | 0.1 | | %/V |
| Internal high-side PMOS On resistance | $R_{DS(ON)P}$ | | | 180 | | mΩ |
| Internal low-side NMOS On resistance | $R_{DS(ON)N}$ | | | 120 | | mΩ |
| Over-current threshold | $I_{OCP}$ | | | 1.2 | | A |
| SW1 pin leakage current | $I_{SW1\_LKG}$ | $V_{SW1}$ = 0 V and 5.0 V, $V_{IN}$ = 5.0 V | | 0.01 | 2 | μA |
| On time | $t_{ON}$ | $V_{IN}$ = 5.0 V, $V_{OUT1}$ = 1.8 V | | 300 | | ns |
| | | $V_{IN}$ = 3.3 V, $V_{OUT1}$ = 1.8 V | | 455 | | ns |
| Minimum Off time | $t_{OFF\_MIN}$ | | | 30 | | ns |
| Switching frequency | $f_{SW}$ | $V_{IN}$ = 3.3 V, $V_{OUT1}$ = 1.8 V, $I_{OUT1}$ = 350 mA | | 1.2 | | MHz |
| PSM threshold | | $V_{IN}$ = 3.0 V to 3.6 V, $V_{OUT1}$ = 1.8 V, $f_{SW}$ = 1.2 MHz, L1 = 1.5 μH, $I_{OUT1}$ decreasing | | | 75 | mA |
| | | Hysteresis | | 25 | | mA |
| Soft start time period | $t_{SS}$ | $V_{IN}$ = $V_{EN1}$ = 0 V to 3.3 V, $R_{LOAD}$ = 9 Ω (200 mA), time to $V_{OUT1}$ = 0.9 × $V_{OUT1\_REG}$ | | 300 | | μs |
| | | $V_{IN}$ > $V_{IN\_UVLO}$, $V_{EN1}$ = 0 V to 3.3 V, $R_{LOAD}$ = 9 Ω (200 mA), time to $V_{OUT1}$ = 0.9 × $V_{OUT1\_REG}$ | | 300 | 400 | μs |

**Table 4. SKY87222 Electrical Specifications (2 of 2) (Note 1)**
**($V_{OUT1}$ = 1.8 V, $V_{OUT2}$ = 1.23 V, $V_{IN}$ = 3.3 V, $V_{EN1}$ = $V_{EN2}$ = 3.3 V, C1 = C2 = 10 μF, C3 = 10 μF, C4 = C5 = 10 μF, L1 = 1.5 μH, L2 = 1.0 μH, R1 = 210 kΩ, R2 = 200 kΩ, $T_A$ = –40 °C to +85°C, Typical Values are $T_A$ = 25 °C, Unless Otherwise Noted)**

| Parameter | Symbol | Test Condition | Min | Typical | Max | Units |
|---|---|---|---|---|---|---|
| ***Step-Down Converter 2*** | | | | | | |
| Output voltage | $V_{OUT2}$ | | 0.6 | | 3.3 | V |
| Feedback voltage | $V_{FB2}$ | 3.0 V ≤ $V_{IN}$ ≤ 3.6 V, $T_A$ = 0 °C to 70 °C | 0.591 | 0.6 | 0.609 | V |
| Feedback bias current | $I_{FB2}$ | $V_{FB2}$ = 0.6 V | | 10 | | nA |
| Load regulation | $\Delta V_{OUT}/\Delta I_{OUT}$ | $I_{OUT2}$ = 250 mA to 1500 mA, $V_{IN}$ = 3.3 V, $V_{OUT2}$ = 1.23 V | | 0.005 | | %/mA |
| Line regulation | $\Delta V_{OUT}/\Delta V_{IN}$ | $I_{OUT2}$ = 1000 mA, $V_{IN}$ = 3.0 V to 3.6 V, $V_{OUT2}$ = 1.23 V | | 0.1 | | %/V |
| Internal high-side PMOS On resistance | $R_{DS(ON)P}$ | | | 90 | | mΩ |
| Internal low-side NMOS On resistance | $R_{DS(ON)N}$ | | | 60 | | mΩ |
| Over-current threshold | $I_{OCP}$ | | | 2.75 | | A |
| SW2 pin leakage current | $I_{SW2\_LKG}$ | $V_{SW2}$ = 0 V and 5.0 V, $V_{IN}$ = 5.0 V | | 0.01 | 2 | μA |
| On time | $t_{ON}$ | $V_{IN}$ = 5.0 V, $V_{OUT2}$ = 1.23 V | | 205 | | ns |
| | | $V_{IN}$ = 3.3 V, $V_{OUT2}$ = 1.23 V | | 311 | | ns |
| Minimum Off time | $t_{OFF\_MIN}$ | | | 30 | | ns |
| Switching frequency | $f_{SW}$ | $V_{IN}$ = 3.3 V, $V_{OUT2}$ = 1.23 V, $I_{OUT2}$ = 1.0 A | | 1.2 | | MHz |
| PSM threshold | | $V_{IN}$ = 3.0 V to 3.6 V, $V_{OUT2}$ = 1.23 V, $f_{SW}$ = 1.2 MHz, L2 = 1.0 μH, $I_{OUT2}$ decreasing | | | 200 | mA |
| | | Hysteresis | | 50 | | mA |
| Soft start time period | $t_{SS}$ | $V_{IN}$ = $V_{EN2}$ = 0 V to 3.3 V, $R_{LOAD}$ = 6 Ω (200 mA), time to $V_{OUT2}$ = 0.9 × $V_{OUT2\_REG}$ | | 300 | | μs |
| | | $V_{IN}$ > $V_{IN\_UVLO}$, $V_{EN2}$ = 0 V to 3.3 V, $R_{LOAD}$ = 6 Ω (200 mA), time to $V_{OUT2}$ = 0.9 × $V_{OUT2\_REG}$ | | 300 | 400 | μs |
| ***Logic*** | | | | | | |
| Input high threshold | $V_{IH}$ | EN1, EN2 | 1.2 | | | V |
| Input low threshold | $V_{IL}$ | EN1, EN2 | | | 0.4 | V |
| Logic input pull-down resistance | $R_{PD}$ | EN1, EN2 pins | 1 | 2 | | MΩ |
| ***Power Good (PG1)*** | | | | | | |
| PG1 upper threshold | $V_{PG1\_HI}$ | | | 1.1 × $V_{OUT1\_REG}$ | | V |
| PG1 lower threshold | $V_{PG1\_LO}$ | | | 0.9 × $V_{OUT1\_REG}$ | | V |
| PG1 delay | $t_{PG1\_DLY}$ | Delay from OUT1 in regulation to PG1 going high | | 90 | | μs |
| PG1 output low | $V_{OL}$ | $I_{OL}$ = 2 mA | | | 0.4 | V |
| PG1 internal pull-up resistor | $R_{PG1\_PU}$ | Pull-up resistor to VIN | | 500 | | kΩ |
| ***Protection*** | | | | | | |
| Thermal shutdown | $T_{SD}$ | | | 140 | | °C |
| Thermal shutdown hysteresis | $T_{SD\_HYS}$ | | | 30 | | °C |

**Note 1:** Performance is guaranteed only under the conditions listed in this table and is not guaranteed over the full operating or storage temperature ranges. Operation at elevated temperatures may reduce reliability of the device.

**Note 2:** Min and Max limits are specified by design, test, or statistical analysis.

## Typical Performance Characteristics

**($V_{OUT1}$ = 1.8 V, $V_{OUT2}$ = 1.23 V, $V_{IN}$ = 3.3 V, $V_{EN1}$ = $V_{EN2}$ = 3.3 V, C1 = C2 = 10 μF, C3 = 10 μF, C4 = C5 = 10 μF, L1 = 1.5 μH, L2 = 1.0 μH, R1 = 210 kΩ, R2 = 200 kΩ, $T_A$ = –40 °C to +85°C, Typical Values are $T_A$ = 25 °C, Unless Otherwise Noted)**

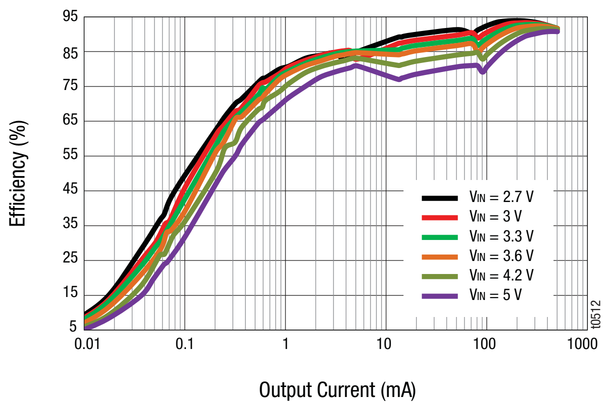



**Figure 3. Buck 1 Efficiency vs Output Current**

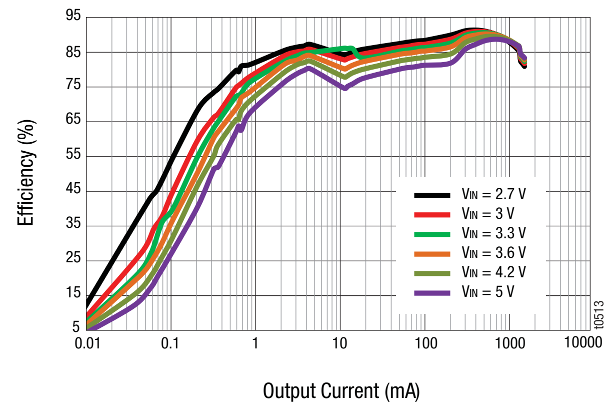



**Figure 4. Buck 2 Efficiency vs Output Current**

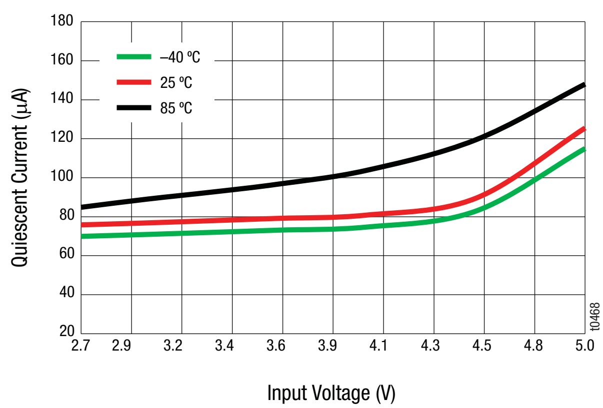



**Figure 5. Quiescent Current vs Input Voltage (Both Bucks Turn-On; No Load; Non-Switching)**

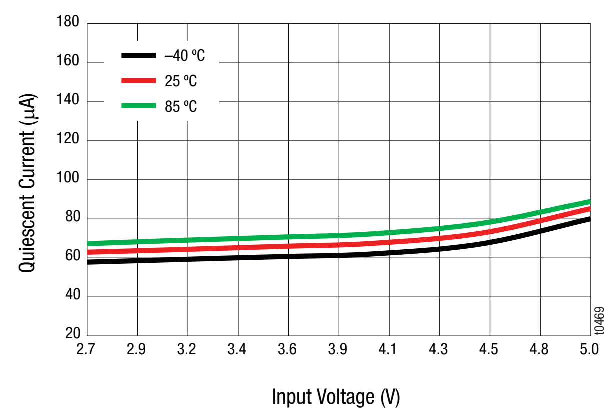



**Figure 6. Quiescent Current vs Input Voltage (Buck 1 Turn-On; No Load; Non-Switching)**

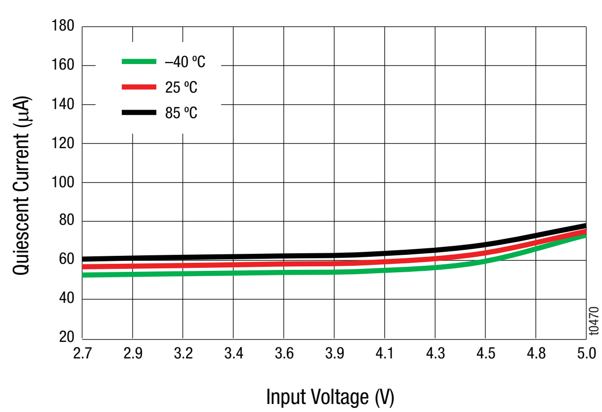



**Figure 7. Quiescent Current vs Input Voltage (Buck 2 Turn-On; No Load; Non-Switching)**

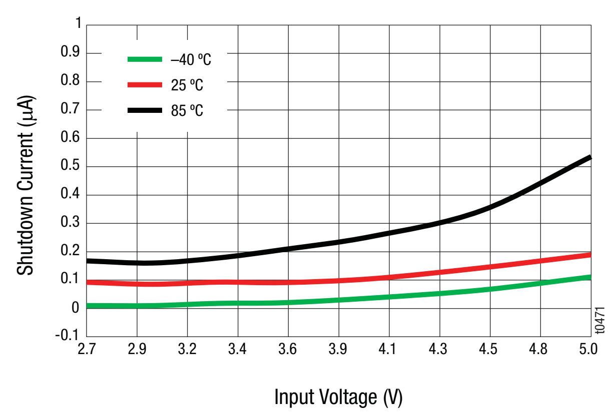



**Figure 8. Shutdown Current vs Input Voltage (Both Bucks Turn-Off)**

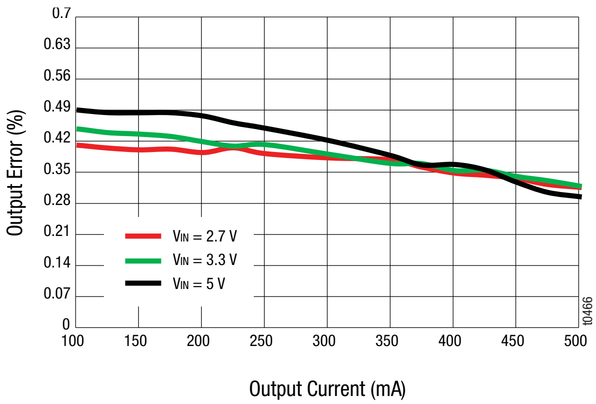



**Figure 9. Buck 1 Load Regulation**

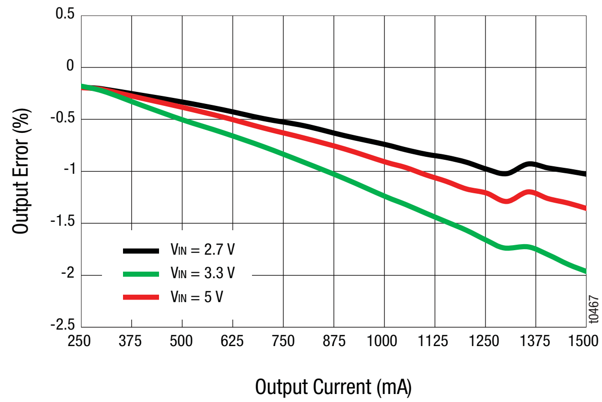



**Figure 10. Buck 2 Load Regulation**

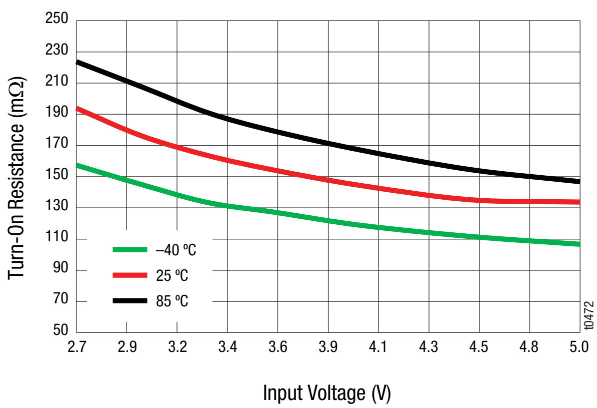



**Figure 11. Buck 1 High-Side PMOS On-Resistance (Isw = 300 mA)**

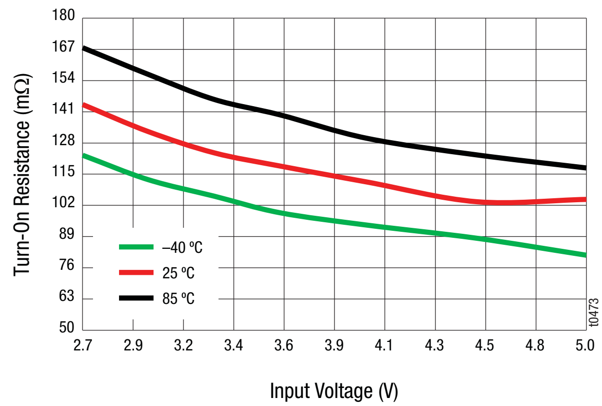



**Figure 12. Buck 1 Low-Side NMOS On-Resistance (Isw = 300 mA)**

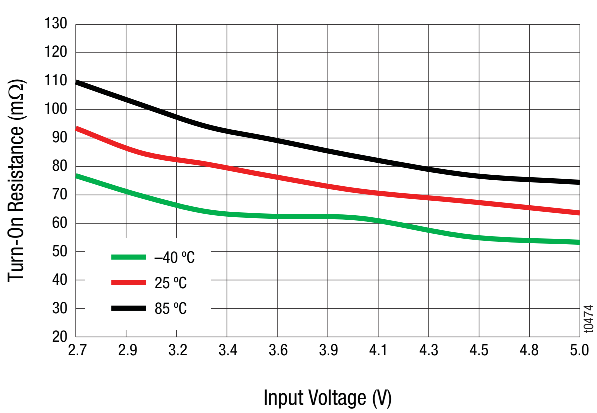



**Figure 13. Buck 2 High-Side PMOS On-Resistance (Isw = 300 mA)**

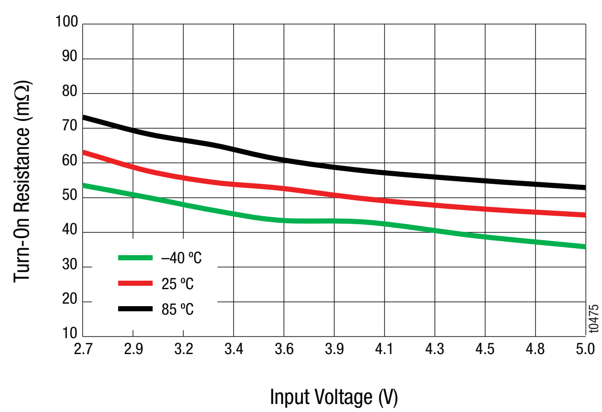



**Figure 14. Buck 2 Low-Side NMOS On-Resistance (Isw = 300 mA)**

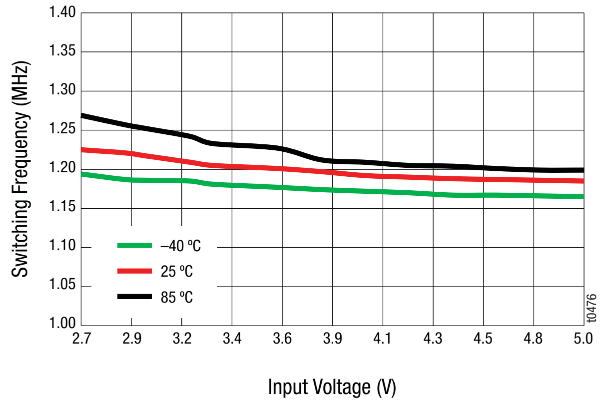



**Figure 15. Buck 1 $V_{IN}$ vs Frequency ($V_{OUT}$=1.8 V, $I_{OUT}$ = 350 mA)**

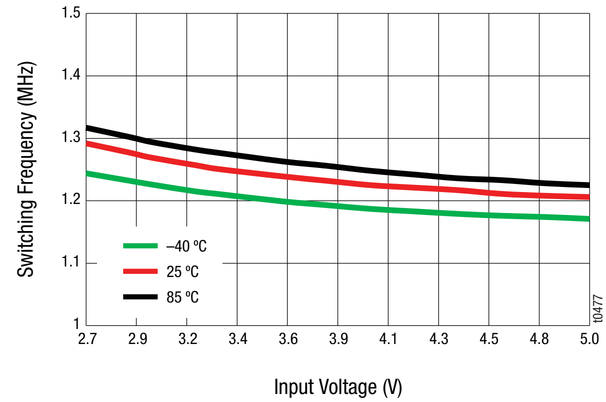



**Figure 16. Buck 2 $V_{IN}$ vs Frequency ($V_{OUT}$=1.23 V, $I_{OUT}$ = 1 A)**

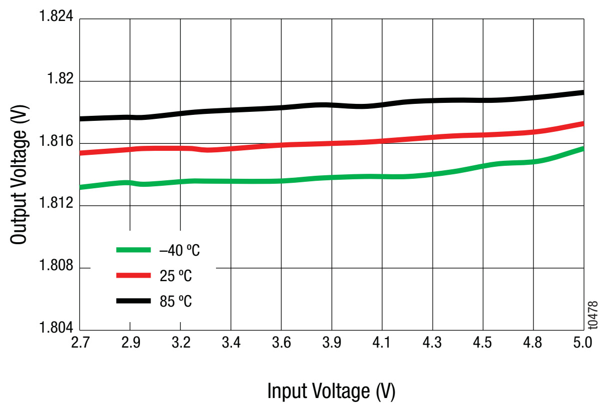



**Figure 17. Buck 1 $V_{OUT}$ vs $V_{IN}$ ($V_{IN}$ = 3.3 V, $I_{OUT}$ = 10 mA)**

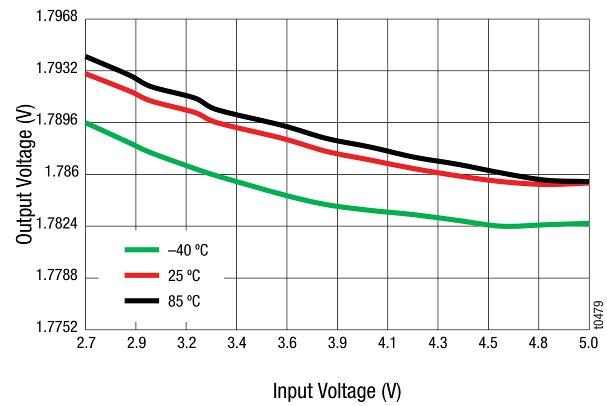



**Figure 18. Buck 1 $V_{OUT}$ vs $V_{IN}$ ($V_{IN}$ = 3.3 V, $I_{OUT}$ = 500 mA)**

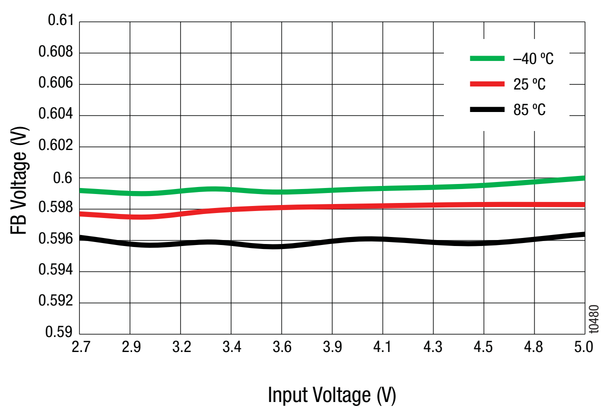



**Figure 19. Buck 1 Feedback Voltage (Test Mode in Open Loop)**

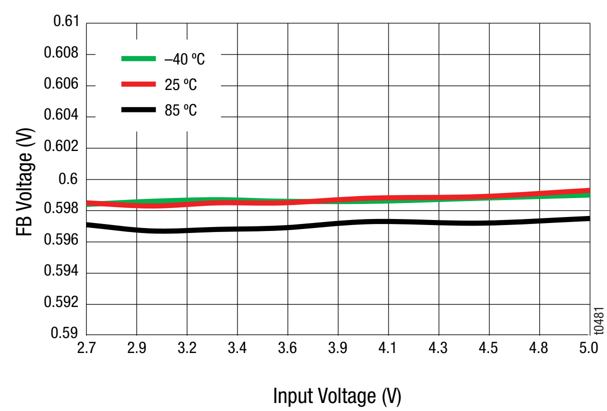



**Figure 20. Buck 2 Feedback Voltage (Test Mode in Open Loop)**

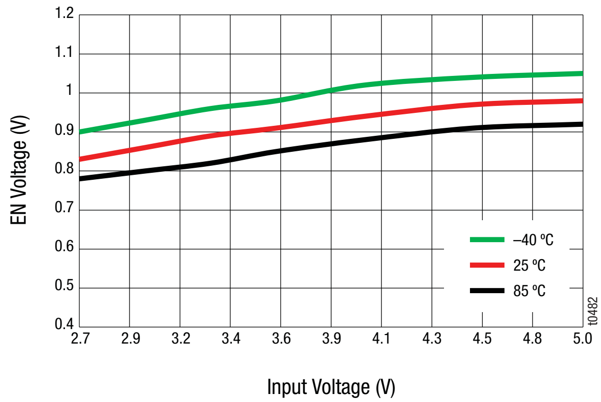



**Figure 21. Enable Logic Voltage vs Input Voltage**

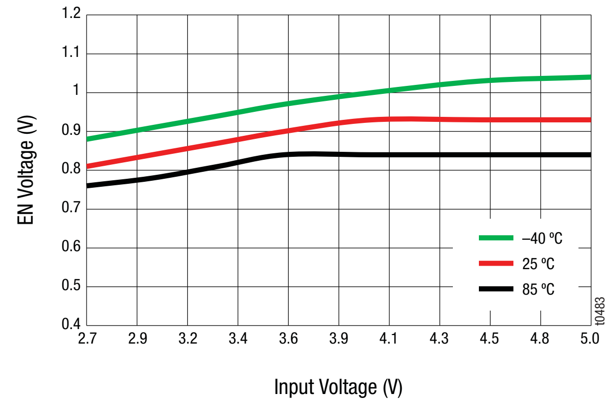



**Figure 22. Disable Logic Voltage vs Input Voltage**

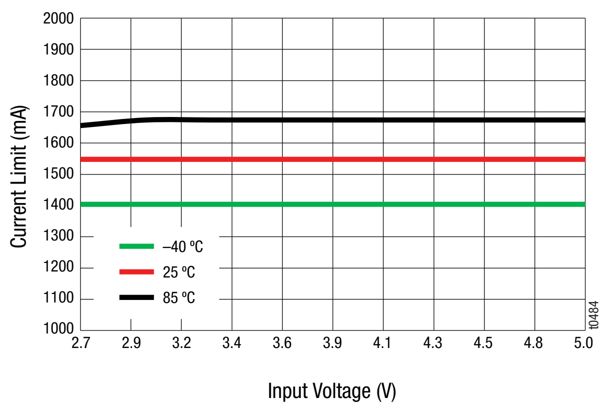



**Figure 23. Buck 1 PMOS Peak Current Limit**

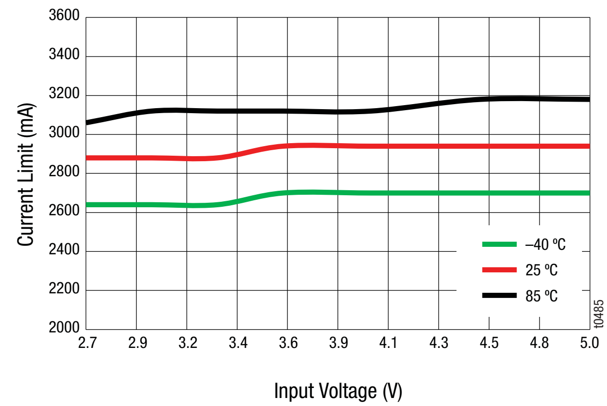



**Figure 24. Buck 2 PMOS Peak Current Limit**

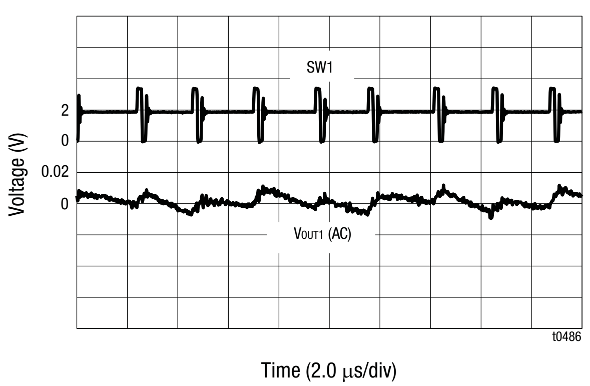



**Figure 25. Buck 1 Output Ripple**
**($V_{IN}$ = EN = 3.3 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 10 mA)**

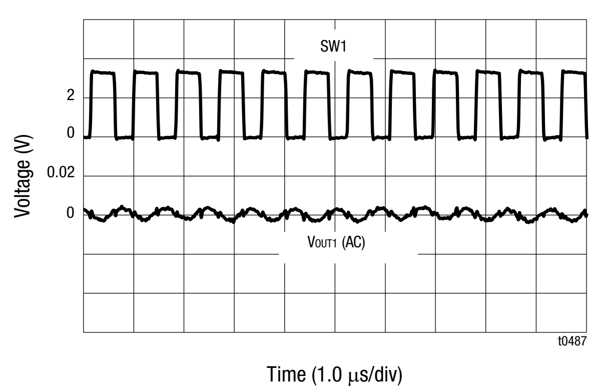



**Figure 26. Buck 1 Output Ripple**
**($V_{IN}$ = EN = 3.3 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 250 mA)**

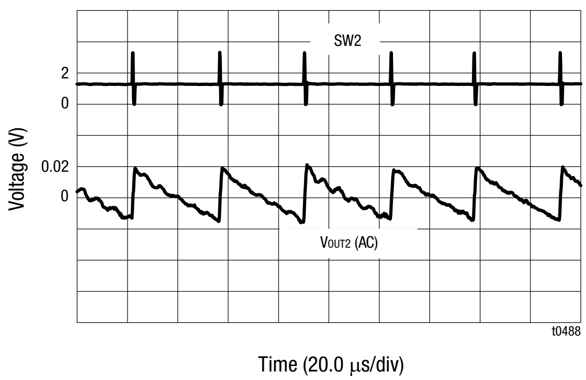



**Figure 27. Buck 2 Output Ripple**
**($V_{IN}$ = EN = 3.3 V, $V_{OUT}$ = 1.23 V, $I_{OUT}$ = 10 mA)**

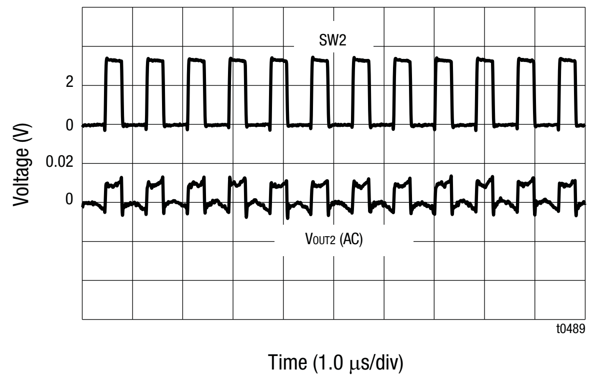



**Figure 28. Buck 2 Output Ripple**
**($V_{IN}$ = EN = 3.3 V, $V_{OUT}$ = 1.23 V, $I_{OUT}$ = 750 mA)**

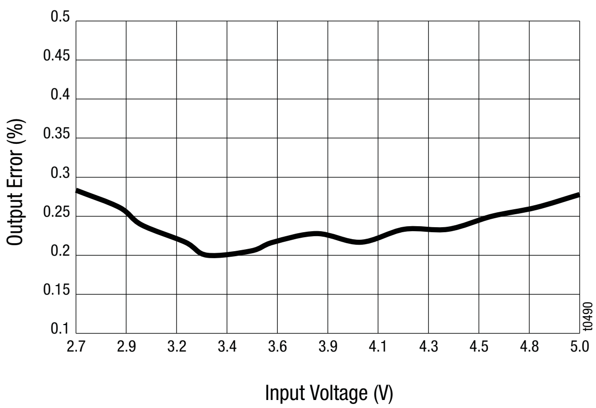



**Figure 29. Buck 1 Output Line Regulation**
**($V_{OUT1}$ = 1.8 V, $I_{OUT}$ = 400 mA)**

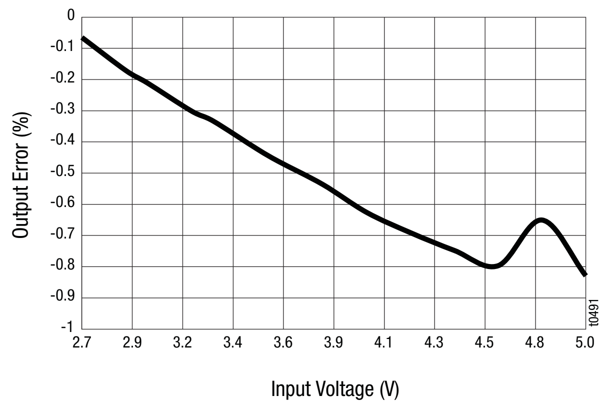



**Figure 30. Buck 2 Output Line Regulation**
**($V_{OUT2}$ = 1.23 V, $I_{OUT}$ = 1 A)**

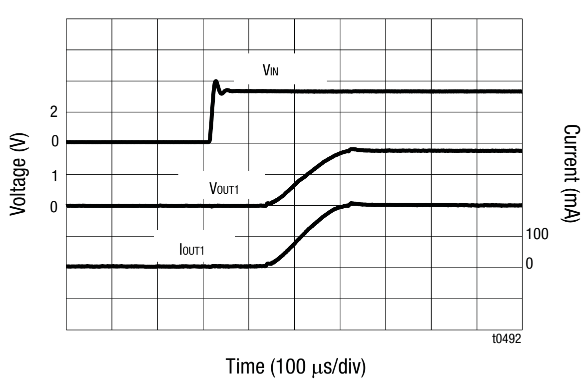



**Figure 31. Buck 1 Output Cold Start**
**($V_{IN}$ = EN = 0 to 3.3 V, $V_{OUT}$ = 1.8 V, $R_{LOAD}$ = 9 Ω)**

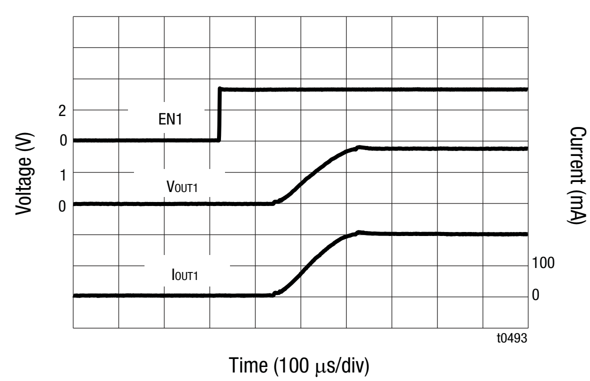



**Figure 32. Buck 1 Output Soft Start**
**($V_{IN}$ = 3.3 V, EN = 0 to 3.3 V, $V_{OUT}$ = 1.8 V, $R_{LOAD}$ = 9 Ω)**

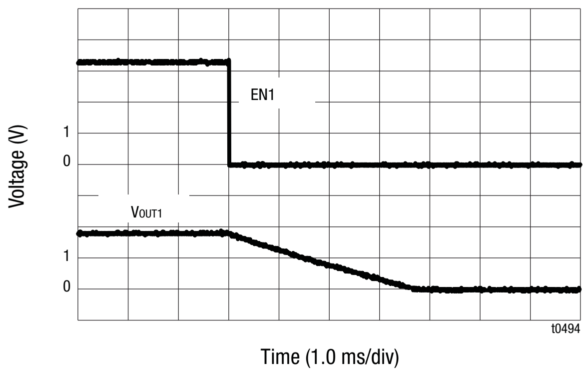



**Figure 33. Buck 1 Output Turn-Off**
**($V_{OUT}$ = 1.8 V, $I_{OUT}$ = 5 mA)**

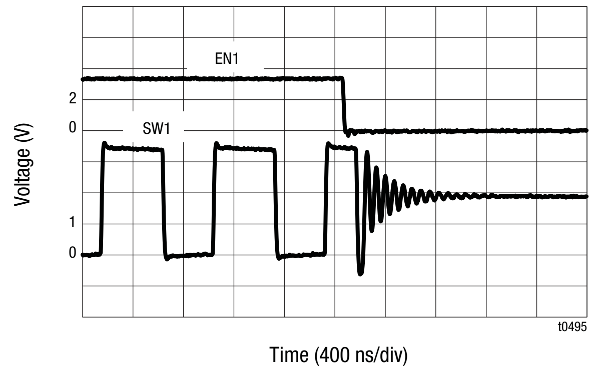



**Figure 34. Buck 1 Output Disable Delay**
**($V_{OUT}$ = 1.8 V, $I_{OUT}$ = 250 mA)**

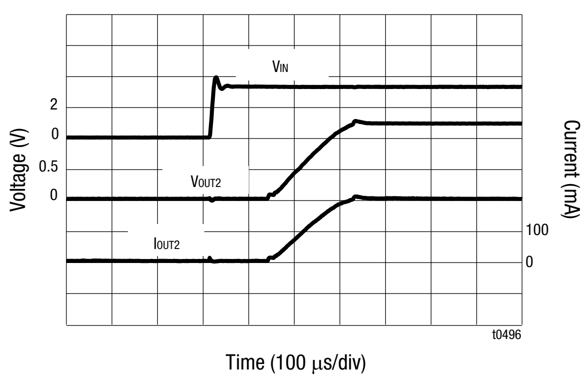



**Figure 35. Buck 2 Output Cold Start**
**($V_{IN}$ = EN = 0 to 3.3 V, $V_{OUT}$ = 1.23 V, $R_{LOAD}$ = 6 Ω)**

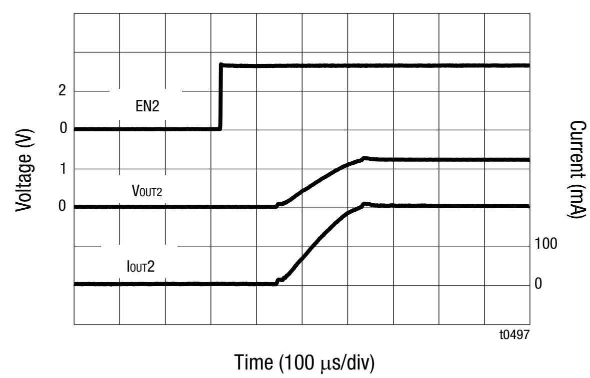



**Figure 36. Buck 2 Output Soft Start**
**($V_{IN}$ = 3.3 V, EN = 0 to 3.3 V, $V_{OUT}$ = 1.23 V, $R_{LOAD}$ = 6 Ω)**

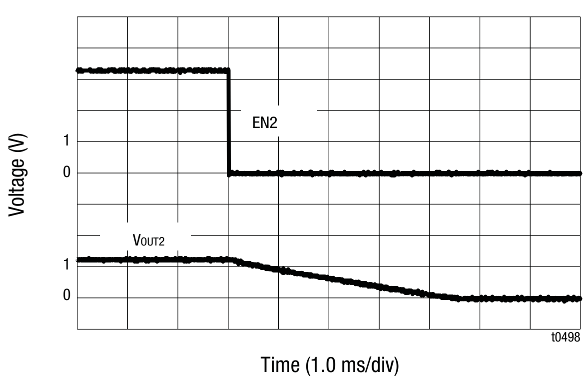



**Figure 37. Buck 2 Output Turn-Off**
**($V_{OUT}$ = 1.23 V, $I_{OUT}$ = 5 mA)**

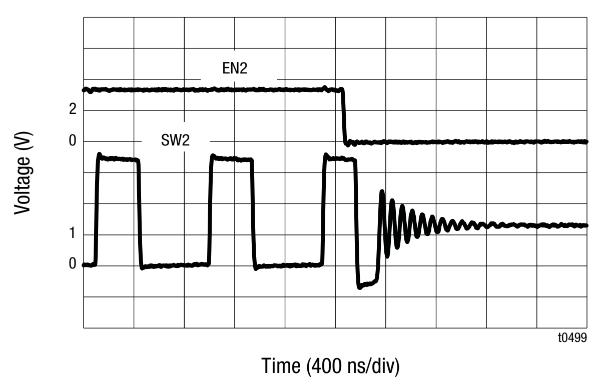



**Figure 38. Buck 2 Output Disable Delay**
**($V_{OUT}$ = 1.23 V, $I_{OUT}$ = 750 mA)**

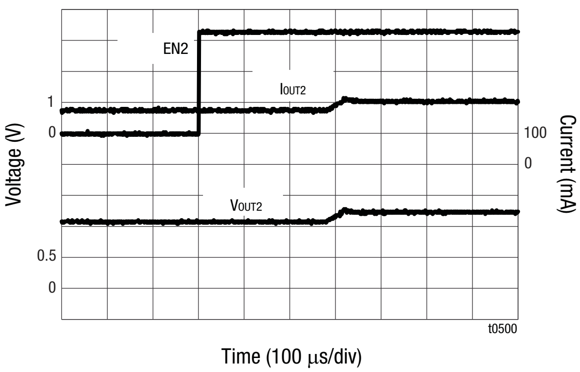



**Figure 39. Buck 2 Pre-bias Soft Start**
**($V_{OUT}$ from 1.1 V Pre-bias to 1.23 V, $I_{OUT}$ = 200 mA)**

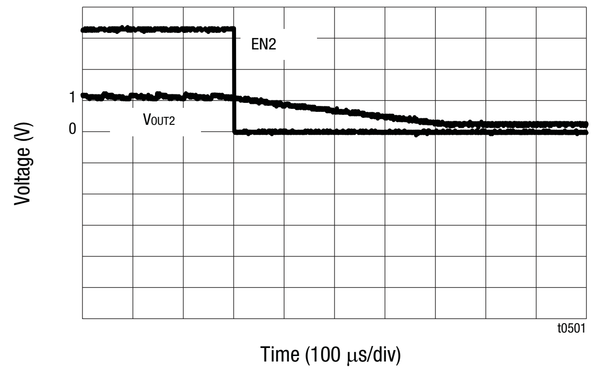



**Figure 40. Buck 2 Output Pre-bias Turn-off**
**($V_{OUT}$ from 1.23 V to 1.1 V Pre-bias, $I_{OUT}$ = 5 mA)**

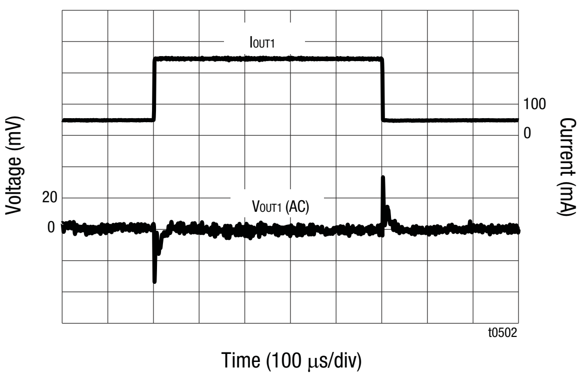



**Figure 41. Buck 1 10% to 50% Load Transient**
**($V_{OUT}$ = 1.8 V, $I_{OUT}$ = 50 to 250 mA within 1.0 μs)**

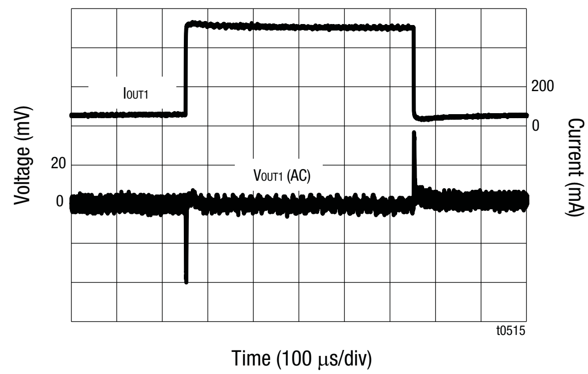



**Figure 42. Buck 1 10% to 100% Load Transient**
**($V_{OUT}$ = 1.8 V, $I_{OUT}$ = 50 to 500 mA within 1.0 μs)**

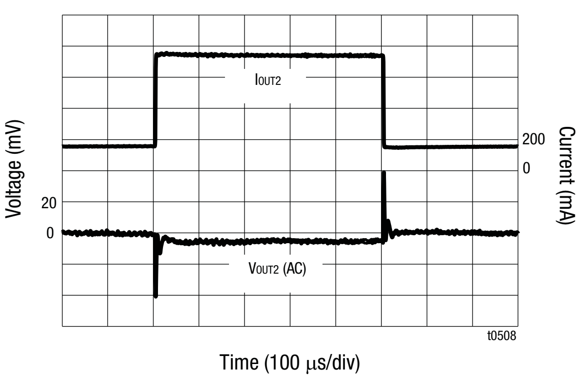



**Figure 43. Buck 2 10% to 50% Load Transient**
**($V_{OUT}$ = 1.23 V, $I_{OUT}$ = 150 to 750 mA within 1.0 μs)**

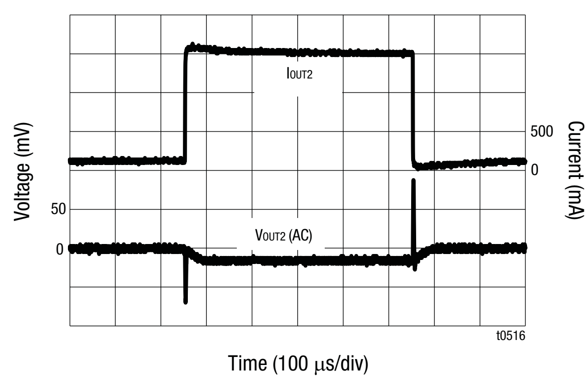



**Figure 44. Buck 2 10% to 100% Load Transient**
**($V_{OUT}$ = 1.23 V, $I_{OUT}$ = 150 to 1500 mA within 1.0 μs)**

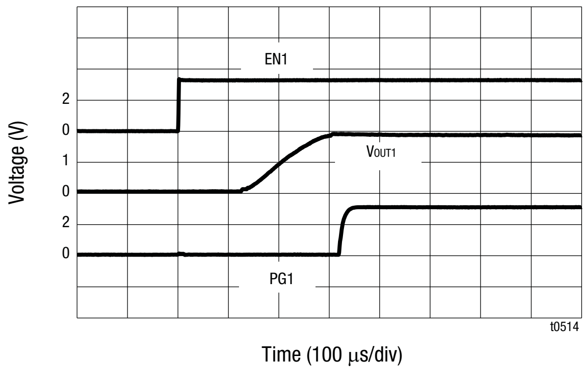



**Figure 45. PG1 Delay**
**($V_{IN}$ = 3.3 V, EN = 0 to 3.3 V, $V_{OUT}$ = 1.8 V)**

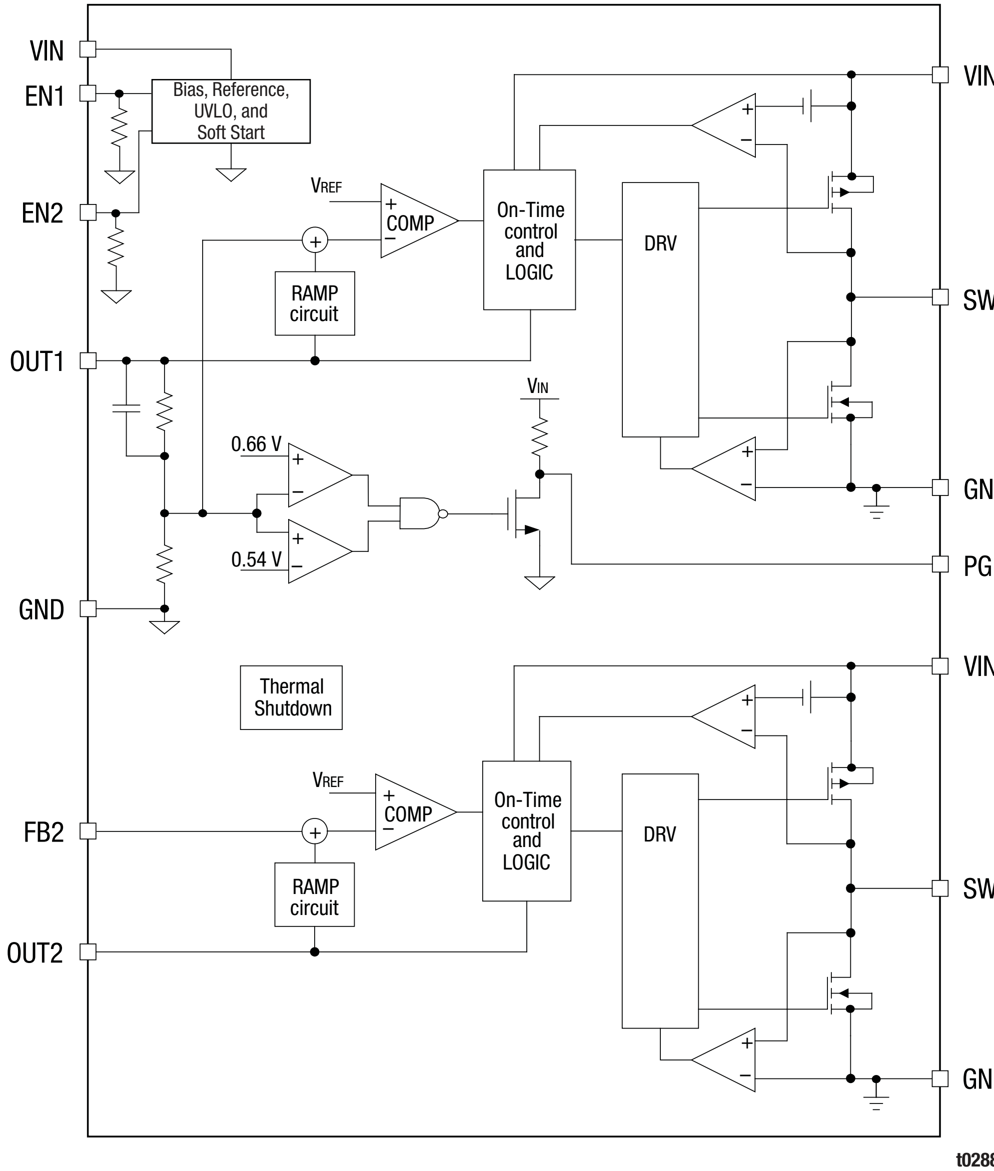



**Figure 46. SKY87222 Functional Block Diagram**

## Functional Description

The SKY87222 is a dual DC-DC step-down converter with one fixed and one adjustable voltage output, and utilizes an adaptive fixed on-time control. A Constant On-time control architecture offers a simpler control loop and faster transient response than a fixed frequency Pulse Width Modulation (PWM) control architecture. A functional block diagram is shown in Figure 46.

The Constant On-time converter maintains a constant output frequency because the "on" time is inversely proportional to the supply voltage. As the input voltage decreases, the "on" time increases, maintaining a relatively constant period.

The device is enabled using the EN input. When the EN pin is pulled high, the converter starts up under the control of a soft start routine. Under light load conditions, the switch enters pulse-skipping mode to ensure regulation is maintained. This effectively changes the switching frequency.

To maintain a wide input voltage range, the switching period is extended when either the minimum "off" or "on" time is reached. The frequency is also affected when switching operates in discontinuous mode. The "on" time of the switching pulses can be estimated using the following equation:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.833\,\mu s$$

The minimum off time is fixed at 30 ns to prevent runaway inductor current during load transients.

### Constant On-Time (COT) Operation

In normal continuous conduction mode, where the inductor current ($I_L$) never reaches zero, the high-side MOSFET is turned on for a fixed interval ($t_{ON}$) determined by the COT sub-circuit (a one-shot timer) within the PWM Control and Logic functional block.

During that fixed interval, the inductor current starts to ramp up. At the end of the $t_{ON}$ period, the high-side MOSFET is turned off and the low-side MOSFET is turned on causing the inductor current to ramp down. At this point, the voltage on the FB pin ($V_{FB}$) goes below the reference voltage ($V_{REF}$) on the comparator, which restarts the one-shot timer and initiates the next cycle. The ideal $t_{ON}$ time in continuous conduction mode is determined by the following relationships:

$$DutyCycle(D) = \frac{V_{OUT}}{V_{IN}}$$

$$OnTime(t_{ON}) = D \times \frac{1}{f_{SW}}$$

If switching frequency ($f_{SW}$) = 1.2 MHz, the on-time equation can be rewritten as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.833\,\mu s$$

The COT circuit generates an “on” time proportional to the ideal duty cycle and holds the switching frequency constant. However, due to nonlinearities in the COT circuit, propagation delays, and non-ideal switch voltage drops due to output current loads, the actual operating frequency will vary slightly.

### Light Load Operation

The SKY87222 transitions to discontinuous conduction mode (DCM) automatically when DC load currents are less than the PSM threshold. When this happens, the SKY87222 monitors the current in the high-side and low-side MOSFETs. During the “on time”, the high-side MOSFET remains on until the high-side current reaches a pre-determined threshold. At this time, the high-side switch turns off and the low-side switch turns on. The low-side switch remains on until the low-side current reaches zero. At this point, the low-side MOSFET is turned off, which prevents the current from going negative. Both the high-side MOSFET and the low-side MOSFETs remain off with the output capacitor supplying the load current until the feedback voltage goes below the reference voltage, triggering a new switching cycle. The switching frequency decreases in light load conditions.

In discontinuous conduction mode, the SKY87222 uses a passive damping scheme to reduce the amplitude and duration of ringing that occurs at the switching node (LX).

### Enable and Soft Start

When input voltage is greater than the Under-Voltage Lockout (UVLO) threshold, either channel of the SKY87222 is enabled by pulling the EN pin higher than 1.2 V. If the EN pin is left floating or pulled down to ground, the regulator is disabled. There is an internal 1.5 MΩ resistor from the EN pin to ground.

The SKY87222 soft-start control prevents output voltage overshoot and limits inrush current when either the input power or the enable input is applied. If the SKY87222’s input and enable are brought up together (normally occurs on the initial power-up) the SKY87222 ramps up the output voltage with a controlled slew rate of ~ 300 μs. Pulling the EN pin low forces the respective converter into a low-power, non-switching state, and forces the switching node into a high-impedance disabled state within 10 μs of disabling the channel.

When both EN signals are pulled low, the respective SKY87222 is forced into a shutdown state that draws less than 1 μA of quiescent current.

Figure 47 shows the soft start and shutdown timing.

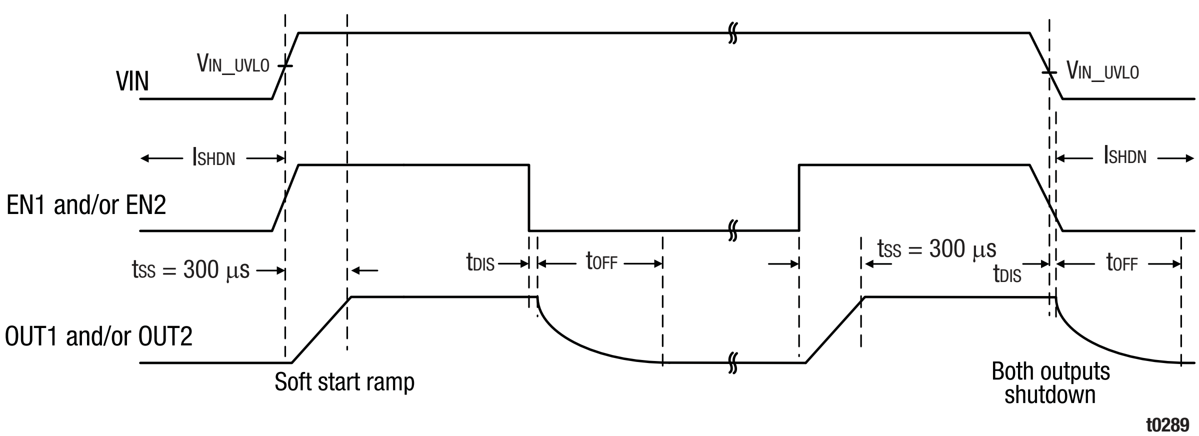



**Figure 47. Soft Start and Shutdown TIming**

### Power Good Pin (PG1)

The SKY87222 has an open-drain, with a 500 kΩ pull-up resistor, Power Good indicator pin (PG1). When the OUT1 pin is within ±10 percent of regulation voltage, the PG1 pin is pulled up to VIN by the internal resistor. If the OUT1 pin voltage is not within ±10 percent of regulation voltage, the PG1 pin is pulled down to ground by an internal MOSFET. The MOSFET has a maximum $R_{DS(ON)}$ of less than 200 Ω.

### Current Limit and Short Circuit Protection

The SKY87222 includes overload protection. The protection turns off the high-side switch when the output current exceeds the over-current threshold of 1.2 A (typ.) for OUT1 or 2.75 A (typ.) for OUT2.

The SKY87222 enters the short-circuit protection mode when the output current hits the current limit. The device tries to recover from the short circuit by entering a "hiccup" mode, in which the regulator disables the output power stage, discharges the soft-start capacitor, and automatically tries a soft start again.

If the short-circuit condition still holds on after a soft start ends, the SKY87222 repeats this protection operation cycle until the short circuit disappears and the output rises back to the regulation level.

### Thermal Protection

An over-temperature thermal shutdown circuit is provided to prevent damage to the IC under adverse operating conditions. An internal temperature monitoring circuit has a junction temperature shutdown threshold of 140 °C. Both converters are disabled during an over-temperature event, and the SKY87222 resets the soft start ramp to 300 µs and automatically restarts when the temperature has fallen below 110 °C.

### Fixed Output Voltage

The SKY87222 has a fixed output voltage of 1.8 V for buck converter 1. The SKY87223 is recommended if an output voltage other than 1.8 V is required.

### Inductor Selection

For OUT1, an inductor value of 1.5 µH is recommended for most SKY87222 applications. For OUT2, inductor values from 0.47 µH to 2.2 µH are recommended. Given the desired input and output voltages, the inductor value and switching frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times f_{SW} \times V_{IN}}$$

Where:

$\Delta I_L$ = Peak-peak inductor ripple current
$f_{SW}$ = Switching frequency
L = Inductor value

Lower ripple current reduces core losses in the inductor, Equivalent Series Resistance (ESR) losses in the output capacitors, and output voltage ripple. Highest efficiency operation is obtained at low frequency with a small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency, and operating frequency.

A reasonable starting point is to choose a ripple current of about 650 mA. The largest ripple current occurs at the highest input voltage, $V_{IN}$. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to the following relationship:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{0.65A \times f_{SW} \times V_{IN}}$$

where $V_{IN}$ = maximum input voltage.

The selected inductance value needs to within ±20% of the calculated value or the PSM threshold may not work properly.

The maximum inductor peak current is calculated according to:

$$I_{PEAK} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

Where:

$I_{PEAK}$ = Peak inductor current
$\Delta I_L$ = Peak-peak inductor ripple current

Manufacturer specifications typically list the inductor current rating based on the inductance change and on the temperature rise. The current that causes the inductance to drop by 30% is generally referred to as the saturation current. The current that causes the temperature to rise by 40 °C is generally referred to as the rms or heating current. Caution should be used when comparing inductors from different manufacturers — make sure that the current ratings are using the same criteria. The inductor current ratings are very important parameters for inductor selection. The ratings must be more than the peak inductor current, $I_{PEAK}$; an adequate margin is important for a safe application.

Always consider the losses associated with DCR and their effect on the total regulator efficiency when selecting an inductor. In general, the DCR of the inductor should be less than the $R_{DS(ON)}$ of the low-side FET of the associated converter. An inductor with high magnetic shield construction is also strongly recommended to suppress EMI noise.

A list of suggested inductors is given in Table 5. Look for inductors that have the lowest DCR and an adequate current rating in a reasonably sized package. Check with the manufacturers for the latest offerings.

## PCB Layout Considerations

The following guidelines should be applied to ensure proper performance when designing a PCB for the SKY87222:

- Place the input capacitors as close to the device as possible to reduce the input ripple.
- Place the output capacitors as close to the device and inductor as possible to reduce the switching noise and output ripple.
- Use wide and short traces for high current paths.
- The feedback trace should be separated from any power trace and connected as close as possible to the load point for better load regulation.

**Table 5. Suggested Inductor Selection**

| Part Number | Value (μH) | DCR (Ω) | $I_{SAT}$ (A)<br>30% drop | $I_{RMS}$ (A)<br>40 °C rise | Package (mm) | Manufacturer |
|---|---|---|---|---|---|---|
| PST25201B-R47MS | 0.47 ± 20% | 0.025 typ.<br>0.029 max. | 3.9 typ<br>3.5 max | 3.7 typ<br>3.33 max | 2.5 × 2.0 × 1.2 | Cyntec |
| PST25201B-1R0MS | 1.0 ± 20% | 0.037 typ<br>0.043 max | 2.7 typ<br>2.45 max | 2.6 typ<br>2.34 max | 2.5 × 2.0 × 1.2 | |
| PST25201B-1R5MS | 1.5 ± 20% | 0.063 typ<br>0.072 max | 2.3 typ<br>2.07 max | 2.2 typ<br>1.98 max | 2.5 × 2.0 × 1.2 | |
| PIFE25201B-R47MS | 0.47 ± 20% | 0.023 typ<br>0.028 max | 5.0 typ<br>4.5 max | 4.5 typ<br>4.0 max | 2.5 × 2.0 × 1.2 | |
| PIFE25201B-R50MS | 0.50 ± 20% | 0.025 typ<br>0.030 max | 4.8 typ<br>4.32 max | 4.3 typ<br>3.87 max | 2.5 × 2.0 × 1.2 | |
| PIFE25201B-1R0MS | 1.0 ± 20% | 0.045 typ<br>0.055 max | 3.8 typ<br>3.3 max | 3.1 typ<br>2.7 max | 2.5 × 2.0 × 1.2 | |
| PIFE25201B-1R5MS | 1.5 ± 20% | 0.058 typ<br>0.070 max | 2.9 typ<br>2.61 max | 2.7 typ<br>1.43 max | 2.5 × 2.0 × 1.2 | |
| PIFE25201B-2R2MS | 2.2 ± 20% | 0.086 typ<br>0.105 max | 2. 5 typ<br>2.2 max | 2.3 typ<br>2.0 max | 2.5 × 2.0 × 1.2 | |
| LQM2HPNR47MJH# | 0.47 ± 20% | 0.037 typ<br>0.046 max | 3.5 typ<br>3.2 max | 3.4 typ<br>2.7 max | 2.5 × 2.0 × 1.2 | Murata |
| LQM2HPNR68MGH# | 0.68 ± 20% | 0.050 typ<br>0.063 max | 4.0 typ<br>3.8 max | 2.9 typ<br>2.3 max | 2.5 × 2.0 × 1.0 | |
| LQM2HPN1R5MGH# | 1.5 ± 20% | 0.065 typ<br>0.081 max | 1.6 typ<br>1.5 max | 2.6 typ<br>2.0 max | 2.5 × 2.0 × 1.0 | |
| VLS252012T-R47N2R1 | 0.47 ± 30% | 0.047 typ.<br>0.056 max. | 3.7 typ<br>3.3 max | 2.2 typ | 2.5 × 2.0 × 1.2 | TDK |
| VLS252012T-1R0N1R7 | 1.0 ± 30% | 0.073 typ.<br>0.088 max. | 2.7 typ<br>2.4 max | 1.8 typ | 2.5 × 2.0 × 1.2 | |
| VLS252012T-1R5N1R4 | 1.5 ± 30% | 0.105 typ.<br>0.126 max. | 2.2 typ<br>2.0 max | 1.5 typ | 2.5 × 2.0 × 1.2 | |

## Evaluation Board Description

The SKY87222 Evaluation Board is used to test the performance of the SKY87222 step-down DC-DC converter. An Evaluation Board schematic diagram is provided in Figure 48. Layer details for the SKY87222 Evaluation Board are shown in Figure 49. The Evaluation Board has additional components for easy evaluation; the actual bill of materials required for the system is shown in Table 6.

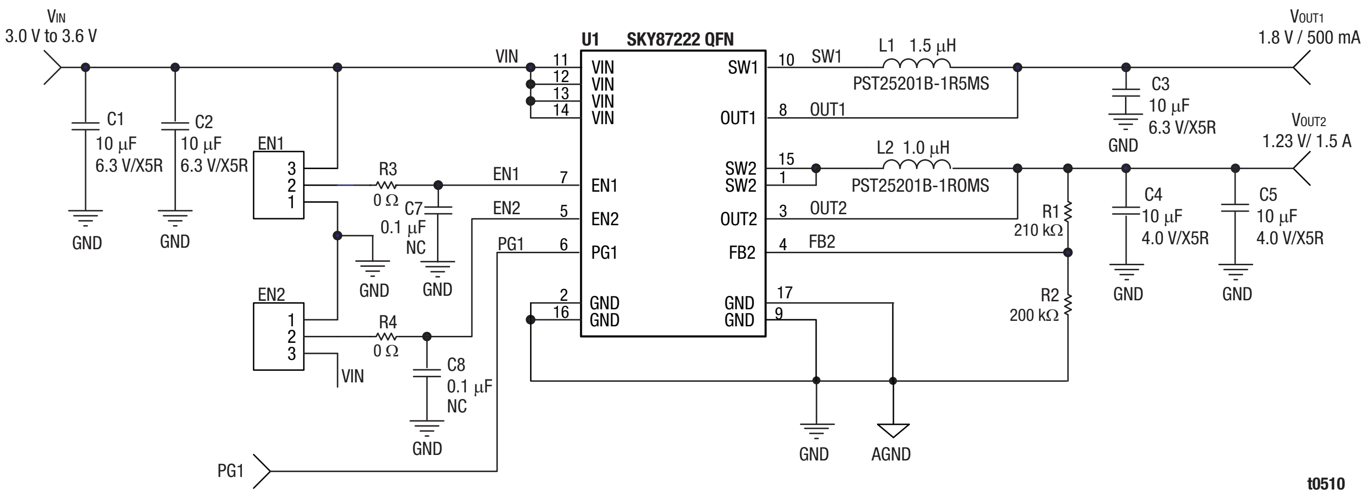



**Figure 48. SKY87222 Evaluation Board Schematic**

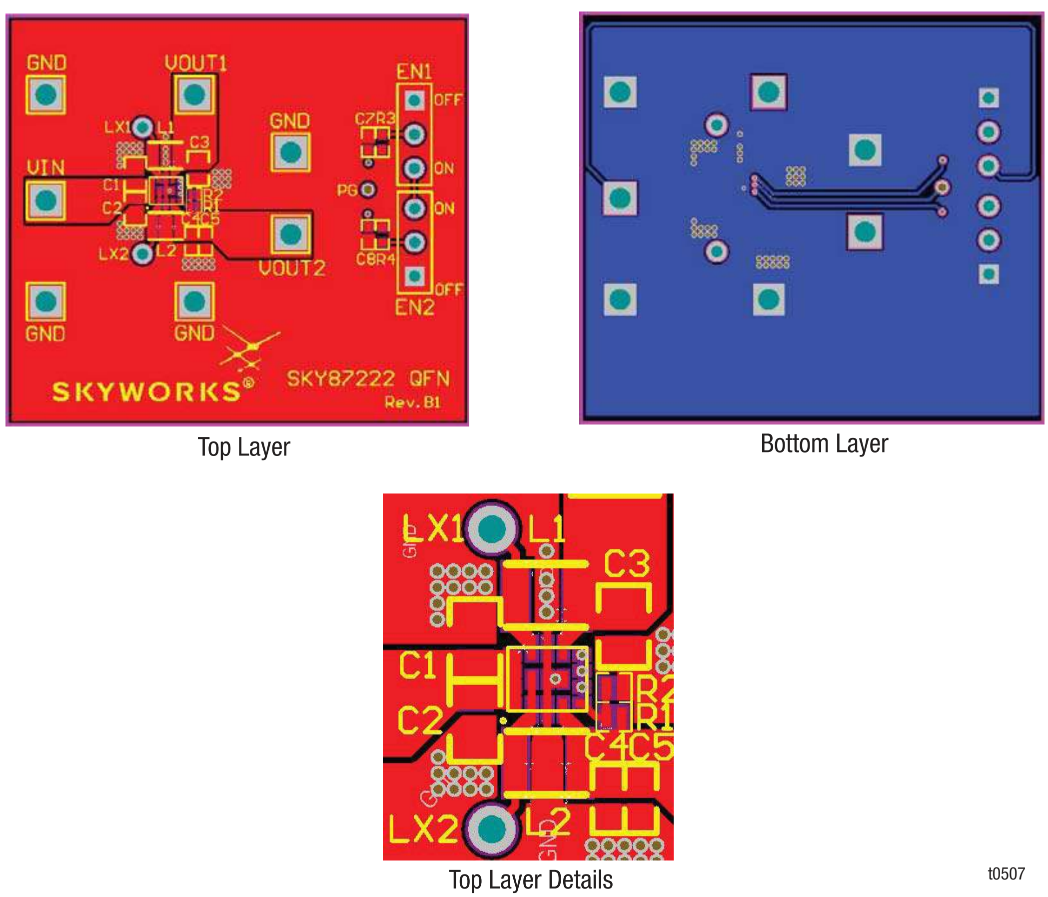



**Figure 49. SKY87222 Evaluation Board Layer Details**

**Table 6. SKY87222 Evaluation Board Bill of Materials**

| Component | Part Number | Description | Manufacturer |
|---|---|---|---|
| C1, C2, C3 | GRM188R60J106ME84# | Ceramic capacitors, 10 μF, 0603, X5R, 6.3 V, 20% | Murata |
| C4, C5 | GRM155R60G106ME44# | Ceramic capacitors, 10 μF, 0402, X5R, 4.0 V, 20% | Murata |
| L1 | PST25201B-1R5MS | Inductor, 1.5 μH, 72 mΩ, 1.98 A, 20% | Cyntec |
| L2 | PST25201B-1R0MS | Inductor, 1.0 μH, 43 mΩ, 2.34 A, 20% | Cyntec |
| R1 | CRCW0201210KFNED | Resistor, 210 kΩ, 0201, 1/20 W, 1% | Vishay |
| R2 | CRCW0201200KFNED | Resistor, 200 kΩ, 0201, 1/20 W, 1% | Vishay |
| R3, R4 | CRCW04020000Z0ED | Resistor, 0 Ω, 0402, 1/16 W, 1% | Vishay |

## Package Information

Typical case markings are shown in Figure 50. Package dimensions for the 17-pin QFN package are shown in Figure 51. Tape and reel dimensions are shown in Figure 52.

## Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY87222 is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, and document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

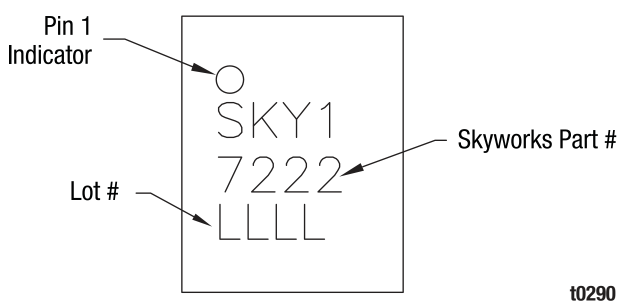
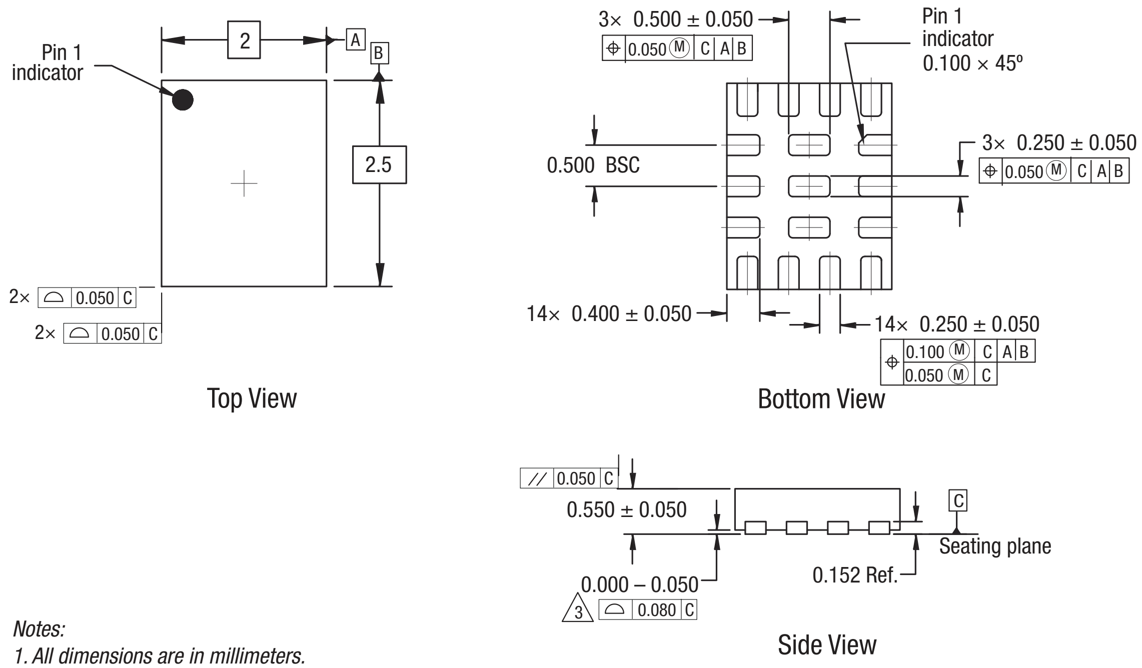
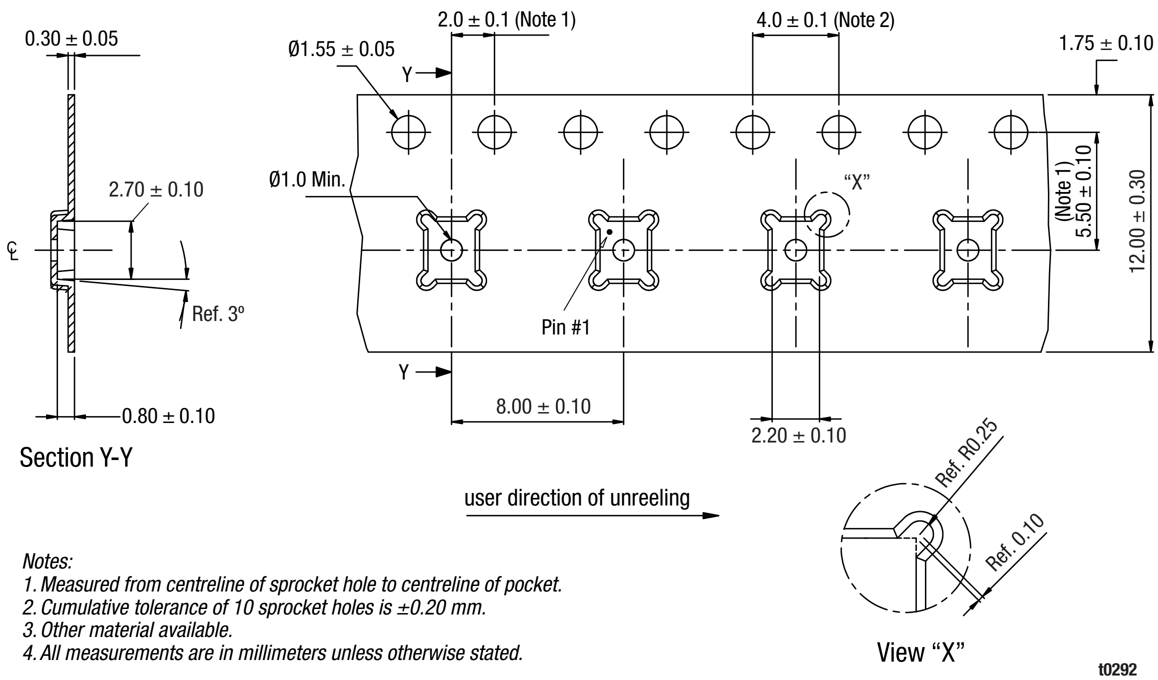



**Figure 50. Typical Case Markings (Top View)**




*Notes:*
*1. All dimensions are in millimeters.*
*2. Plating requirement per source control drawing (SCD) 2504.*
*3. Coplanarity applies to the terminals and all other bottom surface metallization.*

**Figure 51. SKY87222 17-Pin QFN Package Dimensions**




*Notes:*
*1. Measured from centreline of sprocket hole to centreline of pocket.*
*2. Cumulative tolerance of 10 sprocket holes is ±0.20 mm.*
*3. Other material available.*
*4. All measurements are in millimeters unless otherwise stated.*

**Figure 52. SKY87222 Tape and Reel Dimensions**

## Ordering Information

| Model Name | Manufacturing Part Number | Evaluation Board Part Number |
|---|---|---|
| SKY87222: Dual Step-Down Converter | SKY87222-11-653LF | SKY87222-11-653LF-EVB |