ANALOG DEVICES

EVAL-AD7606BFMCZ User Guide

UG-1225

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Evaluating the AD7606B 8-Channel DAS with 16-Bit, 800 kSPS Bipolar Input, Simultaneous Sampling ADC

FEATURES

Full featured evaluation board for the AD7606B
On-board power supplies
Standalone capability
SDP-H1 compatible (EVAL-SDP-CH1Z (SDP-H1))
PC software for control and data analysis (download from the AD7606B product page)
Time and frequency domain

EVALUATION KIT CONTENTS

EVAL-AD7606BFMCZ evaluation board

ADDITIONAL EQUIPMENT NEEDED

System demonstration platform (SDP)—high speed controller board (EVAL-SDP-CH1Z (SDP-H1))
PC running Windows Vista SP2 (32-bit or 64-bit), Windows 7 SP1 (32-bit or 64-bit), Windows 8.1 (32-bit or 64-bit), or Windows 10 (32-bit or 64-bit) with a USB 2.0 port
DC/ac signal source
SMB and USB cables
External supply (optional)

DOCUMENTS NEEDED

AD7606B data sheet
EVAL-AD7606BFMCZ user guide
Schematics
Layout files
Bill of materials

ONLINE RESOURCES

ACE evaluation software
AD7606B ACE plug-in

EVALUATION BOARD DESCRIPTION

The EVAL-AD7606BFMCZ is a full featured evaluation board that allows users to easily evaluate the features of the AD7606B analog-to-digital converter (ADC). The EVAL-AD7606BFMCZ can be controlled by the system demonstration platform controller board (EVAL-SDP-CH1Z (SDP-H1)). The EVAL-SDP-CH1Z (SDP-H1) allows the EVAL-AD7606BFMCZ to be controlled through the USB port of a PC using the AD7606B evaluation software. The software is available for download from the AD7606B product page.

On-board components include an ADP7118 5 V, low noise low dropout regulator (LDO) and an ADR4525 high precision, band gap voltage reference.

Full data on the AD7606B is available in the AD7606B data sheet, which must be consulted in conjunction with this user guide. Full details on the EVAL-SDP-CH1Z are available on the SDP-H1 product page.

EVALUATION BOARD PHOTOGRAPH

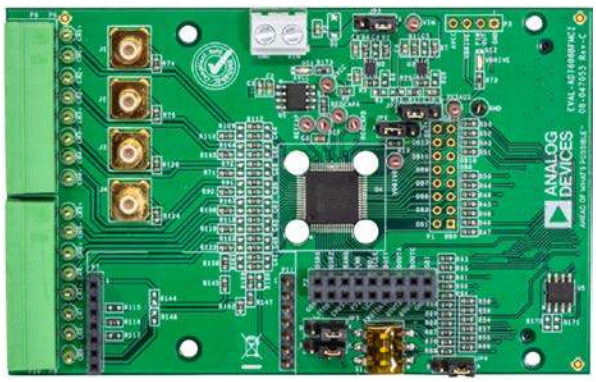

Figure 1.

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REVISION HISTORY

6/2020—Rev. 0 to Rev. A

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5/2019—Revision 0: Initial Version

QUICK START GUIDE

To quickly evaluate the AD7606B ADC, take the following steps:

1. Download and install the Analysis Control Evaluation (ACE) software from the AD7606B product pages. Ensure that the EVAL-SDP-CH1Z (SDP-H1) is disconnected from the USB port of the PC while installing the software. Restart the PC after the installation process completes. For complete software installation instructions, see the Software Installation section.
2. Ensure that the various link options are configured as outlined in Table 2.
3. Connect the EVAL-SDP-CH1Z (SDP-H1) board to the EVAL-AD7606BFMCZ. Ensure that these boards are connected firmly together.
4. By default, the power for the EVAL-AD7606BFMCZ is supplied by the EVAL-SDP-CH1Z (SDP-H1) controller board. A number of power options are available, see the Power Supplies section for more information.
5. Connect the EVAL-SDP-CH1Z (SDP-H1) to the 12 V supply and to the PC via the USB cable. Choose to automatically search for the drivers for the EVAL-SDP-CH1Z (SDP-H1) if prompted by the operating system.
6. Launch the ACE evaluation software from the **Analog Devices** subfolder in the **Programs** menu.
7. Connect an input signal via the CH1 to CH8 terminal blocks.

EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The AD7606B is a 16-bit, 8-channel, simultaneous sampling successive approximation ADC. The device operates from a single 4.75 V to 5.25 V power supply and features throughput rates of up to 800 kSPS. The device has 5 MΩ input impedance for direct connection from the user sensor outputs to the ADC.

HARDWARE LINK OPTIONS

Table 2 details the link option functions and the default power link options. The EVAL-AD7606BFMCZ can be powered by different sources, as described in the Power Supplies section. By default, the power supply required for the EVAL-AD7606BFMCZ comes from the EVAL-SDP-CH1Z (SDP-H1) controller board. The power supply is regulated by the on-board ADP7118 low dropout (LDO) regulators, which generates the 5 V supply.

CONNECTORS AND SOCKETS

The connectors and sockets on the EVAL-AD7606BFMCZ are outlined in Table 1.

Table 1. On-Board Connectors

Connector	Function
P12	FPGA mezzanine card (FMC) connector
P4	External power terminal block, 7 V to 9 V dc input
P6, P8	8-pin connectors for input to Channel 1 through Channel 4
P9, P10	8-pin connectors for input to Channel 5 through Channel 8
J1 to J4	Analog input Subminiature Version B (SMB) connectors to Channel 1 through Channel 4
P7, P11	Channel 8 surfboard evaluation headers
P1, P2	General connectors for debugging purposes or to connect an external controller

The default interface to the EVAL-AD7606BFMCZ is via the FMC connector, which connects the EVAL-AD7606BFMCZ to the EVAL-SDP-CH1Z (SDP-H1).

POWER SUPPLIES

Before applying power and signals to the EVAL-AD7606BFMCZ, ensure that all link positions are set according to the required operating mode. See Table 2 for the complete list of link options.

The supply required for the EVAL-AD7606BFMCZ comes from the EVAL-SDP-CH1Z (SDP-H1) controller board. Alternatively, the EVAL-AD7606BFMCZ can also be supplied with a dc power supply connected to the P4 terminal block. Select the external power supply or the EVAL-SDP-CH1Z (SDP-H1) supply through JP2. The power supply is then connected to the on-board ADP7118 5 V linear regulator that supplies the correct bias to each of the various sections on the EVAL-AD7606BFMCZ.

CHANNEL INPUT

The J1 to J4 connectors allow users to connect external signals to the ADC channel inputs through the SMB inputs. The EVAL-AD7606BFMCZ is supplied with the AD7606B mounted (U4, see Figure 1). The AD7606B is an 8-channel data acquisition system (DAS) with a simultaneous sampling ADC. External signals can be applied to the P8 to P10 terminal blocks on the EVAL-AD7606BFMCZ.

Table 2. Link Options

Link	Default Position	Function
JP2	A	This link selects the power supply source for the evaluation board. In Position A, the unregulated supply to the on-board LDOs is taken from the EVAL-SDP-CH1Z (SDP-H1) 12 V supply. In Position B, the unregulated external supply to the on-board LDOs is taken from the P4 terminal block connector.
JP1	A	The EVAL-AD7606BFMCZ evaluation software controls the STBY pin. When using the EVAL-AD7606BFMCZ board in standalone mode without running the EVAL-AD7606BFMCZ evaluation software, this jumper allows selection of standby mode. In this case, change the R8 and R10 resistors to 0 Ω links. In Position A, the STBY pin is tied to V_{DRIVE}. In Position B, the STBY pin is tied to AGND.

Link	Default Position	Function
JP3	A	Use to select the V_{DRIVE} source for the AD7606B. In Position A, the AD7606B is supplied with 3.3 V V_{DRIVE} from the ADP7118. In Position B, the AD7606B is supplied with 3.3 V from the EVAL-SDP-CH1Z (SDP-H1).
JP4	A	The EVAL-AD7606BFMCZ evaluation software controls the RANGE pin. If using the EVAL-AD7606BFMCZ board in standalone mode, this jumper allows selection of the analog input range in hardware mode. In this case, change the R20 resistor to a 0 Ω link. In Position A, the RANGE pin is tied to V_{DRIVE}, and the ±10 V range is selected. In Position B, the RANGE pin is tied to AGND, and the ±5 V range is selected. In software mode, this pin is ignored.
JP5	A	The EVAL-AD7606BFMCZ evaluation software controls the PAR/SER SEL pin. If using the EVAL-AD7606BFMCZ board in standalone mode, this jumper allows digital interface selection. In this case, change the R19 and R21 resistors to 0 Ω links In Position A, the PAR/SER SEL pin is tied to V_{DRIVE}, and the serial interface is selected. In Position B, the PAR/SER SEL pin is tied to AGND, and the parallel interface is selected.
JP6	A	The EVAL-AD7606BFMCZ evaluation software controls the REF SELECT pin. By default, the internal reference is selected. If switching to the external reference is required through the EVAL-AD7606BFMCZ evaluation software, R1 must be populated. If using the EVAL-AD7606BFMCZ board in standalone mode, this jumper allows reference selection. In this case, change the R13 resistor to a 0 Ω link. In Position A, the REF SELECT pin is tied to AGND, the internal reference is disabled, and the external reference is selected. R1 must be populated. In Position B, the REF SELECT pin is tied to V_{DRIVE}, and the internal reference is enabled and selected. R1 must be unpopulated.
S1	Open	The EVAL-AD7606BFMCZ evaluation software controls the REF SELECT pin. If using the EVAL-AD7606BFMCZ in standalone mode, these switches can select the logic level on the OSx pins.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

Download the ACE evaluation software from the AD7606B product page. Both the EVAL-AD7606BFMCZ software and the EVAL-SDP-CH1Z (SDP-H1) board drivers must be installed.

Warning

The ACE evaluation software and drivers must be installed before connecting the EVAL-AD7606BFMCZ evaluation board and the EVAL-SDP-CH1Z (SDP-H1) board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Installing the ACE Evaluation Software

To install the ACE evaluation software, take the following steps:

1. Download the ACE evaluation software to a Windows®-based PC.
2. Double click the **ACEInstall.exe** file to begin the installation. By default, the software is saved to: **C:\Program Files (x86)> Analog Devices** > **ACE**.
3. A dialog box appears asking for permission to allow the program to make changes to the PC. Click **Yes** to begin the installation process.
4. Click **Next >** to continue the installation, as shown in Figure 2.

Figure 2. Evaluation Software Install Confirmation

5. Read the license and click **I Agree.**

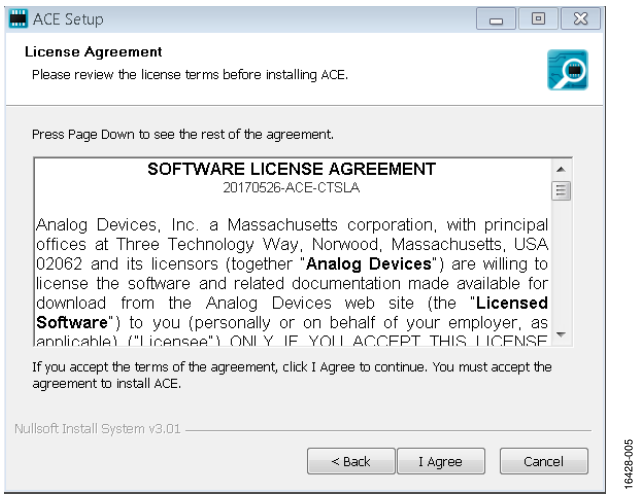

*Figure 3. **License Agreement***

6. Choose the install location and click **Next >**.

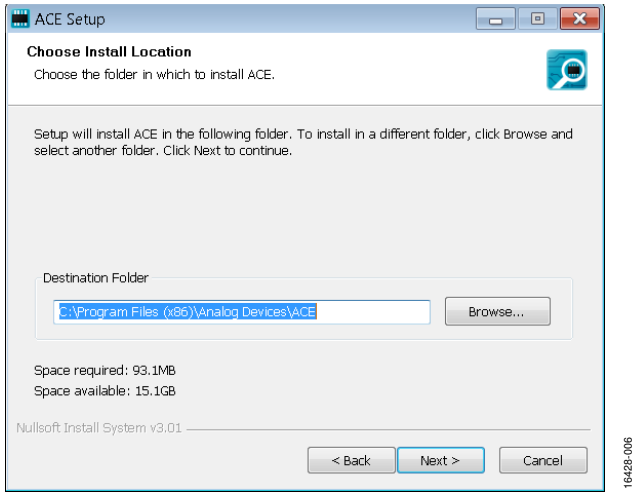

*Figure 4. **Choose Install Location** Window*

7. The components to install are preselected. Click **Install.**

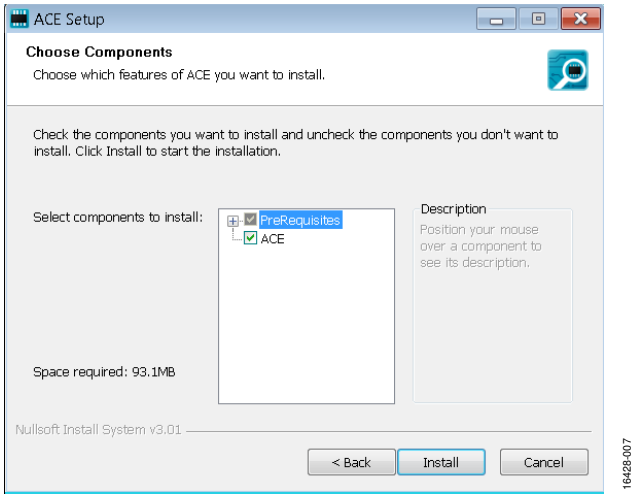

Figure 5. Choose Components

8. The **Windows Security** window appears. Click **Install**.

*Figure 6. **Windows Security** Window*

9. The installation is in progress. No action is required.

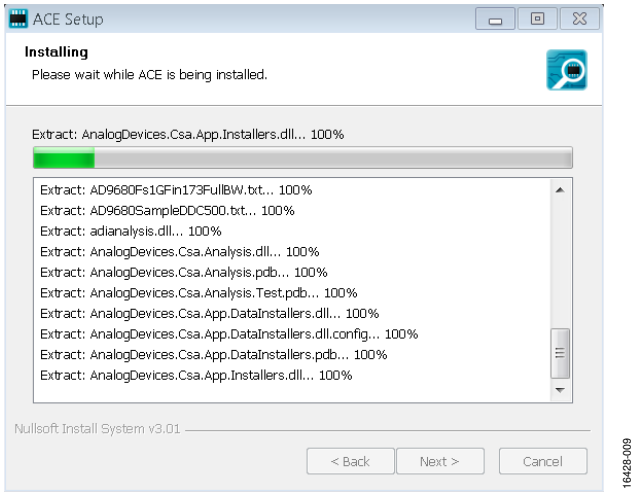

Figure 7. Installation in Progress

10. When the installation is complete, click **Next** >, and then click **Finish** to complete.

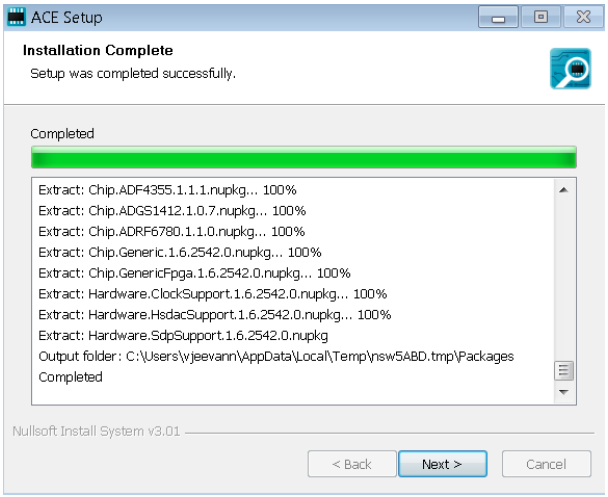

Figure 8. Installation Complete

When first plugging in the EVAL-SDP-CH1Z (SDP-H1) via the USB cable provided, allow the **Found Hardware Wizard** to run. After the drivers are installed, ensure that the EVAL-SDP-CH1Z (SDP-H1) is connected correctly by looking at the **Device Manager** of the PC. The **Device Manager** can be found by right clicking **My Computer** > **Manage** > **Device Manager** from the list of **System Tools**.

The **Analog Devices SDP-H1** (EVAL-SDP-CH1Z (SDP-H1)) appears under **ADI Development Tools**, as shown in Figure 9.

*Figure 9. **Device Manager** Window*

Disconnecting the EVAL-AD7380FMCZ or EVAL-AD7381FMCZ

Always disconnect power from the EVAL-SDP-CH1Z or press the reset tact switch located alongside the mini USB port before removing the EVAL-AD7606BFMCZ evaluation board.

AD7606B EVALUATION SOFTWARE OPERATION

Launching the Software

After the EVAL-AD7606BFMCZ and EVAL-SDP-CH1Z boards are correctly connected to the PC, launch the ACE evaluation software.

1. From the **Start** menu, select **All Programs > Analog Devices > ACE> ACE.exe**, which brings up the window shown in Figure 10.
2. If the EVAL-AD7606BFMCZ evaluation board is not connected to the USB port via the EVAL-SDP-CH1Z when the software is launched, the **AD7606B Eval Board** icon does not show up in the **Attached Hardware** section. Connect the EVAL-AD7606BFMCZ and the EVAL-SDP-CH1Z to the USB port of the PC and wait a few seconds, and then follow the instructions that appear in the dialogue box.
3. Double-click the **AD7606B Eval Board** icon to view the window shown in Figure 10.
4. Double-click the **AD7606B** chip icon to access the window shown in Figure 11.
5. Click **Software Defaults** and then click **Apply Changes.**

DESCRIPTION OF CHIP VIEW

After completing the steps in the Software Installation section, set up the system for data capture.

Block icons that are dark blue are programmable blocks. Clicking a dark blue block icon opens a configurable pop-up window that allows customization for the data capture, as shown for the Channel 1 input range (see Figure 13).

The available programmable blocks in chip view are as follows:

- Analog input range on a per channel basis through the icon located on each PGA block
- Gain, offset, and phase calibration setting on a per channel basis.
- Diagnostic multiplexer.
- Oversampling ratio lines. By setting all the lines high, the AD7606B enters software mode, and the oversampling ratio is set through the memory map. In hardware mode, these lines select the oversampling ratio.
- Data interface, either serial or parallel.
- Reference selection, either internal or external, through the REF SELECT switch.

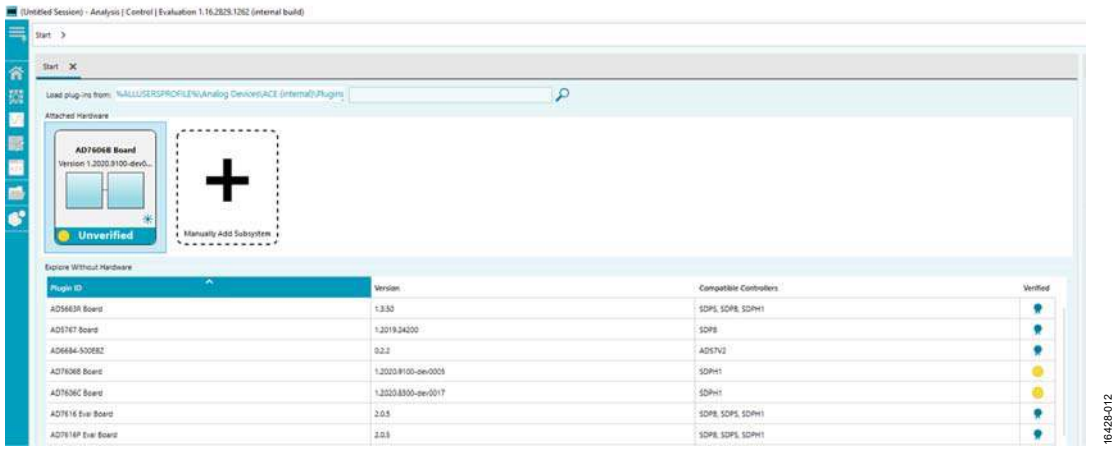

Figure 10. ACE Software Main Window

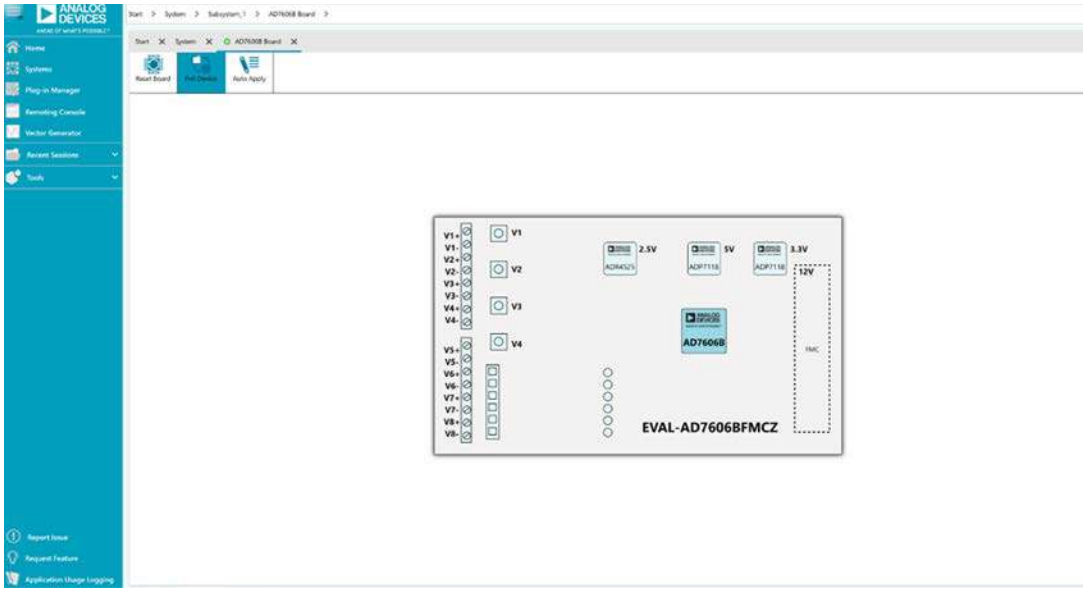

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Figure 11. Board View

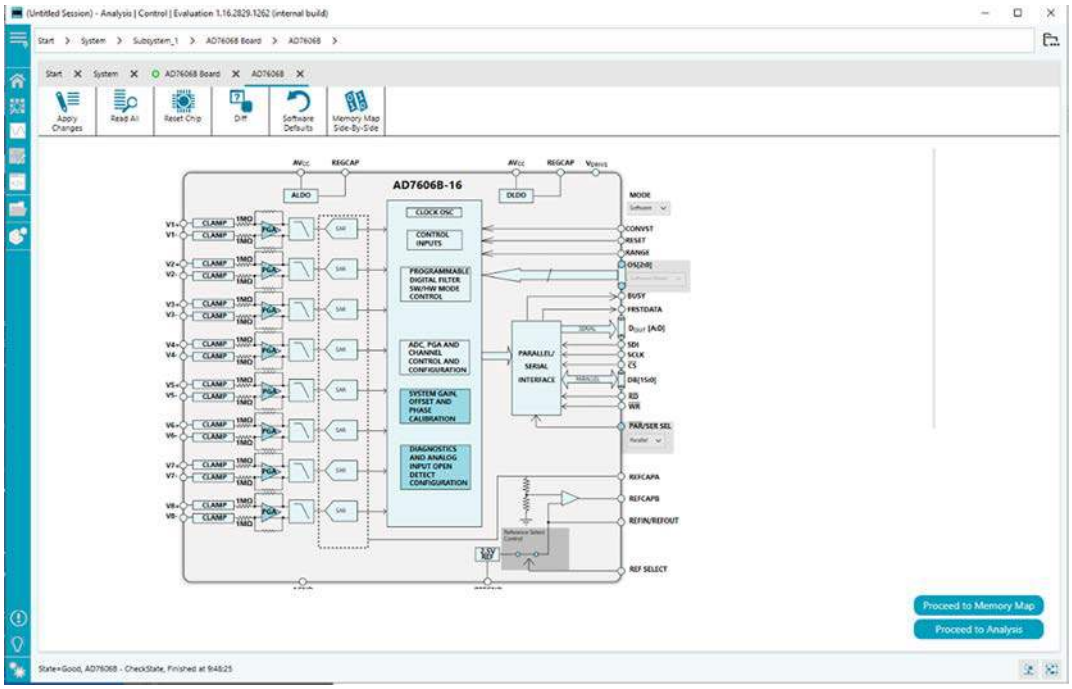

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Figure 12. Chip View

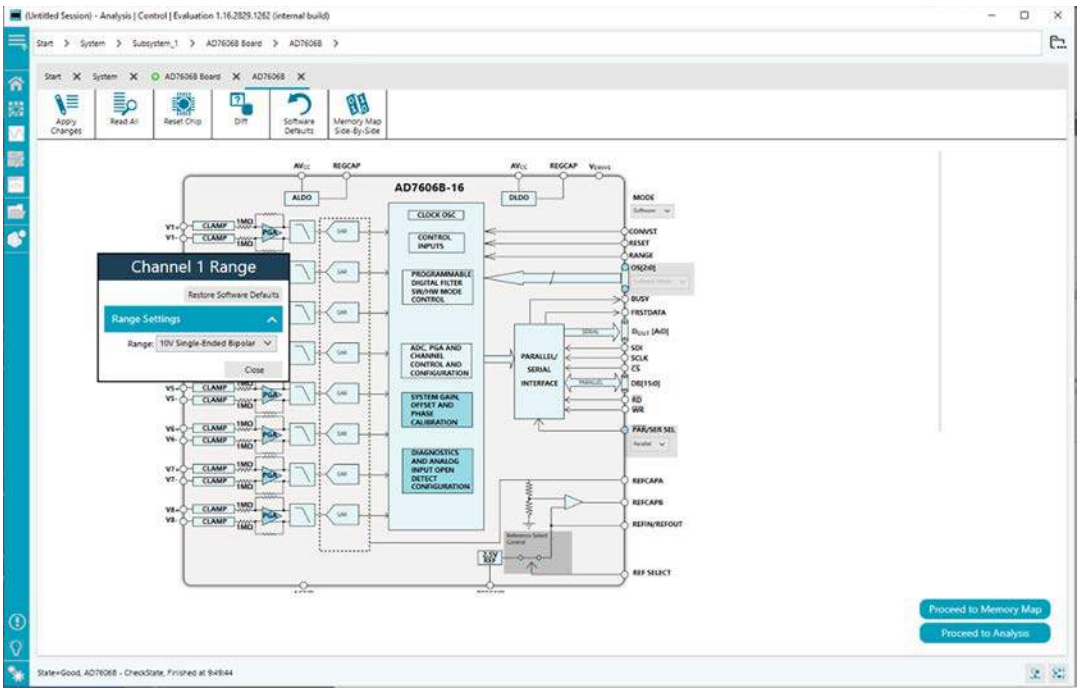

Figure 13. Pop-Up Configurable Window

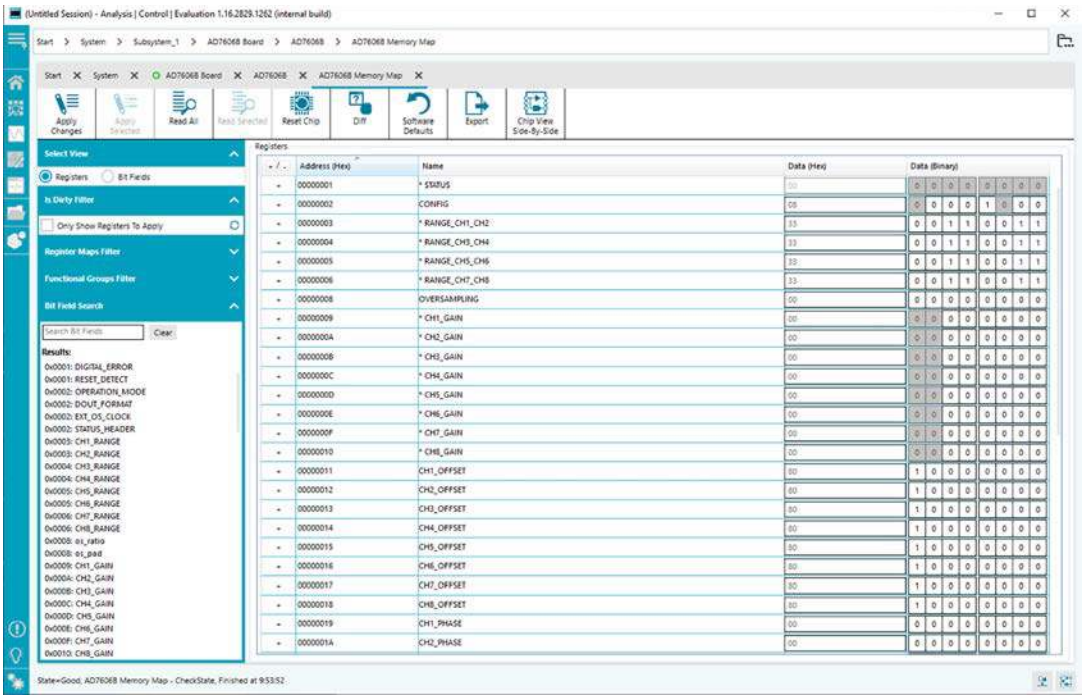

Figure 14. Memory Map View

DESCRIPTION OF MEMORY MAP WINDOW

Click **Proceed to Memory Map** in the chip view to open the window shown in Figure 14. The memory map shows all registers of the AD7606B.

Apply Changes

The registers are in default values when powered up. To implement the values changed in all of the registers, click **Apply Changes** to write to the registers.

Apply Selected

In some cases, the values of all registers are changed, but the user wants to implement changes on a selected register only. Click **Apply Selected** to write the new value on the selected register to the AD7606B.

Read All

Clicking **Read All** results in a read of the values of all the registers from the chip.

Read Selected

Clicking **Read Selected** results in a read of the selected register from the chip.

Reset Chip

Clicking **Reset Chip** causes the software to reset the AD7606B.

Diff

Clicking **Diff** checks for difference in register values between software and chip.

Software Defaults

To revert the register values back to their defaults, click **Software Default**, and then click **Apply Changes** to write to the AD7606B.

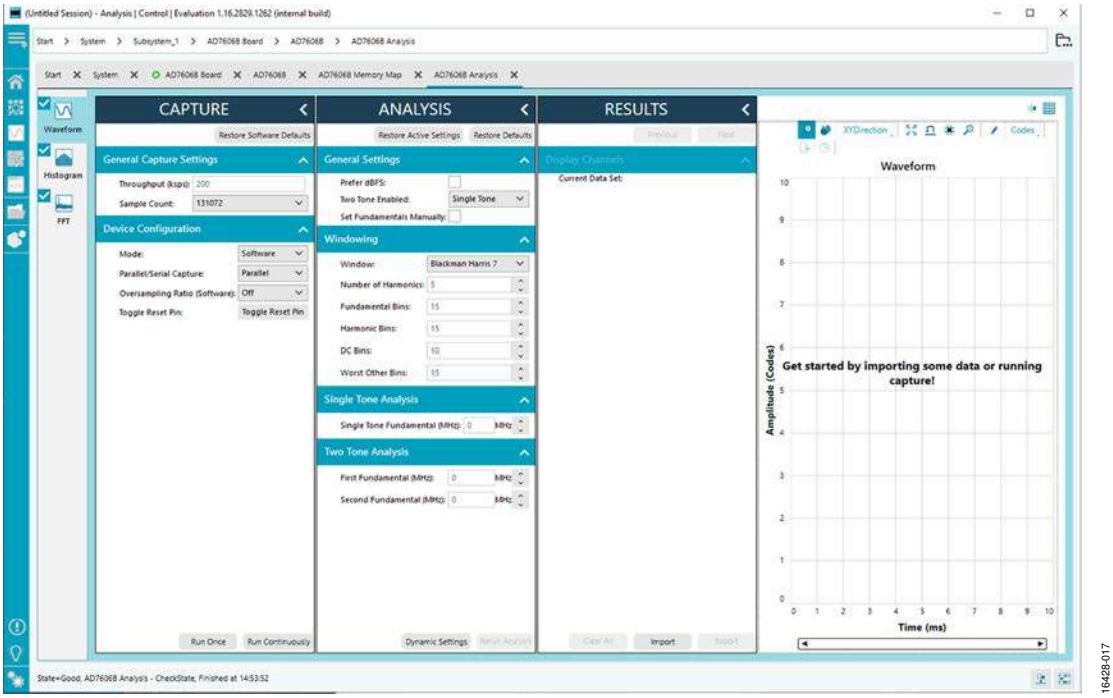

Figure 15. Analysis View

DESCRIPTION OF ANALYSIS WINDOW

Click **Proceed to Analysis** in the chip view to open the window, as shown in Figure 15. The analysis view contains the **Waveform** tab, **Histogram** tab, and **FFT** tab.

WAVEFORM TAB

The **Waveform** tab displays data in form of time vs. discrete data values with the results, as shown in Figure 16. The **Capture** pane contains capture settings, which reflect into the registers automatically before data capture.

Capture

General Capture Settings

The **Sample Count** list allows the user to select the number of samples per channel per capture.

The user can enter the input sample frequency in kSPS in the **Throughput(kSPS)** box. Refer to the AD7606B data sheet to determine the maximum sampling frequency for the selected mode.

Device Configuration

The **Mode** list can be set between hardware mode, meaning that the device is configured through digital input pins, or software mode, which allows reading and writing the memory map and enables a wider range of features. Refer to the AD7606B data sheet to determine the benefits of each mode.

The **Parallel/Serial Capture** list allows the user to select the data interface between parallel or serial.

The **Oversampling Ratio** list can be set between 2 and 64 (in hardware mode) or 256 (in software mode) and provides improved signal-to-noise ratio (SNR) performance. Refer to the AD7606B data sheet to determine the maximum oversampling ratio for the selected oversampling mode.

The **Input Range**, when hardware mode is enabled, allows selection between ±10 V and ±5 V. In software mode, the input span is selected either in the memory map or the pop-up menu in chip view (see Figure 13).

The **Toggle Reset Pin** button allows the user to issue a full reset to the AD7606B. Refer to the AD7606B data sheet for information on the different types of reset available on the device.

Run Once

Click **Run Once** to start a data capture of the samples at the sample rate specified in the **Throughput(KSPS)** box for the number of samples stated in **Sample Count** list. These samples are stored on the FPGA device and are only transferred to the PC when the sample frame is complete.

Run Continuously

Click **Run Continuously** to start a data capture that gathers samples continuously with one batch of data at a time. The **Run Once** operation is run continuously.

Results

Display Channels

Display Channels allows the user to select the channels to capture. The channel data is shown only if that channel is selected before the capture.

Waveform Results

Waveform Results displays amplitude, sample frequency, and noise analysis data for the selected channels.

Export Capture Data

Click **Export** to export captured data. The waveform, histogram, and FFT data is stored in .xml files along with the values of parameters at capture.

Waveform Graph

The data waveform graph shows each successive sample of the ADC output. The user can zoom and pan the waveform using the embedded waveform tools. The channels to display can be selected in **Display Channels.**

Display Units and Axis Controls

Click the **Display Units** dropdown list to select whether the data graph displays in units of hexadecimal, volts, or codes. The axis controls are dynamic.

When selecting either y-scale dynamic or x-scale dynamic, the corresponding axis width automatically adjusts to show the entire range of the ADC results after each batch of samples.

HISTOGRAM TAB

The **Histogram** tab contains the histogram graph and the results pane, as shown in Figure 17.

Results

Results displays the information related to the dc performance.

Histogram Graph

The histogram graph displays the number of hits per code within the sampled data. This graph is useful for dc analysis and indicates the noise performance of the device.

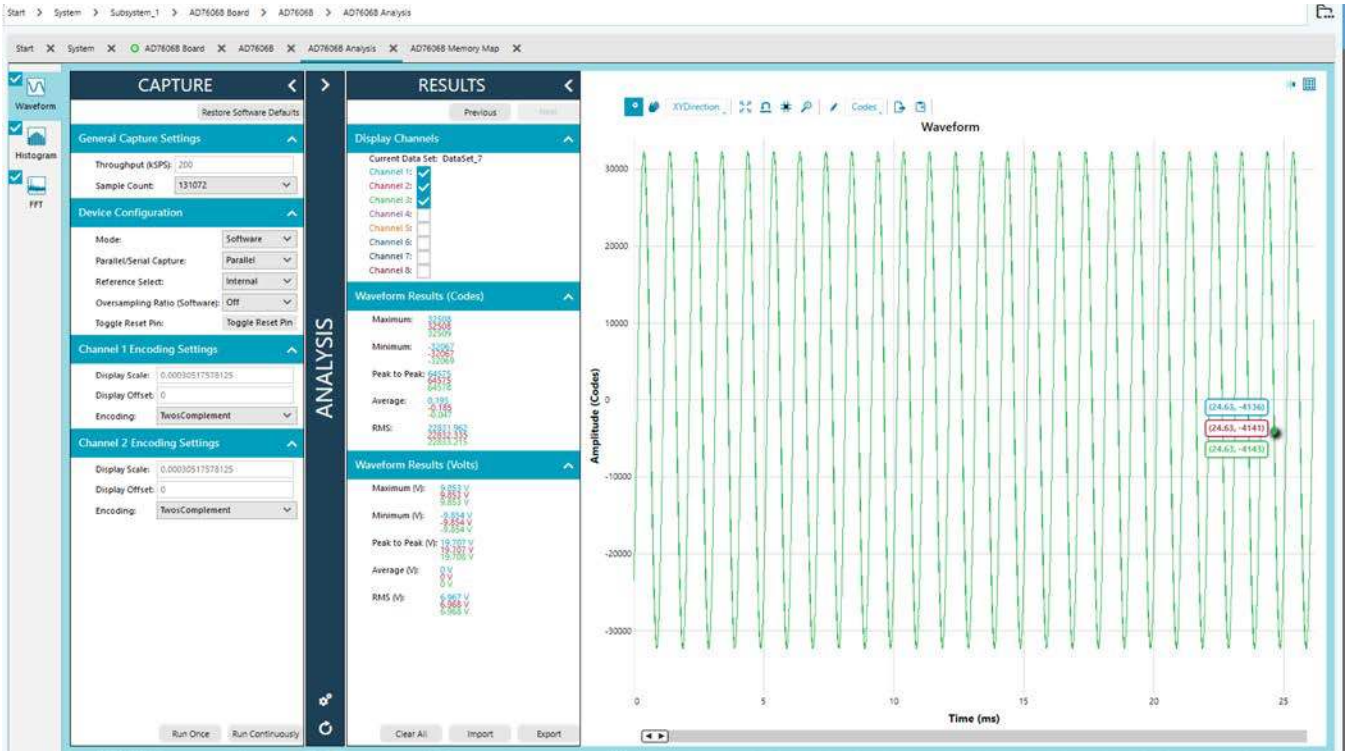

*Figure 16. **Waveform** Tab*

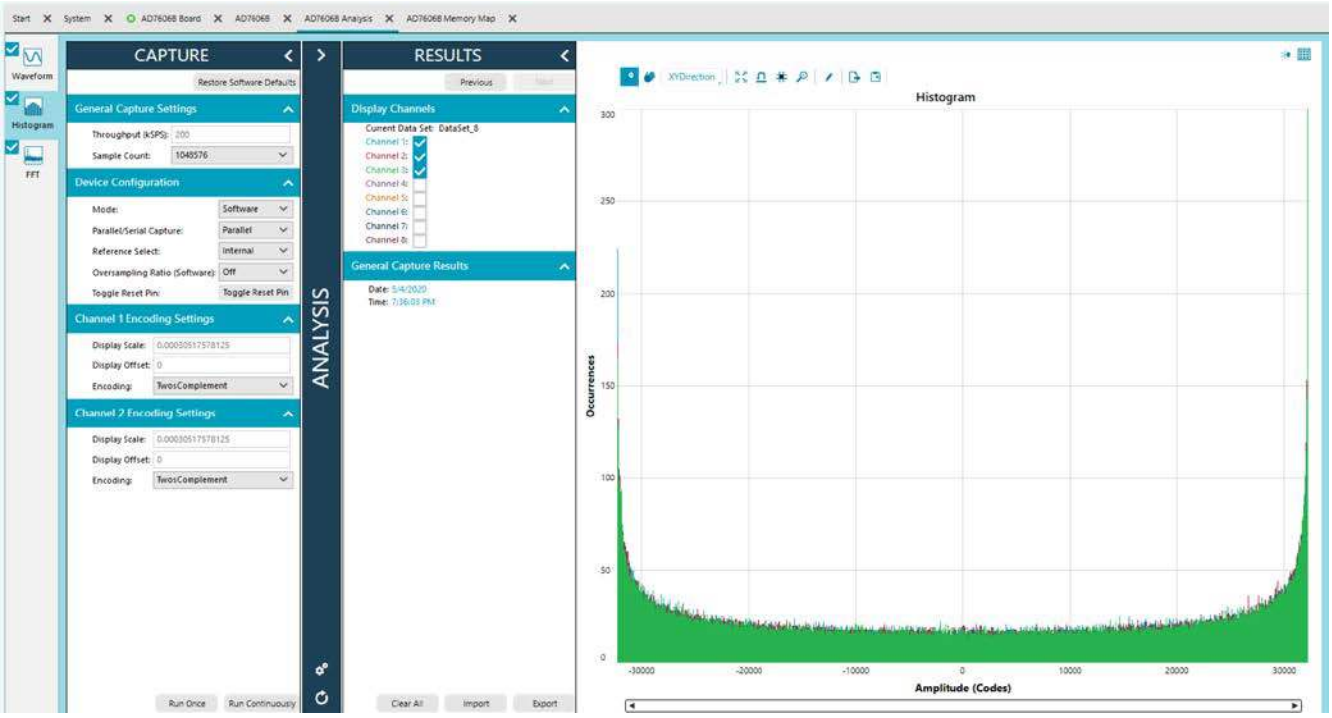

*Figure 17. **Histogram** Tab*

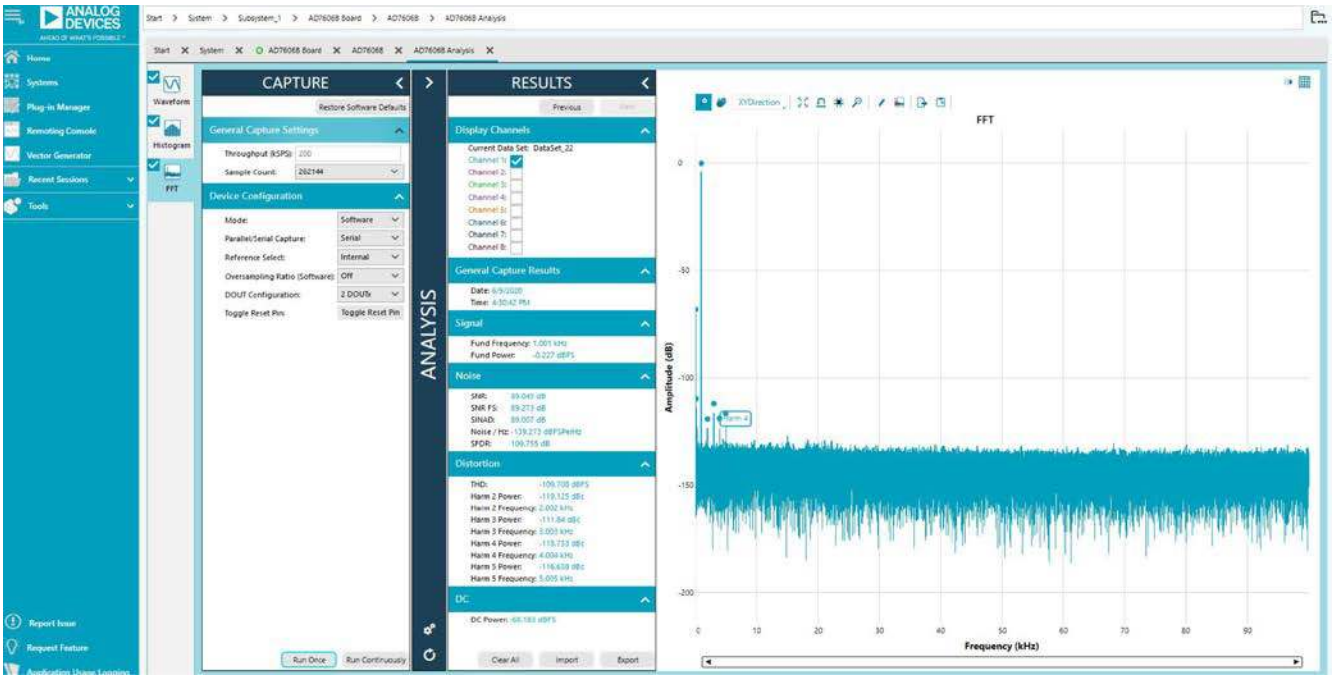

*Figure 18. **FFT** Tab*

FFT TAB

Figure 18 shows the **FFT** tab, which displays fast Fourier transform (FFT) information for the last batch of samples gathered.

Analysis

General Settings

The **General Settings** pane allows the user to set up the preferred configuration of the FFT analysis, including how many tones are analyzed. The fundamental is set manually.

Windowing

The **Windowing** pane allows the user to select the windowing type used in the FFT analysis, the number of harmonic bins, and the number of fundamental bins that must be included.

Single Tone Analysis and Two Tone Analysis

The **Single Tone Analysis** and **Two Tone Analysis** panes allow the user to select the fundamental frequency included in the FFT analysis. Use **Two Tone Analysis** when there are two frequencies that must be analyzed.

Results

Signal

The **Signal** pane displays the sample frequency, fundamental frequency, and fundamental power.

Noise

The **Noise** pane displays the SNR and other noise performance results.

Distortion

The **Distortion** pane displays the harmonic content of the sampled signal and dc power when viewing the FFT analysis.

EXITING THE SOFTWARE

To exit the software, click **File** and then click **Exit**.