PWM Controller for Half-Bridge Converters

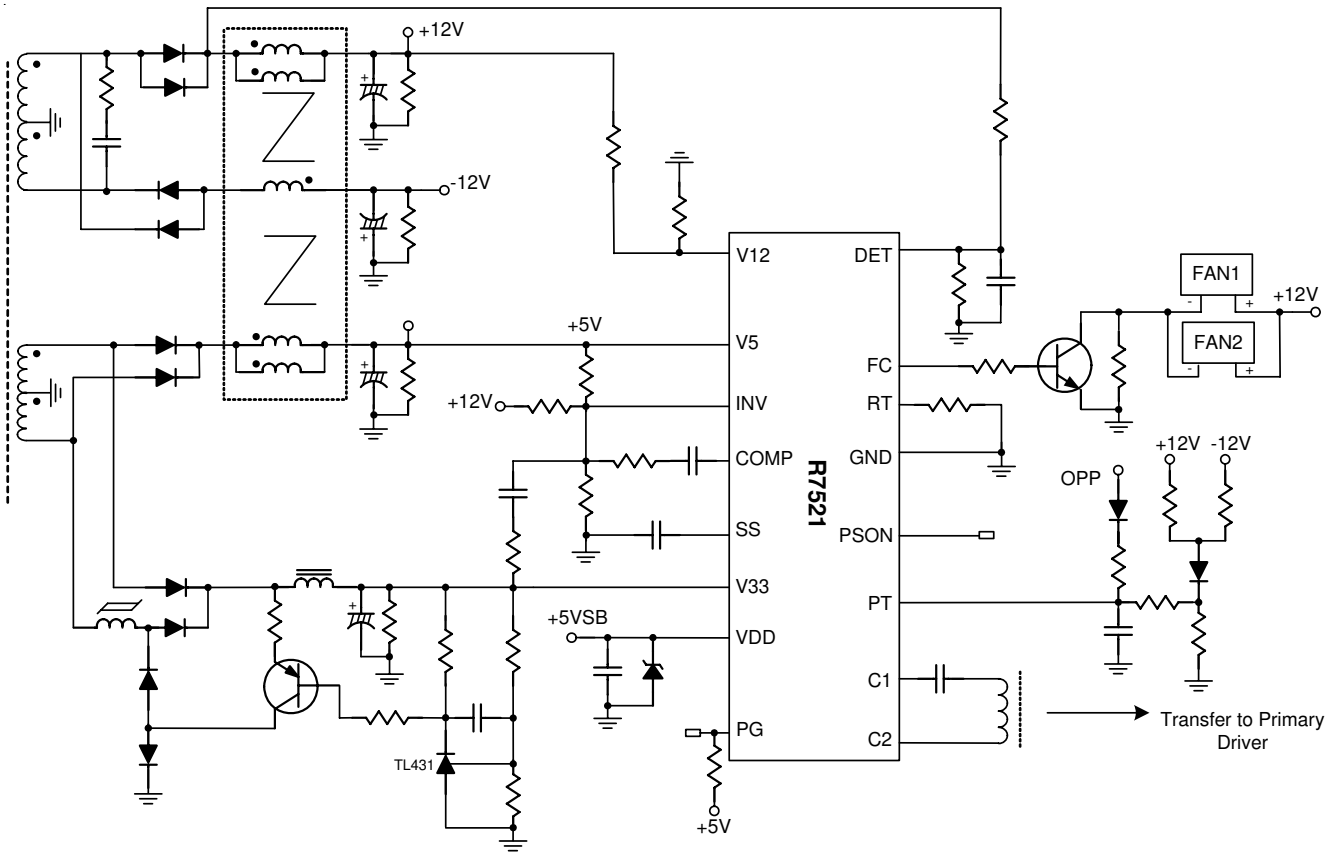
General Description

The R7521 is a with PWM controller with supervisor function inside. The controller can be applied on half-bridge converter or push-pull converter, which needs two interleaved gate drivers with 180 degree phase shift. Four multiple outputs can be monitored by R7521 and there is a "Power Good" signal to acknowledge the following system. The controller also has remote control pin and fully protection of each output, such as output over voltage, under voltage and over power protection. The DET pin is applied to detect AC line condition. R7521 incorporates over power protection. R7521 also contains FC pin to control Fan's speed by PT voltage variation. The integrated control circuit of R7521 provides complete functions and saves the Fan control external circuit of ATX power.

Features

- **Two PWM Driver Outputs for Push-Pull and Half-Bridge Converters**
- **Built-In Supervisor Saves Cost and Components**
- **Voltage Mode PWM Controller**
- **Output Over Voltage and Under Voltage Protections of Each Output**
- **Remote ON/OFF**
- **Power Good Indicator with Adaptive Time Sequence**
- **Input Under Voltage Detector and Warning**
- **Over Power Protection**
- **Adjustable Soft-Start**
- **For ATX Power Application**
- **Fun Speed Control**

Simplified Application Circuit



Ordering Information

R7521 □□

Package Type
N: DIP-16
S: SOP-16

Lead Plating System
G : Green (Halogen Free and Pb Free)

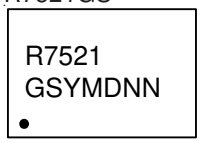
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

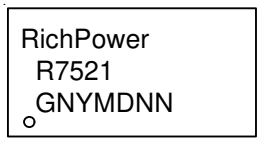
Marking Information

R7521GS



R7521GS : Product Number
YMDNN : Date Code

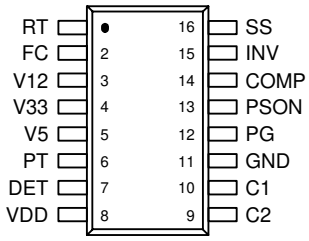
R7521GN



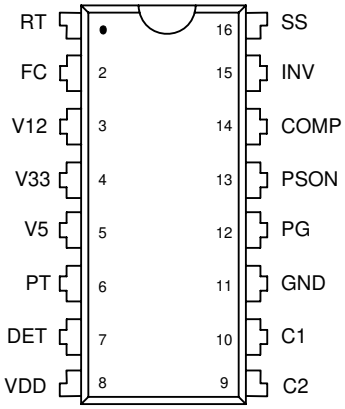
R7521GN : Product Number
YMDNN : Date Code

Pin Configurations

(TOP VIEW)



SOP-16

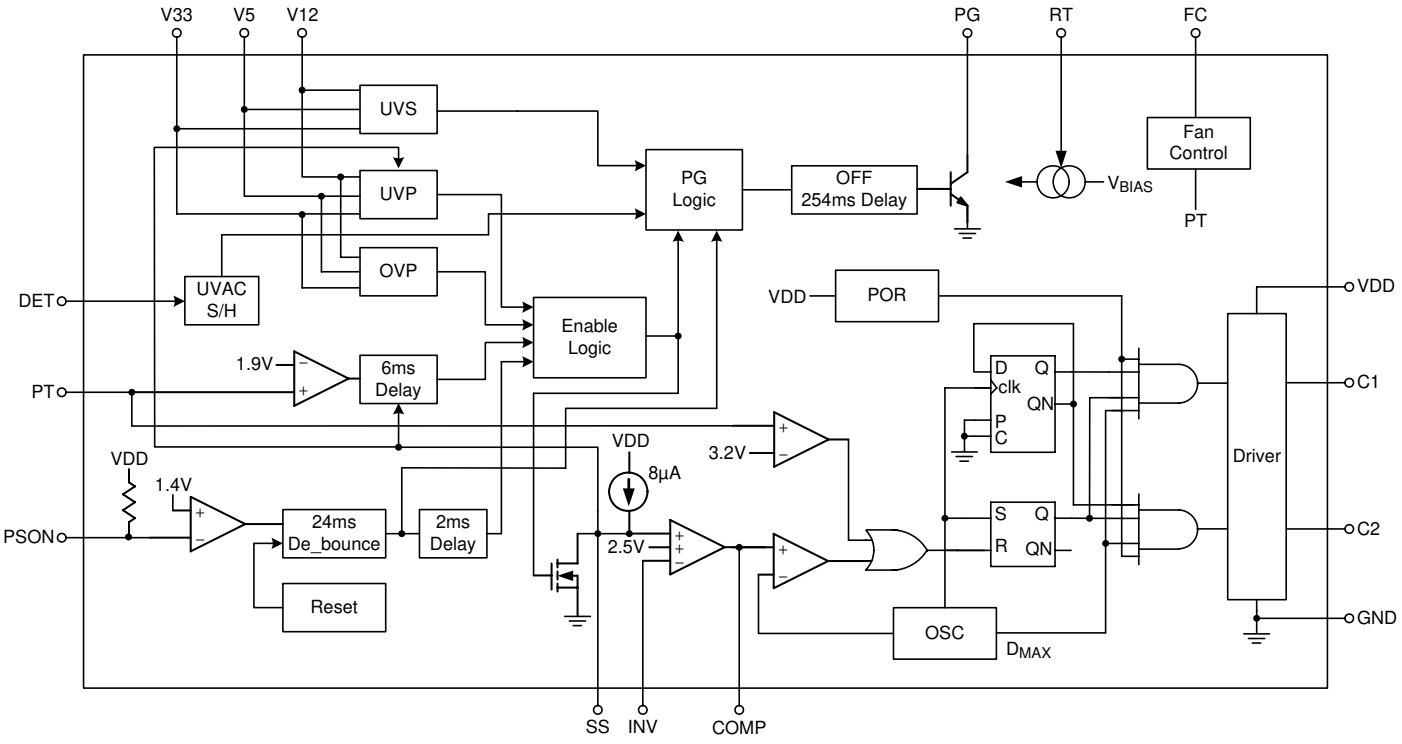


DIP-16

Functional Pin Description

Pin No.		Pin Name	Pin Function
SOP-16	DIP-16		
1	1	RT	Reference Current Setting. Connected to an external resistor to set the internal reference current.
2	2	FC	Fan Control I/O.
3	3	V12	12V Output Sense Pin.
4	4	V33	3.3V Output Sense Pin.
5	5	V5	5V Output Sense Pin.
6	6	PT	Over Power Sense Pin.
7	7	DET	V_{AC} Input Detector Input.
8	8	VDD	Bias of Controller. Source from 5V standby power.
9	9	C2	PWM Driver Output 2.
10	10	C1	PWM Driver Output 1.
11	11	GND	Ground.
12	12	PG	Power Good Signal Output (open collector type.).
13	13	PSON	Remote On/Off Control with 24ms De_bounce Time.
14	14	COMP	Error Amplifier Output.
15	15	INV	Negative Input of error amplifier.
16	16	SS	Soft-Start. SS is as the non-inverting input of error amplifier.

Function Block Diagram



Operation

The R7521 is a PWM controller with supervisor functions. The PWM signal C1 and C2 drive primary-side switching power transistor by transformer, and the supervisor monitors each output. The R7521 provides fruitful protection functions that protect system from damage. Each output is protected by OVP, UVP, and OPP. The functions description as follow :

Output Over-Voltage Protection

The R7521 has an output Over-Voltage Protection (OVP) function, which monitors the 3.3V, 5V and 12V output voltages, to prevent power system and loads from damages during one or more output OV condition(s). The OVP starts monitoring the voltages on V33, V5 and V12 at the end of the PSONB de-bounce time. When an Over-Voltage (OV) condition appears at one of the monitored pins for more than the 0.6ms (typical) deglitch time, the PG voltage goes low to indicate one of the output voltages is out of regulation. Meanwhile the R7521 disables PWM output and protects the power supply system. The OVP condition is latched until PSON is toggled from low to high or VDD restarts.

Output Under-Voltage Protection

The R7521 provides under voltage protection for the 3.3V, 5V and 12V outputs. The UVP continuously monitors the voltage on V33, V5 and V12. When an Under Voltage (UV) protection condition appears at either one of the monitored pins for more than 2ms (typical) deglitch time, the PG voltage goes low to indicate one of the output voltages is out of regulation. Meanwhile, the R7521 disables the PWM output and protects the power supply system. The UVP condition is latched until PSON is toggled from low to high or VDD restarts.

Output Over-Power Protection

The R7521 has an output over-power protection (OPP) function, which monitors total output power. The PT pin of R7521 senses primary-side switching current by current transformer (CT). When over power or output short condition appears, the OPP exceeds the trigger voltage (1.9V) for 6ms (typical), the R7521 disables PWM output and protects the power supply system. In addition, the PT can monitor −12V output voltage, and the OPP condition is latched until PSON is toggled from low to high or VDD restarts.

PG Outputs

In general, the PG voltage pulled high by an external resistor connected to the 5V output, indicates the status of the outputs. The PG keeps at low state when VDD voltage < UVLO threshold, PSON = H, PGI voltage < 1.2V or one of the faults, including UVP, OVP and OPP, occurs.

PSON De-bounce

The R7521 provides a remote ON/OFF control input pin (PSON) for PC power supply applications. A built-in 24ms (typical) de-bounce circuit performs rising and falling edge noise de-bounce functions to identify valid PSON input signals. The PSON also has a TTL logic-compliant input voltage threshold and a hysteresis design against input noise.

Soft-Start

The SS offers an internal 8μA (typical) constant current. Connect a capacitor between the SS and GND pins to set the soft-start time. Therefore, the soft-start time is t_{SS} = 8μ x C_{SS}. During soft-start period, the UVP and OPP protection is disabled to prevent wrong UVP, OPP protection.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD ---------- 5V
- I_{DD} ---------- 30mA
- Power Dissipation, P_D @ T_A = 25°C
  SOP-16 ---------- 0.92W
  DIP-16 ---------- 1.68W
- Package Thermal Resistance (Note 2)
  SOP-16, θ_{JA} ---------- 108.6°C/W
  DIP-16, θ_{JA} ---------- 59.6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 4V to 6V
- Frequency ---------- 60kHz
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 5V, R_T = 62kΩ, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
POR Section						
DC Supply Voltage	V_{DD}		4	--	6	V
On Threshold Voltage	V_{TH_ON}		--	3.65	--	V
Off Threshold Voltage	V_{TH_OFF}		--	3.4	--	V
Operating Supply Current	I_{DD_OP}	V_{DD} = 5V, V_{COMP} = 2.5V	--	--	10	mA
Oscillator Section						
Normal PWM Frequency	f_{OSC}	R_T = 62kΩ	55	60	65	kHz
Maximum Duty Cycle	DCY_{MAX}	Both for C1 and C2	--	46	--	%
Frequency Variation Versus VDD Deviation	f_{DV}	V_{DD} = 5V	--	--	2	%
Frequency Variation Versus Temperature Deviation	f_{DT}	T_A = –20°C to 85°C	--	--	5	%
Ramp of Oscillator	V_P		--	2	--	V
Zero Duty Offset	V_{OFFSET}		--	0.5	--	V
RT Reference Voltage	V_{REF_RT}	f_{OSC} = 35kHz to 70kHz	0.98	1	1.02	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protection Section						
OVP of 3.3V Output	V_{OVP_V33}		3.9	4.1	4.3	V
OVP of 5V Output	V_{OVP_V5}		5.8	6.1	6.5	V
OVP of 12V Output	V_{OVP_V12}	(Note 5)	--	2.5	--	V
UVP of 3.3V Output	V_{UVP_V33}		2	2.6	2.8	V
UVP of 5V Output	V_{UVP_V5}		3	3.6	3.9	V
UVP of 12V Output	V_{UVP_V12}	(Note 5)	--	1.25	--	V
UVS of 3.3V Output	V_{UVS_V33}		2.5	2.8	3	V
UVS of 5V Output	V_{UVS_V5}		4	4.3	4.5	V
UVS of 12V Output	V_{UVS_V12}	(Note 5)	--	1.75	--	V
Time Delay of OVP	T_{OVP}		0.37	0.6	1.35	ms
Time Delay of UVP	T_{UVP}		1.2	2	4.2	ms
Time Delay of UVS	T_{UVS}		0.9	1.4	2.2	ms
Over Power Protection	V_{PT}		1.7	1.9	2.1	V
PT Delay			--	6	--	ms
PT Cycle Limit			2.9	3.2	3.5	V
Power Good Section						
Power Good Time Delay	T_{PG}		--	254	--	ms
DET Voltage Sense for PG	V_{DET}		0.45	0.5	0.55	V
PG Output Saturation Level	V_{OL}	I_{PG} = 5mA	--	--	5	V
PG Leakage Current	I_{LK}	V_{PG} = 5V	--	--	1	µA
Error Amplifier Section						
Reference Voltage	V_{REF2}		2.45	2.5	2.55	V
Open Loop Gain	A_{VOL}		50	60	--	dB
Unit Gain Bandwidth	BW		0.3	1	--	MHz
Power Supply Rejection Ratio	PSRR		50	--	--	dB
Remote On/Off Section						
PSON Threshold Voltage	V_{TH}		1	1.4	2	V
PSON Sourcing Current	I_{PSON}		--	--	0.5	mA
PSON De_bounce Time	T_{DEB}	ON	--	24	--	ms
		OFF	--	8	--	
Delay Time Between PSON = 1 and PG = 0	T_{PSOFF}	(m.o + D-FF)	1.5	2	4	ms
Soft-Start Section						
SS Charging Current	I_{SS}		6.7	8	9.3	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Fan Control Section						
Sourcing Current of FC	I_{FC}		6	--	--	mA
Voltage Range of FC	V_{FC}		0.2	--	4	V
PWM Output Section						
Rising Time	T_R	V_{DD} = 5V, C_L = 1.8nF	--	20	55	ns
Falling Time	T_F	V_{DD} = 5V, C_L = 1.8nF	--	15	50	ns
R_{DS_ON} of Top and Bottom Leg	R_{DS_ON}	V_{DD} = 5V	--	--	4.4	Ω

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

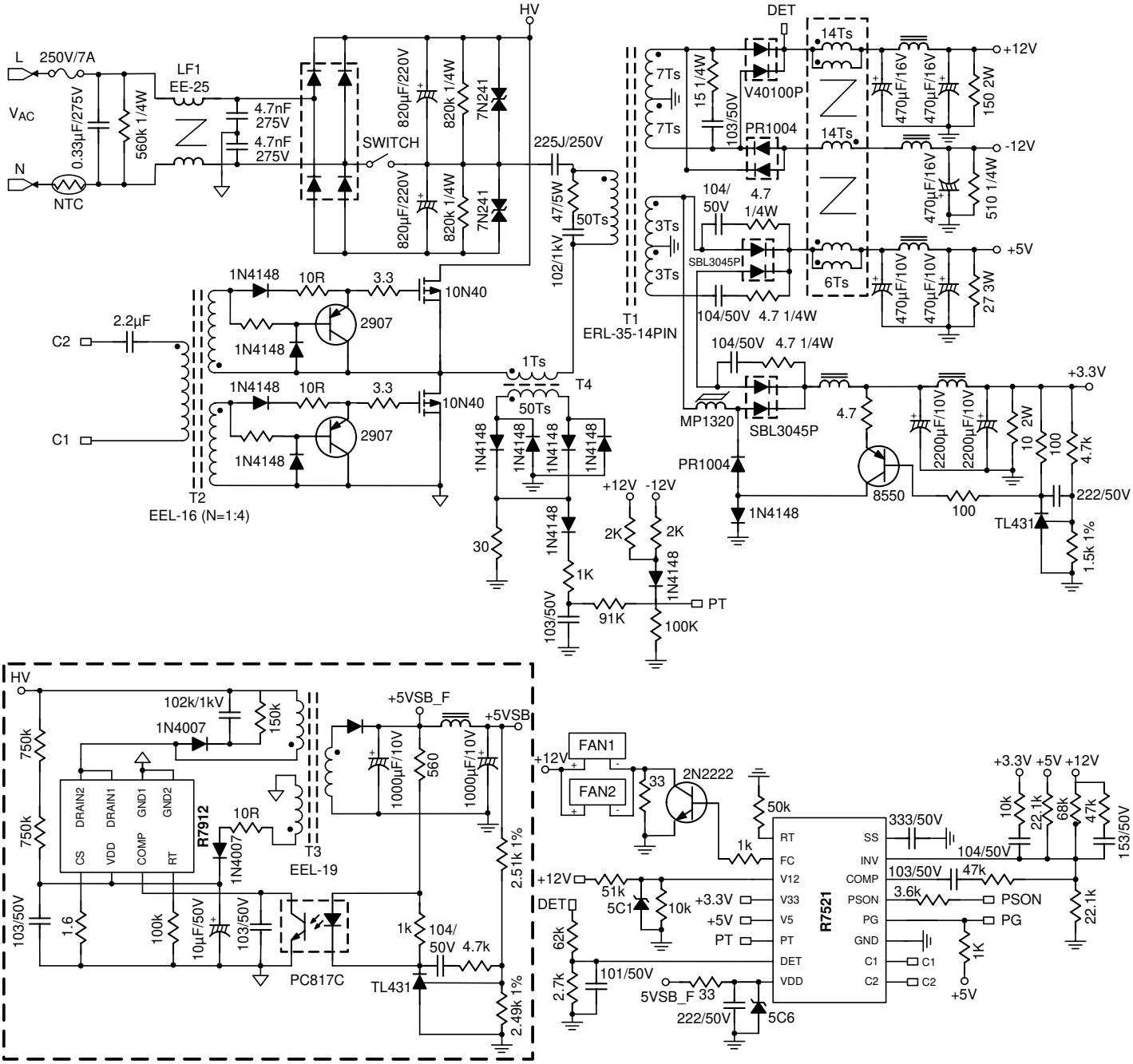
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

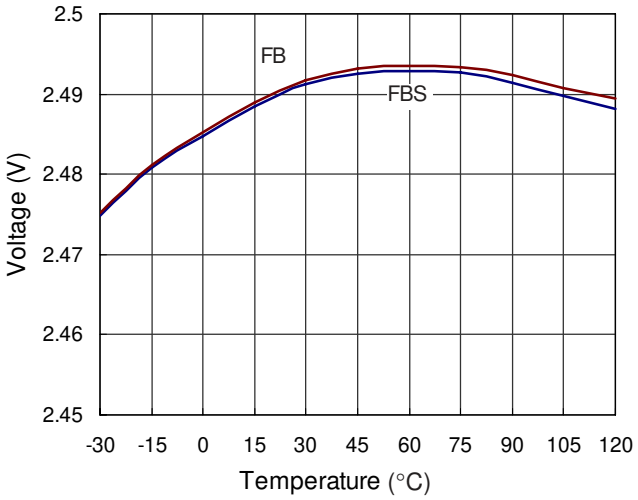
Note 5. The V12 pin must to use divider resistor. Propose setting the ratio is 1/6.

Typical Application Circuit

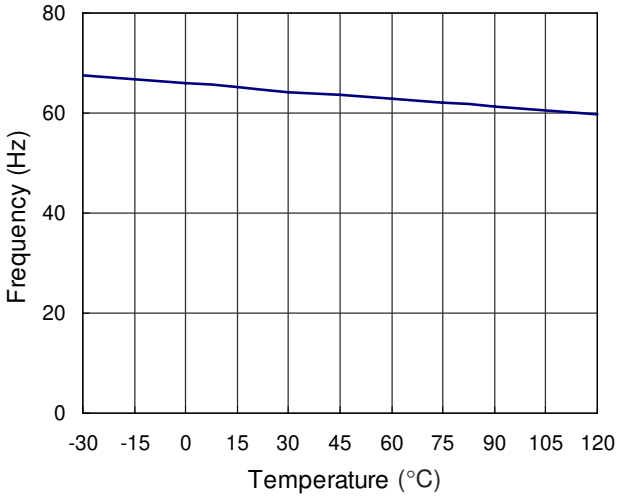


Typical Operating Characteristics

FB & FBS vs. Temperature



Frequency vs. Temperature



Application Information

Fan Control

In order to effectively utilize the fan to disperse heat and reduce acoustic noise, the R7521 provides FC pin to control Fan's speed. Figure 1 shows the relationship between FC voltage and load in ATX 300W power supply application.

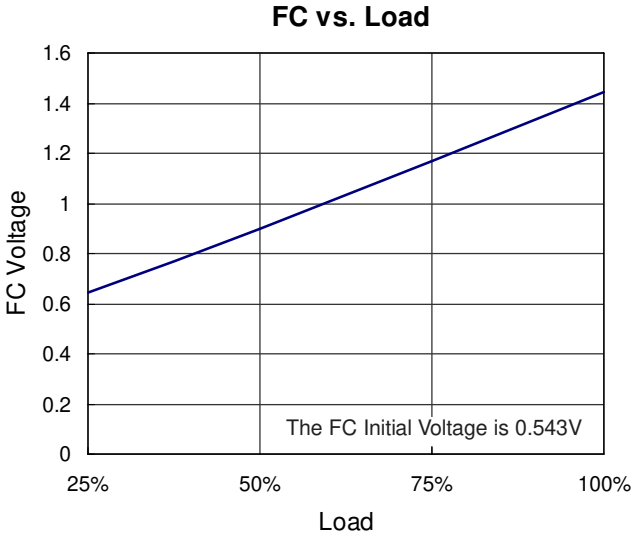


Figure 1. FC Voltage Variation

Over Power Protection

When ATX power is over power or in output short condition, the R7521 will shut down the controller. As shown in Figure 2, if the over power condition appears, PT voltage exceeds the trigger voltage (1.9V) and exists for 6ms (typical), the PWM output will be latched.

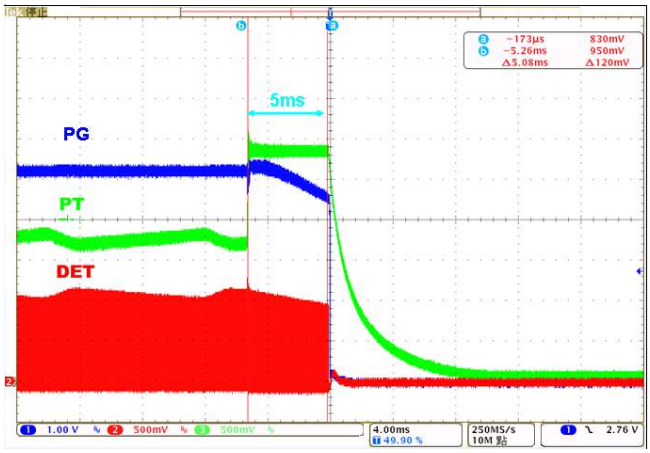


Figure 2. Over Power Protection

Beside, the R7521 has fine over power protection. As Figure 3, total power limit is constant, and won't follow Vin variation. Set the ratio of OPP resistive divider to decide the total limit.

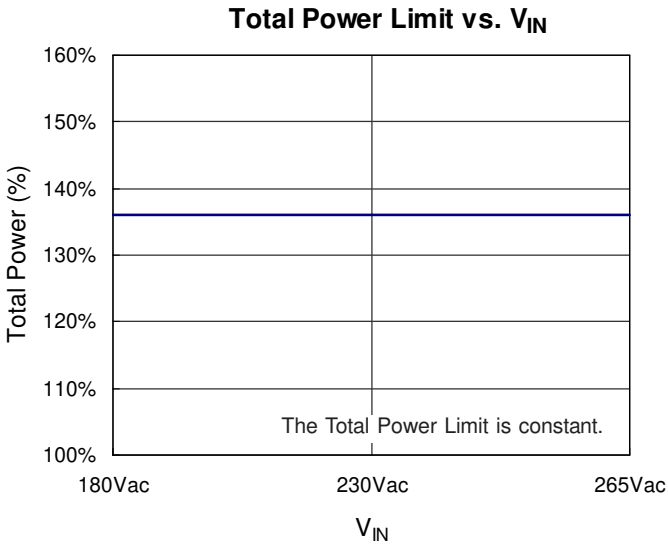


Figure 3. Over Power Limit and V_{IN} Relation Curve

VAC Detecting Protection

DET is connected to secondary winding through a resistive divider for V_{AC} input detecting. When V_{AC} fails, the voltage of DET is lower than 0.5V, and PG signal will be pulled low to indicate V_{AC} power-down. Set the ratio of resistive divider to decide the DET weight. The bypass capacitor is used to filter the switching noise.

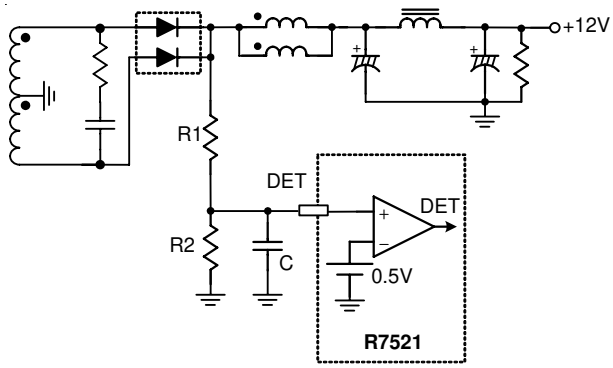


Figure 4. V_{AC} Detecting Circuit

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-16 package, the thermal resistance, θ_{JA}, is 108.6°C/W on a standard JEDEC 51-7 four-layer thermal test board. For DIP-16 package, the thermal resistance, θ_{JA}, is 59.6°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (108.6°C/W) = 0.92W for SOP-16 package

$P_{D(MAX)}$ = (125°C – 25°C) / (59.6°C/W) = 1.68W for DIP-16 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

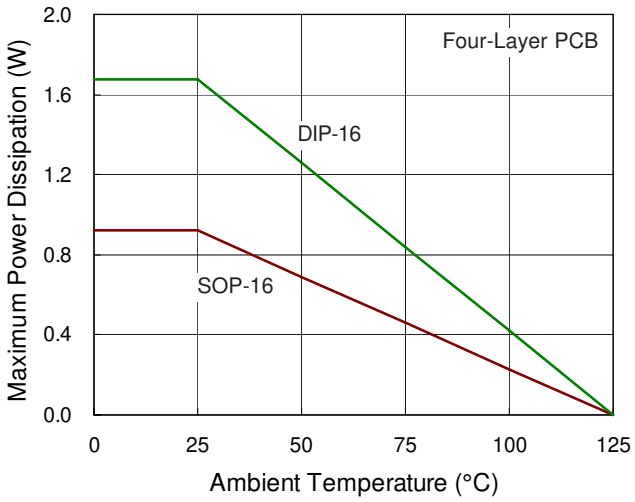
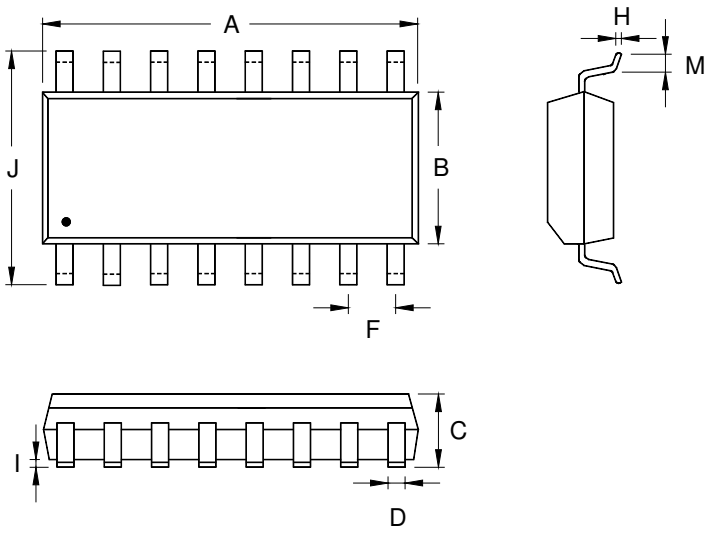


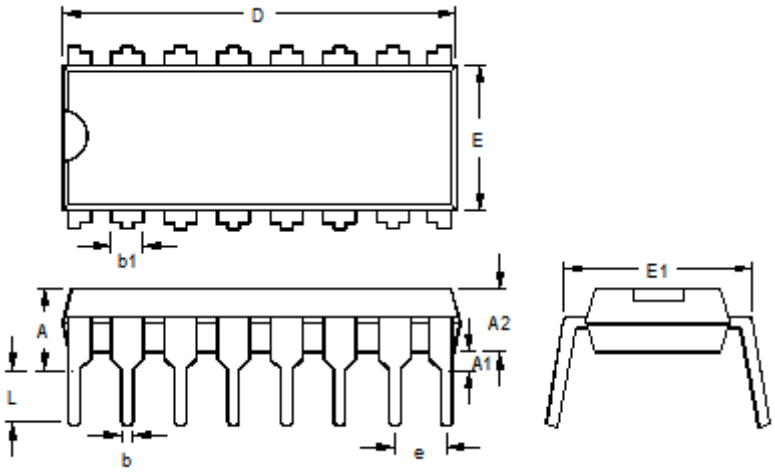
Figure 5. Derating Curve of Maximum Power Dissipation

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	9.804	10.008	0.386	0.394
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

16–Lead SOP Plastic Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.700	4.320	0.146	0.170
A1	0.381	0.710	0.015	0.028
A2	3.200	3.600	0.126	0.142
b	0.360	0.560	0.014	0.022
b1	1.143	1.778	0.045	0.070
D	18.800	19.300	0.740	0.760
E	6.200	6.600	0.244	0.260
E1	7.620	8.255	0.300	0.325
e	2.540		0.100	
L	3.000	3.600	0.118	0.142

16-Lead DIP Plastic Package

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