LM27403EVM-POL600 30A Ultra-Compact DC/DC Regulator Evaluation Module

User's Guide

Literature Number: SNVU330
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LM27403EVM-POL600 Evaluation Module

This user's guide offers perspective regarding point-of-load (POL) DC/DC regulation circuit design and implementation. Specifically, it describes a cost-effective solution to address the challenges a system designer can encounter when a high density and efficient POL regulator is required and PC board real estate is at a premium. Using the LM27403 voltage-mode PWM controller and a Power Block NexFET™ in an embedded module style solution, the LM27403EVM-POL600 synchronous buck regulator delivers an output current up to 30 A. High conversion efficiency is a key parameter in this design—translating into lower power loss, less package temperature rise for a given power throughput, and enabling a higher power density form factor. PCB source and gerber files, as well as component views and fabrication drawings, are available in PowerLab™ for this design.

1 INTRODUCTION

The LM27403EVM-POL600 represents a standalone POL module with benchmark power density surface-mounted on a host board as a mother-daughter configuration. The POL module itself is an independent sub-assembly that is ultra-compact, versatile, tailored to high-volume SMT manufacturing, and fully proven and tested before SMT placement on the host board.

In practice, a POL module such as this is typically parallel stacked onto the system motherboard wherein power and signal connections are realized using SMT connections. As such, the module can be flexibly deployed across multiple systems and applications, greatly easing the design burden of a system engineer. Alternatively, the design is realized as a voltage-regulator-down (VRD) implementation with the components placed directly on the motherboard.

High density and small footprint are the main design tenets, with efficiency as a key performance metric. An output voltage with better than 1% setpoint accuracy is adjustable between 0.6 V and 5.5 V simply by changing a trim resistor. With an output current up to 30 A, the switching frequency is 600 kHz and synchronizable to a higher frequency if required. Nominal input voltage is 12 V but can vary from 3 V to 20 V with suitable adjustment of the programmable UVLO.

The LM27403EVM-POL600 is designed specifically to demonstrate the LM27403 PWM controller in a typical 12-V bus to low output voltage, low duty-cycle application.

1.1 Typical Applications

- Synchronous buck regulators in distributed power architectures
- High current density POL modules
- Communications, cloud, server, storage, graphics
- Embedded computing, FPGAs, ASICs, DSPs

1.2 EVM Features and Electrical Performance

- High conversion efficiency: 91% at 1.8 V, 30 A
- High current and power per unit volume, 200A/in^3
- Tiny converter footprint of 20 mm x 15 mm (0.8" x 0.6")
- Low profile of 8.4 mm (0.33")
- Wide input voltage operating range of 3 V to 20 V
- Nominal output voltage of 1.8 V with 1% feedback accuracy
- Adjustable output voltage from 0.6 V to 5.5 V by changing "trim" resistance
- 600-kHz free-running switching frequency
- Synchronizable to an external clock signal up to 1.2 MHz
- Single supply rail—no additional bias voltage required
- Overcurrent protection via inductor DCR current sensing with thermal compensation
- Programmable thermal shutdown based on remote-sensed BJT temperature
- Soft-start time of 8 ms
- Monotonic pre-bias output voltage startup
- Programmable input UVLO set to turn on and off at 4.4 V and 3.7 V, respectively
- Voltage-mode PWM control supporting all-ceramic or ceramic/electrolytic output capacitor implementations
- Configurable remote output voltage sensing for optimal load regulation performance
- Power Good indicator
- Input circuit damping with optional electrolytic capacitor
- Easy access to key features including PGOOD, Enable, SYNC, and output remote sense

2 ELECTRICAL PERFORMANCE

Table 1. Electrical Performance Specifications

Symbol	Parameter	Notes and Conditions		Min	Nom	Max	Units
INPUT CHARACTERISTICS							
V_{IN}	Input voltage range			4.5	12	20	V
$V_{IN(ON)}$	Input voltage turn on	Set by UVLO/EN resistors			4.4		V
$V_{IN(OFF)}$	Input voltage turn off				3.7		V
$I_{IN(MAX)}$	Input current, full load[(1)]	V_{IN} = 7 V	I_{OUT} = 30 A		8.48		A
		V_{IN} = 12 V			4.95		A
$I_{IN(NL)}$	Input current, no load	V_{IN} = 12 V, I_{OUT} = 0 A			40		mA
$I_{IN(OFF)}$	Input current, disabled	V_{IN} = 12 V, $V_{UVLO/EN}$ = 0 V			1		mA
OUTPUT CHARACTERISTICS							
V_{OUT}	Output voltage			1.782	1.800	1.818[(2)]	V
I_{OUT}	Output current	V_{OUT} ≤ 1.8 V		0		30	A
		V_{OUT} > 1.8 V		0		25	A
ΔV_{OUT}	Output voltage regulation	Load Regulation: I_{OUT} = 0 A to 30 A			0.5%		
		Line Regulation: V_{IN} = 4.5 V to 20 V			0.5%		
$V_{O(RIPPLE)}$	Output voltage ripple	V_{IN} = 12 V, I_{OUT} = 20 A			10		mVpp
$V_{O(PKDEV)}$	Output voltage transient response	I_{OUT} = 0 A to 10 A, 2 A/µs slew rate			50		mV
I_{LIM}	Output overcurrent protection				33		A
t_{SS}	Soft-start time				8		ms
SYSTEMS CHARACTERISTICS							
$F_{SW(NOM)}$	Switching frequency (free running)				600		kHz
F_{SW}	Switching frequency range (using SYNC)			$F_{SW(NOM)}$		1200	kHz
η_{PK}	Peak efficiency[(1)(3)]	V_{IN} = 12 V, I_{OUT} = 12 A			93%		
η_{FULL}	Full load efficiency [(1)(3)]	V_{IN} = 5 V	I_{OUT} = 30 A		91%		
		V_{IN} = 12 V			91%		
		V_{IN} = 20 V			89%		
f_c	Loop bandwidth	V_{IN} = 12 V, I_{OUT} = 15 A			75		kHz
φ_M	Phase margin				55		º
T_A	Ambient temperature[(4)]			-40		85	ºC
T_{OTP}	System-level thermal shutdown				110		ºC

(1) The default output voltage and switching frequency are 1.8 V and 600 kHz, respectively. Efficiency and other parameters will change based on the chosen output voltage, load current, and frequency.
(2) This is equivalent to an output voltage tolerance of 1%.
(3) Input and output voltage measurements are taken local to the module.
(4) The ambient temperature range is provided with the implicit caveat of appropriate output current derating to assure recommended maximum component operating temperatures are not exceeded.

3 CIRCUIT DIAGRAM

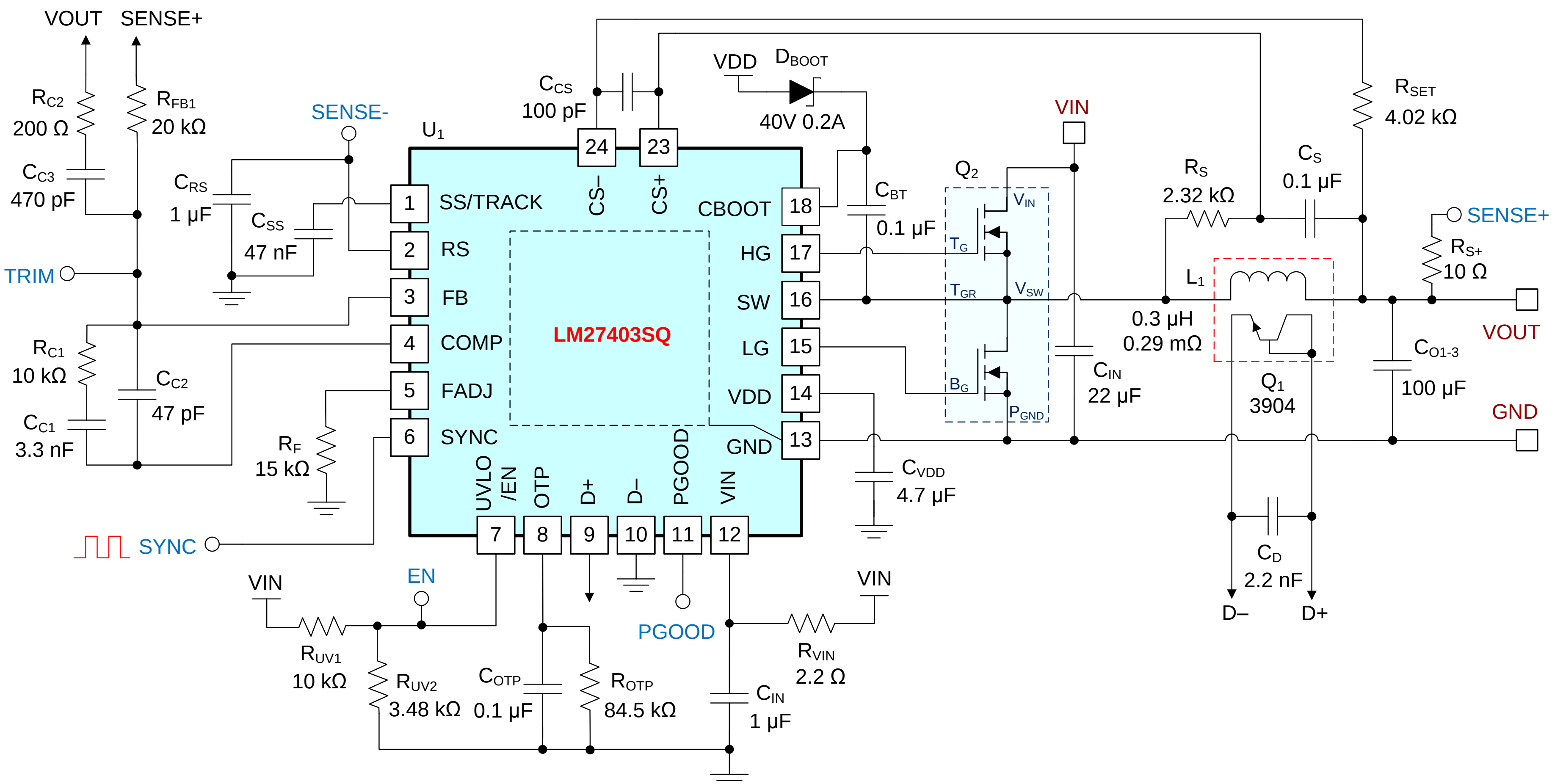

Figure 1. Regulator Circuit Diagram

4 PHOTOS

4.1 Module

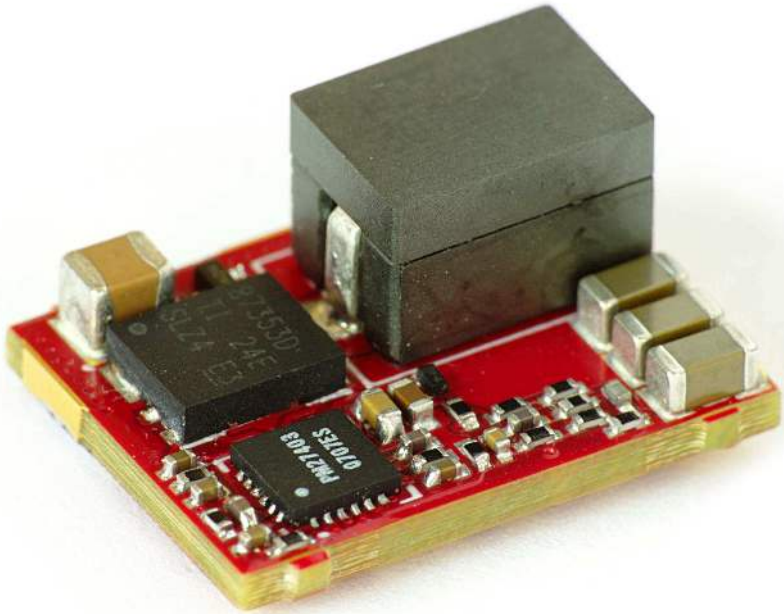

Figure 2. Photo of Module

4.2 Sub-Assembly

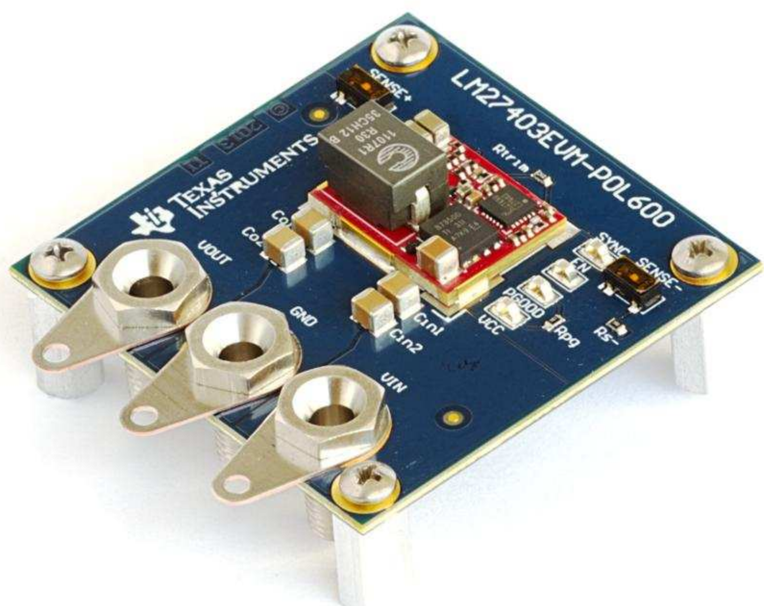

Figure 3. Photo of Module SMT Connected to Host PCB

5 DESIGN CONSIDERATIONS

5.1 Current Sensing in DC/DC Regulators

Availing of intrinsic circuit parasitic elements, such as inductor DCR or MOSFET on-state resistance, for lossless current sensing is quite common as it enables high power density and low-cost circuit implementations. But merely sensing the voltage across the low-side MOSFET in a buck converter is inaccurate given the large initial tolerance of the $R_{DS(ON)}$ (as high as ±30%) and the variation with temperature inherent with the MOSFET die. Also, sensing occurs only when the low-side MOSFET is conducting. By contrast, the tolerance of an inductor's DCR is typically specified at ±8%, sometimes even lower. The inductor DCR current sense technique, achieved by connecting an RC filter network in parallel with the inductor, is widely adopted in DC/DC regulators for high-current applications.

With the trend towards higher switching frequencies coupled with the need for fast load transient response, a relatively low inductance is required. At high output currents, ultra-low DCR ferrite inductors offer reduced copper and core losses. Unfortunately, the current sense signal amplitude derived from sub-mΩ inductor DCR is adversely affected. For example, a 30-A full load current and 0.3-mΩ DCR produces an average voltage signal of only 9 mV (at room temperature), driving the need for low offset circuits to meet accuracy specifications. Also, a design is typically captive to the hard saturation characteristic of ferrite-cored inductors, and the imperative is to never exceed the inductor's saturation current threshold.

5.1.1 Leveraging MOSFET Vertically-Stacked Construction

An increased effective sense resistance (and resultant voltage signal amplitude) is realized by advantageously employing the package structure copper resistance in the vertically-integrated MOSFET device, e.g. TI Power Block NexFET™. Here, the inductor DCR current sensing method is reconfigured to include the copper resistance of the MOSFET's switch clip connecting high-side source and low-side drain. This is shown in the schematic of Figure 19.

The return to the high-side gate drive, designated T_{GR}, is a kelvin connection attached to the low-side MOSFET's drain. The voltage drop across the SW copper plate is now easily sensed and incorporated with the sensed voltage from the inductor DCR. The cumulative signal derived from the DCR and SW clip offers a continuous signal at higher amplitude, thus enabling more accurate current sensing performance. The effective sense resistance on an average basis is the DCR plus the clip resistance weighted by a (1–D) factor, where D is the PWM duty cycle. The sense network time constant is then chosen based on this effective sense resistance.

5.2 Thermal Design

It is critical to minimize power dissipation to reduce component operating temperature, particularly with small footprint implementations. MOSFET switch on-state resistance has a positive temperature coefficient, which means an increase of junction temperature compounds upon itself to increase even further until a steady state thermal equilibrium is obtained. Also, the local ambient and PCB temperatures in high-density PCB layouts can become elevated quickly due to the mutual heating effect inherent with high power dissipation from immediately adjacent power components.

The power and ground planes common to and layered beneath the devices act as heat spreaders throughout the PCB. It's important to bear in mind that the motherboard provides conductive thermal dissipation and heatsinking through the module's surface-mount terminal connections. The power terminals of the module PCB are also edge-plated to connect the inner and outer PCB current-carrying planes as well as increase the surface contact area to the host PCB. A general design recommendation is to position the major power dissipating components—the MOSFETs and inductor—on the top side of the module to purposely capitalize on whatever natural or forced convection is available in the application environment. Moreover, a low thermal impedance MOSFET package (from junction to soldered pin) serves to conduct a large portion of the heat flux through the device pins and utilize the PCB substrate as a heatsinking element.

5.3 Components

5.3.1 PWM Controller

The LM27403EVM-POL600 uses the LM27403 high performance, synchronous buck PWM controller with voltage-mode control loop, integrated MOSFET gate drivers with adaptively-controlled deadtime, inductor DCR current sensing, and 30-ns minimum on-time for low duty-cycle operation. Remote BJT temperature measurement enables (a) DCR sense voltage compensation for accurate current limit across the operating temperature range, and (b) board-level thermal shutdown for increased reliability. The LM27403 is available in a 4-mm × 4-mm WQFN-24 PowerPAD™ package. Please consult the LM27403 datasheet for more details. In addition to WEBENCH® Power Designer, the reader is also encouraged to avail of the LM27403 Design Tool, particularly for quick-start guidance with power train and compensation circuit component selection.

5.3.2 MOSFETs

A CSD87350Q5D Power Block NexFET™ from TI is an optimized MOSFET design for synchronous buck applications offering high current, high efficiency, and high frequency capability in a small SON 5-mm × 6-mm package. Optimized for 5-V gate drive applications, it offers a flexible solution when paired with any 5-V gate drive PWM control stage.

Using a system-optimized grounded leadframe, thick copper clips and vertical die stacking, the asymmetric MOSFETs are optimized for low duty cycle, high power density and efficient operation in high switching frequency applications. The low-side synchronous and high-side control MOSFETs have 1.2-mΩ and 5.0-mΩ effective AC on-impedances at 25°C, and gate charges of 20 nC and 8.4 nC, respectively. With the common source inductance of the high-side MOSFET essentially eliminated by kelvin gate connections, these low charge parameters enable very low switching losses. Leveraging the heat spreading advantages of the grounded tab, total MOSFET power dissipation at 1.8-V and 25-A output in this application, including conduction and switching loss contributions at 100°C junction temperature, is 2.5W.

5.3.3 Filter Inductor

Off-the-shelf component options for low-DCR ferrite inductors with single-turn “staple” winding are widely available; a few examples are given in Table 4. Inductor power dissipation at 30 A, including copper and core loss at 75°C operating temperature, is 0.6 W.

5.4 Output Voltage Setpoint and Rempote Sensing

The module's output voltage is easily changing by appropriate selection of lower feedback resistance. This is designated as *Rtrim* on the motherboard, see schematic in Figure 20. The appropriate trim resistance for various output voltages is provided in Table 2.

Table 2. Output Voltage Trim Resistance

VOUT (V)	TRIM RESISTANCE (kΩ)
0.6	OPEN
0.8	60
0.9	40
1.0	30
1.2	20
1.5	13.3
1.8	10
3.3	4.42
5.0	2.8

6 SIGNAL CONNECTIONS AND TEST POINTS

6.1 Test Point Descriptions

Table 3. Test Point Descriptions

LABEL	DESCRIPTION
VIN	Input voltage connection
GND	GND connection for input and output
VOUT	Output voltage connection
SYNC	SYNC input
EN	UVLO/Enable input, pull to ground to disable converter
PGOOD	Power Good output
VCC	Pullup voltage supply connection for PGOOD

6.2 Signal Connections

6.2.1 Power Good Output

The LM27403EVM-POL600 provides a test point for measuring the Power Good voltage. A 20-kΩ resistor pull-up to an externally provided voltage source, designated VCC, is included. For true open-drain operation with no pullup, remove Rpg or the pullup voltage rail. Then, PGOOD can be connected to the EN terminal of a downstream regulator to provide sequential startup of two LM27403-based regulators.

6.2.2 EN Input

The LM27403EVM-POL600 provides a test point for measuring the LM27403's UVLO/EN pin voltage. Shorting this test point to GND disables the regulator.

6.2.3 SYNC Input

The LM27403EVM-POL600 provides a test point for applying a synchronization (SYNC) input signal. The free-running switching frequency is set at 600 kHz. However, the regulator can align in frequency and phase with that of the applied SYNC signal up to 1.2 MHz. The applied SYNC voltage should not exceed 5.5 V.

CAUTION

Proper control loop compensation, as related to the installed output capacitance appropriately derated for DC bias voltage, is imperative. Consult the LM27403 datasheet, LM27403 design tool, or WEBENCH® Designer for guidance with component selection.

6.3 Remote Sense Configuration

Two switches on the motherboard, designated *SENSE+* and *SENSE–*, are used to configure output voltage remote sensing. For local voltage sensing at the module's VOUT and SGND terminals, move the switch sliders to their respective inside positions (i.e. towards the module). Conversely, to achieve remote voltage sensing at the VOUT and GND banana plug connectors, move the switch sliders to their respective outer positions (i.e. away from the module).

7 TEST SETUP

Figure 4 shows the recommended test setup to evaluate the LM27403EVM-POL600. Working at an ESD workstation, make sure that any wrist straps, boot straps or mats are connected referencing the user to earth ground before power is applied to the EVM.

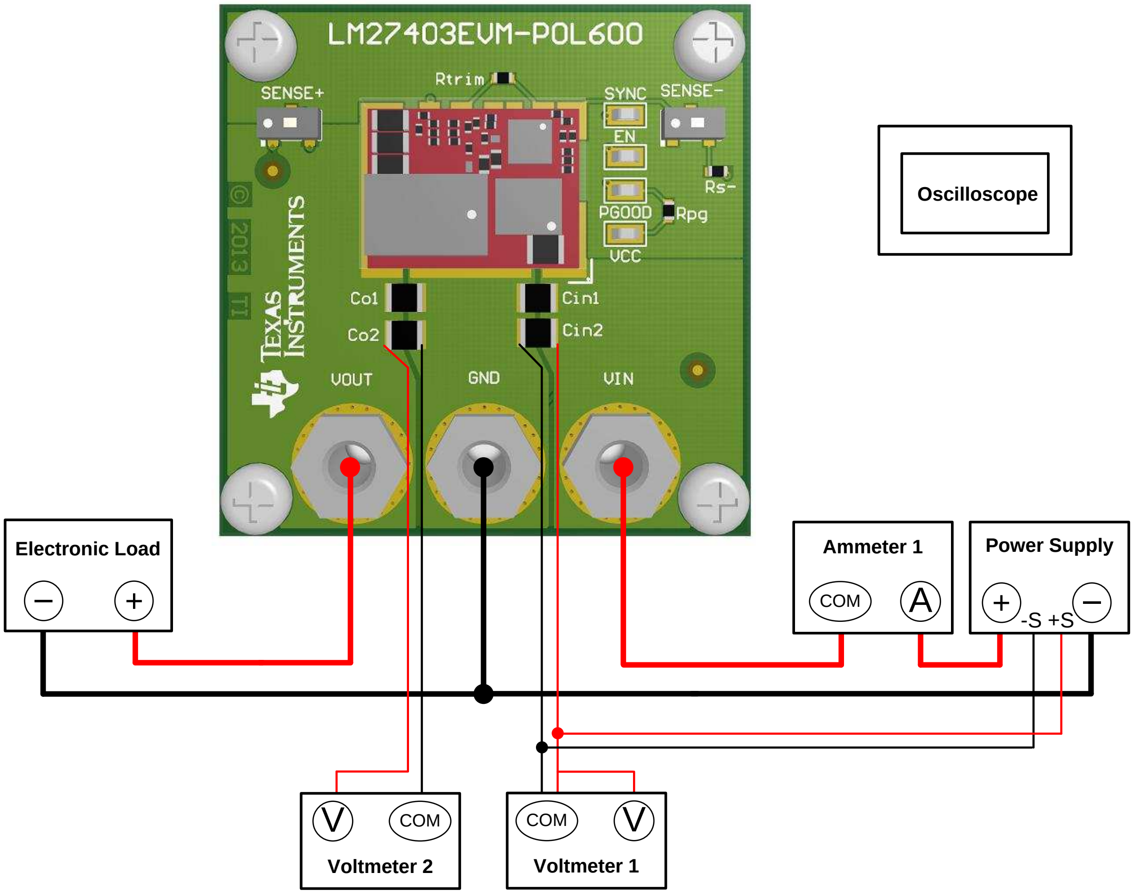

Figure 4. Connection Diagram

7.1 Test Equipment

Voltage Source: The input voltage source VIN should be a 0–20-V variable dc source capable of supplying 10 A.

Multimeters:

- **Voltmeter 1:** Input voltage at VIN to GND
- **Voltmeter 2:** Output voltage at the output connector lugs (or locally at the module, depending on the remote sense configuration)
- **Ammeter 1:** Input current (or use the power supply readout if its accuracy is deemed acceptable)

Electronic Load: The output load should be an electronic constant-resistance or constant-current mode load capable of 0 Adc to 30 Adc at 1.8 V.

Oscilloscope: A digital or analog oscilloscope can be used to measure pertinent converter waveforms. With the scope set to 20-MHz bandwidth and AC coupling, the output voltage ripple can be measured directly across an output capacitor with a short ground lead normally provided with the scope probe. Place the oscilloscope probe tip on the positive terminal of the output capacitor, holding the probe's ground barrel through the ground lead to the capacitor's negative terminal. It is not recommended to use a long leaded ground connection because this may induce additional noise given a large ground loop. To measure other waveforms, adjust the oscilloscope as needed.

Fan: Some of this EVM's components may exceed temperatures of 60°C during operation. Although not mandatory, a small fan capable of 200–400 LFM can be used to reduce component temperatures while the EVM is operating. Exercise care when touching the EVM while the fan is not running. Always exercise caution when touching any circuits that may be live or energized.

Recommended Wire Gauge:

- **Input Source to VIN and GND:** The recommended wire size is 1 × AWG #14 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).
- **VOUT to LOAD:** The minimum recommended wire size is 2 × AWG #14, with the total length of wire less than 4 feet (2 feet input, 2 feet return).

7.2 Recommended Test Setup

7.2.1 Input Connections

- Prior to connecting the DC input source, it is advisable to limit the source current to 10 A maximum. Make sure the input source is initially set to 0 V and connected to VIN and GND banana connections as shown in Figure 4. An additional high-ESR electrolytic input capacitor may be required if long input lines are used.
- Connect voltmeter 1 at VIN and GND connector lugs to measure the input voltage.
- Connect ammeter 1 to measure the input current.

7.2.2 Output Connections

- Connect an electronic load to VOUT and GND connections. Set the load to constant-resistance mode or constant-current mode at 0 Adc before input voltage is applied. Use short load lines to minimize voltage drop to the load.
- Connect voltmeter 2 at the output connectors' solder lugs to measure the output voltage.
- The output current level is taken from the electronic load readout (if its accuracy is deemed acceptable).

7.2.3 Local or Remote Output Voltage Sensing

Slider switches designated SENSE+ and SENSE- on the host PCB are used to select local or remote output voltage sensing as follows:

- Move the switches to their respective inner positions (i.e. towards the module) for local sensing at the VOUT and SGND module terminals.
- Move the switches to their respective outer positions (i.e. away from the module) for remote sensing at the VOUT and GND banana power connectors.

7.3 Test Procedure

7.3.1 Load, Line Regulation and Efficiency

- Set up the EVM as described above.
- Set load to constant resistance or constant current mode and to sink 0 Adc.
- Increase input source from 0 V to 12 V, using voltmeter 1 to measure input voltage.
- Use voltmeter 2 to measure output voltage, V_{OUT}.
- Vary load from 0 to 30 Adc, V_{OUT} should remain within load regulation specification.
- Vary input source voltage from 4.5 V to 20 V, V_{OUT} should remain within line regulation specification.
- Decrease load to 0 A. Decrease input source voltage to 0 V.

8 TEST DATA AND PERFORMANCE CURVES

Figure 5 through Figure 18 present typical performance curves for the LM27403EVM-POL600. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

8.1 Efficiency

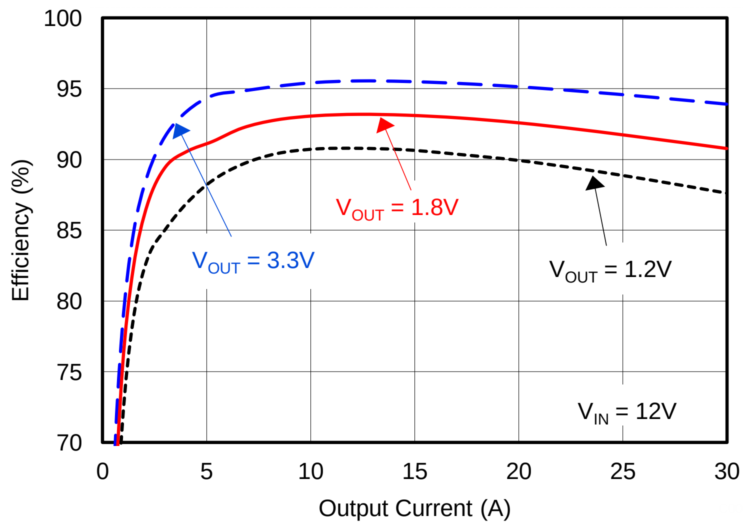

Figure 5. Efficiency

8.2 Load Regulation

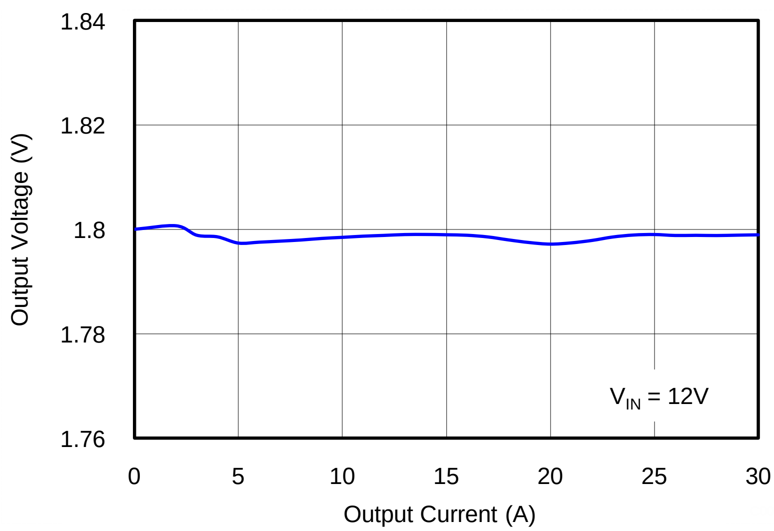

Figure 6. Load Regulation

8.3 Line Regulation

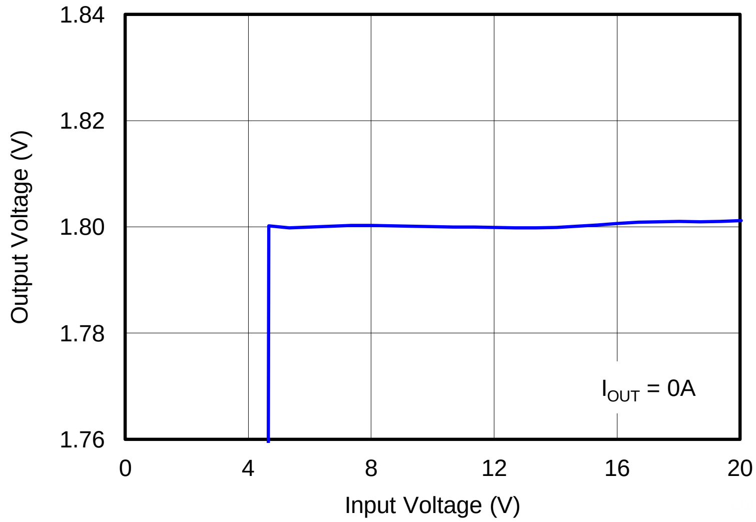

Figure 7. Line Regulation

8.4 Current Limit Hiccup Mode

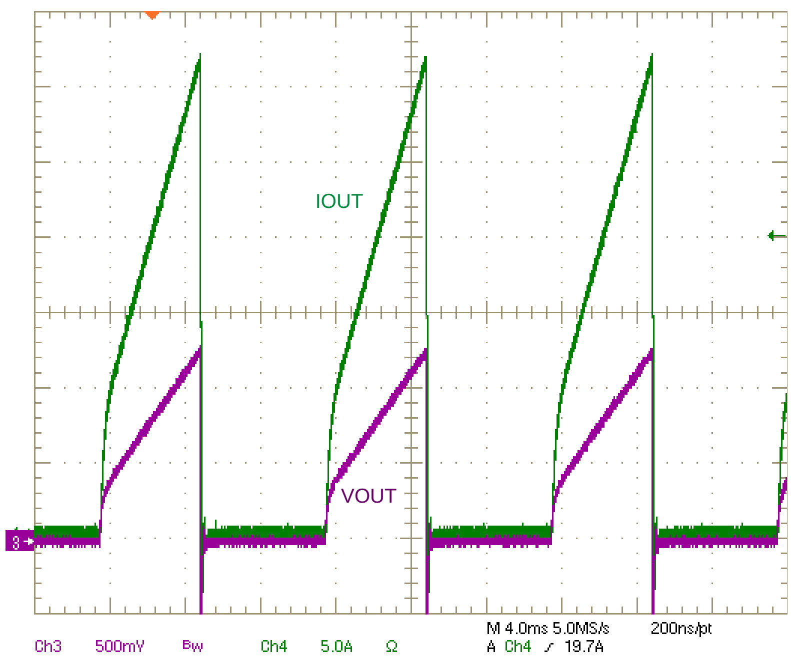

Figure 8. Current Limit Hiccup Mode

8.5 Load Transient Response

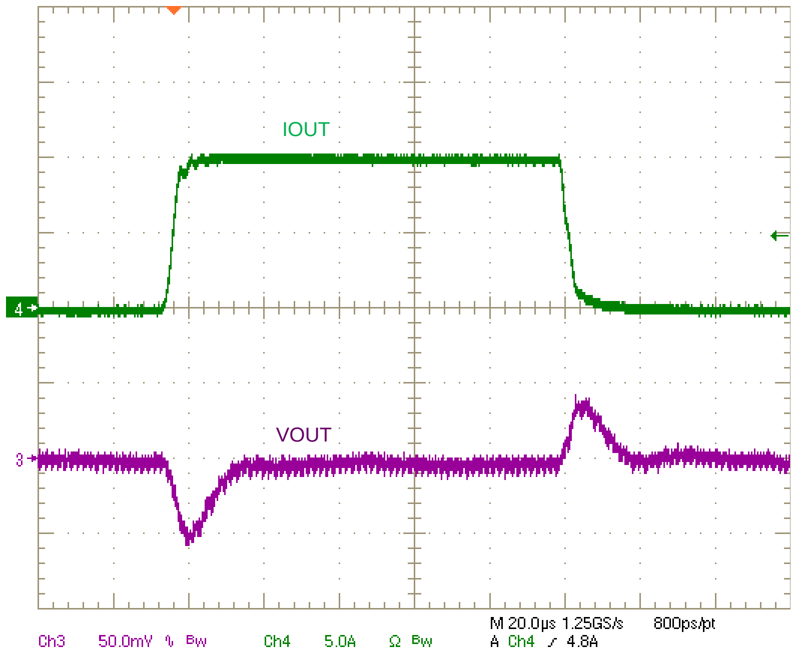

Figure 9. Load Transient Response; V_{IN} = 12 V, V_{OUT} = 1.8 V, 0 A to 10 A at 2 A/µs

8.6 Output Ripple

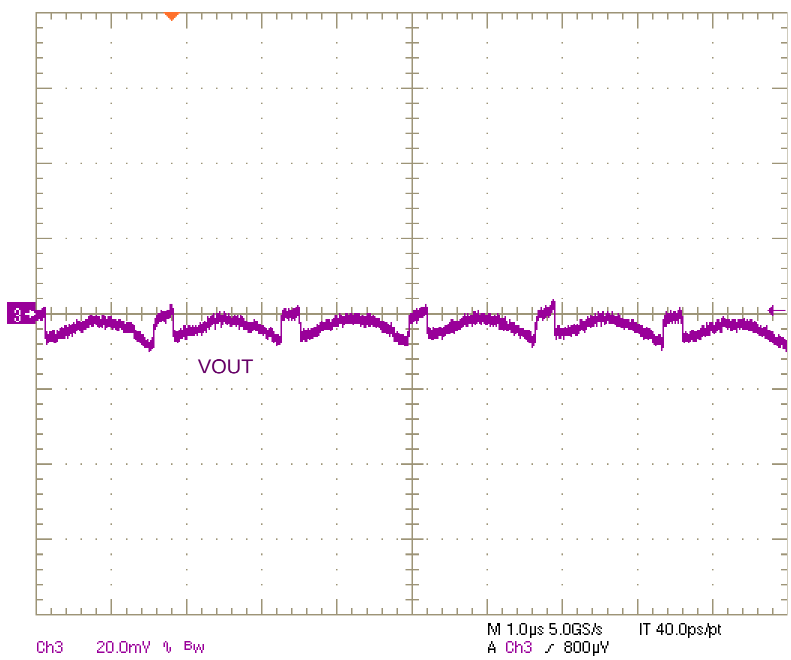

Figure 10. Output Voltage Ripple; V_{IN} = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 20 A

8.7 Startup and Shutdown – VIN

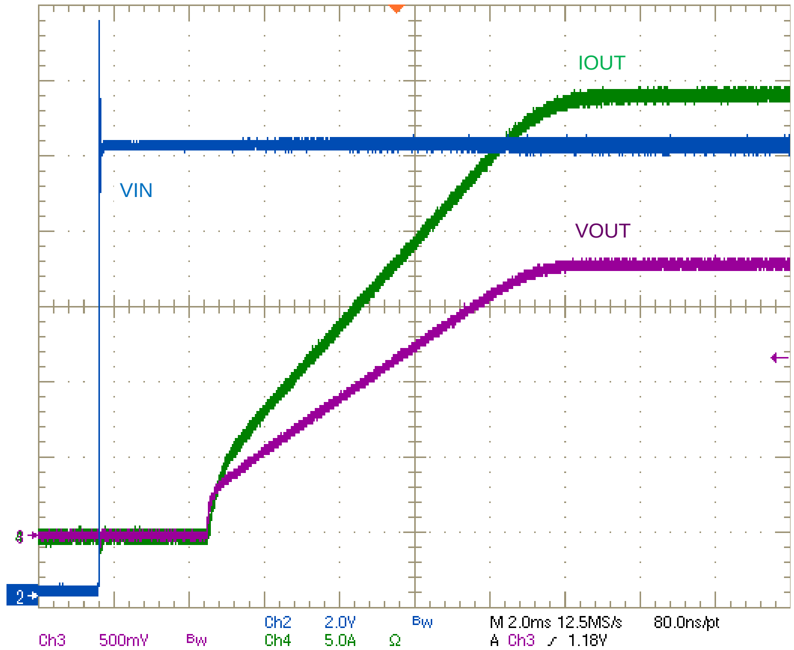

Figure 11. Startup with VIN Stepped to 12 V; V_{OUT} = 1.8 V, 30-A Resistive Load

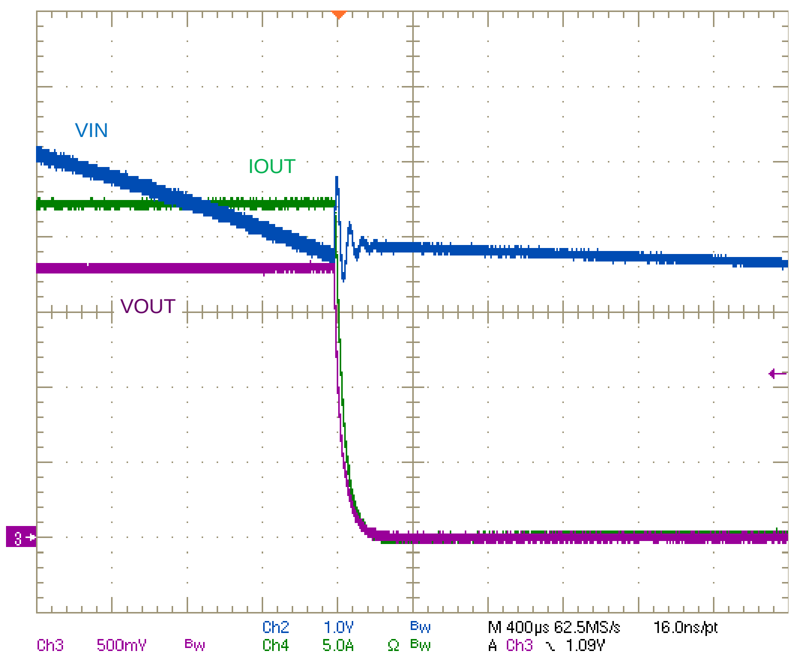

Figure 12. Shutdown After VIN Disconnected; V_{IN} = 12 V, V_{OUT} = 1.8 V, 22-A Resistive Load

8.8 Startup and Shutdown – Enable

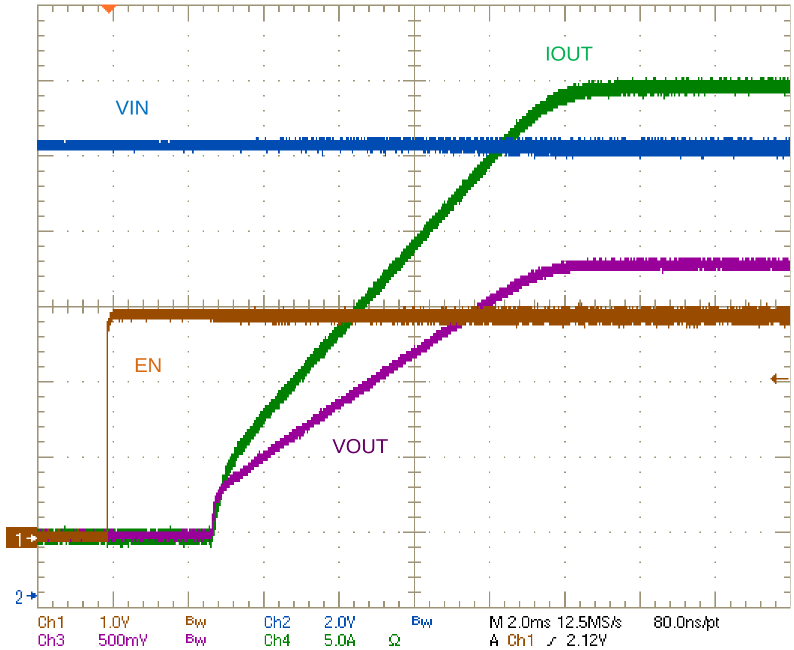

Figure 13. Startup with EN Stepped to 3 V; V_{IN} = 12 V, V_{OUT} = 1.8 V, 30-A Resistive Load

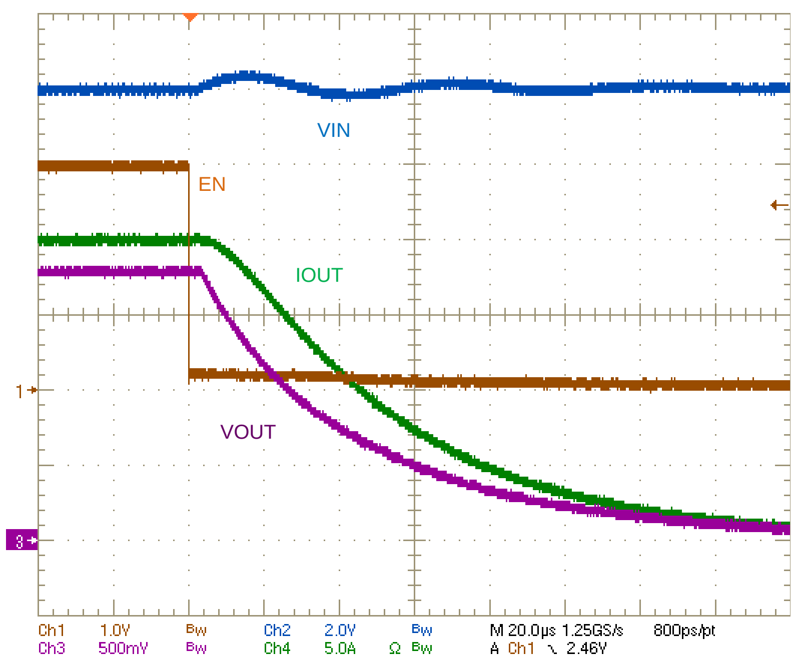

Figure 14. Shutdown with EN Pulled To GND; V_{IN} = 12 V, V_{OUT} = 1.8 V, 20-A Resistive Load

8.9 Pre-Bias Startup

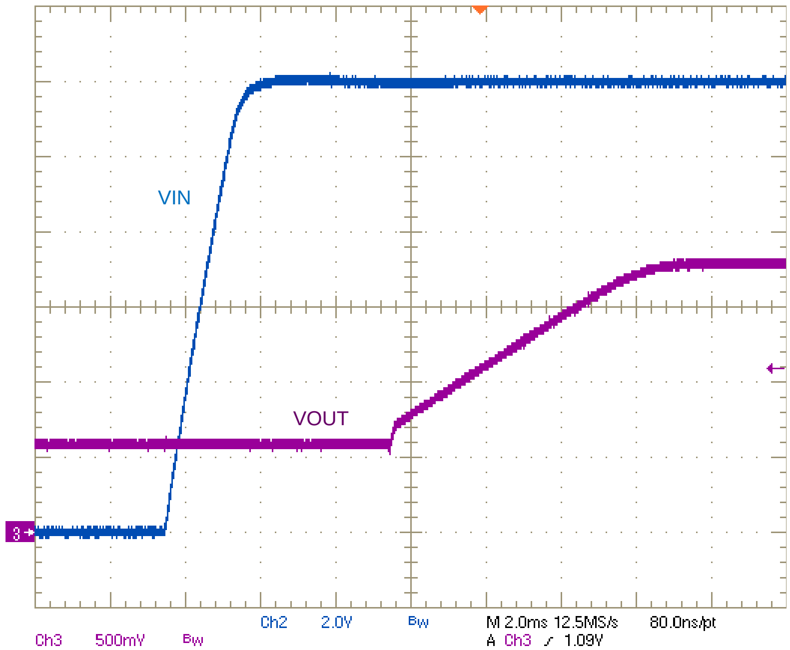

Figure 15. Pre-bias Startup; V_{IN} = 12 V, No Load, 0.6-V Pre-bias

8.10 Switch Node

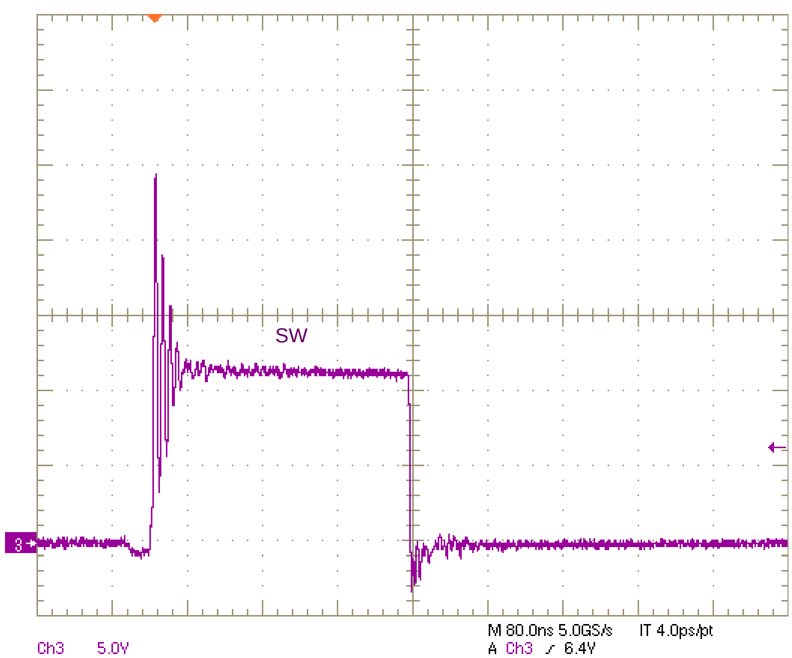

Figure 16. Switch Node Voltage; V_{IN} = 12 V, V_{OUT} = 1.8 V

8.11 Switch Deadtimes

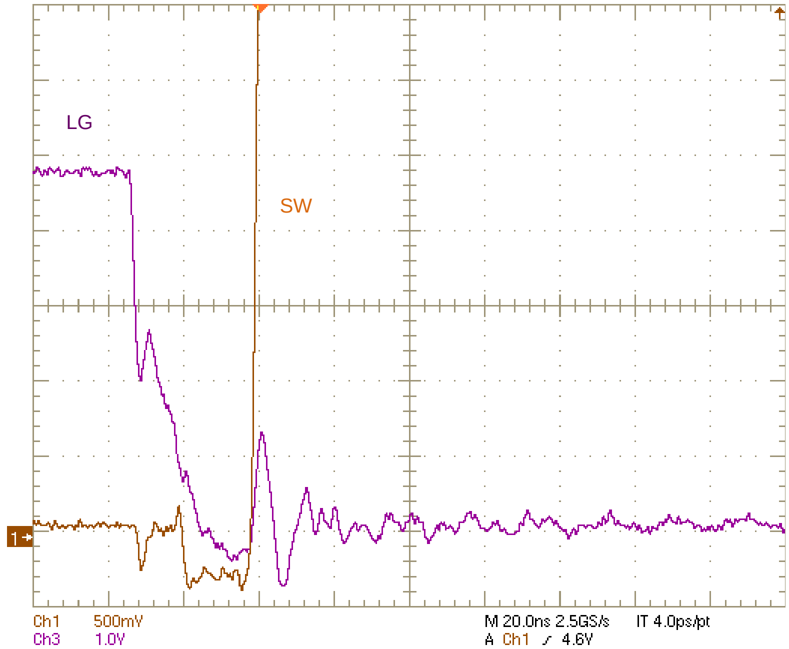

Figure 17. Deadtime Prior To High-side MOSFET Turn-on; V_{IN} = 12 V, V_{OUT} = 1.8 V, 120-mΩ Load

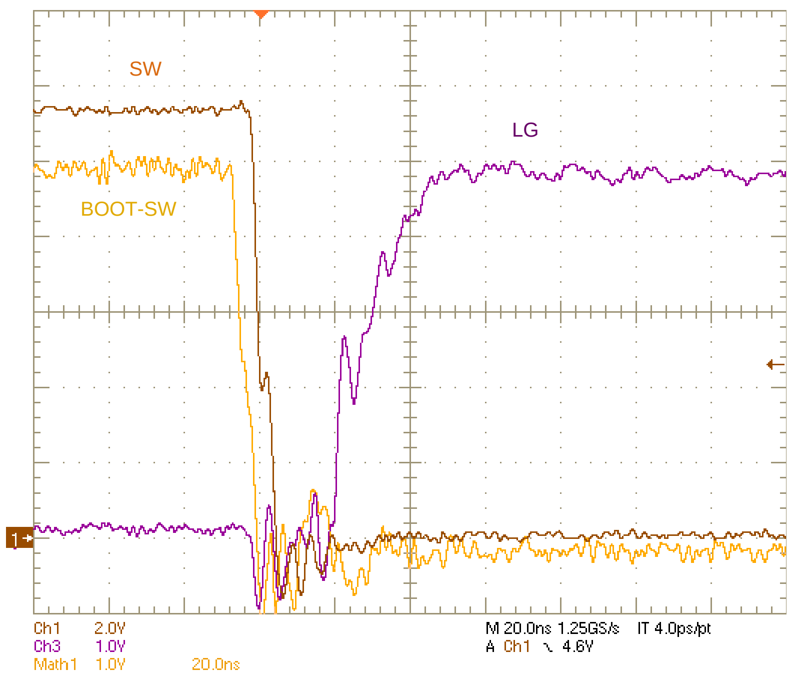

Figure 18. Deadtime Prior To High-side MOSFET Turn-off; V_{IN} = 12 V, V_{OUT} = 1.8 V, 120-mΩ Load

9 EVM DOCUMENTATION

9.1 Schematics

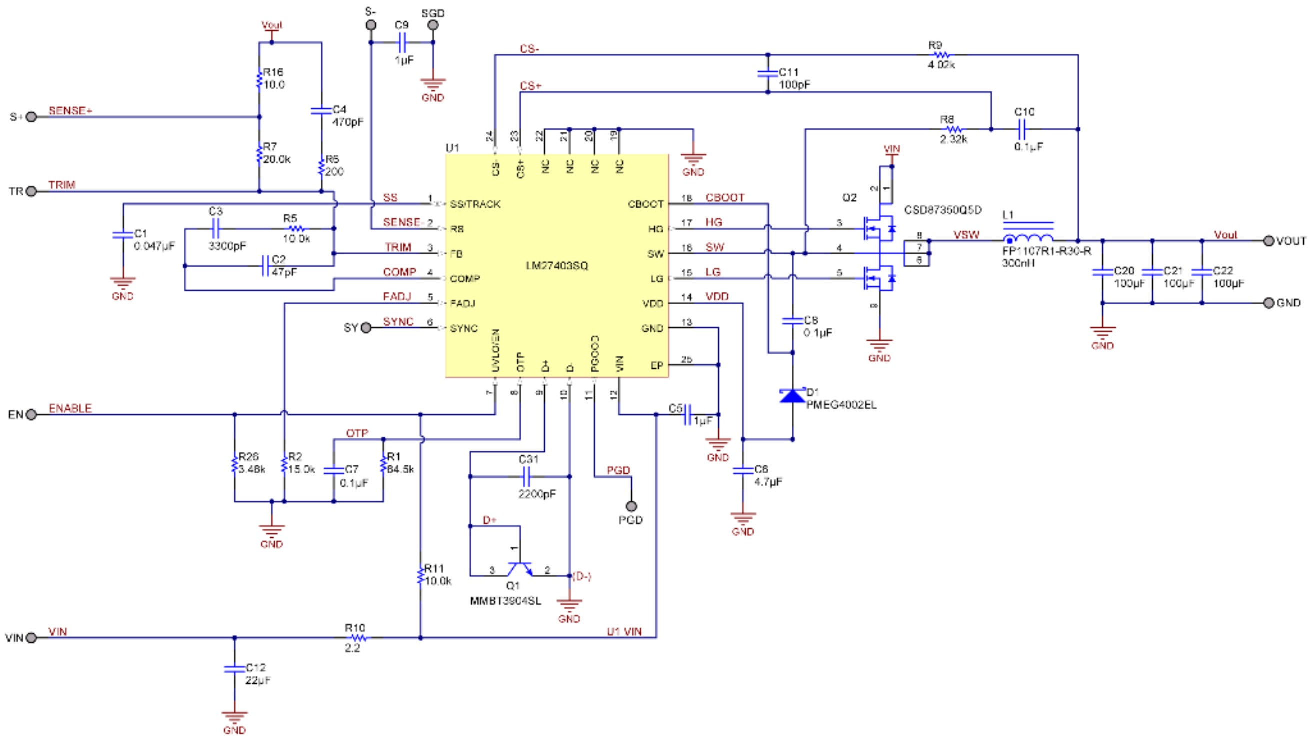

Figure 19. Module Schematic

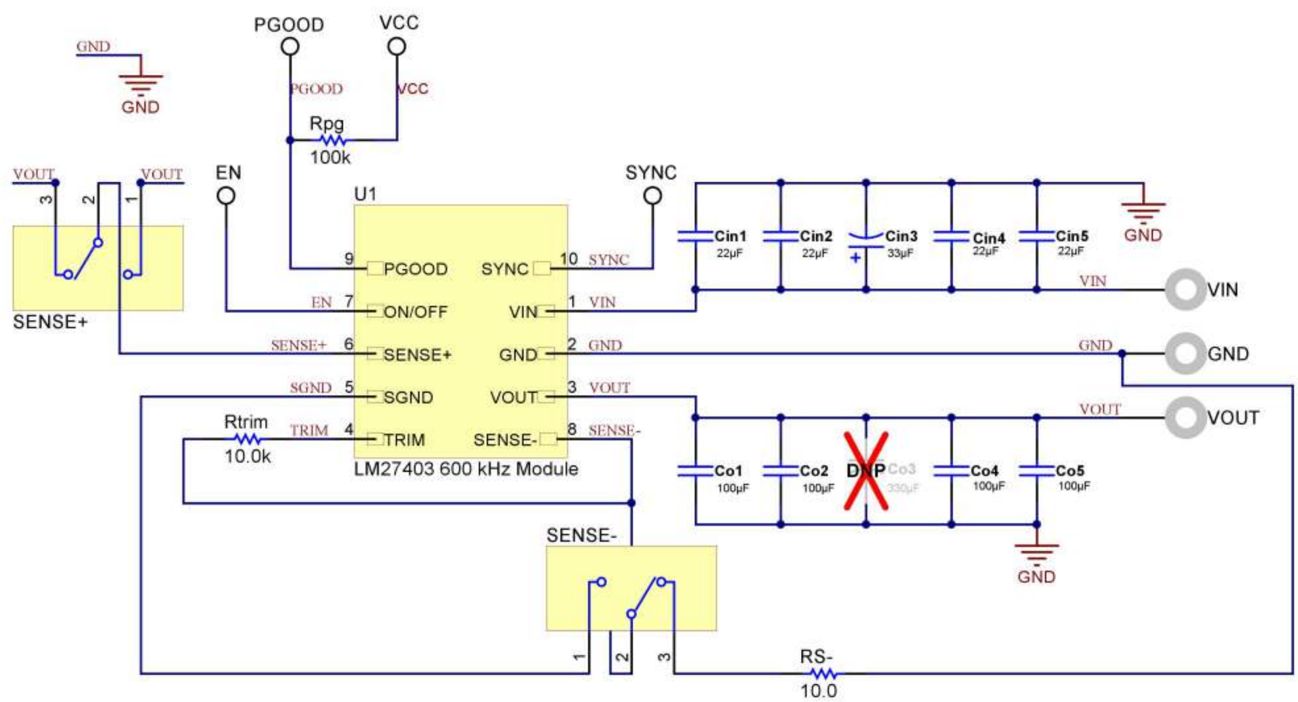

Figure 20. Motherboard Schematic

9.2 Module PCB Layout

Figure 21 through Figure 24 show the LM27403EVM-POL600 4-layer module PCB (2-oz copper). This is a single-sided design with bottom-side SMT pads for power and signal connections to the host PCB.

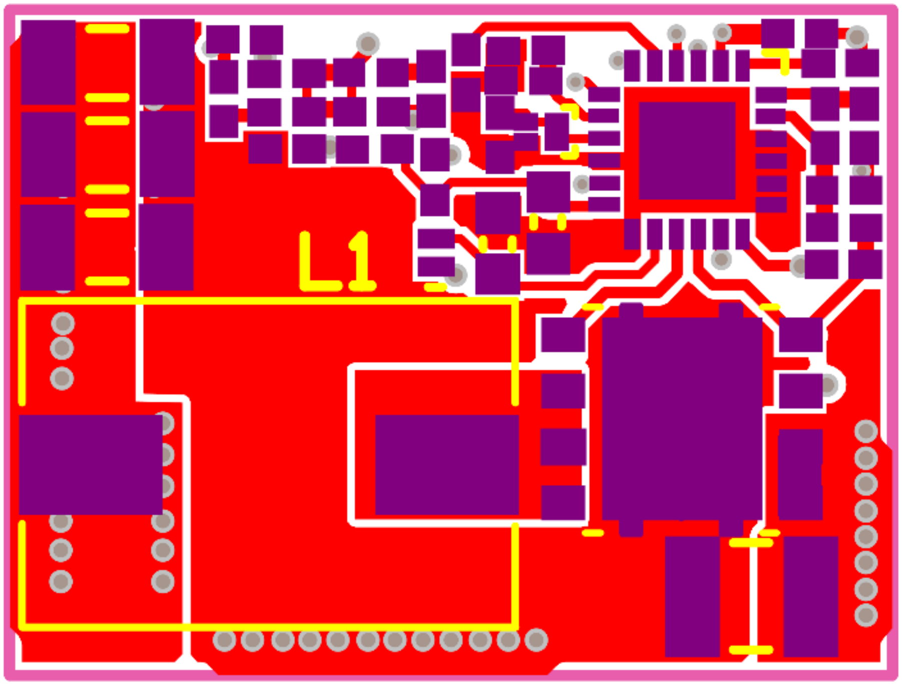

Figure 21. Top Copper and Paste Layers

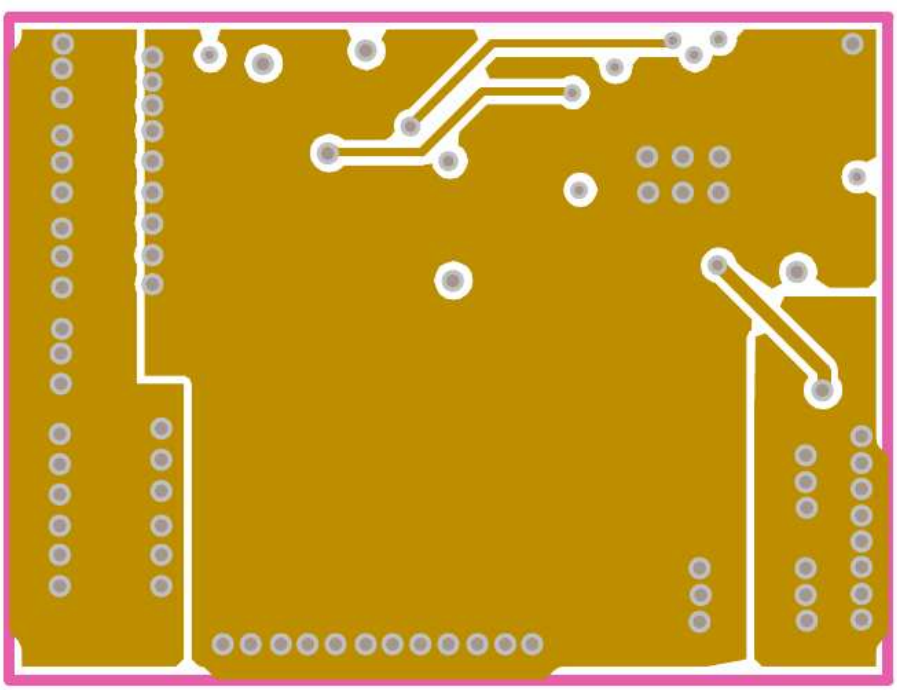

Figure 22. Internal Layer 2 (Top view)

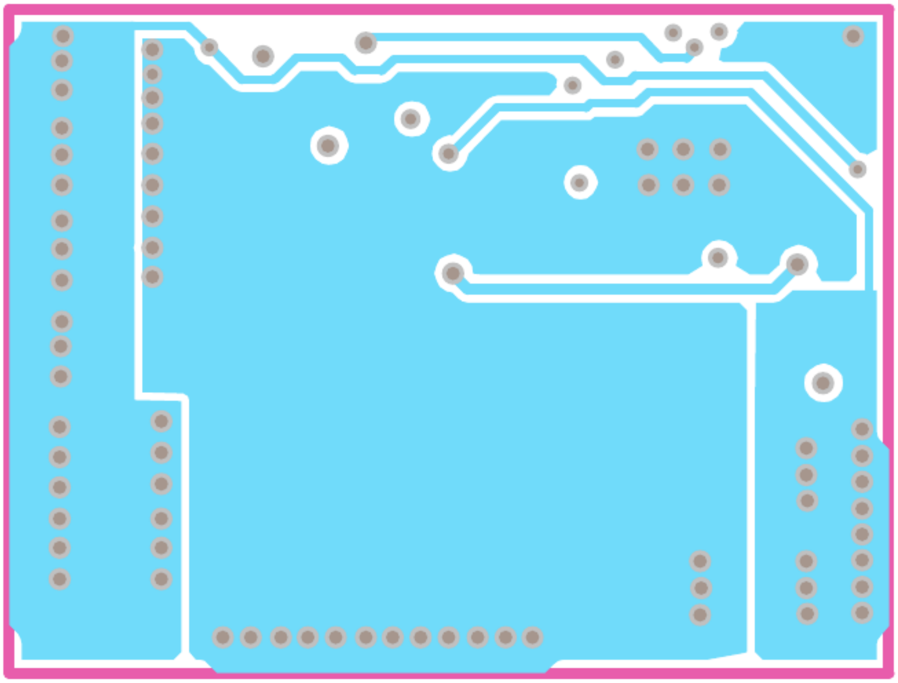

Figure 23. Internal Layer 3 (Top view)

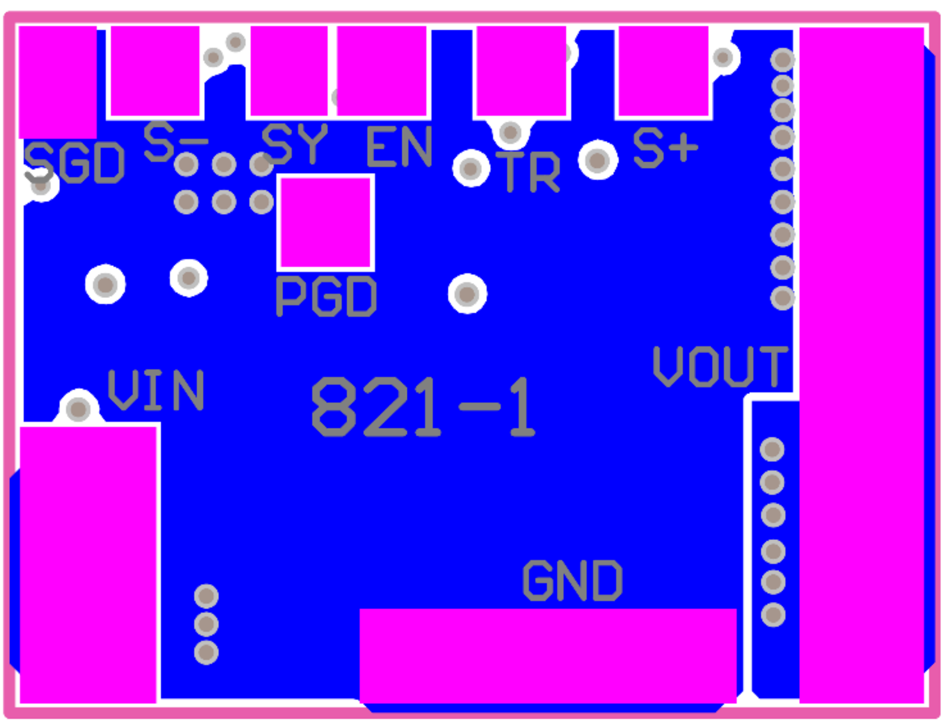

Figure 24. Bottom Copper and Paste Layers (Bottom view)

9.3 Motherboard PCB Layout

Figure 25 through Figure 28 show the motherboard PCB (2-oz copper).

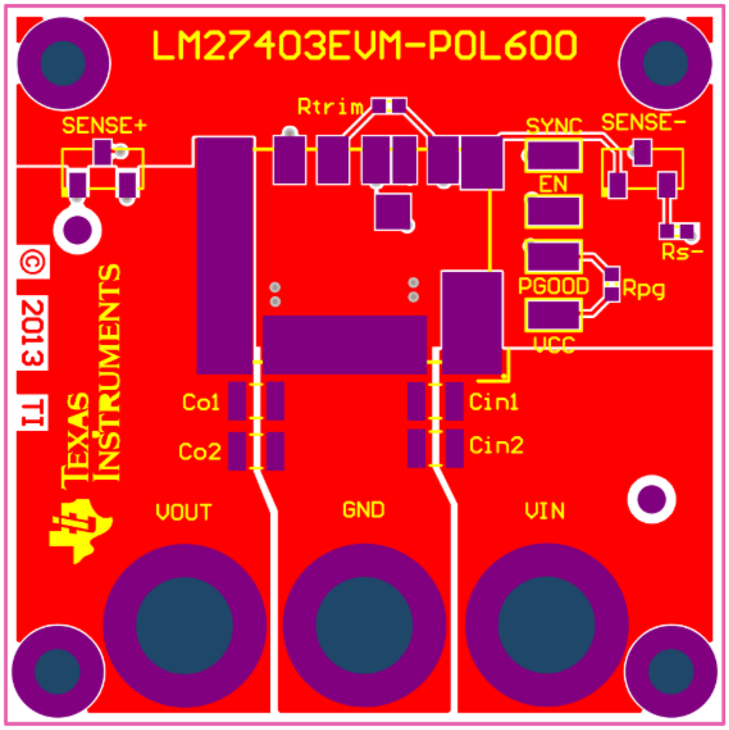

Figure 25. Top Copper and Paste Layers

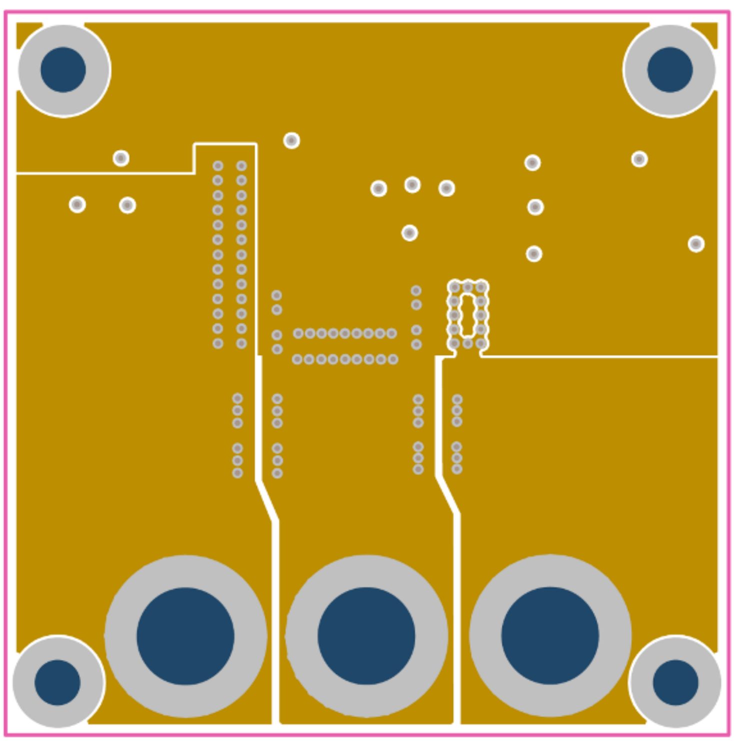

Figure 26. Internal Layer 2 (Top view)

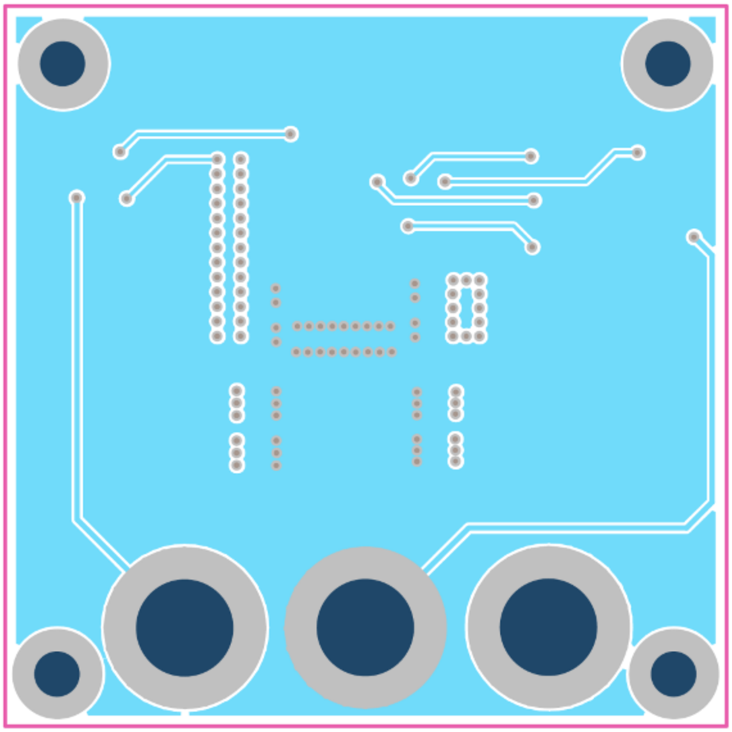

Figure 27. Internal Layer 3 (Top view)

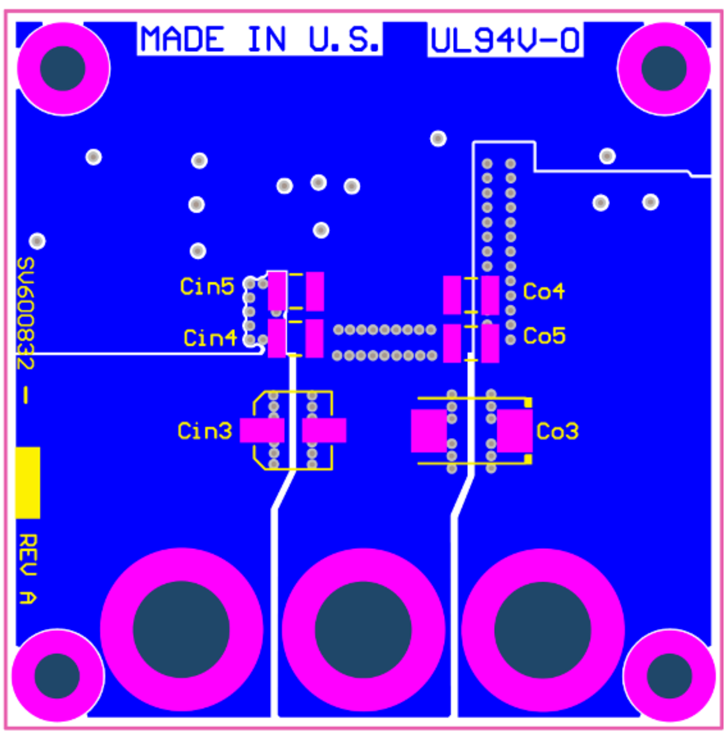

Figure 28. Bottom Copper and Paste Layers (Bottom view)

9.4 Assembly Drawings

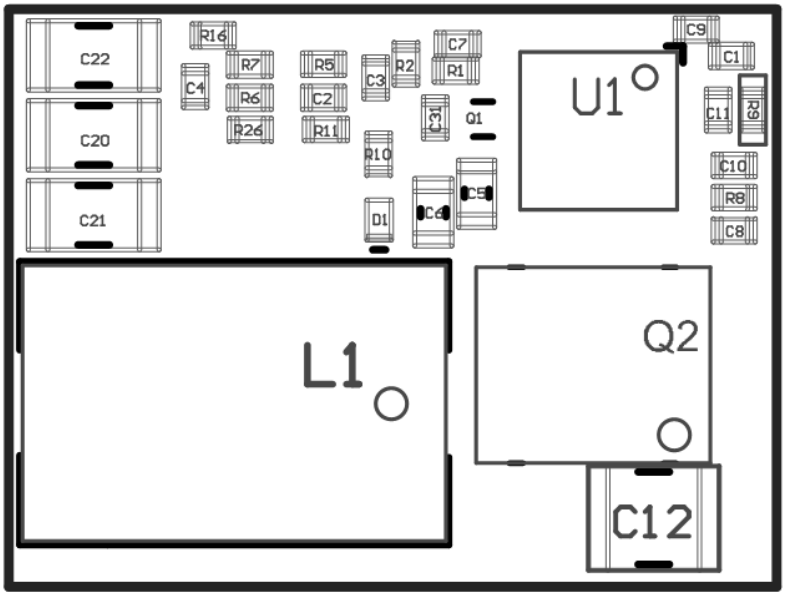

Figure 29. Module Assembly Drawing

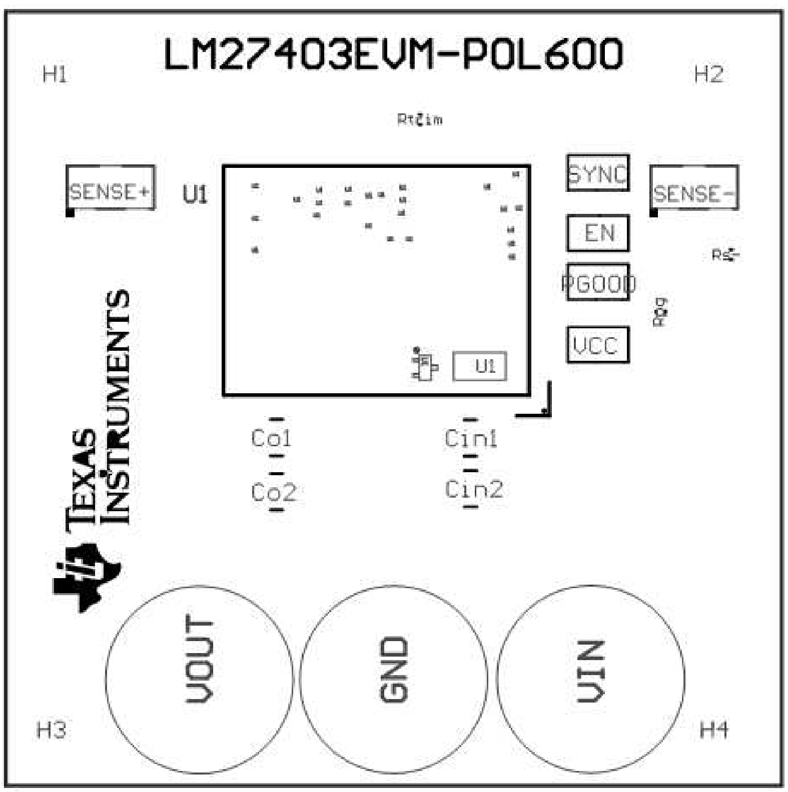

Figure 30. Motherboard Assembly Drawing

9.5 Bill of Materials

Table 4. Bill of Materials – Module

Count	Ref Des	Description	Part Number	Manufacturer
1	C1	Capacitor, Ceramic, 47nF, 25V, X7R, 10%, 0402	Generic	Multi-sourced
1	C2	Capacitor, Ceramic, 47pF, 50V, C0G/NPO, 5%, 0402	Generic	Multi-sourced
1	C3	Capacitor, Ceramic, 3300pF, 50V, X7R, 10%, 0402	Generic	Multi-sourced
1	C4	Capacitor, Ceramic, 470pF, 50V, C0G/NPO, 5%, 0402	Generic	Multi-sourced
1	C5	Capacitor, Ceramic, 1µF, 25V, X5R, 10%, 0603	Generic	Multi-sourced
1	C6	Capacitor, Ceramic, 4.7µF, 10V, X5R, 10%, 0603	C0603C475K8PACTU	Kemet
3	C7, C8, C10	Capacitor, Ceramic, 0.1µF, 50V, X7R, 10%, 0402	Generic	Multi-sourced
1	C9	Capacitor, Ceramic, 1µF, 10V, X5R, 20%, 0402	Generic	Multi-sourced
1	C11	Capacitor, Ceramic, 100pF, 50V, X7R, 10%, 0402	Generic	Multi-sourced
1	C12	Capacitor, Ceramic, 22µF, 25V, X5R, 10%, 1210	12103D226KAT2A	AVX
3	C20, C21, C22	Capacitor, Ceramic, 100µF, 6.3V, X5R, 20%, 1206	C1206C107M9PACTU	Kemet
1	C31	Capacitor, Ceramic, 2200pF, 50V, X7R, 10%, 0402	Generic	Multi-sourced
1	D1	Diode Schottky, 40V, 200mA, SOD-882	PMEG4002EL	NXP
1	L1	Inductor, 300nH, 0.29mΩ DCR, 34A Isat	FP1107R1-R30-R	Coiltronics
			744308025	Würth Electronik
			SLC1175-301MEC	Coilcraft
			PCDC1107-R30EMO	Cyntec
1	PCB	PCB, FR4, 4 layer, 20 mm x 15 mm	PCB1	Multi-sourced
1	Q1	Transistor, NPN, 40V, 0.2A, SOT-923	MMBT3904LP	Diodes Inc.
1	Q2	Synchronous Buck NexFET™ Power Block, N-Channel, 30V	CSD87350Q5D	TI
1	R1	Resistor, Chip, 84.5kΩ, 1/16W, 1%, 0402	Generic	Multi-sourced
1	R2	Resistor, Chip, 15kΩ, 1/16W, 1%, 0402	Generic	Multi-sourced
2	R5, R11	Resistor, Chip, 10kΩ, 1/16W, 1%, 0402	Generic	Multi-sourced
1	R6	Resistor, Chip, 200Ω, 1/16W, 1%, 0402	Generic	Multi-sourced
1	R7	Resistor, Chip, 20kΩ, 1/16W, 1%, 0402	Generic	Multi-sourced
1	R8	Resistor, Chip, 2.32kΩ, 1/16W, 1%, 0402	Generic	Multi-sourced
1	R9	Resistor, Chip, 4.02kΩ, 1/16W, 1%, 0402	Generic	Multi-sourced
1	R10	Resistor, Chip, 2.2Ω, 1/16W, 5%, 0402	Generic	Multi-sourced
1	R16	Resistor, Chip, 10Ω, 1/16W, 1%, 0402	Generic	Multi-sourced
1	R26	Resistor, Chip, 3.48kΩ, 1/16W, 1%, 0402	Generic	Multi-sourced
1	U1	IC, Synchronous Buck Controller with DCR Current Sensing and Thermal Compensation, 4-mm x 4-mm WQFN-24 PowerPAD™ package	LM27403SQ	TI

Table 5. Bill of Materials – Motherboard

Count	Ref Des	Description	Part Number	Manufacturer
4	Cin1, Cin2, Cin4, Cin5	Capacitor, Ceramic, 22µF, 25V, X5R, 10%, 1210	12103D226KAT2A	AVX
1	Cin3	Capacitor, Oscon, 33µF, 25V, 20%, 80mΩ, SMD	EEHZA1E330R	Panasonic
4	Co1, Co2, Co4, Co5	Capacitor, Ceramic, 100µF, 6.3V, X5R, 20%, 1210	GRM32ER60J107ME20L	Murata
4	H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B&F Fastener Supply
4	H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone
1	MOD1	POL Module, 20 mm x 15 mm	-	-
1	RS-	Resistor, Chip, 10Ω, 1/10W, 1%, 0603	Generic	Multi-sourced
1	Rpg	Resistor, Chip, 100kΩ, 1/10W, 1%, 0603	Generic	Multi-sourced
1	Rtrim	Resistor, Chip, 10kΩ, 1/10W, 1%, 0603	Generic	Multi-sourced
1	PCB	PCB, FR4, 6 layer, 50 mm x 50 mm	PCB2	Multi-sourced
3	VIN, VOUT, GND	Banana Jack Power Terminal	108-0740-001	Emerson
4	VCC, EN, PGOOD, SYNC	Test Point, SMT, Miniature	5015	Keystone
2	SENSE+, SENSE-	Switch, slide, SPDT, 100mA, SMT	CAS-210TA	Copal Electronics

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User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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