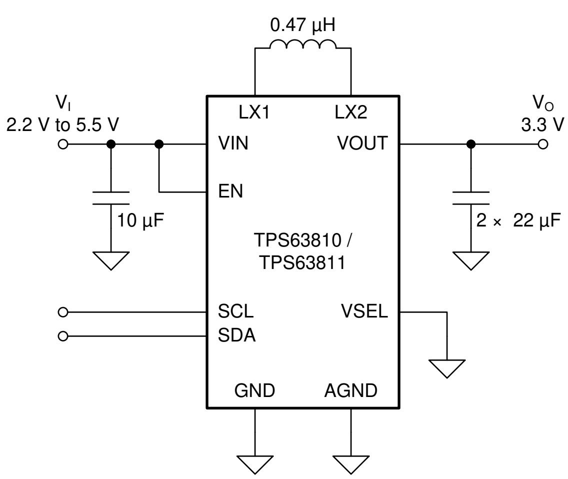
TPS63810 and TPS63811 – 2.5-A Buck-Boost Converters with I²C Interface

1 Features

- Input voltage range: 2.2 V to 5.5 V
- Output voltage range: 1.8 V to 5.2 V
  - I²C-configurable during operation and shutdown
  - VSEL pin to toggle between two output voltage presets
- Output current
  - Up to 2.5 A for $V_I \geq 2.5$ V, $V_O = 3.3$ V
  - Up to 2.5 A for $V_I \geq 2.8$ V, $V_O = 3.5$ V
- High efficiency over entire load range
  - Low 13-µA operating quiescent current
  - Automatic power save mode and forced PWM mode (I²C-configurable)
- Peak current mode buck-boost architecture
  - Defined transitions between buck, buck-boost and boost operation
  - Forward and reverse current operation
  - Start-up into pre-biased outputs
- Safety and robust operation features
  - Integrated soft start
  - Overtemperature and overvoltage protection
  - True load disconnect during shutdown
  - Forward and backward current limit
- Two device options:
  - TPS63810: Pre-programmed output voltages (3.3 V, 3.45 V)
  - TPS63811: Program output voltages prior to start-up
- Solution size of < 20 mm² with only four external components

Simplified Schematic



2 Applications

- System pre-regulator (smartphone, tablet, tracking and telematics, EPOS, TWS earphones, medical hearing aids)
- Point-of-load regulation (Time-of-Flight camera sensors, port/cable adapter and dongle)
- Thermoelectric device supply (TEC, optical modules)
- Broadband network radio or SoC supply (IoT, home automation, EPOS)

3 Description

The TPS63810 and TPS63811 are high efficiency, high output current buck-boost converters fully programmable through I²C. Depending on the input voltage, they automatically operate in boost, buck or in a novel 4-cycle buck-boost mode when the input voltage is approximately equal to the output voltage.

The transitions between modes happen at defined thresholds and avoid unwanted toggling within the modes to reduce output voltage ripple.

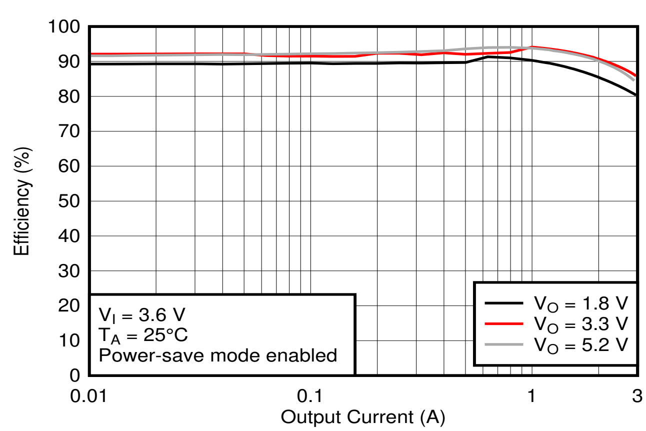
Two registers, accessible through I²C, set the output voltage, and a VSEL pin selects which output voltage register is active. Thus the devices can support dynamic voltage scaling. If the output voltage register is changed during operation or the VSEL pin is toggled, the device transits in a defined, programmable ramp-rate.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS63810	DSBGA (15)	2.3 mm × 1.4 mm
TPS63811		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Efficiency versus Output Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2019) to Revision C **Page**

- Changed the unit in Figure 2 7
- Changed "Output Disabled (Hi-Z)" to "Output Discharge Active" in Table 2 13
- Changed "EN pin is low" to "EN pin is low or the ENABLE bit is set to zero" in the *Output Discharge* section 17
- Changed "TPS63810" to "Start-up value for TPS63810" in bit 5 of Table 3 22

Changes from Revision A (October 2019) to Revision B **Page**

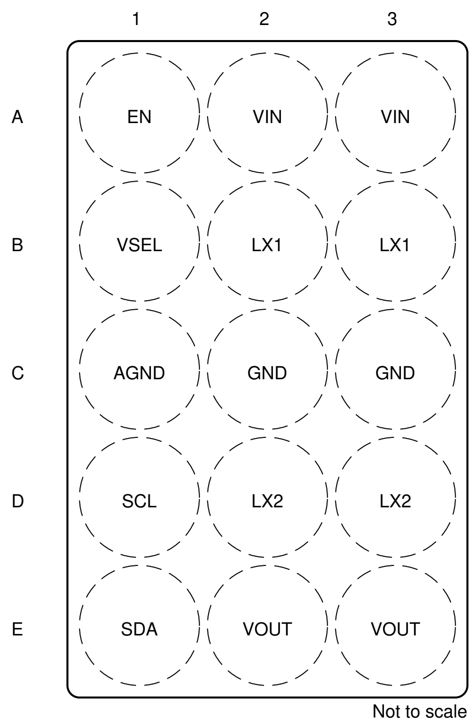
- Changed product status from Advance Information to Production Data 1

5 Device Comparison Table

PART NUMBER	OUTPUT START-UP STATE	OUTPUT VOLTAGE
TPS63810	Enabled	VSEL = Low: 3.3 V VSEL = High: 3.45 V
TPS63811	Disabled	Programmable at start-up

6 Pin Configuration and Functions

YFF Package
15-Ball DSBGA
Top View



BGA Package (YFF) Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	EN	I	Device enable. A high logic level on this pin enables the device; a low logic level on this pin disables the device.
A2	VIN	—	Supply voltage for power stage
A3	VIN	—	Supply voltage for power stage
B1	VSEL	I	This pin selects which VOUT register is active. When a low logic level is applied to this pin, the VOUT1 register sets the output voltage. When a high logic level is applied to this pin, the VOUT2 register sets the output voltage.
B2	LX1	—	Inductor connection
B3	LX1	—	Inductor connection
C1	AGND	—	Analog ground
C2	GND	—	Power ground
C3	GND	—	Power ground
D1	SCL	I/O	I^2C serial interface clock. Pull this pin up to the I^2C bus voltage with a resistor or a current source.
D2	LX2	—	Inductor connection
D3	LX2	—	Inductor connection
E1	SDA	I/O	I^2C serial interface data. Pull this pin up to the I^2C bus voltage with a resistor or a current source.
E2	VOUT	—	Converter output
E3	VOUT	—	Converter output

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage (VIN, LX1, LX2, VOUT, SCL, SDA, EN, VSEL)(2)	–0.3	6	V
	Input voltage for less than 10 ns (LX1, LX2)(2)	–3	9	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage		2.2		5.5	V
V_O	Output voltage	Low range	1.8		4.975	V
		High range	2.025		5.2	
V_{IH}	High-level input voltage	SCL, SDA, VSEL	1.3		V_I	V
V_{IL}	Low-level input voltage	SCL, SDA, VSEL	0		0.3	V
$V_{(EN)}$	Input voltage	EN	0		V_I	V
I_O	Output current(1)	V_O = 3.3 V, $V_I \geq$ 2.5 V			2.5	A
		V_O = 3.5 V, $V_I \geq$ 2.5 V			2	
		V_O = 3.5 V, $V_I \geq$ 2.8 V			2.5	
		V_O = 3.3 V, $V_I \geq$ 3 V			3	
C_I	Input capacitance(2)		5			µF
C_O	Output capacitance(2)		13	16		µF
L	Inductance		390	470	560	nH
T_A	Operating free-air temperature range		–40		85	°C
T_J	Operating junction temperature range		–40		125	°C

(1) The device can sustain the maximum recommended output current only for short durations before its junction temperature gets too hot. Users must verify that the thermal performance of the end application can support the maximum output current.
(2) Effective capacitance after DC bias effects have been considered.

7.4 Thermal Information

THERMAL METRIC[1]		TPS63810, TPS63811 YFF (DSBGA) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.6 V, V_O = 3.3 V and T_J = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY							
$I_{Q;VIN}$	Supply current into VIN		V_I = 3.6 V, V_O = 3.3 V, $V_{(EN)}$ = 3.6 V, not switching, T_J = 25°C		13		µA
	Supply current into VIN		V_I = 3.6 V, V_O = 0 V, $V_{(EN)}$ = 3.6 V, Output disabled with ENABLE bit in Control Register T_J = 25°C		15		µA
I_{SD}	Shutdown current into VIN		V_I = 3.6 V, V_O = 0 V, $V_{(EN)}$ = 0 V T_J = 25°C		0.35		µA
V_{IT+}	Positive-going UVLO threshold voltage			2	2.1	2.2	V
V_{hys}	UVLO threshold voltage hysteresis				200		mV
I/O SIGNALS							
V_{IT+}	Positive-going input threshold voltage	SCL, SDA, VSEL				1.2	V
		EN		1.07	1.1	1.13	
V_{IT-}	Negative-going input threshold voltage	SCL, SDA, VSEL		0.4			V
		EN		0.97	1	1.03	
V_{hys}	Hysteresis voltage	EN		40			mV
I_{IH}	High-level input current	SCL, SDA, VSEL	$V_{(SCL)}$ = $V_{(SDA)}$ = $V_{(VSEL)}$ = 1.8 V, no pullup resistor		±0.01	±0.1	µA
I_{IL}	Low-level input current	SCL, SDA, VSEL	$V_{(SCL)}$ = $V_{(SDA)}$ = $V_{(VSEL)}$ = 0 V, no pullup resistor		±0.01	±0.1	µA
I_{OL}	Low-level output current	SCL, SDA	V_{OL} = 0.4 V	20			mA
I_{IB}	Input bias current	EN	$V_{(EN)}$ = 0 V to 5.5 V		±0.01	±0.1	µA
POWER STAGE							
V_O	Output voltage range		Low range	1.8		4.975	V
			High range	2.025		5.2	
	Output voltage accuracy		PWM operation	–1.5		1.5	%
			PSM operation	–1.5		3.5	
	Default output voltage (RANGE = 0)		VSEL = low		3.3		V
			VSEL = high		3.45		
	Switch current limit		V_I = 2.9 V, V_O = 3.6 V, boost operation, output sourcing current	5.2		6.5	A
			V_I = 4.1 V, V_O = 3.3 V, buck operation, output sourcing current	3.8	4.3	5.2	
			V_I = 5 V, V_O = 3.3 V, reverse-boost operation, output sinking current	–1.3		–0.35	
$I_{T–(PSM)}$	PSM entry threshold (peak) current		V_I = 4.2 V; V_O = 3.3 V		0.85		A

Electrical Characteristics (continued)

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at V_I = 3.6 V, V_O = 3.3 V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output discharge current	V_I = 3.6 V, V_O ≥ 0.8 V	50			mA
$V_{T+(PG)}$	Positive-going power-good threshold voltage			95		%
$V_{T-(PG)}$	Negative-going power-good threshold voltage			90		%
	Positive-going input overvoltage threshold	Reverse current operation		5.7		V
I²C INTERFACE						
	7-Bit slave address			75h		
THERMAL SHUTDOWN						
	Thermal shutdown threshold temperature	T_J rising		150		°C
	Thermal shutdown hysteresis			20		°C

7.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	
		Fast mode plus	0		1000	
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
$t_{SU;STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{HD;STA}$	Hold time (repeated) START condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{SU;DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			
		Fast mode plus	50			
$t_{HD;DAT}$	Data hold time	Standard mode	0			µs
		Fast mode	0			
		Fast mode plus	0			
t_r	Rise time of both SDA and SCL signals	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus			120	
t_f	Fall time of both SDA and SCL signals	Standard mode			300	ns
		Fast mode	$20 \times V_{DD}/5.5$		300	
		Fast mode plus	$20 \times V_{DD}/5.5$		120	
$t_{su;STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			

Timing Requirements (continued)

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

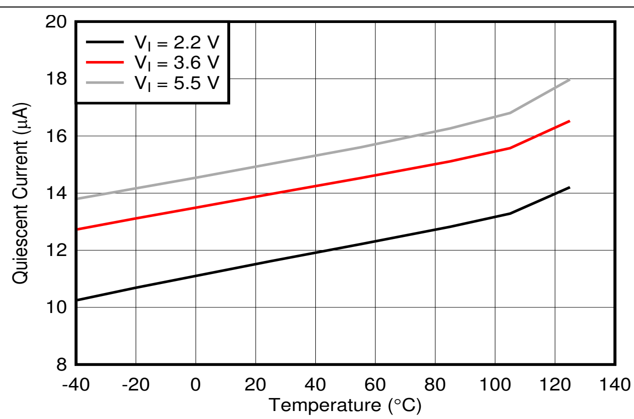
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{VD;DAT}$	Data valid time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus			0.45	
$t_{VD;ACK}$	Data valid acknowledge time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus			0.45	
C_b	Capacitive load for each bus line	Standard mode			400	
		Fast mode			400	
		Fast mode plus			550	
$t_{w(VSEL)}$	VSEL pulse duration	VSEL = high or low	5			µs

7.7 Switching Characteristics

Over operating junction temperature range and recommended input voltage range (unless otherwise noted). Typical values are at V_I = 3.6 V, V_O = 3.3 V, and T_J = 25°C (unless otherwise noted).

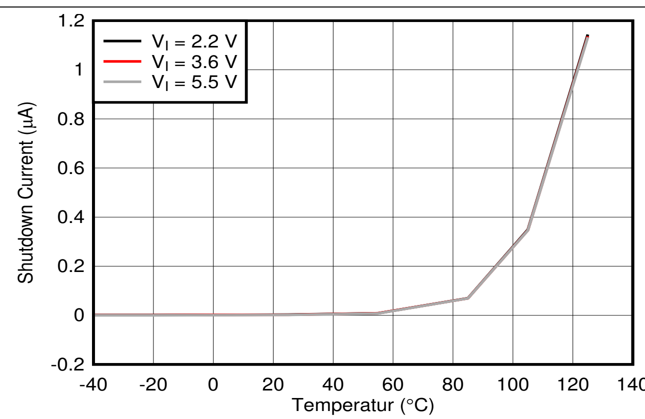
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(EN)}$	Delay between a rising edge on the EN pin and the start of the output voltage ramp	T_J = 25°C, V_I = 3.6 V		229	440	µs
$t_{d(PG)}$	Power-good delay	V_O falling		50		µs
SR	Slew rate of internal ramp during dynamic voltage scaling	SLEW = 00b, forced-PWM operation		±1		V/ms
		SLEW = 01b, forced-PWM operation		±2.5		
		SLEW = 10b, forced-PWM operation		±5		
		SLEW = 11b, forced-PWM operation		±10		
f_{SW}	Inductor Switching Frequency, Boost Mode	V_I = 2.3 V, V_O = 3.3 V, no Load, PWM operation		2.6		MHz
	Inductor Switching Frequency, Buck-Boost Mode	V_I = 3.3 V, V_O = 3.3 V, no Load, PWM operation		1.6		MHz
	Inductor Switching Frequency, Buck Mode	V_I = 4.3 V, V_O = 3.3 V, no Load, PWM operation		2.0		MHz
$t_{d(VSEL)}$	Delay between rising edge of VSEL and start of DVS ramp	Measured from rising edge of VSEL to start of ramp.			5	µs

7.8 Typical Characteristics



MODE = LOW V_O = 3.3 V I_O = 0 mA, not switching

Figure 1. Quiescent Current versus Temperature



EN = LOW

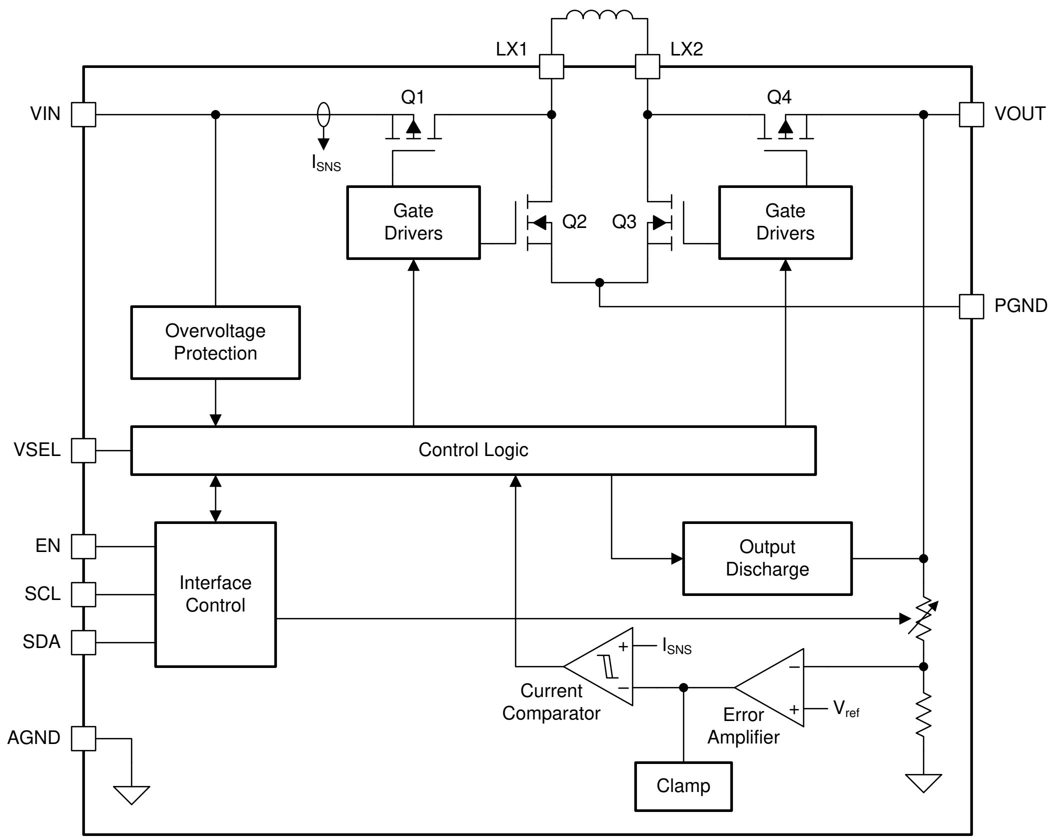
Figure 2. Shutdown Current versus Temperature

8 Detailed Description

8.1 Overview

The TPS63810 and TPS63811 devices are high-efficiency buck-boost converters. Each device uses four switches to maintain synchronous power conversion under all operating conditions, so that the device achieves high efficiency power conversion over a wide range of input voltages and output currents. The device automatically switches between buck, boost, and buck-boost operation as required by the operating conditions. The device operates as a true buck converter when $V_I > V_O$ and as a true boost converter when $V_I < V_O$. When $V_I \approx V_O$, the device operates in a 4-cycle buck-boost mode. The RMS current through the switches and the inductor is thus kept to a minimum, minimizing switching and conduction losses. Controlling the switches this way lets the converter achieve high efficiency over the whole input voltage range.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Control Scheme

The device automatically selects the best switching scheme for the operating conditions. To make sure of stable operation, the selection logic includes hysteresis (see Figure 3).

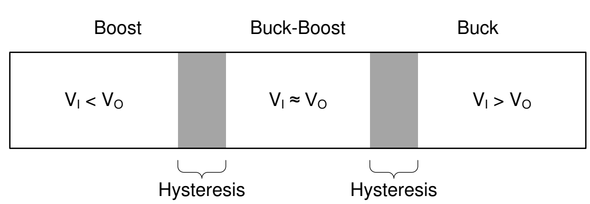


Figure 3. Switching Scheme Selection

Feature Description (continued)

8.3.1.1 Buck Operation

When $V_I > V_O$, the device switches like a buck converter:

- Q1 is the switch.
- Q2 is the rectifier.
- Q3 is permanently off.
- Q4 is permanently on.

See Figure 4. During buck operation, one switching cycle comprises two phases: on–off.

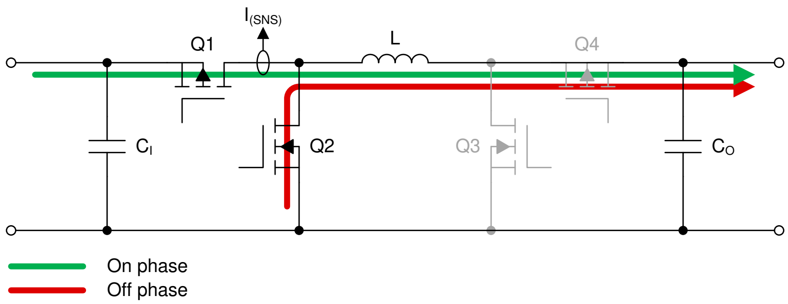


Figure 4. Buck Switch Configuration

8.3.1.2 Boost Operation

When $V_I < V_O$, the device switches like a boost converter:

- Q1 is permanently on.
- Q2 is permanently off.
- Q3 is the switch.
- Q4 is the rectifier.

See Figure 5. During boost operation, one switching cycle comprises two phases: on–off.

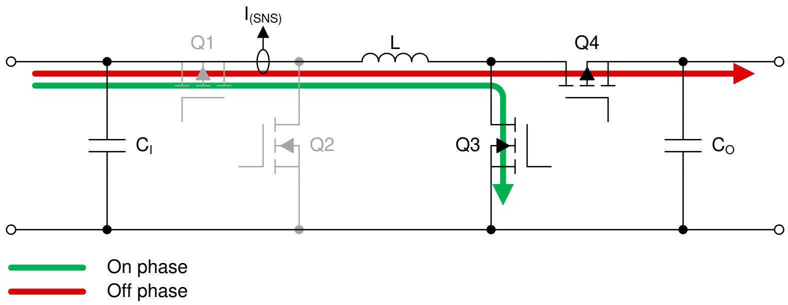


Figure 5. Boost Switch Configuration

8.3.1.3 Buck-Boost Operation

When $V_I \approx V_O$, all four transistors switch continuously (see Figure 6). During buck-boost operation, one switching cycle comprises four phases: on–commutate–off–commutate.

Feature Description (continued)

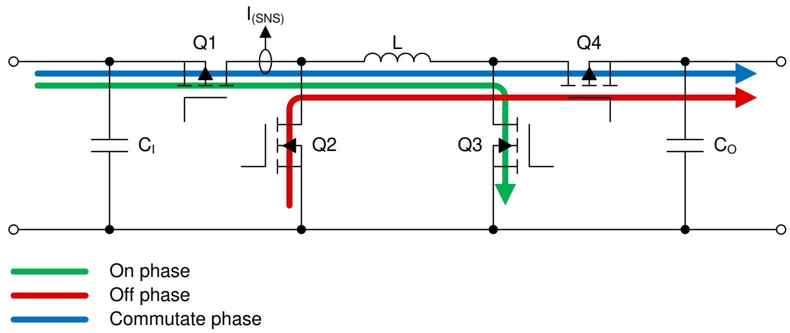


Figure 6. Buck-Boost Switch Configuration

8.3.2 Control Scheme

The device uses a constant off-time, peak-current-mode control scheme where an outer voltage control loop generates the demand signal for an inner current control loop. During the on-time, the inner current control loop monitors the inductor current, and when the inductor current equals the demand signal from the error amplifier, the on-time stops and the next part of the switching cycle starts.

The off-time is a function of V_I and V_O and the operating mode (buck, boost, or buck-boost) of the converter.

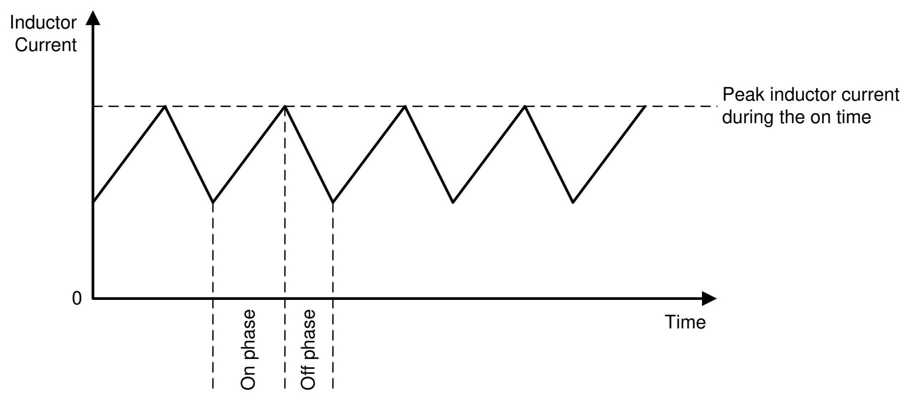


Figure 7. Peak Current Control (Buck and Boost Operation)

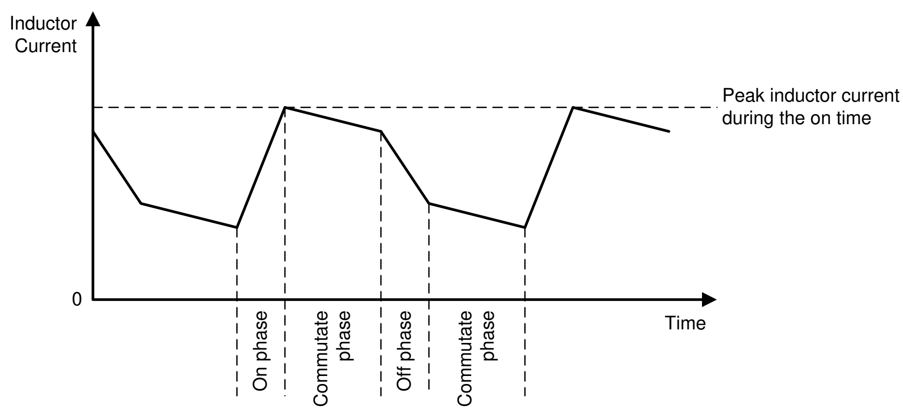


Figure 8. Peak Current Control – Buck-Boost Operation with $V_I < V_O$

Feature Description (continued)

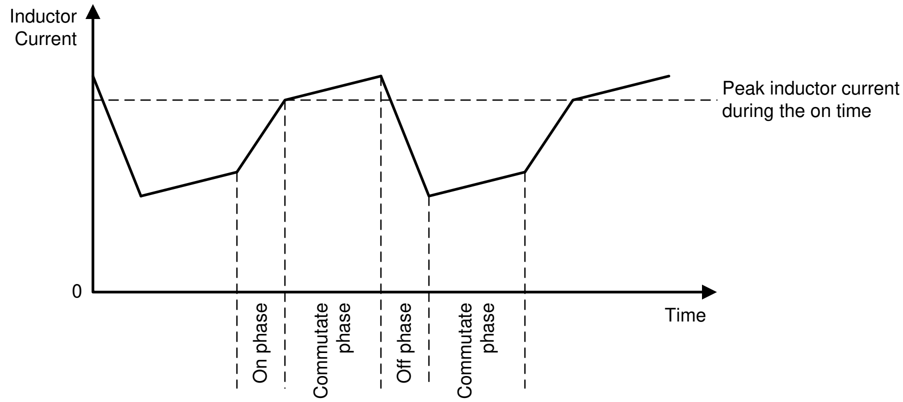


Figure 9. Peak Current Control – Buck-Boost Operation with $V_I > V_O$

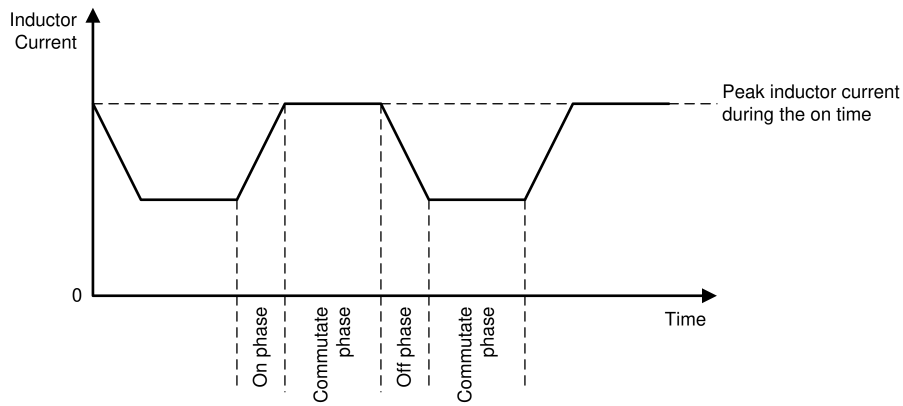


Figure 10. Peak Current Control – Buck-Boost Operation with $V_I = V_O$

During PWM operation, current can flow in the reverse direction (from output to input). In this case, the error amplifier provides a negative peak current target. Note that the average reverse current is greater (more negative) than the peak current (see Figure 11 and Figure 12).

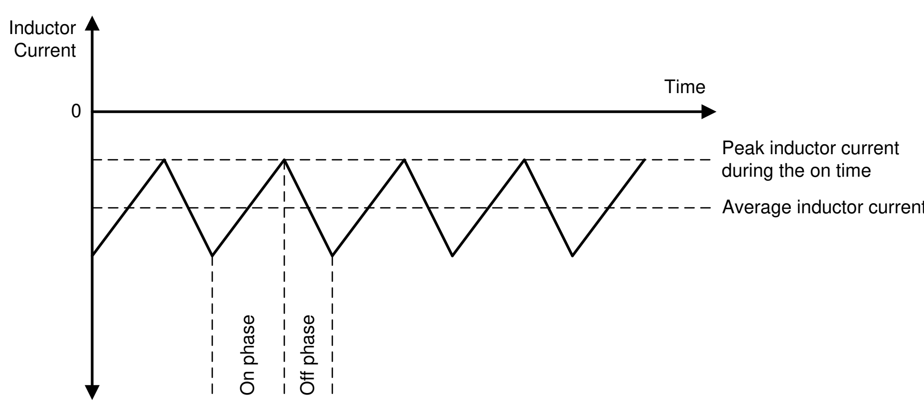


Figure 11. Reverse Peak Current Control – Buck and Boost Operation

Feature Description (continued)

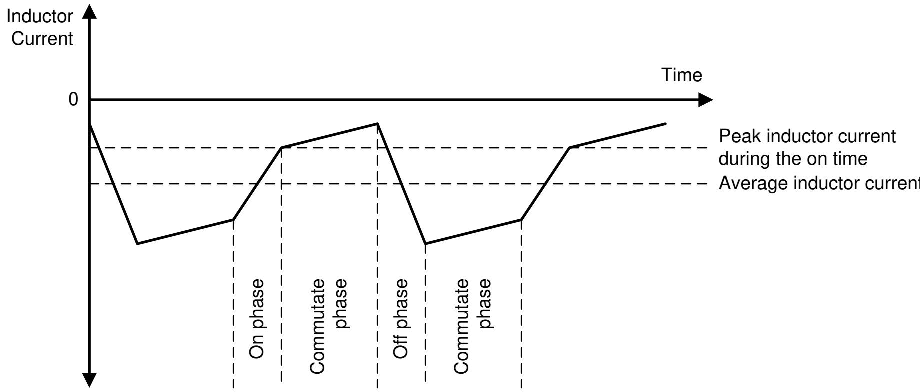


Figure 12. Reverse Peak Current Control – Buck-Boost Operation, with $V_I > V_O$

8.3.3 Power-Save Mode Operation (PSM)

To increase efficiency across a wide range of operating conditions, the device automatically changes from pulse-width modulation (PWM) at medium and high output currents to pulse-frequency modulation (PFM) at low output currents.

- During PWM operation, the device switches continuously and adjusts the duty cycle of each switching cycle to regulate the output voltage.
- During PFM operation, the device switches in bursts of a few switching cycles, separated by periods when the device does not switch (see Figure 13). PFM operation increases efficiency at low output currents because when the device does not switch, there are no switching losses and most of the internal circuitry is disabled, which reduces quiescent power consumption. A comparator with hysteresis compares the output voltage of the error amplifier to a predefined PFM threshold voltage. When the output voltage of the error amplifier is greater than the burst threshold voltage, the device starts switching. When the output voltage of the error amplifier is less than the burst threshold voltage, the device stops switching. This scheme automatically adjusts the frequency and the duration of the switching bursts to regulate the output voltage. During PFM operation, the output voltage ripple can be higher and the transient response is not as good as during PWM operation (see Table 1).

To enable power-save mode, clear the FPWM bit in the Control register to 0.

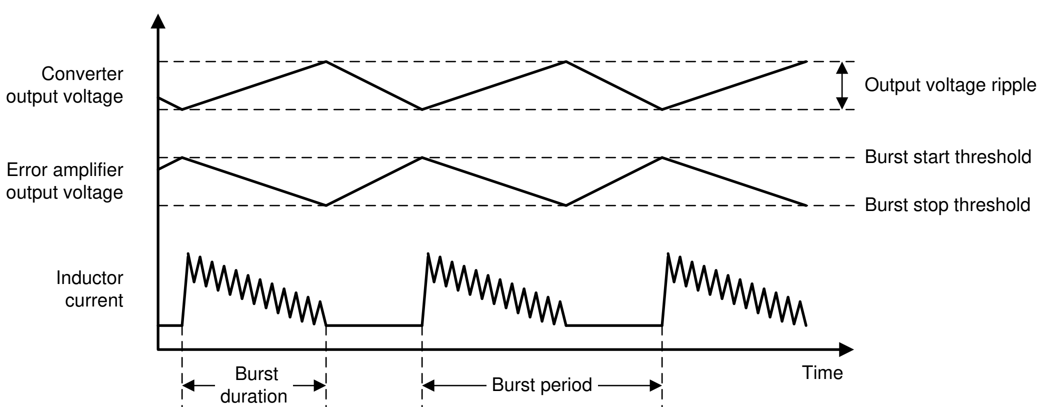


Figure 13. Pulse-Frequency Modulation

Table 1. Forced-PWM versus Power-Save Mode Performance Comparison

PERFORMANCE PARAMETER	BEST OPERATING MODE
Low-power efficiency	Power-Save Mode (PSM)
Medium- and high-power efficiency	No difference
DC Output voltage accuracy	Forced-PWM
Transient response	Forced-PWM
Output voltage ripple	Forced-PWM

8.3.4 Forced-PWM Operation (FPWM)

During forced-PWM operation, the device uses PWM for all operating conditions. Forced-PWM operation has lower output voltage ripple and better transient response than power-save mode operation, but lower efficiency at low output currents (see Table 1).

Note that the device inhibits forced-PWM operation during start-up (that is, until the converter output has reached power-good for the first time).

To enable forced-PWM operation, set the FPWM bit in the Control register to 1.

8.3.5 Ramp-PWM Operation (RPWM)

If Ramp-PWM operation is enabled, the device operates in forced-PWM when it ramps from one output voltage to another during dynamic voltage scaling. This function is useful if you want the device to operate in power-save mode, but you want to make sure that dynamic voltage scaling ramps the output voltage up and down in a controlled way. If the device operates in power-save mode and Ramp-PWM is disabled, the device cannot always control the ramp from a higher output voltage to a lower output voltage, because in power-save mode the device cannot sink current (see Figure 14).

To enable Ramp-PWM operation, set the RAMP bit in the Control register to 1. To disable Ramp-PWM operation, clear the RAMP bit in the Control register to 0.

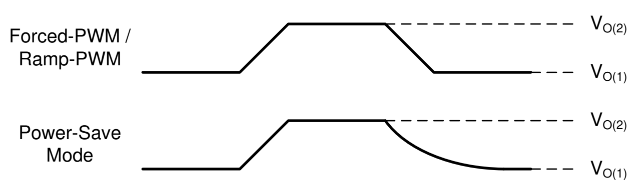


Figure 14. Ramp-PWM Operation

8.3.6 Device Enable (EN)

The EN pin enables and disables the device.

- When the EN pin is high, the device is enabled.
- When the EN pin is low, the device is disabled.

You can also use the ENABLE bit in the Control register to enable and disable the output of the converter (see the *Register Map*).

Table 2. Device Enable Truth Table

ENABLE PIN (EN)	ENABLE BIT	DEVICE STATE	OUTPUT STATE
0	X	Device in Shutdown	Output Discharge Active
1	0	Programming Interface Active	Output Discharge Active
1	1	Device Active	Output Enabled

8.3.7 Undervoltage Lockout (UVLO)

The device has an undervoltage lockout function that disables the device when the supply voltage is too low for correct operation.

8.3.8 Soft Start

To minimize inrush current and output voltage overshoot during start-up, the device has a soft-start function. At turn on, the switch current limit ramps gradually to its maximum value and the device starts up in a controlled way. The gradual increase of the current limit generates the smallest inrush current for no-load conditions. It is also possible to start into a high load as long as the load does not exceed the device current limit.

The rise time of the output voltage changes with the application circuit and the operating conditions. The output voltage rise time increases if the following occurs:

- The output capacitance is large.
- The load current is large.
- The device operates in boost mode.

See the *Application and Implementation* section for output voltage rise times in a typical application.

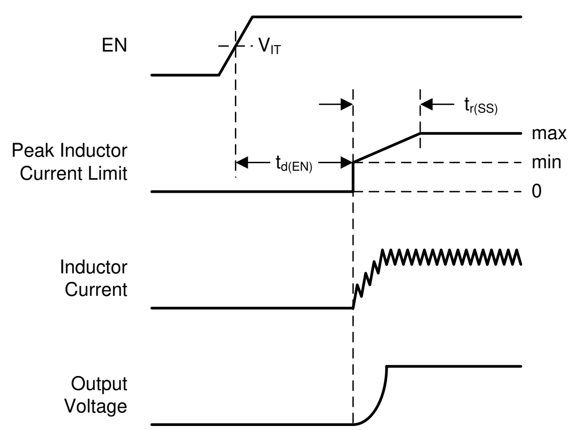


Figure 15. Device Start-Up

8.3.9 Output Voltage Control

The device can generate output voltages from 1.8 V to 5.2 V with a resolution of 25 mV. To set the output voltage, you must first program the RANGE bit in the Control register to select the output voltage range:

- When RANGE = 0, you can program the output voltage from 1.8 V to 4.975 V.
- When RANGE = 1, you can program the output voltage from 2.025 V to 5.2 V.

When you have selected the output voltage range, you can program the VOUT1 register and VOUT2 register to set the output voltage:

- When RANGE = 0, V_O = (VOUT[6:0] × 0.025) + 1.8 V
- When RANGE = 1, V_O = (VOUT[6:0] × 0.025) + 2.025 V

VOUT[6:0] is the 7-bit value in the VOUT1 register or VOUT2 register, whichever is active.

The VSEL pin selects which VOUT register is active:

- When VSEL = low, the VOUT1 register sets the output voltage.
- When VSEL = high, the VOUT2 register sets the output voltage.

NOTE

To prevent output voltage transients, TI recommends that you do not change the output voltage range while the converter is in operation. Instead, clear the ENABLE bit in the Control register to 0 to disable the DC/DC converter before you change the RANGE bit.

8.3.9.1 Dynamic Voltage Scaling

The device has a dynamic voltage scaling (DVS) function which lets you change the output voltage in a controlled way during operation. Figure 16 shows a simplified block diagram of the DVS function. The VSEL pin controls a multiplexer which selects either the VOUT1 register or the VOUT2 register to control the set voltage. The ramp control block detects when the target output voltage is different from the actual output voltage and ramps the output voltage to the target voltage in 25-mV steps. You can use the 2-bit SLEW parameter in the Control register to select one of four slew rates from 0.5 V/ms to 10 V/ms.

The device starts a DVS ramp when you change the logic level on the VSEL pin or program to a new value in the active VOUT register.

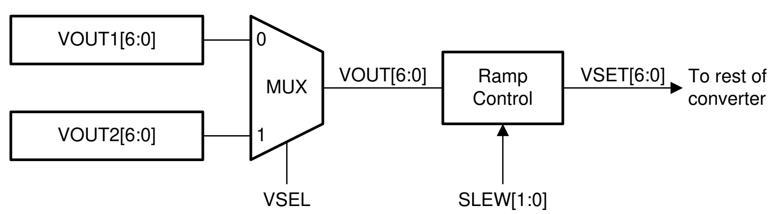
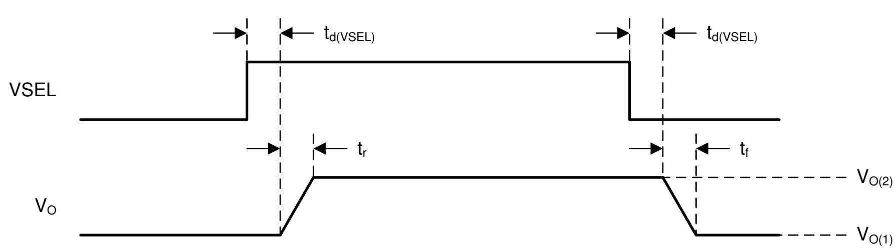


Figure 16. Dynamic Voltage Scaling Block Diagram

Note that if you change the contents of the active VOUT register or change the state of the VSEL pin during start-up (that is, before the end of the soft start), the converter uses the new value immediately and does not ramp gradually to the final value.

Figure 17 shows the timing diagram when you use the VSEL pin to change between the output voltage values in the VOUT1 and VOUT2 registers.



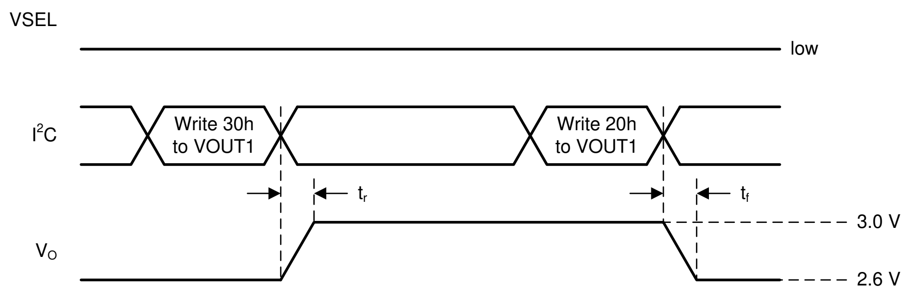
$$t_r = t_f = \frac{|V_{O(1)} - V_{O(2)}|}{SR}$$

Where

- $V_{O(1)}$ is the output voltage set by the VOUT1 register
- $V_{O(2)}$ is the output voltage set by the VOUT2 register
- SR is the slew rate set by the SLEW bits in the CONTROL register

Figure 17. DVS Timing Diagram Using the VSEL Pin

Figure 18 shows the timing diagram when you use the I^2C interface to change the output voltage value in one of the VOUT registers.



$$t_r = t_f = \frac{|3.0 - 2.6|}{SR}$$

Where SR is the slew rate set by the SLEW bits in the CONTROL register.

Figure 18. DVS Timing Using the I^2C Interface

8.3.10 Protection Functions

8.3.10.1 Input Voltage Protection (IVP)

Under certain operating conditions, current can flow from the output of the device to the input. For example, this can occur during dynamic voltage scaling when the output ramps down to a lower voltage and the VOUT pin sinks current from the output capacitor. Under such conditions, if the voltage source supplying the device cannot sink current, the voltage on the VIN pin can rise uncontrollably.

To make sure the input voltage stays within the permitted range, the device stops switching if the voltage on the VIN pin is greater than 5.7 V. The device automatically starts to switch again when the voltage on the VIN pin is less than 5.7 V.

The device sets the $\overline{PG}$ bit in the Status register when an input overvoltage event occurs. The device clears the $\overline{PG}$ bit if the Status register is read when the power-not-good condition no longer exists.

8.3.10.2 Current Limit Mode and Overcurrent Protection

The device has a clamp circuit which limits the peak inductor current in the event of an overload. The exact value of the output current during an overload changes with the operating conditions (V_I and V_O) and the switching mode (buck, buck-boost, or boost) – see Figure 52.

Overloads increase the power dissipation in the device, which increases its temperature. If the device becomes too hot, the thermal shutdown function turns off the converter. When the device cools down, the thermal shutdown function automatically turns on the converter again. Thus, under a permanent overload condition, the device can periodically turn on and off, as it cools down and then heats up.

8.3.10.3 Thermal Shutdown

The device has a thermal shutdown function which turns off the converter if the junction temperature is greater than 150°C. The device automatically turns on the converter again when the junction temperature is less than 130°C. You can still use the I^2C interface to read and write to the registers when the device is in an overtemperature condition.

When the device detects an overtemperature condition, it sets the TSD bit in the Status register to 1. The device clears the TSD bit to 0 if you read the Status register when the junction temperature of the device is less than 130°C.

8.3.11 Power Good

The device has a power-good function which indicates if the output of the DC/DC converter is in regulation or not. The device detects a power-good condition when the output voltage is greater than 95% of its nominal value and detects a power-not-good condition when the output voltage is less than 90% of its nominal value.

When a power-not-good condition occurs, the device sets the $\overline{PG}$ bit in the Status register to 1. The device clears the $\overline{PG}$ bit to 0 if you read the Status register when a power-good condition exists.

8.3.12 Load Disconnect

During device shutdown, the input is disconnected from the output. This prevents any current flow from the output to the input or from the input to the output.

8.3.13 Output Discharge

The device actively discharges the output when the EN pin is low or the ENABLE bit is set to zero.

8.4 Device Functional Modes

The device has two functional modes: off and on. The device enters the on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters the off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.

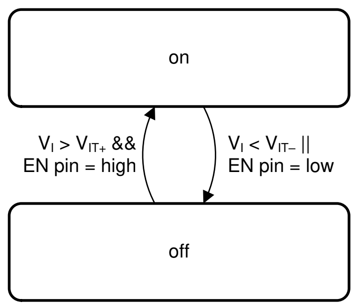


Figure 19. Device Functional Modes

8.5 Programming

8.5.1 Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see *NXP Semiconductors, UM10204 – I^2C-Bus Specification and User Manual*). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C-compatible devices connect to the I^2C bus through open-drain I/O pins, SDA, and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and transmits data on the bus under control of the master device.

The device works as a slave and supports the following data transfer modes, as defined in the I^2C-Bus Specification:

- Standard-mode (100 kbps)
- Fast-mode (400 kbps)
- Fast-mode Plus (1 Mbps)

The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values, depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.1 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore, it is referred to as F/S-mode in this document. The device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is 75h (1110101b).

To make sure that the I^2C function in the device is correctly reset, it is recommended that the I^2C master initiates a STOP condition on the I^2C bus after the initial power up of SDA and SCL pullup voltages.

Programming (continued)

8.5.2 Standard-, Fast-, and Fast-Mode Plus Protocol

The master initiates a data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 20. All I^2C-compatible devices recognize a start condition.

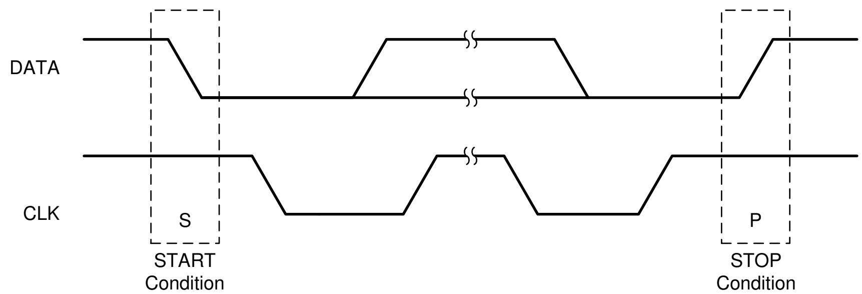


Figure 20. START and STOP Conditions

The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit, R/W, on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 21). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 22) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

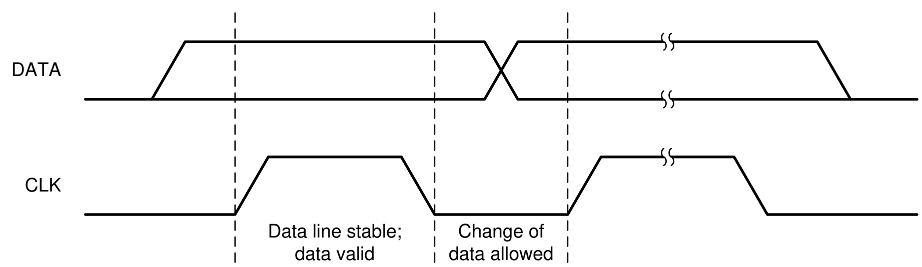


Figure 21. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 20). This releases the bus and stops the communication link with the addressed slave. All I^2C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

Programming (continued)

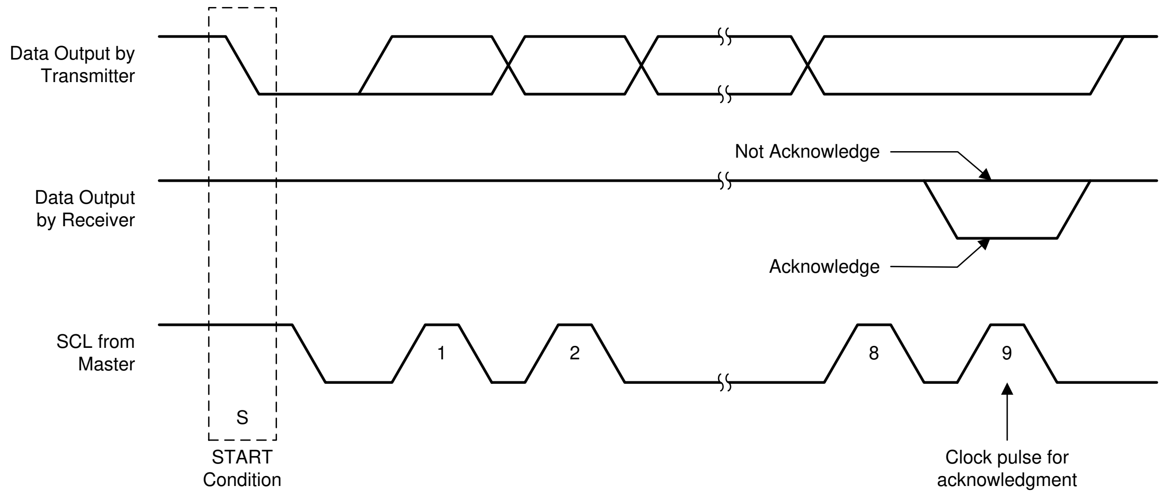


Figure 22. Acknowledge on the I²C Bus

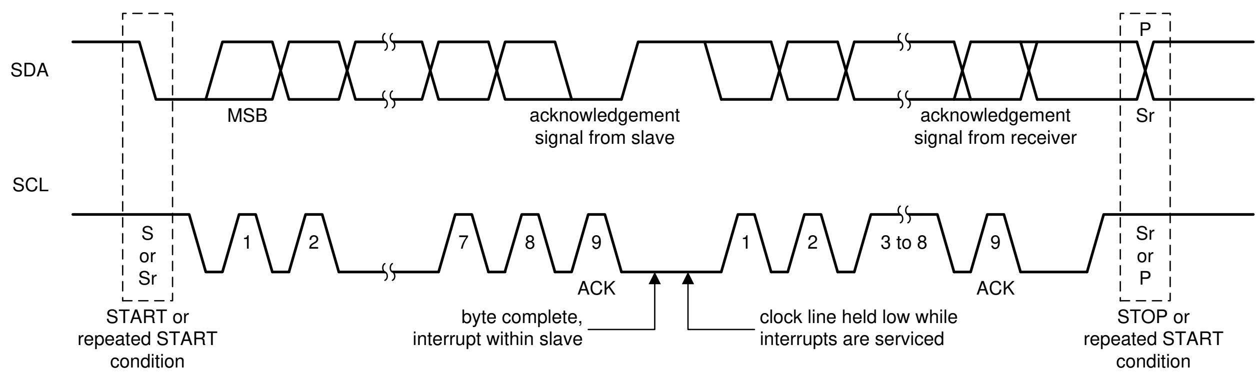


Figure 23. Bus Protocol

8.5.3 I²C Update Sequence

A single update requires the following:

- A start condition
- A valid I²C slave address
- A register address
- A data byte

To acknowledge the receipt of each byte, the device pulls the SDA line low during the high period of a single clock pulse. The device performs an update on the falling edge of the acknowledge signal that follows the last byte.

Programming (continued)

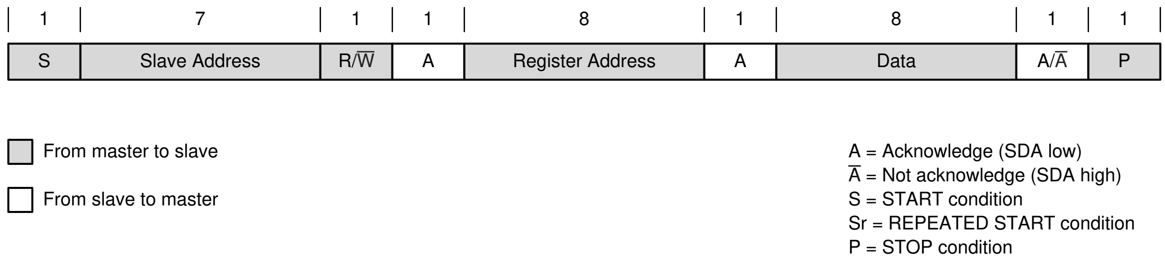


Figure 24. “Write” Data Transfer Format in Standard, Fast, and Fast-Plus Modes

Figure 25. “Read” Data Transfer Format in Standard, Fast, and Fast-Plus Modes

8.6 Register Map

8.6.1 Register Description

8.6.1.1 Register Map

ADDRESS	ACRONYM	REGISTER NAME	SECTION
0x01	CONTROL	Control Register	Go
0x02	STATUS	Status Register	Go
0x03	DEVID	DEVID Register	Go
0x04	VOUT1	VOUT1 Register	Go
0x05	VOUT2	VOUT2 Register	Go

8.6.1.2 Register CONTROL (Slave address: 0b1110101; Register address: 0x01; Default: 0x00 or 0x20)

Return to Register Map.

Figure 26. Register CONTROL Format

7	6	5	4	3	2	1	0
RESERVED	RANGE	ENABLE	RESERVED	FPWM	RPWM	SLEW[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only

Table 3. Register CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	Reserved for future use. This bit can be written to and read from but it has no function. For compatibility with possible future device variants, it is recommended to program this bit to 0.
6	RANGE	R/W	0	This bit selects the output voltage range. **0: Low range (1.800 V to 4.975 V)** 1 : High range (2.025 V to 5.200 V)
5	ENABLE	R/W	X	This bit controls operation of the converter. 0 : Converter operation disabled (Start-up value for TPS63811) 1 : Converter operation enabled (Start-up value for TPS63810)
4	RESERVED	R/W	0	Reserved for future use. This bit can be written to and read from but it has no function. For compatibility with possible future device variants, it is recommended to program this bit to 0.
3	FPWM	R/W	0	This bit controls the forced-PWM function. **0: Forced-PWM operation disabled** 1 : Forced-PWM operation enabled
2	RPWM	R/W	0	This bit controls the ramp-PWM function. **0: Ramp-PWM operation disabled** 1 : Ramp-PWM operation enabled
1:0	SLEW[1:0]	R/W	00	These bits control the slew rate of the DVS function. **00: 1.0 V/ms** 01: 2.5 V/ms 10: 5.0 V/ms 11: 10.0 V/ms

8.6.1.3 Register STATUS (Slave address: 0b1110101; Register address: 0x02; Default: 0x00)

Return to Register Map.

Figure 27. Register STATUS Format

7	6	5	4	3	2	1	0
NIL[5:0]						TSD	PGn
R						R	R

LEGEND: R/W = Read/Write; R = Read only

Table 4. Register STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7:2	NIL[5:0]	R	000000	Not used. These bits always return 0 when read.
1	TSD	R	0	This bit shows the status of the thermal shutdown function. This bit is cleared if the STATUS register is read when the overtemperature condition no longer exists. **0: Temperature good** 1 : An overtemperature event was detected.
0	PGn	R	0	This bit shows the status of the power-good comparator. This bit is cleared if the STATUS register is read when the power-not-good condition no longer exists. **0: Power-good** 1 : A power-not-good event was detected.

8.6.1.4 Register DEVID (Slave address: 0b1110101; Register address: 0x03; Default: 0x04)

Return to Register Map.

Figure 28. Register DEVID Format

7	6	5	4	3	2	1	0
MANUFACTURER[3:0]				MAJOR[1:0]		MINOR[1:0]	
R				R		R	

LEGEND: R/W = Read/Write; R = Read only

Table 5. Register DEVID Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MANUFACTURER[3:0]	R	0000	These bits identify the device manufacturer. **0000: Texas Instruments**
3:2	MAJOR[1:0]	R	01	These bits identify the major silicon revision. 00: A (initial silicon) **01: B (first major revision)** 10: C (second major revision) 11: D (third major revision)
1:0	MINOR[1:0]	R	00	These bits identify the minor silicon revision. **00: 0 (initial silicon)** 01: 1 (first minor revision) 10: 2 (second minor revision) 11: 3 (third minor revision)

8.6.1.5 Register VOUT1 (Slave address: 0b1110101; Register address: 0x04; Default: 0x3C)

Return to Register Map.

Figure 29. Register VOUT1 Format

7	6	5	4	3	2	1	0
NIL	VOUT1[6:0]						
R	R/W						

LEGEND: R/W = Read/Write; R = Read only

Table 6. Register VOUT1 Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL	R	0	Not used This bit always returns 0 when read.
6:0	VOUT1[6:0]	R/W	0111100	These bits set the output voltage when the VSEL pin is low. Output voltage = 1.800 + (VOUT1[6 :0] × 0.025) V (low range) (default = 3.3 V) Output voltage = 2.025 + (VOUT1[6 :0] × 0.025) V (high range) (default = 3.525 V)

8.6.1.6 Register VOUT2 (Slave address: 0b1110101; Register address: 0x05; Default: 0x42)

Back to Register Map.

Figure 30. Register VOUT2 Format

7	6	5	4	3	2	1	0
NIL	VOUT2[6:0]						
R	R/W						

LEGEND: R/W = Read/Write; R = Read only

Table 7. Register VOUT2 Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL	R	0	Not used This bit always returns 0 when read.

Table 7. Register VOUT2 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	VOUT2[6:0]	R/W	1000010	These bits set the output voltage when the VSEL pin is high. Output voltage = 1.800 + (VOUT2[6 :0] × 0.025) V (low range) (default = 3.45 V) Output voltage = 2.025 + (VOUT2[6 :0] × 0.025) V (high range) (default = 3.675 V)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS63810 and TPS63811 devices are high efficiency, high current buck-boost converters, suitable for applications where the input voltage is higher, lower, or equal to the output voltage. The maximum peak current in the switches is limited to a typical value of 6 A.

9.2 Typical Applications

9.2.1 1.8-V to 5.2-V Output Smartphone Power Supply

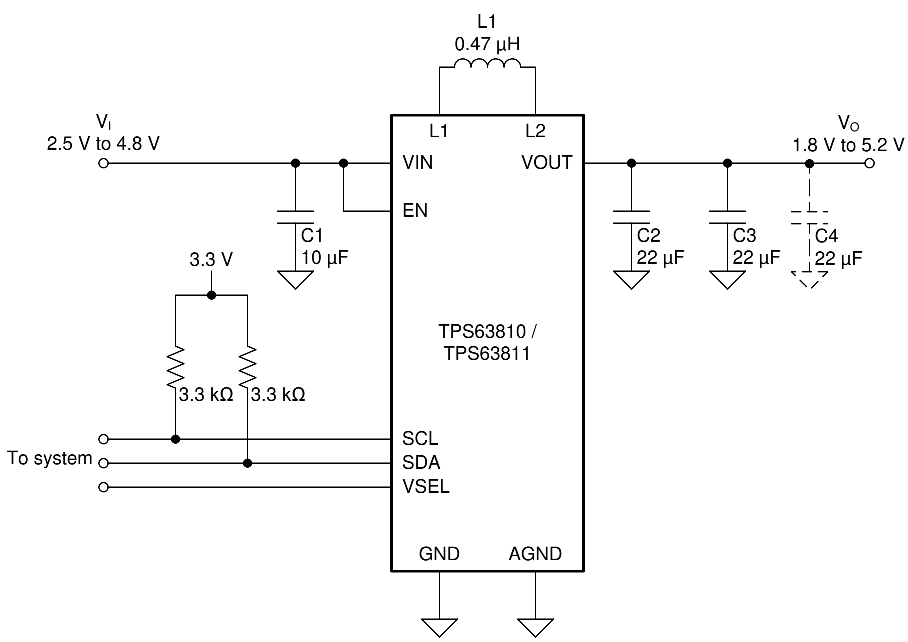


Figure 31. Typical Application Schematic

9.2.1.1 Design Requirements

This example uses the design parameters listed in Table 8.

Table 8. Design Parameters

DESIGN PARAMETER	SYMBOL	EXAMPLE VALUE
Input voltage	V_I	2.5 V to 4.8 V
Output voltage	V_O	1.8 V to 5.2 V
Output current	I_O	2 A
I^2C bus voltage	V_{BUS}	3.3 V
I^2C bus capacitance	C_b	100 pF
I^2C bus speed		Fast-mode (400 kHz)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Input Capacitor Selection

TI recommends a minimum input capacitance (including DC bias effects) of 5 µF. A 10-µF, 10-V ceramic capacitor is suitable for typical applications. If the input supply is located more than a few centimeters from the converter, you may need to add additional bulk capacitance (a 47-µF electrolytic or tantalum capacitor is a typical choice).

The output capacitance does not have an upper limit; you can make it as big as you want.

9.2.1.2.2 Inductor Selection

TI recommends you use the TPS63810 device with 0.47-µH inductors. For high efficiencies, use an inductor with a low DC resistance (DCR) and low core losses.

The saturation current of the inductor must be greater than the maximum inductor current in your application. To include sufficient margin for worst-case and transient operating conditions, TI recommends you use an inductor with saturation current that is at least 20% higher than the maximum inductor current in your application. The maximum current in the inductor occurs when the device operates in boost mode and the following is true:

- The input voltage is at its minimum value.
- The output voltage is at its maximum value.
- The output current is at its maximum value.

To calculate the maximum inductor current, first use Equation 1 to calculate the maximum duty cycle during boost operation (which is when the maximum inductor current occurs).

$$D = \frac{V_O - V_I}{V_O}$$

where

- D is the duty cycle
- V_I is the input voltage
- V_O is the output voltage (1)

$$D = \frac{5\ V - 2.5\ V}{5\ V} = 0.5$$

Next, use Equation 2 to calculate the maximum inductor current.

$$I_{LM} = \frac{I_O}{\eta(1 - D)} + \frac{DV_I}{2fL}$$

where

- I_{LM} is the peak inductor current
- I_O is the output current
- η is the converter efficiency (use the value from the application curves or assume 90%)
- D is the duty cycle (calculated with Equation 1)
- V_I is the input voltage
- f is the switching frequency (assume 2 MHz)
- L is the inductance (use 0.47 µH) (2)

$$I_{LM} = \frac{2\ A}{(0.9)(1 - 0.5)} + \frac{(0.5)(2.5\ V)}{(2)(2\ MHz)(0.47\ \mu H)} = 5.1\ A$$

To include enough margin for transient conditions, TI recommends you use an inductor with a saturation current rating at least 20% higher than the calculated maximum current. In this example, TI recommends an inductor with a saturation current of at least 6.1 A.

9.2.1.2.3 *Output Capacitor Selection*

TI recommends a minimum output capacitance (including DC bias effects) of 16 µF. Two 22-µF, 10-V ceramic capacitors are suitable for typical applications with $V_O \le 3.6$ V. For $V_O > 3.6$ V, three 22-µF or two 47-µF ceramic capacitors are suitable. If you want to minimize switching noise on the output, connect a small ceramic capacitor (100 nF is a typical value) in parallel to the two main output capacitors and place it closest to the VOUT pin. Smaller capacitors have lower parasitic inductance and are more effective at filtering high frequencies than the two main output capacitors.

The output capacitance does not have an upper limit, however, very large values of output capacitance make the transient response of the converter slower.

It is important that the effective capacitance is given according to the recommended value in Recommended Operating Conditions. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a trade-off between size and transient behavior as higher capacitance reduces transient response overshoot and undershoot and increases transient response time. Table 9 lists possible output capacitors.

Table 9. List of Recommended Capacitors(1)

CAPACITOR [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (METRIC)
22	6.3	10	GRM187R60J226ME15	Murata	0603 (1608)
22	10	40	GRM187R61A226ME15	Murata	0603 (1608)
47	6.3	43	GRM188R60J476ME15	Murata	0603 (1608)
47	6.3	43	GRM219R60J476ME44	Murata	0805 (2012)

(1) See *Third-party Products Disclaimer*.

9.2.1.2.4 I²C Pullup Resistor Selection

Refer to the *NXP Semiconductors, UM10204 – I²C-Bus Specification and User Manual* for the specifications relevant to your application.

Use Equation 3 to calculate the maximum permitted pullup resistor value for the bus speed used in the application.

$$R_P(\max) = \frac{t_r}{0.8473 \times C_b}$$

where

- t_r is the maximum permitted rise time (300 ns for Fast-mode)
- C_b is the capacitive load on each bus line (3)

$$R_P(\max) = \frac{300\ \text{ns}}{0.8473 \times 100\ \text{pF}} = 3.541\ \text{k}\Omega$$

If you do not know what the bus capacitance is in your application, start with a 1-kΩ pullup resistor and measure the rise time with an oscilloscope. Use Equation 3 to calculate the bus capacitance and thus the maximum permitted pullup resistor.

Use Equation 4 to calculate the minimum permitted pullup resistor value for different bus speeds.

$$R_P(\min) = \frac{V_{BUS} - V_{OL}}{I_{OL}}$$

where

- V_{BUS} is the I^2C bus pullup voltage
- V_{OL} is the low-level output voltage (0.4 V)
- I_{OL} is the low-level output current (3 mA for Fast-mode) (4)

$$R_P(\min) = \frac{3.3\ V - 0.4\ V}{3\ mA} = 967\ \Omega$$

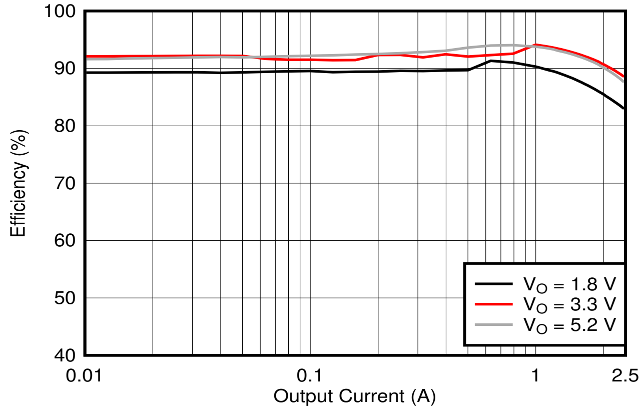
A pullup resistor value of 3.3 kΩ meets both of these requirements.

9.2.1.3 Application Curves

Table 10 lists the components that were used for the measurements contained in the following pages.

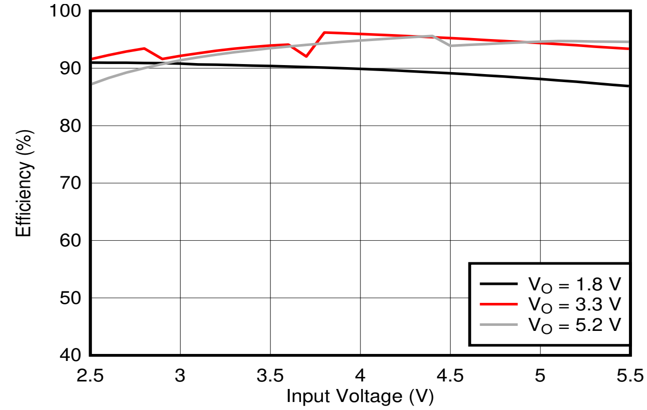
Table 10. Components for Application Characteristic Curves

REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER
C1	Capacitor, 10 µF, 10 V, 0603, ceramic	GRM188R61A106ME69	Murata
C2, C3	Capacitor, 22 µF, 10 V, 0603, ceramic	GRM187R61A226ME15	Murata
L1	Inductor, 0.47 µH	XFL4015-471MEC	Coilcraft
U1	Integrated circuit	TPS63810YFF	Texas Instruments



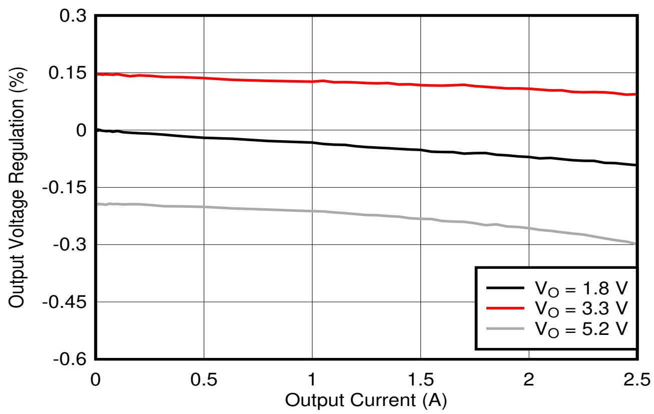
V_I = 3.6 V PSM T_A = 25°C

Figure 32. Efficiency versus Output Current



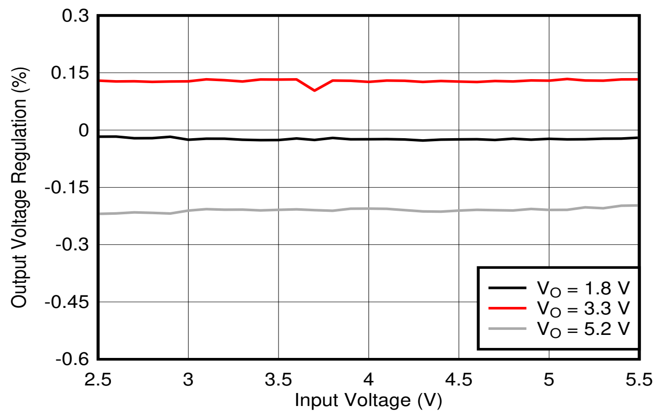
I_O = 1 A PSM T_A = 25°C

Figure 33. Efficiency versus Input Voltage



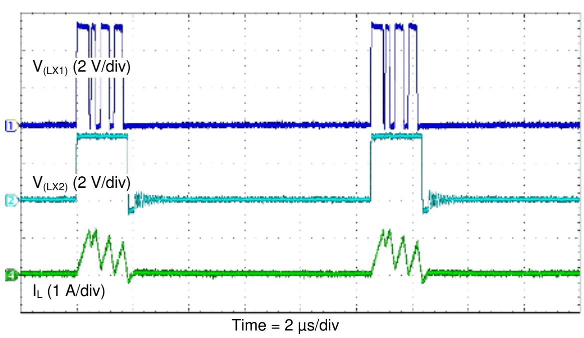
V_I = 3.6 V FPWM T_A = 25°C

Figure 34. Load Regulation



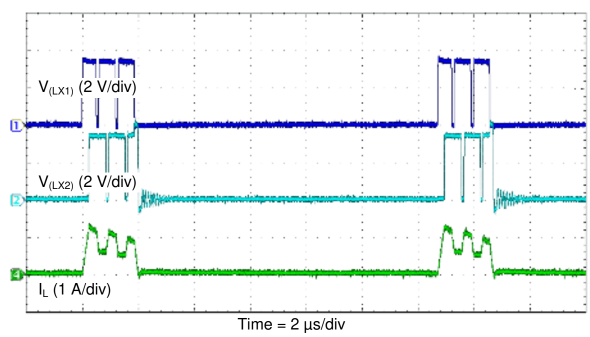
I_O = 1 A FPWM T_A = 25°C

Figure 35. Line Regulation



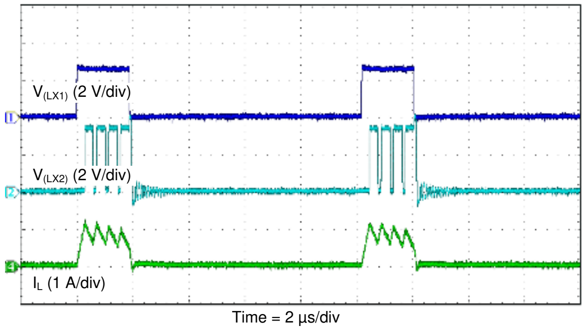
V_I = 5 V PSM T_A = 25°C
V_O = 3.3 V I_O = 100 mA

Figure 36. PFM Switching Waveforms (Buck Operation)



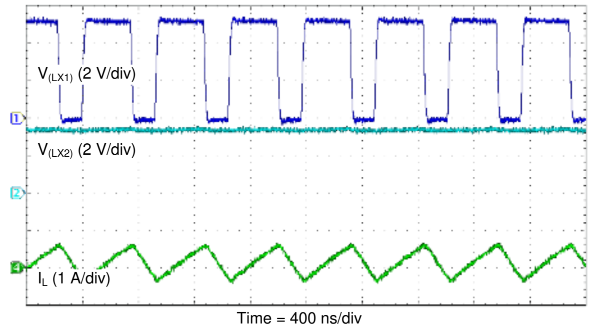
V_I = 3.3 V PSM T_A = 25°C
V_O = 3.3 V I_O = 100 mA

Figure 37. PFM Switching Waveforms (Buck-Boost Operation)



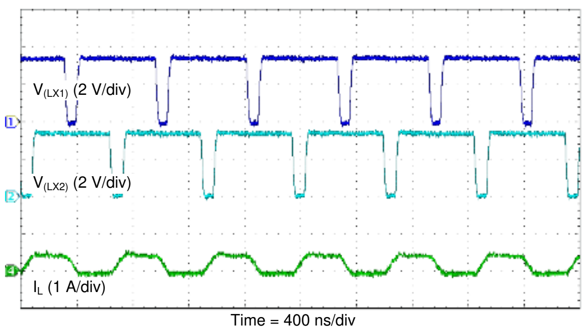
V_I = 2.5 V, V_O = 3.3 V, PSM, I_O = 100 mA, T_A = 25°C

Figure 38. PFM Switching Waveforms (Boost Operation)



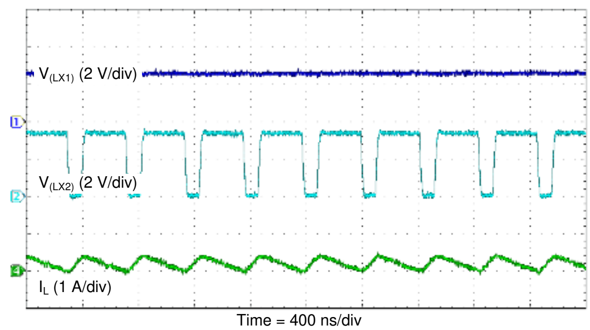
V_I = 5 V, V_O = 3.3 V, FPWM, I_O = 100 mA, T_A = 25°C

Figure 39. PWM Switching Waveforms (Buck Operation)



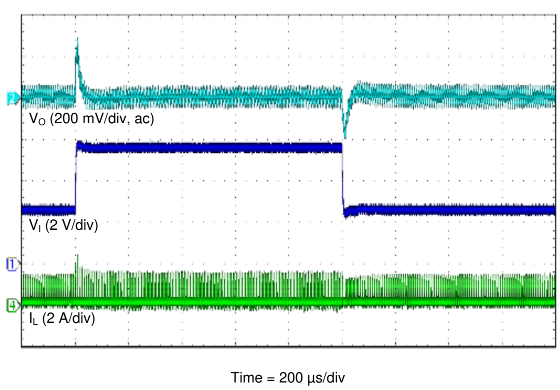
V_I = 3.3 V, V_O = 3.3 V, FPWM, I_O = 100 mA, T_A = 25°C

Figure 40. PWM Switching Waveforms (Buck-Boost Operation)



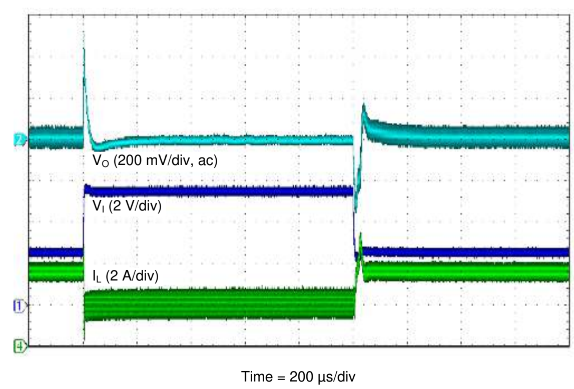
V_I = 2.5 V, V_O = 3.3 V, FPWM, I_O = 100 mA, T_A = 25°C

Figure 41. PWM Switching Waveforms (Boost Operation)



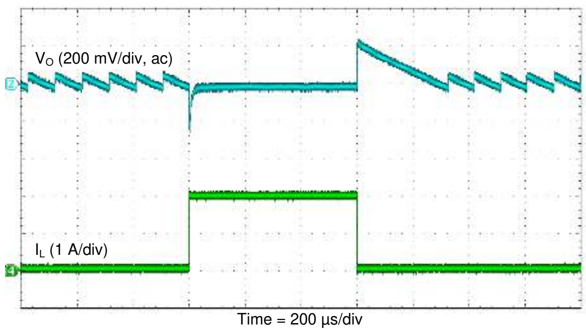
V_I = 2.5 V to 5.5 V, V_O = 3.3 V, PSM, I_O = 200 mA, T_A = 25°C

Figure 42. Line Transient Response



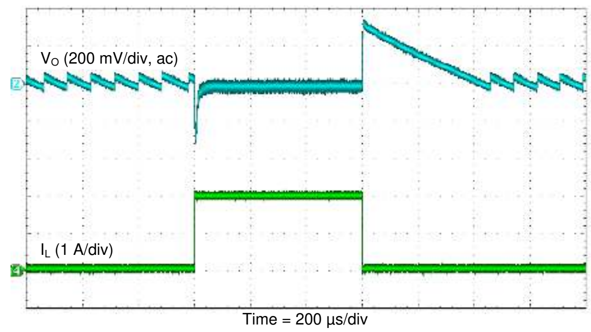
V_I = 2.5 V to 5.5 V, V_O = 3.3 V, PSM, I_O = 2 A, T_A = 25°C

Figure 43. Line Transient Response



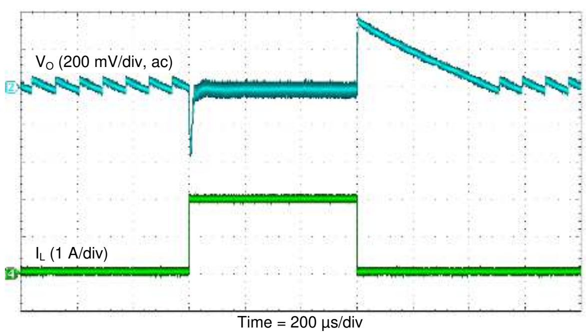
V_I = 4.2 V PSM T_A = 25°C
V_O = 3.3 V I_O = 10 mA to 2 A

Figure 44. Load Transient Response (Buck)



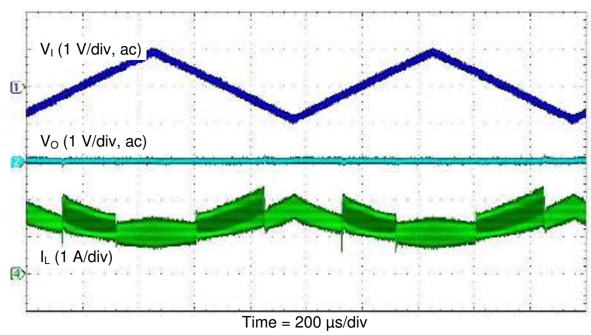
V_I = 3.3 V PSM T_A = 25°C
V_O = 3.3 V I_O = 10 mA to 2 A

Figure 45. Load Transient Response (Buck-Boost)



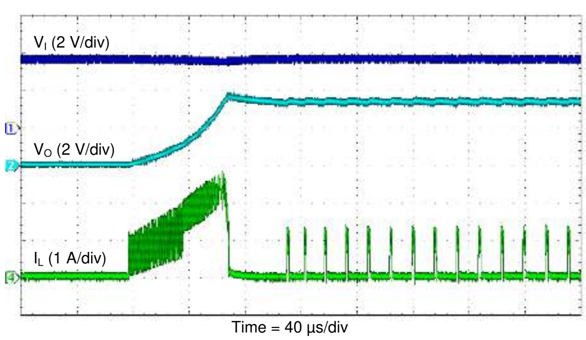
V_I = 2.6 V PSM T_A = 25°C
V_O = 3.3 V I_O = 10 mA to 2 A

Figure 46. Load Transient Response (Boost)



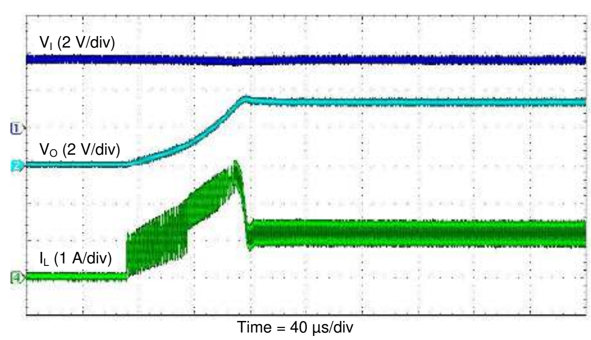
V_I = 3.3 V ±0.9 V FPWM T_A = 25°C
V_O = 3.3 V R_L = 3 Ω

Figure 47. Line Sweep (PWM)



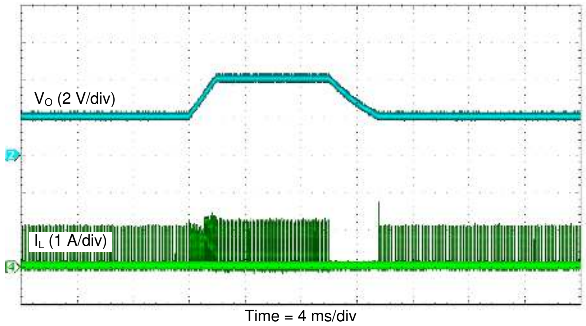
V_I = 3.6 V PSM T_A = 25°C
V_O = 3.3 V R_L = 33 Ω

Figure 48. Start-Up Waveforms (Light Load)



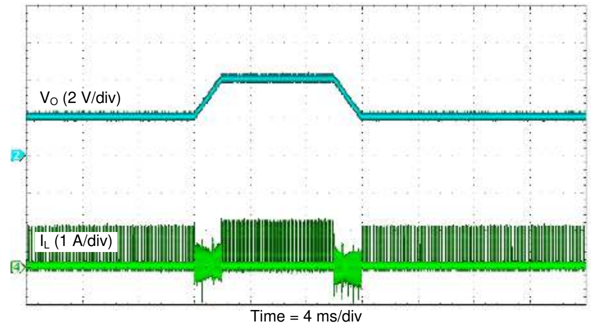
V_I = 3.6 V PSM T_A = 25°C
V_O = 3.3 V R_L = 3.3 Ω

Figure 49. Start-Up Waveforms (Heavy Load)



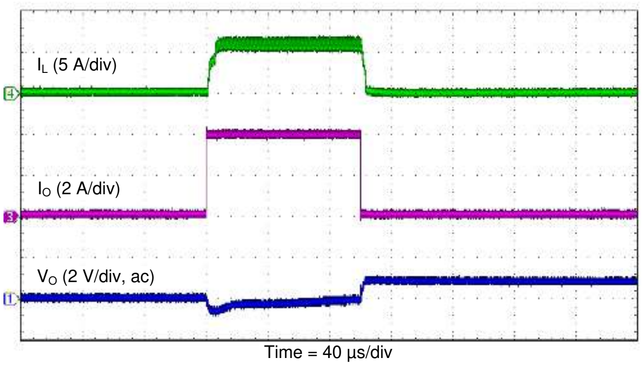
V_I = 3.6 V   PSM T_A = 25°C
V_O = 2 V to 4 V R_L = 330 Ω

Figure 50. Dynamic Voltage Scaling (PFM)



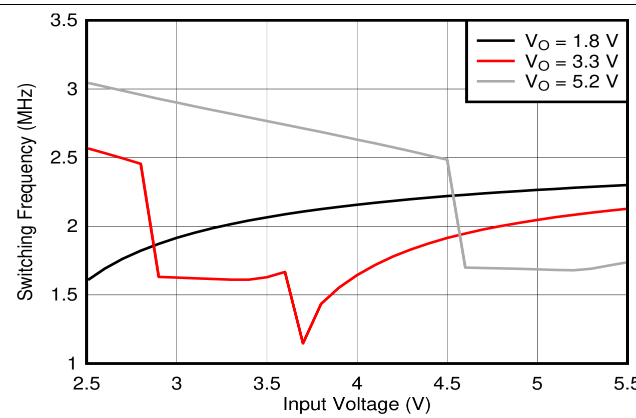
V_I = 3.6 V   PSM T_A = 25°C
V_O = 2 V to 4 V   RPWM R_L = 330 Ω

Figure 51. Dynamic Voltage Scaling (RPWM)



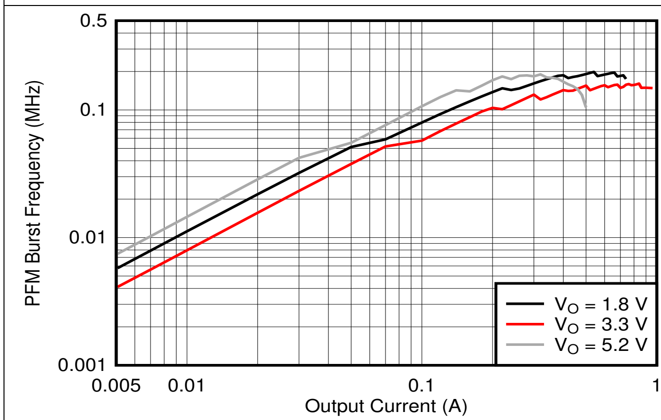
V_I = 3.6 V   PSM T_A = 25°C
V_O = 3.3 V

Figure 52. Overcurrent Protection



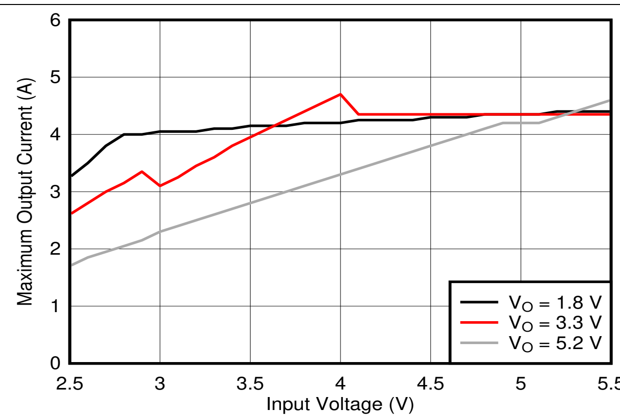
I_O = 1 A   FPWM T_A = 25°C
V_I rising

Figure 53. Switching Frequency versus Input Voltage



V_I = 3.6 V   PSM T_A = 25°C

Figure 54. Burst Switching Frequency versus Output Current



PSM T_A = 25°C

Figure 55. Maximum Output Current versus Input Voltage

10 Power Supply Recommendations

The device is designed to operate with a DC supply voltage in the range 2.2 V to 5.5 V. If the input supply is more than a few centimeters from the device, TI recommends adding some bulk capacitance to the ceramic bypass capacitors. A 47-µF electrolytic capacitor is a typical selection for the bulk capacitance.

11 Layout

11.1 Layout Guidelines

Correct PCB layout is necessary to obtain the full performance from the device. TI recommends to follow these basic principles:

- Place input and output capacitors close to the device to minimize the input and output loop areas.
- If you combine different-sized capacitors to make up the total input capacitance, place the smallest capacitor closest to the device. The same applies to the output capacitance.
- Keep PCB traces short and wide to minimize parasitic resistance and inductance.
- Use the following PCB layer stack (or something similar):
  - Layer 1 (top): All components and all power traces
  - Layer 2 (inner): Signals
  - Layer 3 (inner): Signals
  - Layer 4 (bottom): Ground plane

Figure 56 shows an example of the PCB layout used for all of the measurement data in *Application Curves*.

11.2 Layout Example

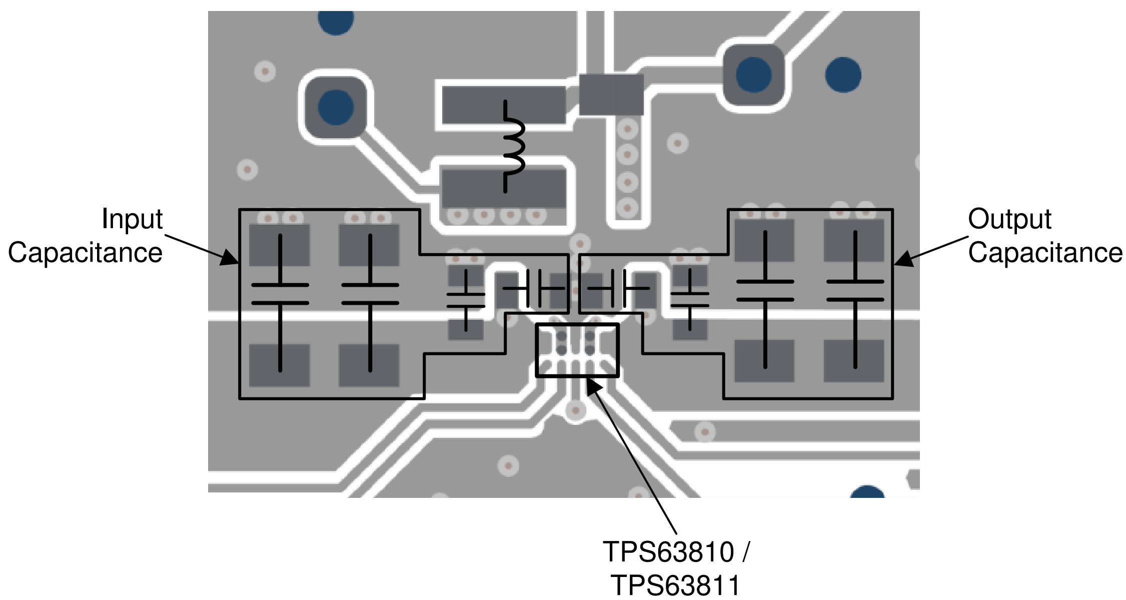


Figure 56. Recommended PCB Layout for the TPS63810 Device

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *NXP Semiconductors, UM10204 – I^2C-Bus Specification and User Manual*
- Texas Instruments, *TPS63810 EVM User Guide*

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 11. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS63810	Click here	Click here	Click here	Click here	Click here
TPS63811	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.6 Trademarks

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All other trademarks are the property of their respective owners.

12.7 Glossary

SLYZ022– *TI Glossary*

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63810YFFR	ACTIVE	DSBGA	YFF	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63810	Samples
TPS63811YFFR	ACTIVE	DSBGA	YFF	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TPS63811	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

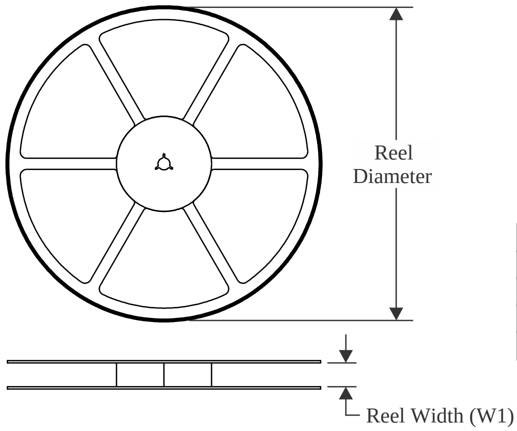
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

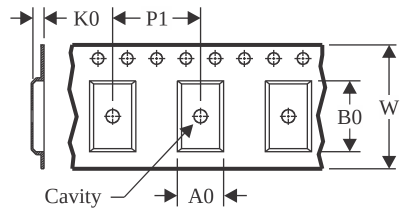
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

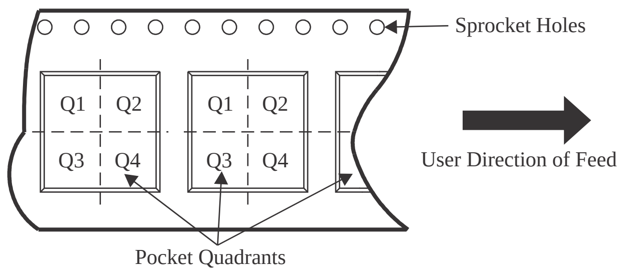


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

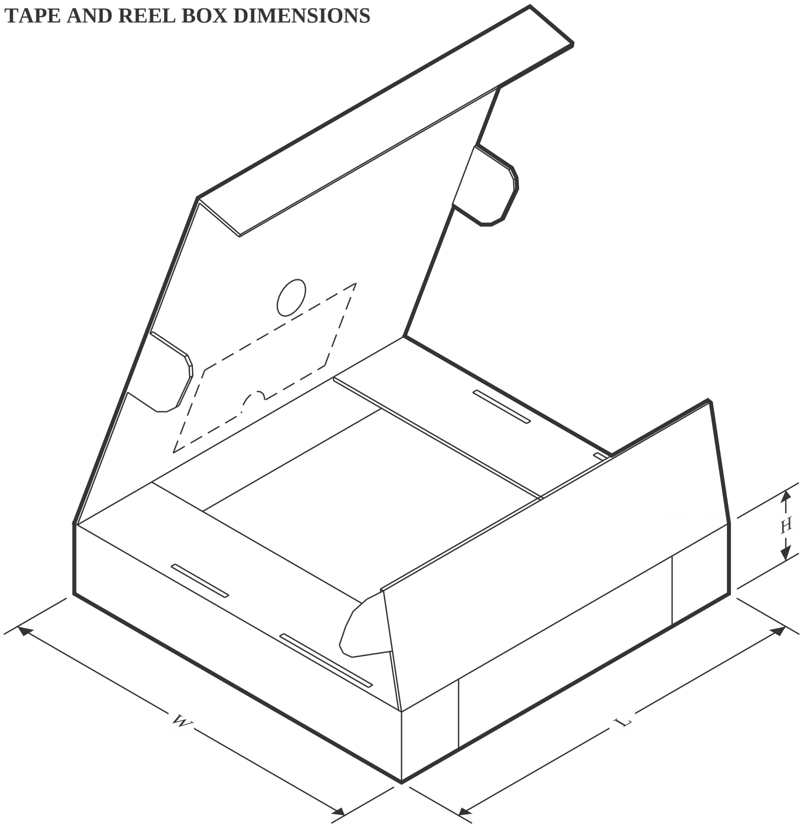
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

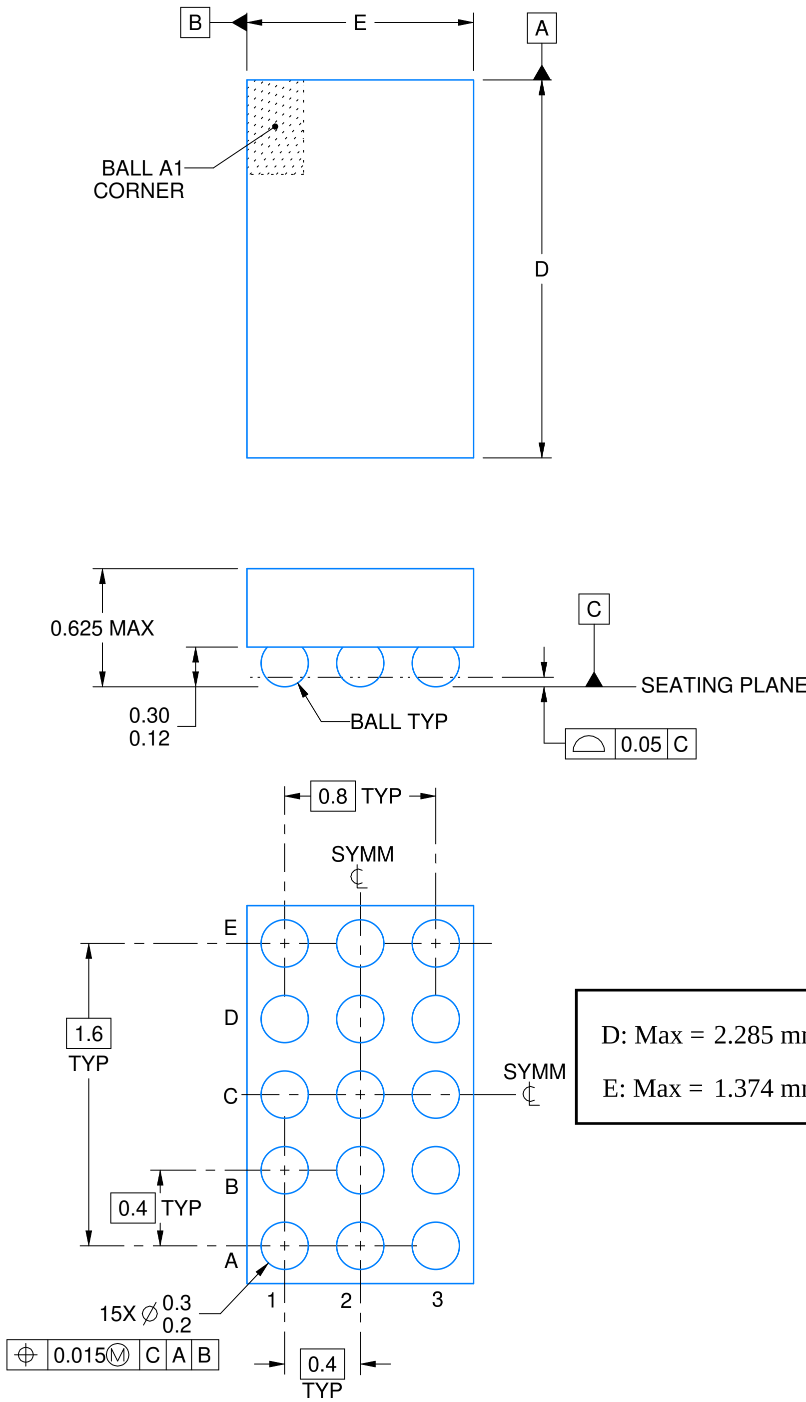
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63810YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.5	2.42	0.75	4.0	8.0	Q1
TPS63811YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.5	2.42	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63810YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0
TPS63811YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0



D: Max = 2.285 mm, Min =2.225 mm

E: Max = 1.374 mm, Min =1.314 mm

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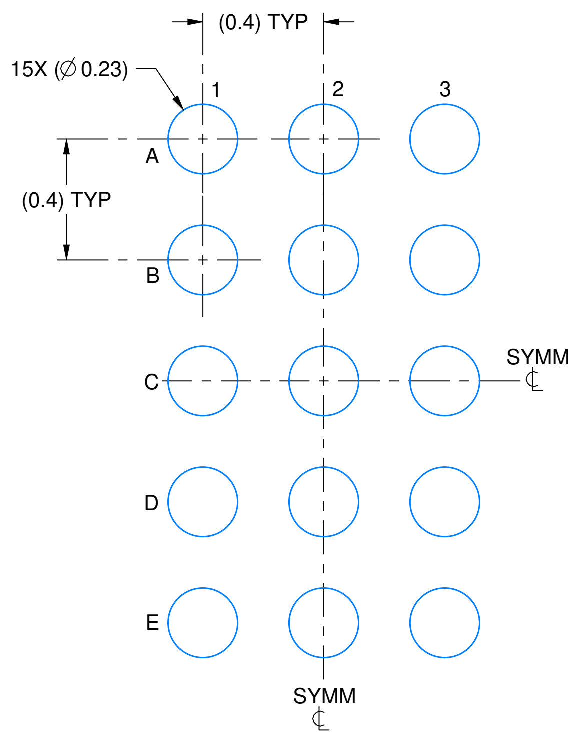
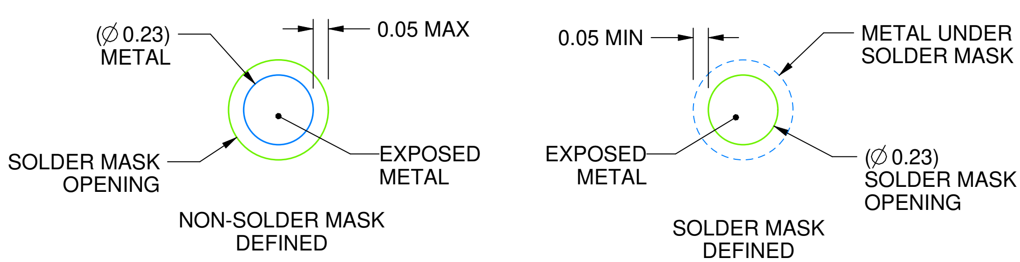
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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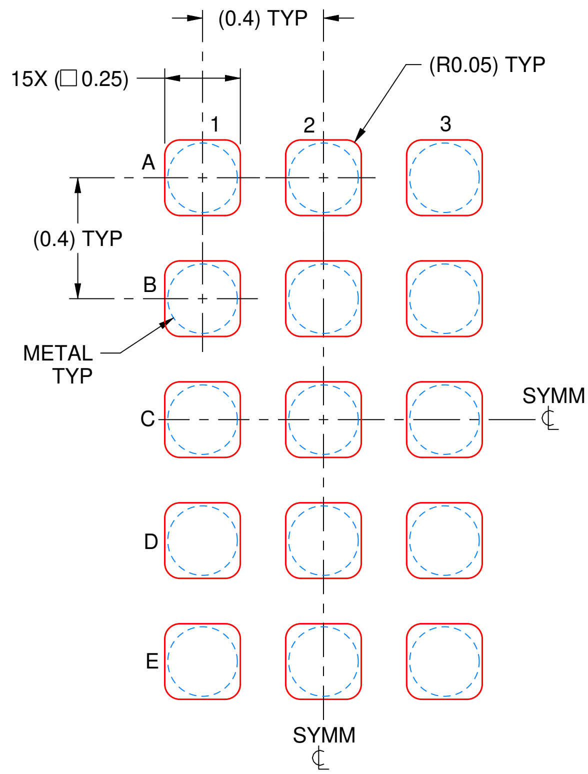
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.