

## LM4850 Boomer® Audio Power Amplifier Series Mono 1.5 W / Stereo 300 mW Power Amplifier

Check for Samples: [LM4850](#)

### FEATURES

- Mono 1.5W BTL or Stereo 300mW Output
- Headphone Sense
- “Click and Pop” Suppression Circuitry
- No Bootstrap Capacitors Required
- Thermal Shutdown Protection
- Unity-Gain Stable
- WSON, TSSOP, and VSSOP Packaging

### APPLICATIONS

- Portable computers
- Desktop computers
- PDA's
- Handheld games

### KEY SPECIFICATIONS <sup>(1)</sup>

- n Output Power at 1% THD+N, 1kHz:
  - LM4850LD 3Ω BTL, 1.9W (Typ)
  - LM4850LD 4Ω BTL, 1.7W (Typ)
  - LM4850MM, MT 4Ω BTL, 1.5W (Typ)
  - LM4850LD, MM, MT 8Ω BTL, 1.1W (Typ)
  - LM4850LD, MM, MT 8Ω SE, 300mW (Typ)
  - LM4850LD, MM, MT 32Ω SE, 95mW (Typ)
- THD+N at 1kHz, 95mW into 32Ω SE, 1% (Typ)
- Single Supply Operation, 2.4 to 5.5V
- Shutdown Current, 44μA (Typ)

(1) An LM4850LD that has been properly mounted to a circuit board will deliver 1.9W into 3Ω (at 1% THD+N). The other package options for the LM4850 will deliver 1.1W into 8Ω (at 1% THD+N). See [Application Information](#) sections for further information concerning the LM4850LD, LM4850MM, and LM4850MT.

### DESCRIPTION

The LM4850 is an audio power amplifier capable of delivering 1.5W (typ) of continuous average power into a mono 4Ω bridged-tied load (BTL) with 1% THD+N or 95mW per channel of continuous average power into stereo 32Ω single-ended (SE) loads with 1% THD+N, using a 5V power supply.

The LM4850 can automatically switch between mono BTL and stereo SE modes utilizing a headphone sense pin. It is ideal for any system that provides both a monaural speaker output and a stereo line or headphone output

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4850 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4850 features an externally controlled, micropower consumption shutdown mode and thermal shutdown protection. The unity-gain stable LM4850's gain is set by external gain-setting resistors



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Typical Application

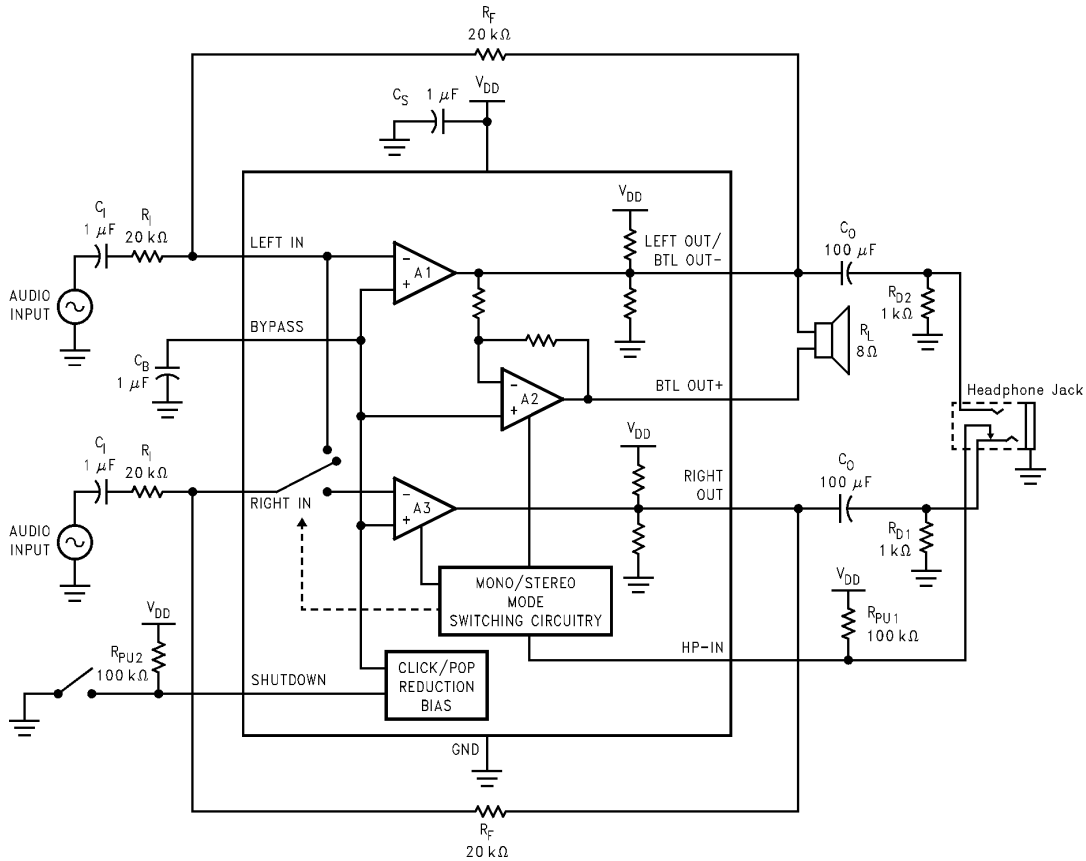


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

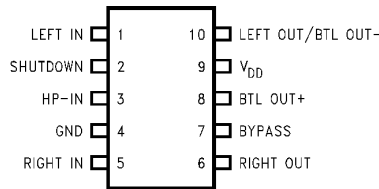


Figure 2. Top View  
10 Lead VSSOP  
See Package Number DGS

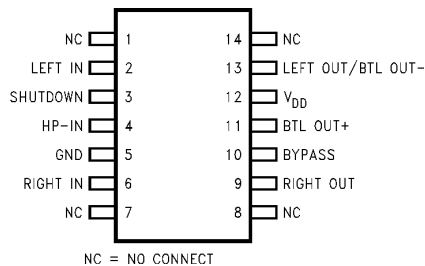
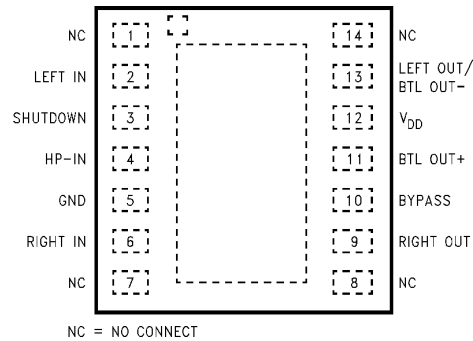


Figure 3. Top View  
14 Lead TSSOP  
See Package Number PW



**Figure 4. Top View  
14 Lead WSON  
See Package Number NHE0014A**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

Supply Voltage		6.0V
Storage Temperature		-65°C to +150°C
ESD Susceptibility <sup>(3)</sup>		3.5kV
ESD Machine model <sup>(4)</sup>		250V
Junction Temperature (T <sub>J</sub> )		150°C
Small Outline Package	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
Thermal Resistance	θ <sub>JA</sub> (typ)—DGS	194°C/W
	θ <sub>JC</sub> (typ)—DGS	52°C/W
	θ <sub>JA</sub> (typ)—PW	150°C/W
	θ <sub>JC</sub> (typ)—PW	40°C/W
	θ <sub>JA</sub> (typ)—NHE0014A <sup>(5)</sup>	56°C/W
	θ <sub>JC</sub> (typ)—NHE0014A	4.3°C/W

- (1) Absolute Maximum Rating indicate limits beyond which damage to the device may occur.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Human body model, 100pF discharged through a 1.5kΩ resistor.
- (4) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).
- (5) The given θ<sub>JA</sub> is for a LM4850LD with the Exposed-DAP soldered to an exposed 1in<sup>2</sup> area of 1oz printed circuit board copper.

### Operating Ratings<sup>(1)</sup>

Temperature Range		-40°C ≤ to 85°C
Supply Voltage V <sub>DD</sub>		2.4V ≤ V <sub>DD</sub> ≤ 5.5V

- (1) Absolute Maximum Rating indicate limits beyond which damage to the device may occur.

## Electrical Characteristics<sup>(1) (2)</sup>

The following specifications apply for  $V_{DD} = 5.0V$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	LM4850		Units (Limits)
			Typical <sup>(3)</sup>	Limit <sup>(4)</sup>	
$V_{DD}$	Supply Voltage			2.4	V (min)
				5.5	V (max)
$I_{DD}$	Supply Current	BTL Mode; $V_{IN} = 0V$ ; $I_O = 0A$	2.4	7.0	mA
		SE Mode; $V_{IN} = 0V$ ; $I_O = 0A$	2.4	7.0	mA
$I_{SD}$	Shutdown Current	SD Mode	44		$\mu A$
$V_{OS}$	Output Offset Voltage	BTL Mode; $A_V = 2$ BTL OUT+ to BTL OUT-	5.0	40	mV
$P_O$	Output Power	LM4850LD; BTL Mode; $R_L = 3\Omega$ THD+N = 1% <sup>(5)</sup>	1.9		W
		LM4850LD; BTL Mode; $R_L = 4\Omega$ THD+N = 1% <sup>(5)</sup>	1.7		W
		LM4850MT, MM; BTL Mode; $R_L = 4\Omega$ THD+N = 1%	1.5		W
		BTL Mode; $R_L = 8\Omega$ THD+N = 1%	1.1		W
		SE Mode; $R_L = 8\Omega$ THD+N = 1%	300		mW
		SE Mode; $R_L = 32\Omega$ THD+N = 1%	95		mW
$V_{IH}$	Shutdown Input Voltage High	$I_S < 80\mu A$		2.0	V (min)
$V_{IL}$	Shutdown Input Voltage Low	$I_S > 0.5mA$		0.8	V (max)
Crosstalk	Channel Separation	SE Mode, $R_L = 32\Omega$ ; $f = 1kHz$	73		dB

- (1) Absolute Maximum Rating indicate limits beyond which damage to the device may occur.
- (2) All voltages are measured with respect to the ground pin, unless otherwise specified.
- (3) Typical specifications are specified at  $+25^\circ C$  and represent the most likely parametric norm.
- (4) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.
- (5) When driving 3 $\Omega$  or 4 $\Omega$  loads from a 5V supply, the LM4850 must be mounted to a circuit board.

## Electrical Characteristics<sup>(1)(2)</sup>

The following specifications apply for  $V_{DD} = 3.3V$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	LM4850		Units (Limits)
			Typical <sup>(3)</sup>	Limit <sup>(4)</sup>	
$I_{DD}$	Supply Current	BTL Mode; $V_{IN} = 0V$ ; $I_O = 0A$	2.0		mA
		SE Mode; $V_{IN} = 0V$ ; $I_O = 0A$	2.0		mA
$I_{SD}$	Shutdown Current	SD Mode	30		$\mu A$
$V_{OS}$	Output Offset Voltage	BTL Mode; $A_V = 2$ BTL OUT+ to BTL OUT-	5.0	40	mV
$P_O$	Output Power	BTL Mode; $R_L = 8\Omega$ THD+N = 1%	440		mW
		SE Mode; $R_L = 32\Omega$ THD+N = 1%	40		mW
$V_{IH}$	Shutdown Input Voltage High	$I_S < 80\mu A$		2.0	V (min)
$V_{IL}$	Shutdown Input Voltage Low	$I_S > 0.5mA$		0.8	V (max)

- (1) Absolute Maximum Rating indicate limits beyond which damage to the device may occur.
- (2) All voltages are measured with respect to the ground pin, unless otherwise specified.
- (3) Typical specifications are specified at  $+25^\circ C$  and represent the most likely parametric norm.
- (4) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

**Electrical Characteristics<sup>(1)(2)</sup>**

 The following specifications apply for  $V_{DD} = 2.7V$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	LM4850		Units (Limits)
			Typical <sup>(3)</sup>	Limit <sup>(4)</sup>	
$I_{DD}$	Supply Current	BTL Mode; $V_{IN} = 0V$ ; $I_O = 0A$	1.8		mA
		SE Mode; $V_{IN} = 0V$ ; $I_O = 0A$	1.8		mA
$I_{SD}$	Shutdown Current	SD Mode	25		$\mu A$
$V_{OS}$	Output Offset Voltage	BTL Mode; $A_V = 2$ BTL OUT+ to BTL OUT-	5.0	40	mV
$P_O$	Output Power	BTL Mode; $R_L = 8\Omega$ THD+N = 1%	300		mW
		SE Mode; $R_L = 32\Omega$ THD+N = 1%	25		mW
$V_{IH}$	Shutdown Input Voltage High	$I_S < 80 \mu A$		2.0	V (min)
$V_{IL}$	Shutdown Input Voltage Low	$I_S > 0.5mA$		0.8	V (max)

- (1) Absolute Maximum Rating indicate limits beyond which damage to the device may occur.  
 (2) All voltages are measured with respect to the ground pin, unless otherwise specified.  
 (3) Typical specifications are specified at  $+25^\circ C$  and represent the most likely parametric norm.  
 (4) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

**External Components Description**

 (Refer to [Figure 1.](#))

Components		Functional Description
1.	$R_i$	Inverting input resistance which sets the closed-loop gain in conjunction with $R_f$ . This resistor also forms a high pass filter with $C_i$ at $f_c = 1/(2\pi R_i C_i)$ .
2.	$C_i$	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a highpass filter with $R_i$ at $f_c = 1/(2\pi R_i C_i)$ . Refer to the section, <a href="#">PROPER SELECTION OF EXTERNAL COMPONENTS</a> , for an explanation of how to determine the value of $C_i$ .
3.	$R_f$	Feedback resistance which sets the closed-loop gain in conjunction with $R_i$ .
4.	$C_s$	Supply bypass capacitor which provides power supply filtering. Refer to the <a href="#">POWER SUPPLY BYPASSING</a> section for information concerning proper placement and selection of the supply bypass capacitor.
5.	$C_B$	Bypass pin capacitor which provides half-supply filtering. Refer to the section, <a href="#">PROPER SELECTION OF EXTERNAL COMPONENTS</a> , for information concerning proper placement and selection of $C_B$ .
6.	$C_O$	Output coupling capacitor which blocks the DC voltage at the amplifier's output. Forms a high pass filter with the single-ended load $R_L$ at $f_o = 1/(2\pi R_L C_O)$ .

### Typical Performance Characteristics LD Specific Characteristics

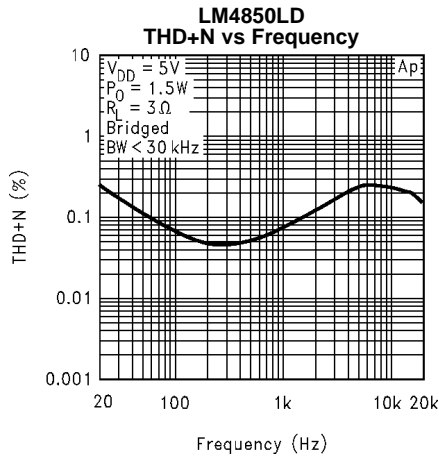


Figure 5.

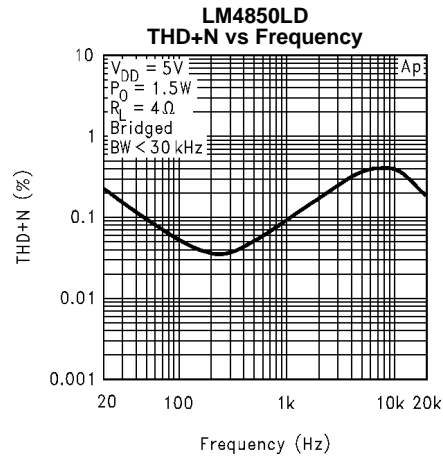


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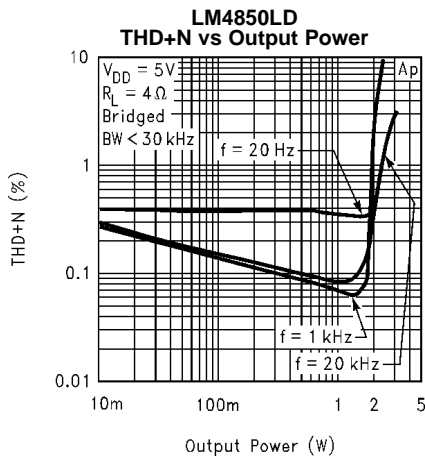


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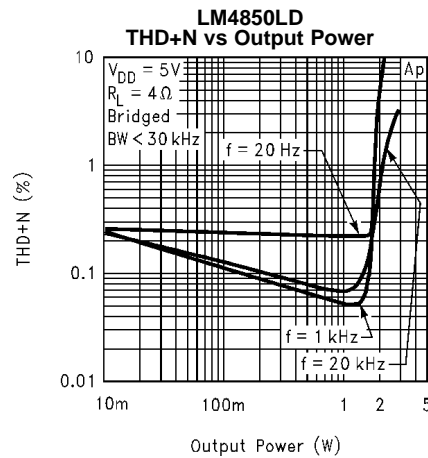


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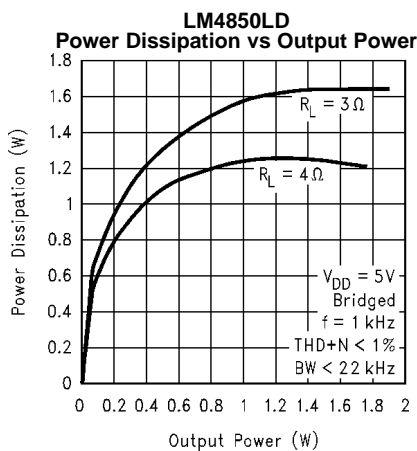


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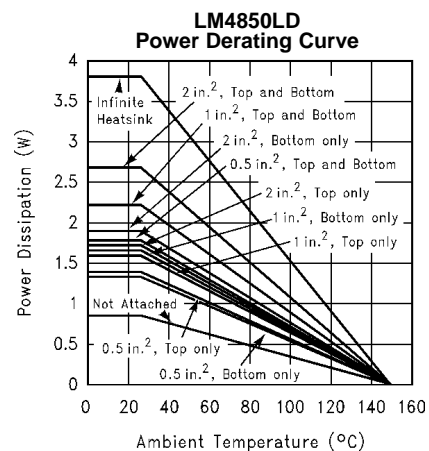


Figure 10.

This curve shows the LM4850LD's thermal dissipation ability at different ambient temperatures given the exposed-DAP of the part is soldered to a plane of 1oz. Cu with an area given in the label of each curve. This label also designated whether the plane exists on the same (top) layer as the chip, on the bottom layer, or on both layers. Infinite heatsink and unattached (no heatsink) conditions are also shown.

Typical Performance Characteristics  
Non-LD Specific Characteristics

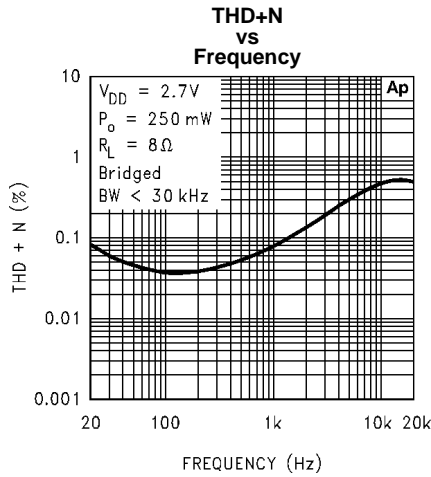


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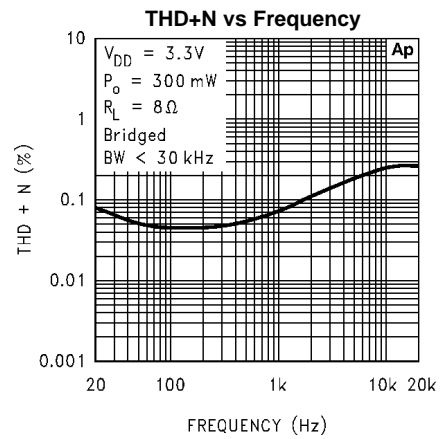


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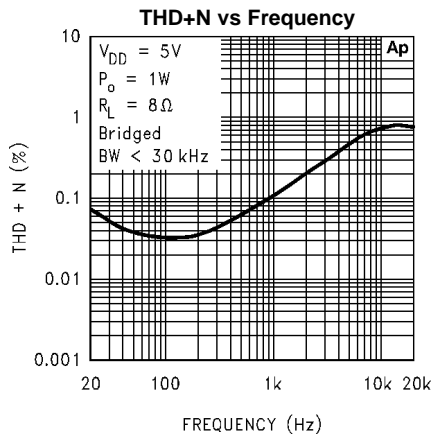


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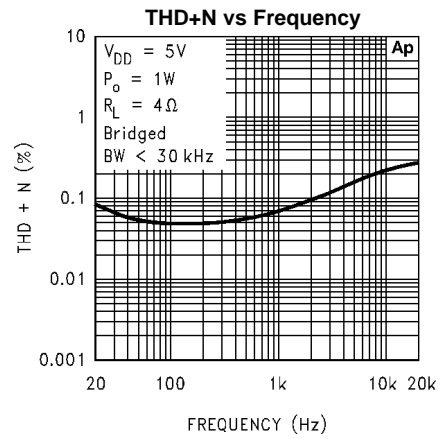


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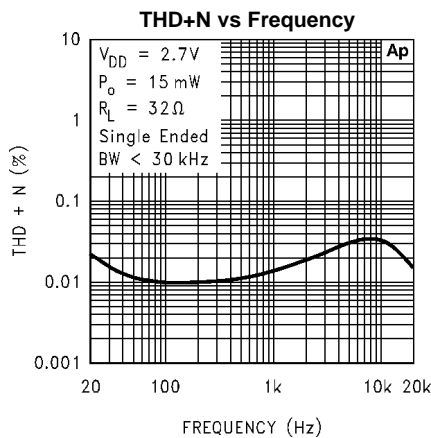


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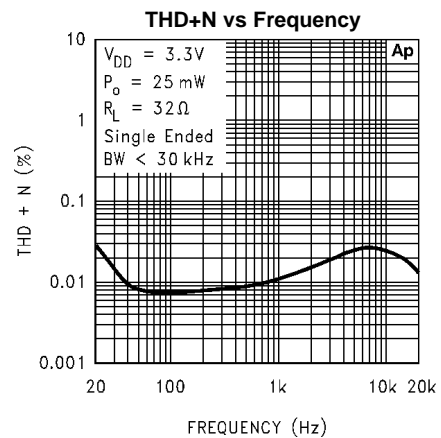


Figure 16.

Typical Performance Characteristics

Non-LD Specific Characteristics (continued)

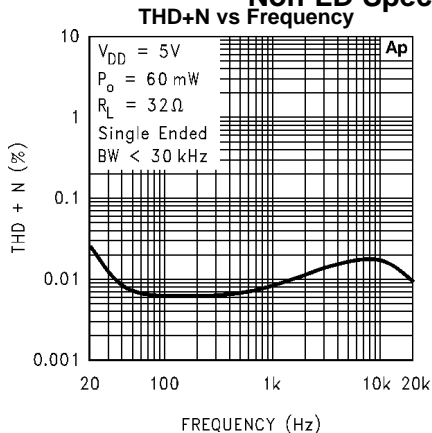


Figure 17.

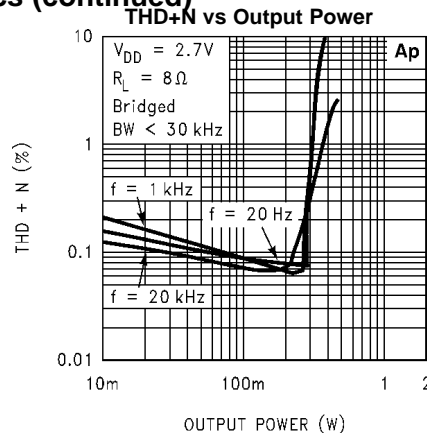


Figure 18.

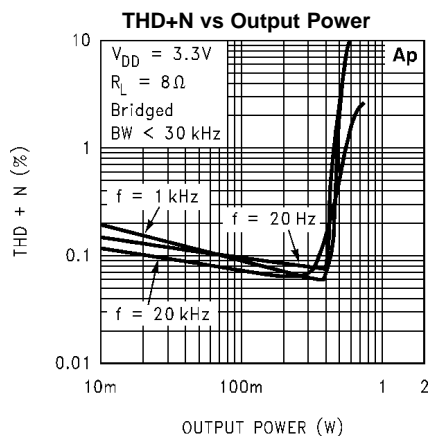


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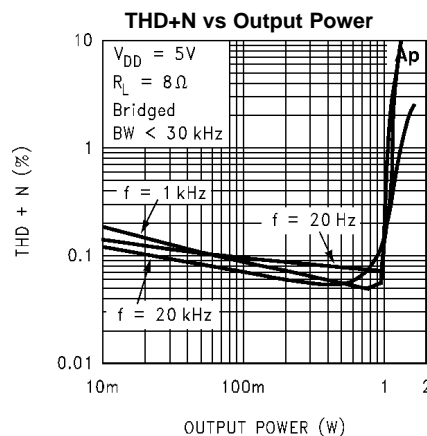


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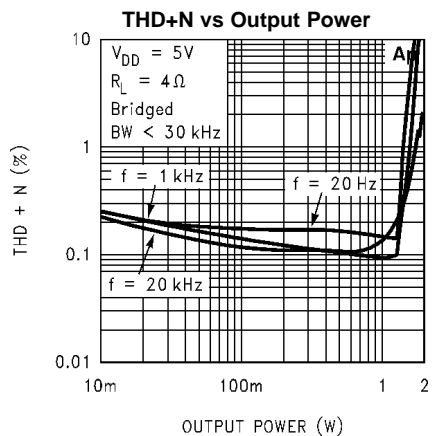


Figure 21.

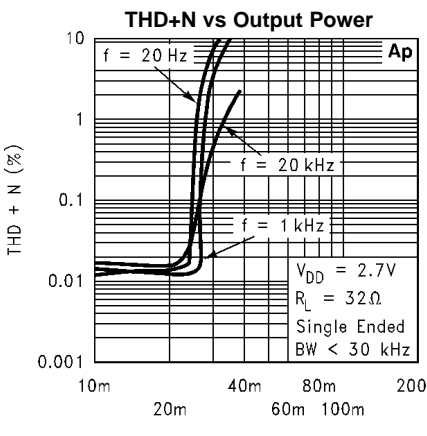


Figure 22.



Typical Performance Characteristics

Non-LD Specific Characteristics (continued)

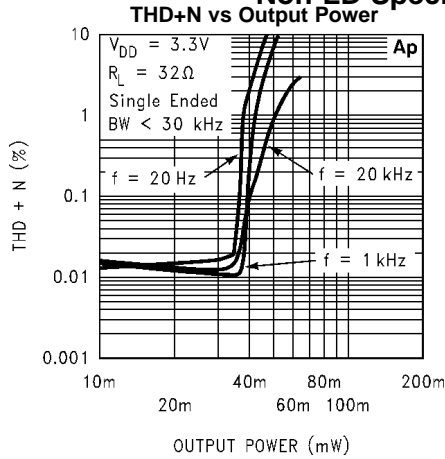


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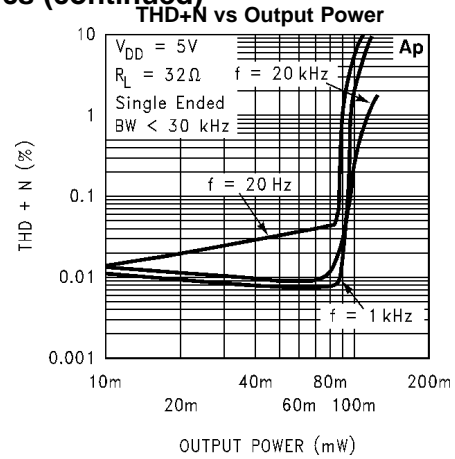


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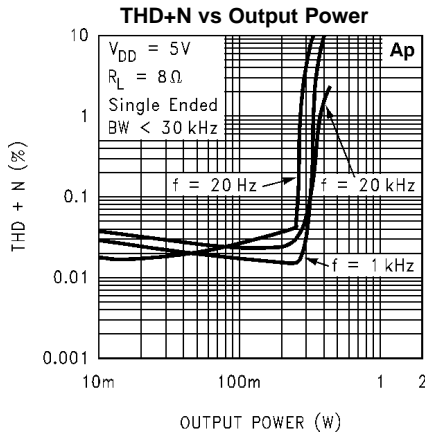


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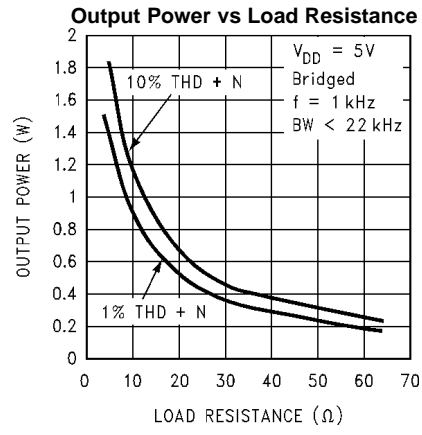


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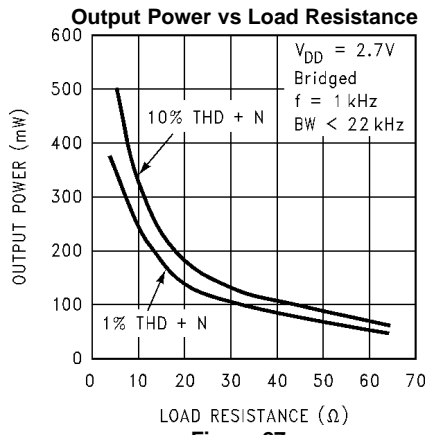


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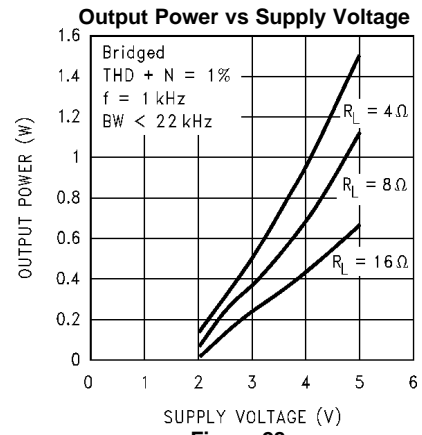


Figure 28.

Typical Performance Characteristics

Non-LD Specific Characteristics (continued)

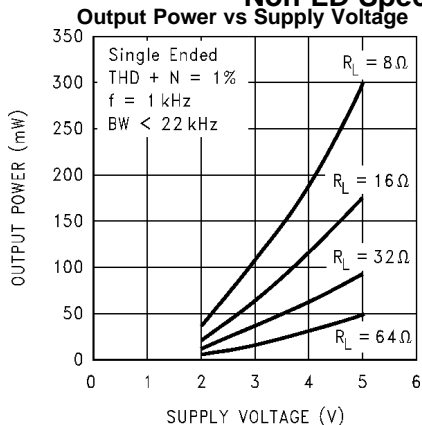


Figure 29.

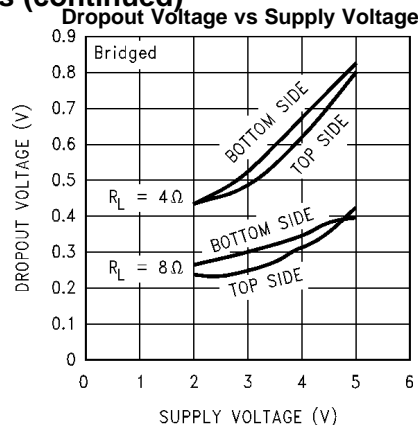


Figure 30.

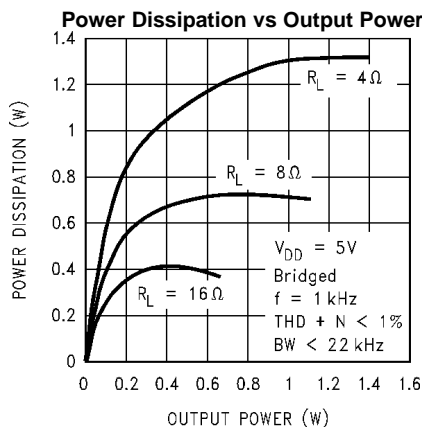


Figure 31.

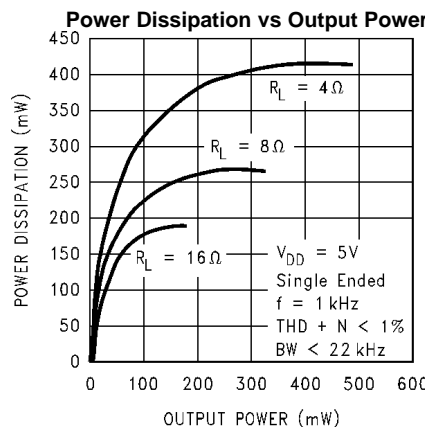


Figure 32.

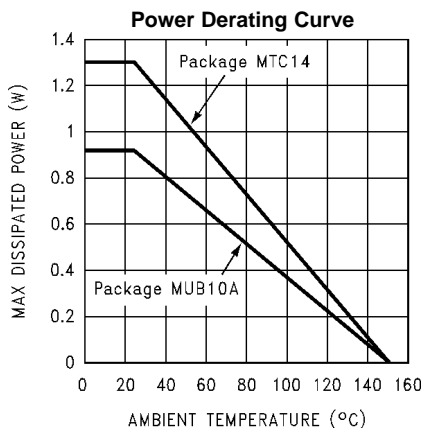


Figure 33.

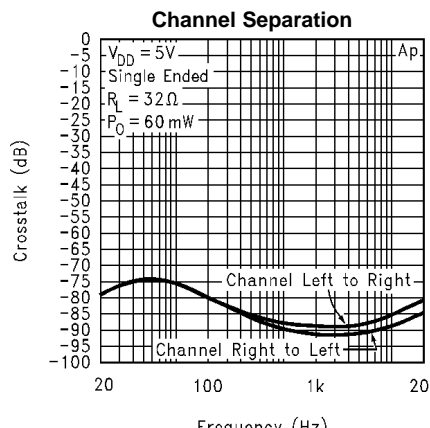


Figure 34.

Typical Performance Characteristics

Non-LD Specific Characteristics (continued)

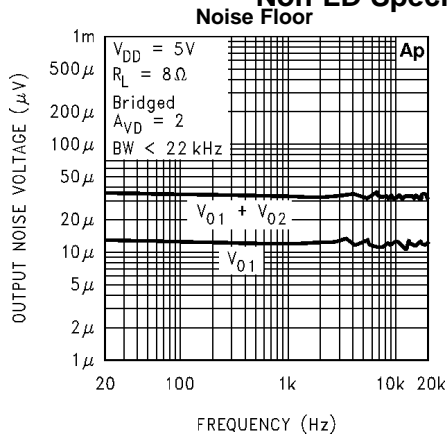


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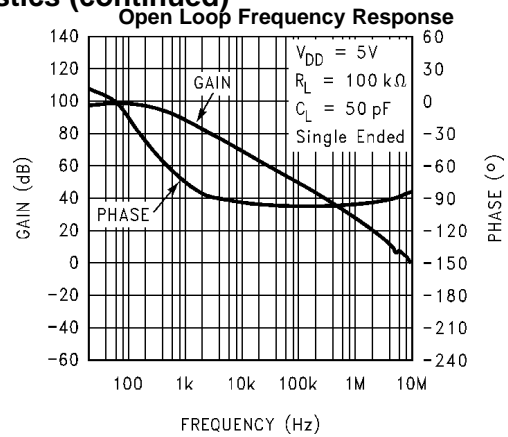


Figure 36.

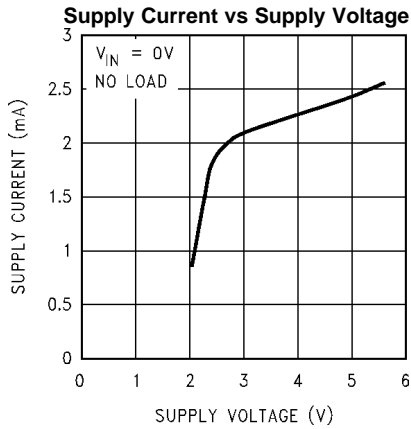


Figure 37.

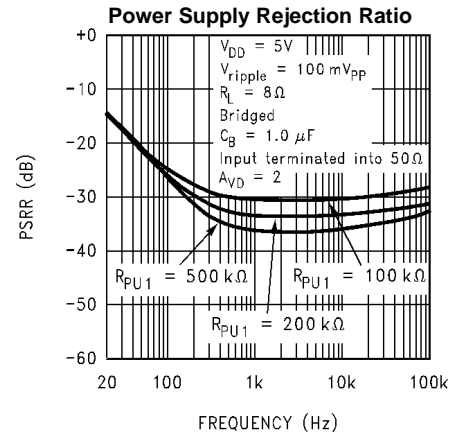


Figure 38.

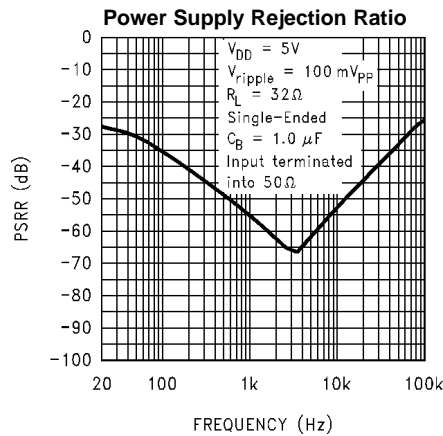


Figure 39.

## APPLICATION INFORMATION

### BRIDGED AND SINGLE-ENDED OPERATION

As shown in [Figure 1](#), the LM4850 contains three operational amplifiers (A1-A3). These amplifiers can be configured for SE or BTL modes.

In the SE mode, the LM4850 operates as a high current output dual op amp. A1 and A3 are independent amplifiers with an externally configured gain of  $A_V = -R_F/R_I$ . The outputs of A1 and A3 are used to drive an external set of headphones plugged into the headphone jack. Amplifier A2 is shut down to a high output impedance state in SE mode. This prevents any current flow into the mono bridge-tied load, thereby muting it.

In BTL mode, A3 is shut down to a high impedance state. The audio signal from the RIGHT IN pin is directed to the inverting input of A1. As a result, the LEFT IN and RIGHT IN audio signals,  $V_{INL}$  and  $V_{INR}$ , are summed together at the input of A1. A2 is then activated with a closed-loop gain of  $A_V = -1$  fixed by two internal 20k $\Omega$  resistors. The outputs of A1 and A2 are then used to drive the mono bridged-tied load.

### EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATION

The LM4850's exposed-DAP (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air. The result is a low voltage audio power amplifier that produces 1.7W at  $\leq 1\%$  THD+N with a 4 $\Omega$  load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4850's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The LD package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with 4(2x2) vias. The via diameter should be 0.012in-0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plating through the vias.

Best thermal performance is achieved with the largest practical heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in<sup>2</sup> area is necessary for 5V operation with a 4 $\Omega$  load. Heatsink areas not placed on the same PCB layer as the LM4850 should be 5in<sup>2</sup> (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. The LM4850's power de-rating curve in the [Typical Performance Characteristics](#) shows the maximum power dissipation versus temperature. An example PCB layout for the LD package is shown in the [Demonstration Board Layout](#) section. Further detailed and specific information concerning PCB layout, fabrication, and mounting an LD (WSON) package is available from Texas Instruments' Package Engineering Group under application note AN1187 ([SNOA401](#)).

### BRIDGE CONFIGURATION EXPLANATION

When the LM4850 is in BTL mode, the output of amplifier A1 serves as the input to amplifier A2, which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the mono channel is:

$$A_{VD} = V_{OUT} / (V_{INL} + V_{INR}) = 2 \times (R_F / R_I) \quad (1)$$

Driving a load differentially through the BTL OUT- and BTL OUT+ outputs is an amplifier configuration commonly referred to as "bridged mode". Bridged mode operation is different from the classical single-ended amplifier configuration where one side of its load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration. It drives a load differentially, which doubles output swing for a specified supply voltage. This produces four times the output power as that produced by a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive output signal clipping, please refer to the [AUDIO POWER AMPLIFIER DESIGN Design a 1W / 8 \$\Omega\$  Bridged Audio Amplifier](#) section.

A bridge configuration, such as the one used in LM4850, also creates a second advantage over single-ended amplifiers. Since the differential outputs, BTL OUT- and BTL OUT+, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for the output coupling capacitor that a single supply, single-ended amplifier configuration requires. Eliminating an output coupling capacitor in a single-ended configuration forces the half-supply bias voltage across the load. This increases internal IC power dissipation and may cause permanent loudspeaker damage.

## POWER DISSIPATION

Whether the power amplifier is bridged or single-ended, power dissipation is a major concern when designing the amplifier. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified load.

$$P_{\text{DMAX}} = (V_{\text{DD}})^2 / (2\pi^2 R_L): \text{Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Equation 3 states the maximum power dissipation point for a bridge amplifier operating at the same given conditions.

$$P_{\text{DMAX}} = 4 \times (V_{\text{DD}})^2 / (2\pi^2 R_L): \text{Bridge Mode} \quad (3)$$

The LM4850 is designed to drive either two single-ended loads simultaneously or one mono bridged-tied load. In SE mode, the maximum internal power dissipation is 2 times that of Equation 2. In BTL mode, the maximum internal power dissipation is the result of Equation 3. Even with this substantial increase in power dissipation, the LM4850 does not require heatsinking. The power dissipation from Equation 3 must not be greater than the power dissipation predicted by Equation 4:

$$P_{\text{DMAX}} = (T_{\text{JMAX}} - T_{\text{A}}) / \theta_{\text{JA}} \quad (4)$$

For the package PW14,  $\theta_{\text{JA}} = 150^\circ\text{C/W}$ , and for the package MUA10A,  $\theta_{\text{JA}} = 194^\circ\text{C/W}$ .  $T_{\text{JMAX}} = 150^\circ\text{C}$  for the LM4850. Depending on the ambient temperature,  $T_{\text{A}}$ , of the surroundings, Equation 4 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 3 is greater than that of Equation 4, then either the supply voltage must be decreased, the load impedance increased, or the ambient temperature reduced. For the typical application of a 5V power supply, and an  $8\Omega$  bridged load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately  $55^\circ\text{C}$  for package PW. This assumes the device operates at maximum power dissipation and uses surface mount packaging. Internal power dissipation is a function of output power. If typical operation is not around the maximum power dissipation point, operation at higher ambient temperatures is possible. Refer to the [Typical Performance Characteristics](#) curves for power dissipation information for different output power levels.

## POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. The value of the pin bypass capacitor,  $C_{\text{B}}$ , directly affects the LM4850's half-supply voltage stability and PSRR. The stability and supply rejection increase as the bypass capacitor's value increases. Typical applications employ a 5V regulator with a  $10\mu\text{F}$  and a  $0.1\mu\text{F}$  bypass capacitors which aid in supply filtering. This does not eliminate the need for bypassing the supply nodes of the LM4850. The selection of bypass capacitors, especially  $C_{\text{B}}$ , is thus dependent upon desired PSRR requirements, click and pop performance, system cost, and size constraints.

## SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4850 features amplifier bias circuitry shutdown. This shutdown function is activated by applying a logic high to the SHUTDOWN pin. The trigger point is 2.0V minimum for a logic high level, and 0.8V maximum for a logic low level. It is best to switch between ground and the supply,  $V_{\text{DD}}$ , to ensure correct shutdown operation. By switching the SHUTDOWN pin to  $V_{\text{DD}}$ , the LM4850 supply current draw will be minimized in idle mode. Whereas the device will be disabled with shutdown voltages less than  $V_{\text{DD}}$ , the idle current may be greater than the typical value of  $44\mu\text{A}$ . In either case, the SHUTDOWN pin should be tied to a fixed voltage to avoid unwanted state changes.



## PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical for optimum device and system performance. While the LM4850 is tolerant to a variety of external component combinations, consideration must be given to the external component values that maximize overall system quality.

The LM4850's unity-gain stability allows a designer to maximize system performance. The LM4850's gain should be set no higher than necessary for any given application. A low gain configuration maximizes signal-to-noise performance and minimizes THD+N. However, a low gain configuration also requires large input signals to obtain a given output power. Input signals equal to or greater than  $1V_{RMS}$  are available from sources such as audio codecs. Please refer to the section, [AUDIO POWER AMPLIFIER DESIGN](#), for a more complete explanation of proper gain selection.

### Selecting Input and Output Capacitor Values

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in [AUDIO POWER AMPLIFIER DESIGN](#). The input coupling capacitor  $C_i$  and resistor  $R_i$  form a first order high pass filter that limits low frequency response.  $C_i$ 's value should be based on the desired frequency response weighed against the following: Large value input and output capacitors are both expensive and space consuming for portable designs. Clearly a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Thus, large value input and output capacitors may not increase system performance.

## AUDIO POWER AMPLIFIER DESIGN

### Design a 1W / 8Ω Bridged Audio Amplifier

Given:

- Power Output:  $1W_{RMS}$
- Load Impedance  $8\Omega$
- Input Level:  $1V_{RMS}$
- Input Impedance:  $20k\Omega$
- Bandwidth: 100Hz - 20kHz  $\pm$  0.25dB

A designer must first determine the minimum supply voltage needed to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the [Typical Performance Characteristics LD Specific Characteristics](#) section, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required  $V_{OPEAK}$  using [Equation 5](#) and add the dropout voltage. This results in [Equation 6](#), where  $V_{ODTOP}$  and  $V_{ODBOT}$  are extrapolated from the Dropout Voltage vs Supply Voltage curve in the [Typical Performance Characteristics](#) section.

$$V_{OPEAK} = \sqrt{2 R_L P_O} \quad (5)$$

$$V_{DD} \geq (V_{OPEAK} + (V_{ODTOP} + V_{ODBOT})) \quad (6)$$

Using the Output Power vs Supply Voltage graph for an  $8\Omega$  load, the minimum supply rail is 4.7V. But since 5V is a standard supply voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4850 to reproduce peaks in excess of 1W without producing audible distortion. However, the designer must make sure that the chosen power supply voltage and output load does not violate the conditions explained in the [POWER DISSIPATION](#) section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from [Equation 7](#).

$$A_{VD} \geq \sqrt{P_O R_L} / (V_{IN}) = V_{ORMS} / V_{INRMS} \quad (7)$$

$$R_F / R_I = A_{VD} / 2 \quad (8)$$

From [Equation 6](#), the minimum  $A_{VD}$  is 2.83; use  $A_{VD} = 3$ .

The desired input impedance was  $20k\Omega$ , and with an  $A_{VD}$  of 3, using [Equation 8](#) results in an allocation of  $R_I = 20k\Omega$  and  $R_F = 30k\Omega$ .



The final design step is to set the amplifier's  $-3\text{dB}$  frequency bandwidth. To achieve the desired  $\pm 0.25\text{dB}$  pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The variation for both response limits is  $0.17\text{dB}$ , well within the  $\pm 0.25\text{dB}$  desired limit. This results in:

$$f_L = 100\text{Hz} / 5 = 20\text{Hz} \quad (9)$$

$$f_H = 20\text{kHz} \times 5 = 100\text{kHz} \quad (10)$$

As stated in the [External Components Description](#) section,  $R_1$  in conjunction with  $C_1$  create a highpass filter. Find the coupling capacitor's value using [Equation 9](#).

$$C_1 \geq 1 / (2\pi R_1 f_L) \quad (11)$$

$$C_1 \geq 1 / (2\pi \times 20\text{k}\Omega \times 20\text{Hz}) = 0.397\mu\text{F} \quad (12)$$

Use a  $0.39\mu\text{F}$  capacitor, the closest standard value.

The high frequency pole is determined by the product of the desired high frequency pole,  $f_H$ , and the differential gain,  $A_{VD}$ . With  $A_{VD} = 3$  and  $f_H = 100\text{kHz}$ , the resulting  $\text{GBWP} = 150\text{kHz}$  which is much smaller than the LM4850  $\text{GBWP}$  of  $10\text{MHz}$ . This difference indicates that a designer can still use the LM4850 at higher differential gains without bandwidth limitations.

## PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING $3\Omega$ AND $4\Omega$ LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependant on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example,  $0.1\Omega$  trace resistance reduces the output power dissipated by a  $4\Omega$  load from  $2.0\text{W}$  to  $1.95\text{W}$ . This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

## Demonstration Board Layout

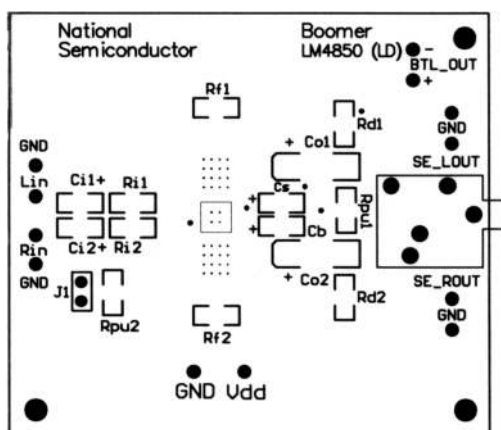


Figure 41. Recommended LD PC Board Layout:  
Component-Side SilkScreen



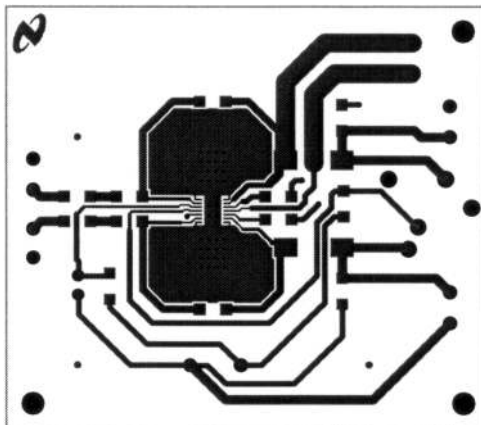


Figure 42. Recommended LD PC Board Layout:  
Component-Side Layout

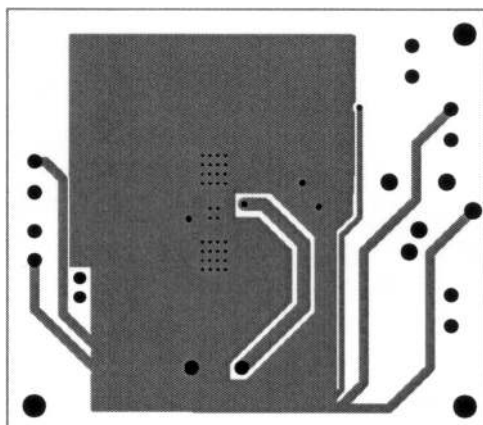


Figure 43. Recommended LD PC Board Layout:  
Bottom-Side Layout

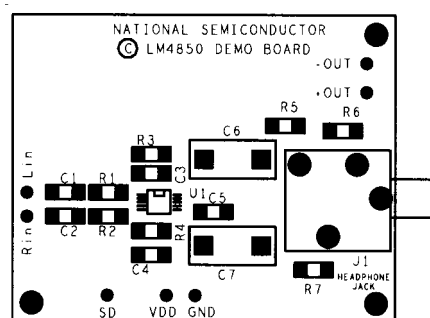
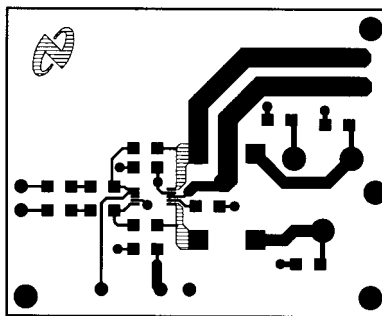
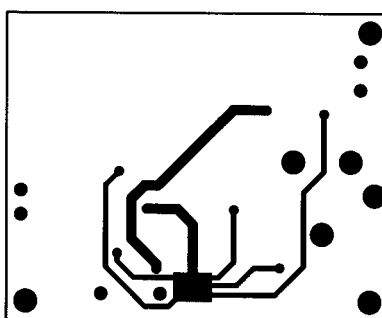


Figure 44. Recommended MM PC Board Layout:  
Component-Side SilkScreen



**Figure 45. Recommended MM PC Board Layout:  
Component-Side Layout**



**Figure 46. Recommended MM PC Board Layout:  
Bottom-Side Layout**

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