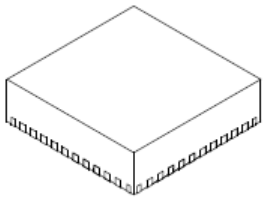
Bi-CMOS Linear Integrated Circuit, Silicon Monolithic

TB9053FTG,TB9054FTG

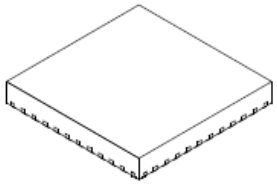
PWM-type, dual-channel, H-bridge, brushed DC motor driver for automotive application

TB9053FTG



P-LQFN40-0606-0.50-001

TB9054FTG



P-VQFN40-0606-0.50-004

1. Overview

TB9053FTG and TB9054FTG integrated circuit (IC) incorporates in each two output driver channels for direct drive of a brushed DC motor for automotive application.

PWM control with low on-resistance enables highly efficient motor drive output.
The PWM1 and PWM2 pins specify forward, reverse, or brake modes for motor 1, and the PWM3 and PWM4 pins specify these modes for motor 2. The ENABLE pins (EN1/ENB1 and EN2/ENB2) specify drive or stop mode for the motor.
The ISEL1 pin specifies whether the motor drive uses the PWM1 and PWM2 pins or SPI.
The ISEL2 pin specifies whether the motor drive uses the PWM3 and PWM4 pins or SPI.
The output current capacity is 6.5 A (typ.), which is suitable for a wide range of automotive applications such as control of the throttle valve, various engine valves, retractable door mirrors, and seat heater.

2. Application

Automotive applications such as control of the throttle valve, various engine valves, retractable door mirrors, and seat heater.

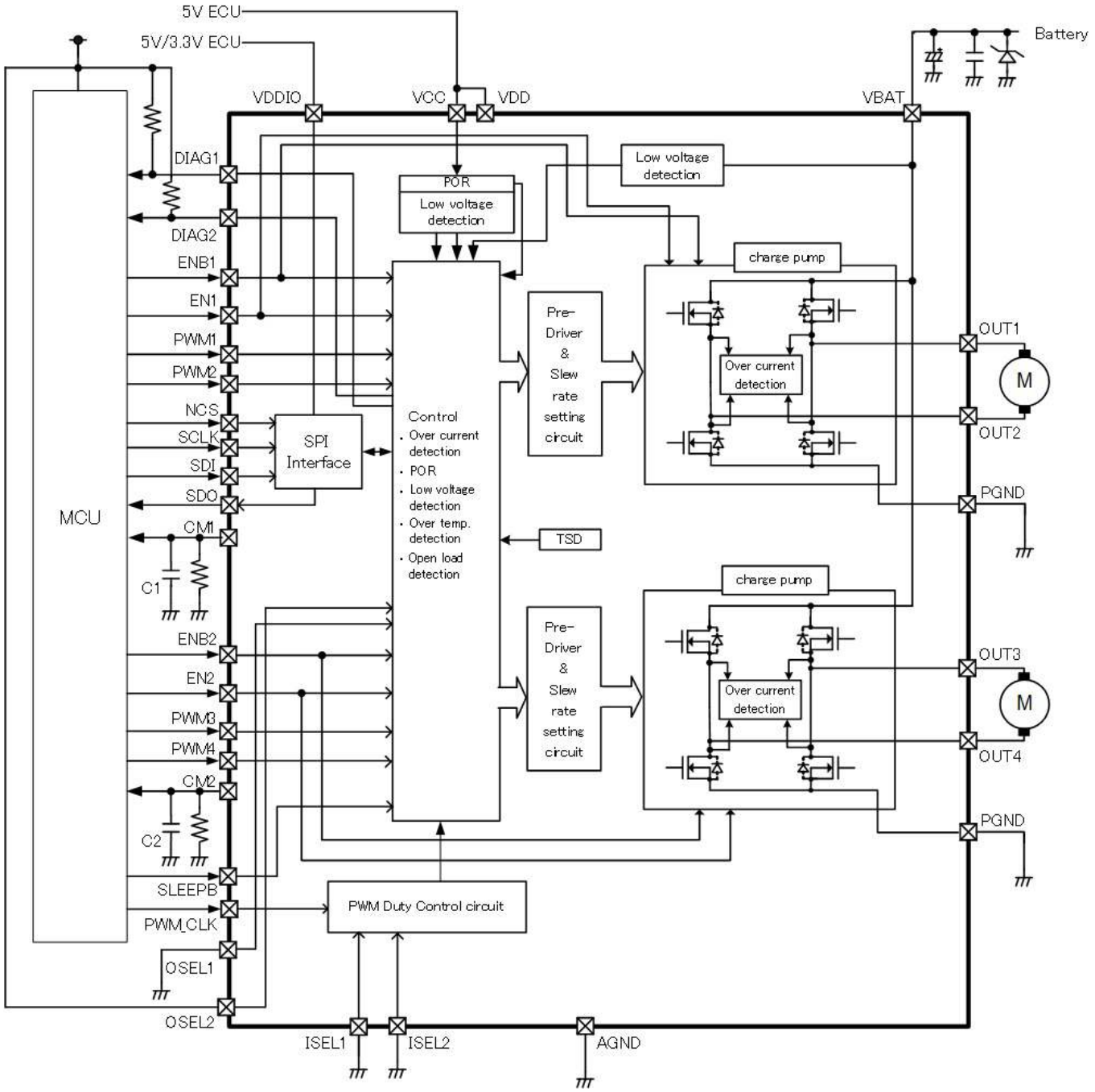
3. Features

- Motor driver block: Dual-channel, H-bridge driver
  (Ron(Nch+Nch)) < 350 mΩ (Max @ Tj = 150°C, VBAT = 8 V)
  Dual-Channel Mode and Combined-Channel Mode selectable, connecting two outputs externally allows this IC to function as a single-channel H-bridge circuit and the device is also used as a 4-channel Half Bridge driver.
- Detection features: Over-current detection, over-temperature detection, VBAT under-voltage detection, and VCC under-voltage detection
- Initial diagnosis: Power supply fault detection circuit (VBAT under-voltage and VCC under-voltage)
- PWM control output
- Forward/reverse/brake modes
- Current limit control: Chopper-type current limiter
- High-side output current monitoring function (CM1 and CM2 pins)
- Open-load detection: During operation/non-operation
- DIAG output (DIAG1 and DIAG2 pins)
- H-Bridge Mode/Half-Bridge Mode selectable (OSEL1 and OSEL2 pins)
- Low-power Sleep Mode
- Through-current prevention circuit
- AEC-Q100/AEC-Q006 Capable

- SPI communication: fault reporting, device settings and motor control through the SPI registers
- Operating voltage range: VBAT = 4.5 to 28 V (absolute rating of power supply voltage = 40 V (max.) (0.5 s))
  VCC = 4.5 to 5.5 V
  VDDIO = 3.0 to 5.5 V
- Operating temperature range: Ta = -40 to 125°C
- Small flat package: TB9053FTG(P-LQFN40-0606-0.50-001),
- TB9054FTG(P-VQFN40-0606-0.50-004)

- If the label of the shipping box indicates "[[G]]/RoHS COMPATIBLE", "[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s)", "RoHS COMPATIBLE", or "RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV", then this product is compatible with the EU RoHS Directive (2011/65/EU) in the manner the indication states.

4. Block diagram



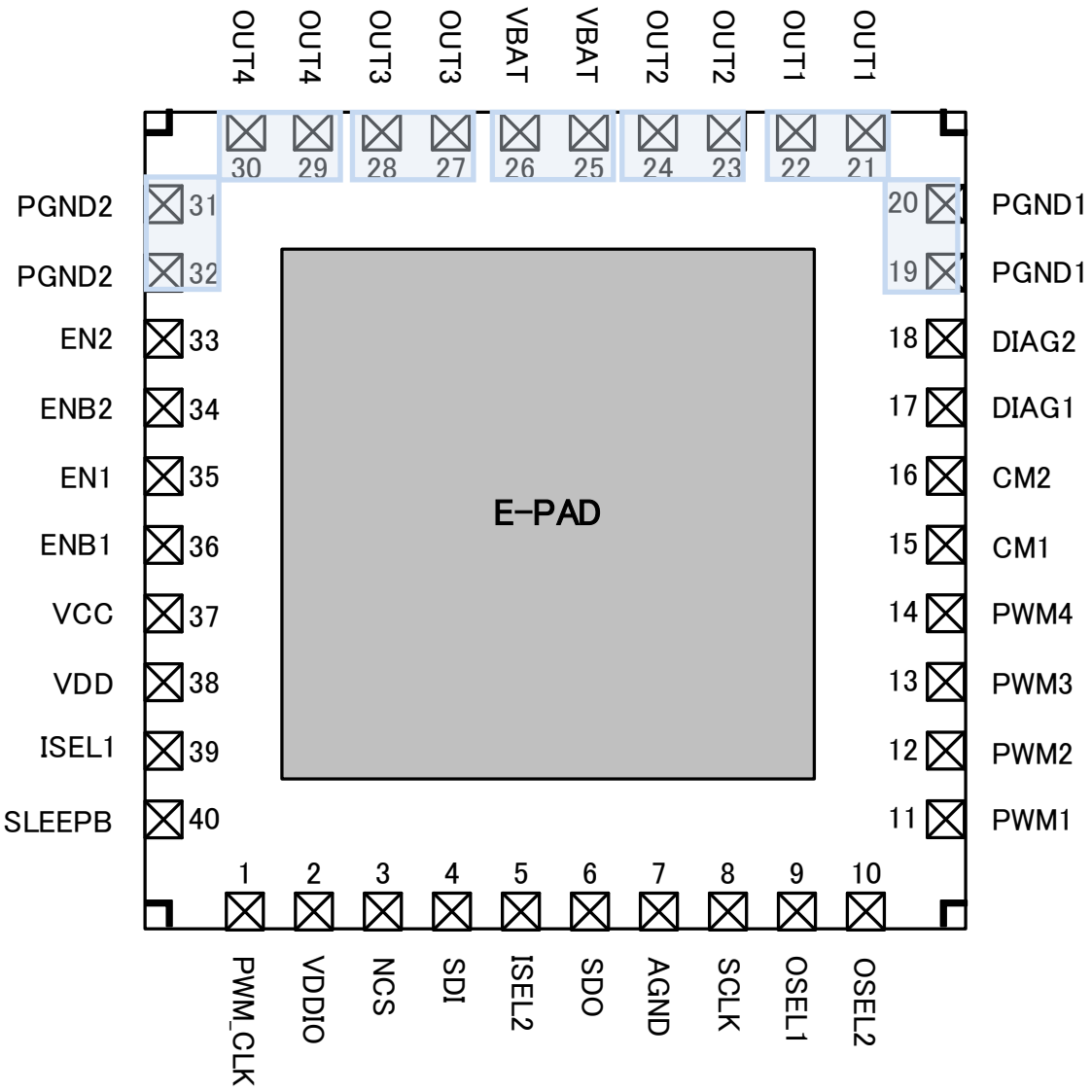
C1,C2 capacitance value: 0.1μF to 1μF

Figure 4.1. Block diagram

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.
The signal supplied to each driver output circuit is not generated by a logical operation between the EN and ENB pin inputs, the independent EN and ENB signals are directly supplied to each driver output circuit Instead.

5. Pin assignment

Pin assignment (top view)



Pins short-circuited on the frame: 19-20
21-22
23-24
25-26
27-28
29-30
31-32

Figure 5.1. Pin assignment

6. Pin description

6.1. Pin description

Table 6.1. Pin description

Pin No.	Pin name	Input/ output	Pin description	Remarks
Corner pin (E-PAD)				
1	PWM_CLK	IN	External MCU inputs PWM_CLK; used for the IC clock during PWM operation	Pull-down
2	VDDIO	Power supply	Power supply for SPI	
3	NCS	IN	SPI input (chip select)	Pull-up
4	SDI	IN	SPI input (DATA)	Pull-down
5	ISEL2	IN	Select pin for SPI or direct PWM	Pull-down
6	SDO	OUT	SPI output (DATA output)	
7	AGND	GND	Analog GND	
8	SCLK	IN	SPI input (CLK)	Pull-down
9	OSEL1	IN	Select pin for Half Mode	Pull-down
10	OSEL2	IN	Select pin for SMALL (2 channels) or LARGE (combined channel) Mode	Pull-down
Corner pin (E-PAD)				
11	PWM1	IN	PWM input	Pull-down
12	PWM2	IN	PWM input	Pull-down
13	PWM3	IN	PWM input	Pull-down
14	PWM4	IN	PWM input	Pull-down
15	CM1	OUT	CM output(Composed of 5V system circuit)*2	
16	CM2	OUT	CM output(Composed of 5V system circuit)*2	
17	DIAG1	OUT	DIAG output (open-drain) (*1)	
18	DIAG2	OUT	DIAG output (open-drain) (*1)	
19	PGND1	GND	Power GND	
20	PGND1	GND	Power GND	
Corner pin (E-PAD)				
21	OUT1	OUT	Motor output 1	
22	OUT1	OUT	Motor output 1	
23	OUT2	OUT	Motor output 2	
24	OUT2	OUT	Motor output 2	
25	VBAT	Power supply	Battery voltage	
26	VBAT	Power supply	Battery voltage	
27	OUT3	OUT	Motor output 3	
28	OUT3	OUT	Motor output 3	
29	OUT4	OUT	Motor output 4	
30	OUT4	OUT	Motor output 4	

Pin No.	Pin name	Input/ output	Pin description	Remarks
Corner pin (E-PAD)				
31	PGND2	GND	Power GND	
32	PGND2	GND	Power GND	
33	EN2	IN	EN input	Pull-down
34	ENB2	IN	ENB input	Pull-up
35	EN1	IN	EN input	Pull-down
36	ENB1	IN	ENB input	Pull-up
37	VCC	Power supply	VCC input	
38	VDD	Power supply	VDD input	
39	ISEL1	IN	Select pin for SPI or direct PWM	Pull-down
40	SLEEPB	IN	Sleep input	Pull-down

Note: Connect the corner pins and exposed-pad pins to GND in your system. No testing before shipment is performed on these pins.

*1: Connect the external pull-up resistors for the DIAG1 and DIAG2 pins to VDDIO (MCU power supply). If SPI communication is not used, connect the VDDIO pin and the external pull-up resistors for the DIAG1 and DIAG2 pins to the VCC power supply.

*2: The CM1/CM2 pins use a circuit with a 5 V power supply; if you use a 3 V MCU power supply, be careful not to exceed the absolute withstand voltage.

7. Function description

In the specifications below, DT and SB denote the motor drive operations "dead time" and "short brake", respectively.

7.1. Motor drive output circuit

The output circuit operates in the following modes (Table 7.1):
In Table 7.1 to Table 7.7, the following notation are used. X: Don't care, H: High, L: Low, and Z: High impedance.

	OSEL1	OSEL2
LARGE Mode (2 channels combined; 1 motor)	L	L
Half Mode	H	L
SMALL Mode (2 channels separate; 2 motors)	L	H
Prohibited Mode (motor output OFF)	H	H

Note: The OSEL1 and OSEL2 pin inputs are latched when the initial diagnosis starts. If the IC enters Prohibited Mode, reset the VCC power supply (by lowering it below the VCC under-voltage and POR detection voltage) to restart the IC.

7.1.1. Dual-Channel Mode (SMALL Mode) (OSEL1 = L and OSEL2 = H)

Table 7.1. H-bridge motor function 1

	PWM1	PWM2	EN1	ENB1	SLEEPB	**OUT1**	**OUT2**
Forward	H	L	H	L	H	**H**	**L**
Short brake	L	L	H	L	H	**L**	**L**
Reverse	L	H	H	L	H	**L**	**H**
Short brake	H	H	H	L	H	**H**	**H**
EN Disable	X	X	L	L	H	**Z**	**Z**
ENB Disable	X	X	H	H	H	**Z**	**Z**
Sleep Mode	X	X	X	L/H	L	**Z**	**Z**
EN Disconnected	X	X	Z	X	X	**Z**	**Z**
ENB Disconnected	X	X	X	Z	X	**Z**	**Z**
PWM1 Disconnected	Z	L/H	H	L	H	**L**	**L/H**
PMM2 Disconnected	L/H	Z	H	L	H	**L/H**	**L**

	PWM3	PWM4	EN2	ENB2	SLEEPB	**OUT3**	**OUT4**
Forward	H	L	H	L	H	**H**	**L**
Short brake	L	L	H	L	H	**L**	**L**
Reverse	L	H	H	L	H	**L**	**H**
Short brake	H	H	H	L	H	**H**	**H**
EN2 Disable	X	X	L	L	H	**Z**	**Z**
ENB2 Disable	X	X	H	H	H	**Z**	**Z**
Sleep Mode	X	X	X	L/H	L	**Z**	**Z**
EN2 Disconnected	X	X	Z	X	X	**Z**	**Z**
ENB2 Disconnected	X	X	X	Z	X	**Z**	**Z**
PWM3 Disconnected	Z	L/H	H	L	H	**L**	**L/H**
PMM4 Disconnected	L/H	Z	H	L	H	**L/H**	**L**

Note: When changing the motor rotation from forward to reverse or vice versa, always insert a regenerative brake. Otherwise, the IC may break down.
Note: When current limit control is applied, operation differs from the motor function table above. For details, refer to "7.7. Current limit control".
Note: The SLEEPB pin sets a low-power Sleep Mode. When SLEEPB = L, the system enters Sleep Mode. When SLEEPB = H, the system cancels Sleep Mode.
Note: When SLEEPB = L, the ENB1/2 pins does not use OPEN, set the ENB1/2 pins to L or H.

7.1.2. Combined-Channel Mode (LARGE Mode) (OSEL1 = L and OSEL2 = L)

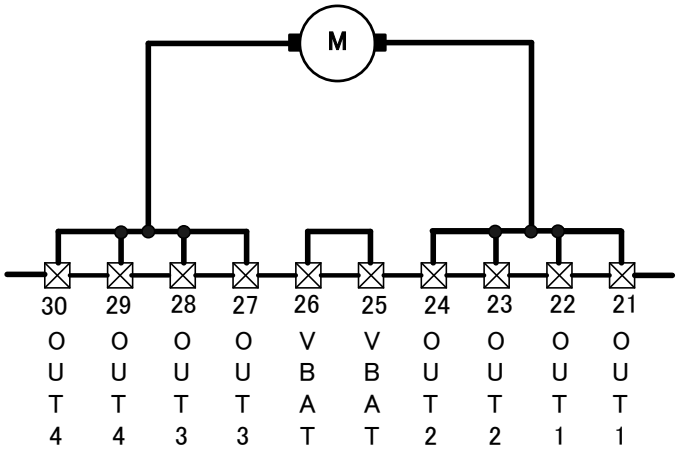
PWM3 and PWM4 are ineffective.
Externally short-circuit ISEL1/2, EN1/2, ENB1/2, OUT1/2, and OUT3/4.

Table 7.2. H-bridge motor function 2

	PWM1	PWM2	EN	ENB	SLEEPB	**OUT1/2**	**OUT3/4**
Forward	H	L	H	L	H	**H**	**L**
Short brake	L	L	H	L	H	**L**	**L**
Reverse	L	H	H	L	H	**L**	**H**
Short brake	H	H	H	L	H	**H**	**H**
EN Disable	X	X	L	L	H	**Z**	**Z**
ENB Disable	X	X	H	H	H	**Z**	**Z**
Sleep Mode	X	X	X	L/H	L	**Z**	**Z**
EN Disconnected	X	X	Z	X	X	**Z**	**Z**
ENB Disconnected	X	X	X	Z	X	**Z**	**Z**
PWM1 Disconnected	Z	L/H	H	L	H	**L**	**L/H**
PMM2 Disconnected	L/H	Z	H	L	H	**L/H**	**L**

Note: When SLEEPB = L, the ENB1/2 pins does not use OPEN, set the ENB1/2 pins to L or H.

- Combined-Channel Mode (LARGE Mode) uses the IC as a single-channel device by short-circuiting the outputs as follows:



7.1.3. Half Mode (OSEL1 = H and OSEL2 = L)

Table 7.3. Half-bridge motor functions

	PWM1	PWM2	EN1	ENB1	SLEEPB	**OUT1**	**OUT2**
OUT1 H	H	X	H	L	H	**H**	**X**
OUT1 L	L	X	H	L	H	**L**	**X**
OUT2 H	X	H	H	L	H	**X**	**H**
OUT2 L	X	L	H	L	H	**X**	**L**
EN Disable	X	X	L	L	H	**Z**	**Z**
ENB Disable	X	X	H	H	H	**Z**	**Z**
Sleep Mode	X	X	X	L/H	L	**Z**	**Z**
EN Disconnected	X	X	Z	X	X	**Z**	**Z**
ENB Disconnected	X	X	X	Z	X	**Z**	**Z**
PWM1 Disconnected	Z	L/H	H	L	H	**L**	**L/H**
PMM2 Disconnected	L/H	Z	H	L	H	**L/H**	**L**

Note: In Half-Bridge Mode, only the motor drive with the PWM1 and PWM2 pins is usable.
Note: In Half-Bridge Mode,Set the ISEL1 pin to L.
Note: In Half-Bridge Mode, If ISEL1 = H, the system enters Prohibited Mode (output OFF). During Prohibited Mode, Prohibited Mode (output OFF) is canceled when ISEL1 is set to L again.
Note: When SLEEPB = L, the ENB1/2 pins does not use OPEN, set the ENB1/2 pins to L or H.

	PWM3	PWM4	EN2	ENB2	SLEEPB	**OUT3**	**OUT4**
OUT3 H	H	X	H	L	H	**H**	**X**
OUT3 L	L	X	H	L	H	**L**	**X**
OUT4 H	X	H	H	L	H	**X**	**H**
OUT4 L	X	L	H	L	H	**X**	**L**
EN2 Disable	X	X	L	L	H	**Z**	**Z**
ENB2 Disable	X	X	H	H	H	**Z**	**Z**
Sleep Mode	X	X	X	L/H	L	**Z**	**Z**
EN2 Disconnected	X	X	Z	X	X	**Z**	**Z**
ENB2 Disconnected	X	X	X	Z	X	**Z**	**Z**
PWM3 Disconnected	Z	L/H	H	L	H	**L**	**L/H**
PMM4 Disconnected	L/H	Z	H	L	H	**L/H**	**L**

Note: In Half-Bridge Mode, only the motor drive with the PWM1 and PWM2 pins is usable.
Note: In Half-Bridge Mode,Set the ISEL1 pin to L.
Note: In Half-Bridge Mode, If ISEL1 = H, the system enters Prohibited Mode (output OFF). During Prohibited Mode, Prohibited Mode (output OFF) is canceled when ISEL1 is set to L again.
Note: When SLEEPB = L, the ENB1/2 pins does not use OPEN, set the ENB1/2 pins to L or H.

7.2. Notes on half-bridge usage

Using the OSEL1 pin sets this IC to function as a half-bridge circuit.
Note that the following functions are partially disabled.

See the following table:

Table 7.4. Half-bridge specifications

Half-bridge specifications	
VBAT under-voltage detection	Enabled
VCC under-voltage detection	Enabled
VCCPOR	Enabled
Output S/R	Enabled
Output dead time	Enabled
Current limit	Disabled
Current limit at high temperature	Disabled
TSD (over-temperature detection)	Enabled
ISD (over-current detection)	Enabled; however, output pins (OUT1/2/3/4) may individually enter a Hi-Z state, which only occurs in Half-Bridge Mode (Operation differs from the ISD function for H-Bridge Mode, in which OUT1/2 enter a Hi-Z state simultaneously)
DIAG	Enabled
CM (current monitor)	Disabled
Open load during operation	Disabled
Open load during non-operation	Disabled
Motor drive using SPI	Disabled
Cancellation of output OFF (Hi-Z) when the ISD (over-current detection) circuit is activated	Use SPI settings (write "1", one-shot pulse) to cancel the Hi-Z state (latched) individually for the output pins (OUT1/2/3/4); SPI communication is mandatory for Half-Bridge Mode

Note: When using the IC as a half-bridge circuit, there is no current-limit functionality, as no current-limit circuit is embedded in the upper part of the circuit. Therefore, the current increases until over-current is detected.

7.2.1. Dual-Channel Mode (SMALL Mode, which uses two channels)

Table 7.5. Function operation during abnormality detection (1)

	PWM1	PWM2	EN1	ENB1	OUT1	OUT2
Over-temperature detection 1 (*1)	・Regardless of the input signals, the motor output changes to OFF when an abnormality is detected ・Signals generated by various detection circuits trigger the function ・Upon the open load detection (during operation/non-operation), the motor output is not turned OFF but follows the input signals				Z	Z
Over-current detection					Z	Z
VBAT under-voltage detection					Z	Z
VCC under-voltage detection					Z	Z
Open-load detection (during operation)					L/H/Z	L/H/Z
Open-load detection (during non-operation)					L/H/Z	L/H/Z

	PWM3	PWM4	EN2	ENB2	OUT3	OUT4
Over-temperature detection 1 (*1)	・Regardless of the input signals, the motor output changes to OFF when an abnormality is detected ・Signals generated by various detection circuits trigger the function ・Upon the open load detection (during operation/non-operation), the motor output is not turned OFF but follows the input signals				Z	Z
Over-current detection					Z	Z
VBAT under-voltage detection					Z	Z
VCC under-voltage detection					Z	Z
Open-load detection (during operation)					L/H/Z	L/H/Z
Open-load detection (during non-operation)					L/H/Z	L/H/Z

*1: The detection signal of the over-temperature detection circuit retains its state even when VBAT falls below the under-voltage detection voltage.

7.2.2. Combined-Channel Mode (LARGE Mode, which uses the IC as one channel)

Table 7.6. Function operation during abnormality detection (2)

	PWM1	PWM2	EN1	ENB1	OUT1/2	OUT3/4
Over-temperature detection 1 (*1)	・Regardless of the input signals, the motor output changes to OFF when an abnormality is detected ・Signals generated by various detection circuits trigger the function ・Upon the open load detection (during operation/non-operation), the motor output is not turned OFF but follows the input signals				Z	Z
Over-current detection					Z	Z
VBAT under-voltage detection					Z	Z
VCC under-voltage detection					Z	Z
Open-load detection (during operation)					L/H/Z	L/H/Z
Open-load detection (during non-operation)					L/H/Z	L/H/Z

Note: In Combined-Channel Mode, (LARGE Mode), PWM3 and PWM4 are ineffective.
Note: In Combined-Channel Mode (LARGE Mode), externally short-circuit ISEL1/2, EN1/2, ENB1/2, OUT1/2, and OUT3/4.
*1: The detection signal of the over-temperature detection circuit retains its state even when VBAT falls below the under-voltage detection voltage.

Table 7.7. Output state

OUT	High-side driver	Low-side driver
H	ON	OFF
L	OFF	ON
Z	OFF (Hi-Z)	OFF (Hi-Z)

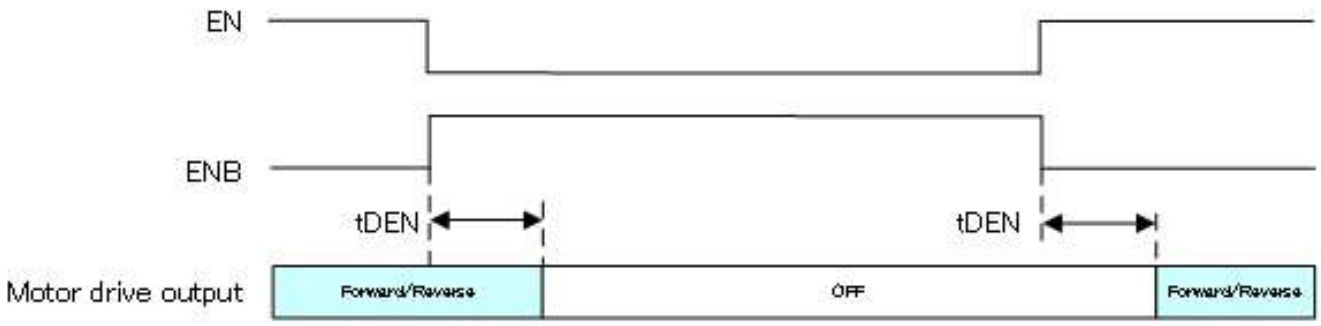


Figure 7.1. EN/ENB signals and motor drive output

Note: When disabling the output using the EN and ENB pins, the output changes to OFF without the inclusion of dead time.
Sleep Mode requires a recovery time, because the IC turns off its internal functions to reduce power consumption.

7.3. Slew rate

The following table shows the possible slew rate settings using SPI:

Table 7.8. Slew rate setting

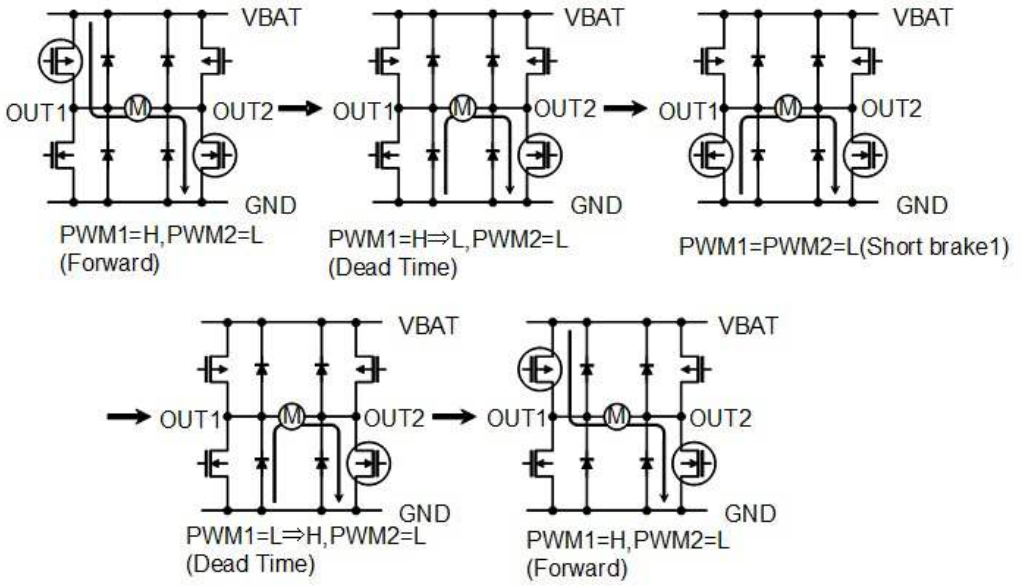
	Slew rate V/μs (design data)	(Reference) μs for 14 V (design data)	SPI setting
Slow1	1.09	12.80	CONFIG1/2 DATA[14:12] = 001
Slow2	2.19	6.40	CONFIG1/2 DATA[14:12] = 010
Slow3	4.38	3.20	CONFIG1/2 DATA[14:12] = 011
Slow4	8.75	1.60	CONFIG1/2 DATA[14:12] = 100
Normal	17.50	0.80	CONFIG1/2 DATA[14:12] = 000
Fast2	21.88	0.64	CONFIG1/2 DATA[14:12] = 101
Fast1	26.25	0.53	CONFIG1/2 DATA[14:12] = 110

7.4. Dead time

Dead time prevents motor output through-current. The system monitors the gate voltage of the internal DMOS. After detecting that the high side in the IC changes to OFF, the low side automatically changes to ON to prevent through-current.

7.5. PWM Function

7.5.1. PWM function (forward rotation, low-side regeneration) (EN=H, ENB=L) (Figure 7.2 and Figure 7.3)

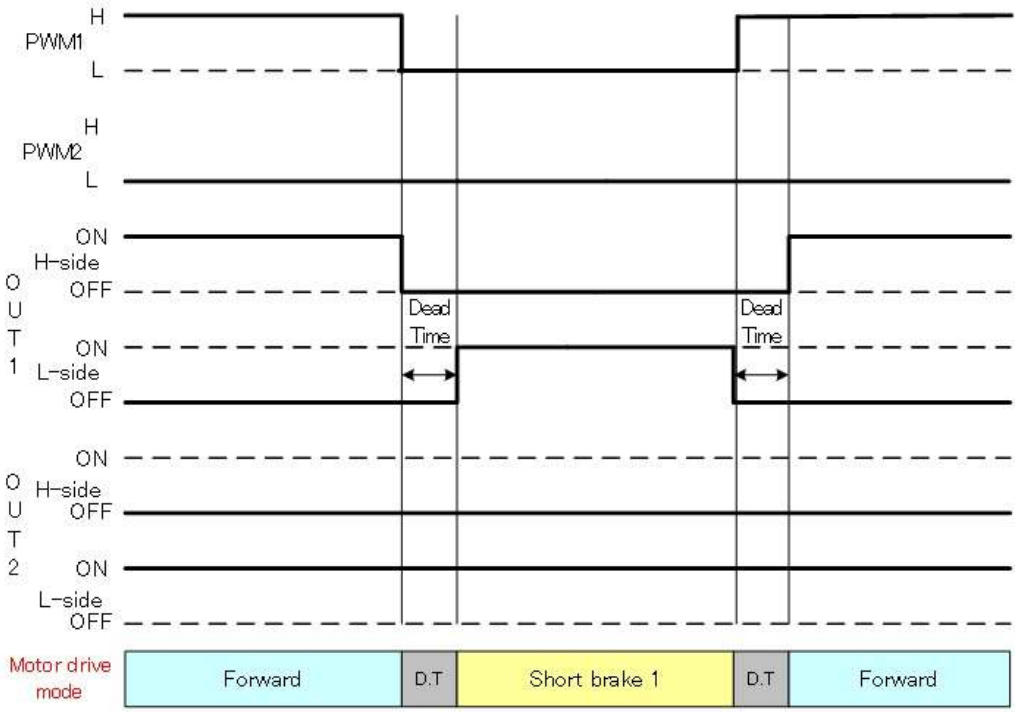


* ○ indicates a DMOS transistor that is ON.

Figure 7.2. Current path for PWM function (forward rotation, low-side regeneration)

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

7.5.2. PWM function (forward) timing chart



* D.T: Dead time

Figure 7.3. PWM function (forward rotation, low-side regeneration) timing chart

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.5.3. PWM function (forward rotation, high-side regeneration) (EN=H, ENB=L)(Figure 7.4 and Figure 7.5)

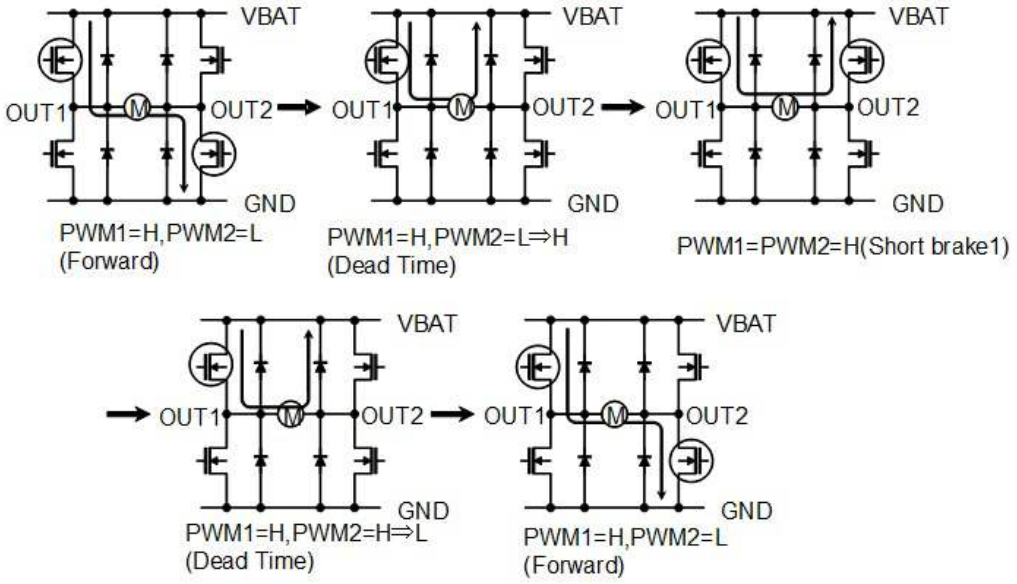
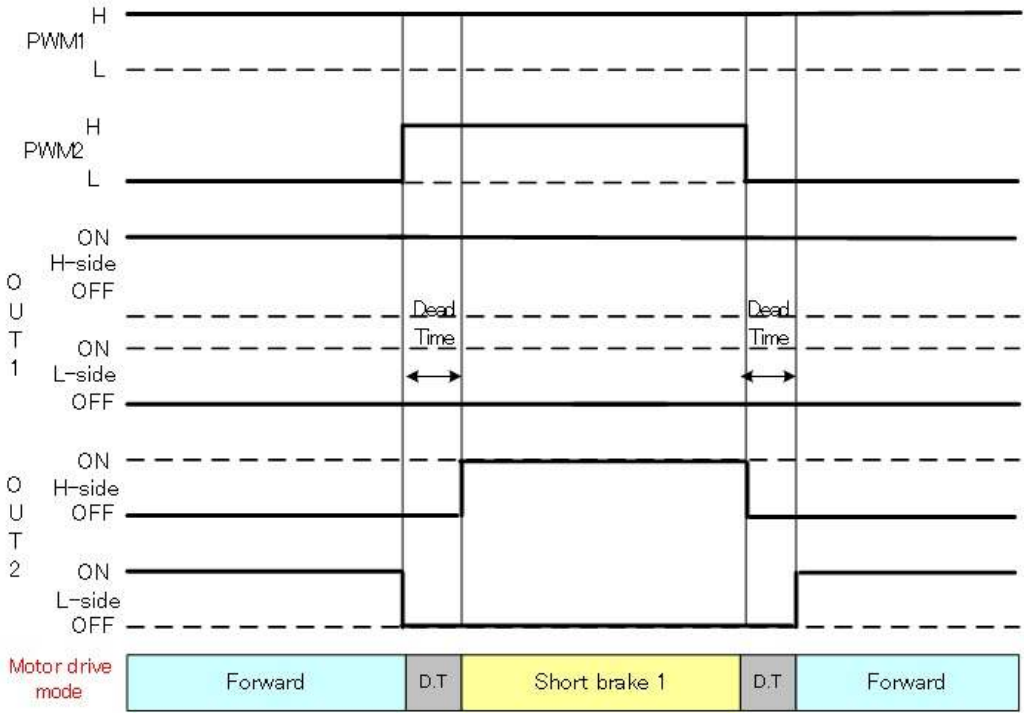


Figure 7.4. Current path for PWM function (forward rotation, high-side regeneration)

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

7.5.4. PWM function (forward) timing chart

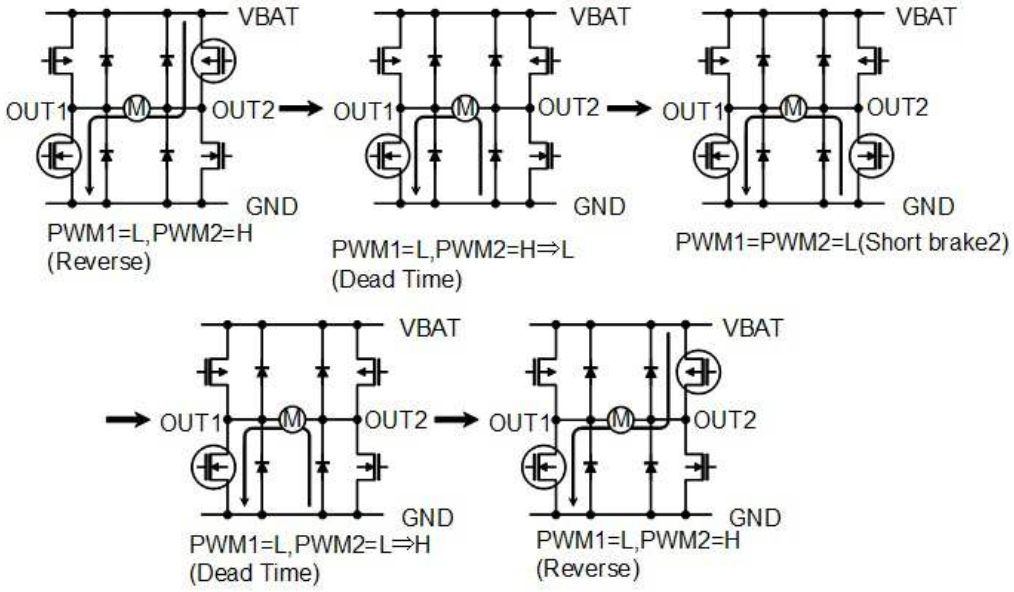


* D.T: Dead time

Figure 7.5. PWM function (forward rotation, high-side regeneration) timing chart

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.5.5. PWM function (reverse rotation, low-side regeneration) (EN=H, ENB=L)(Figure 7.6 and Figure 7.7)

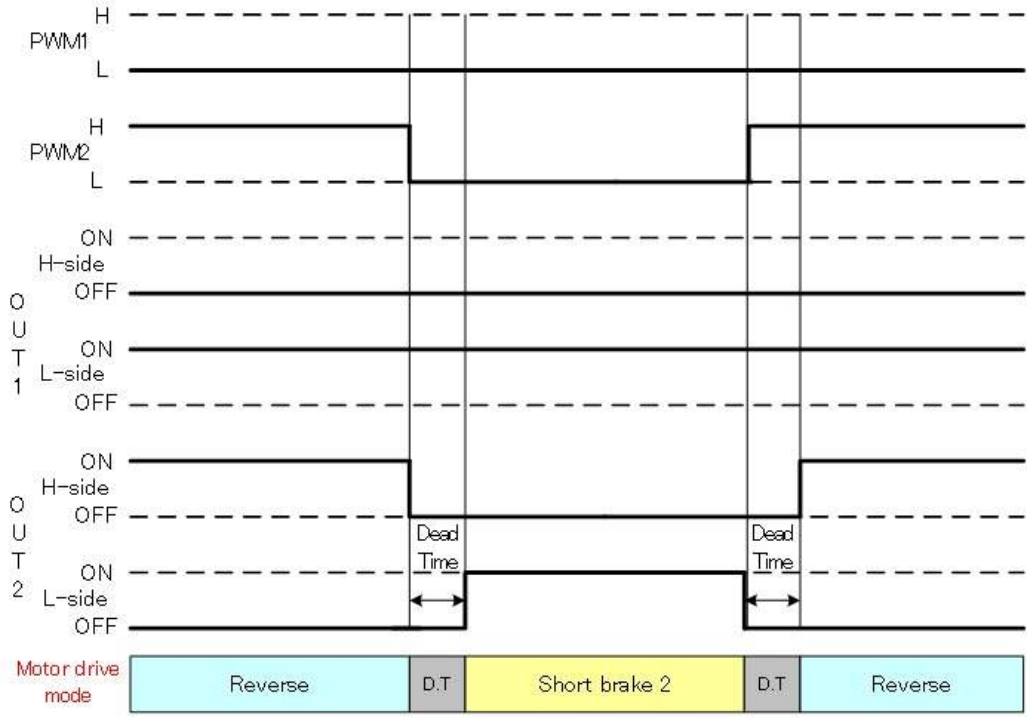


* The circled DMOS FET indicates active. .

Figure 7.6. Current path for PWM function (reverse rotation, low-side regeneration)

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

7.5.6. PWM function (reverse) timing chart



* D.T: Dead time

Figure 7.7. PWM function (reverse rotation, low-side regeneration) timing chart

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.5.7. PWM function (reverse rotation, high-side regeneration) (EN=H, ENB=L) (Figure 7.8 and Figure 7.9)

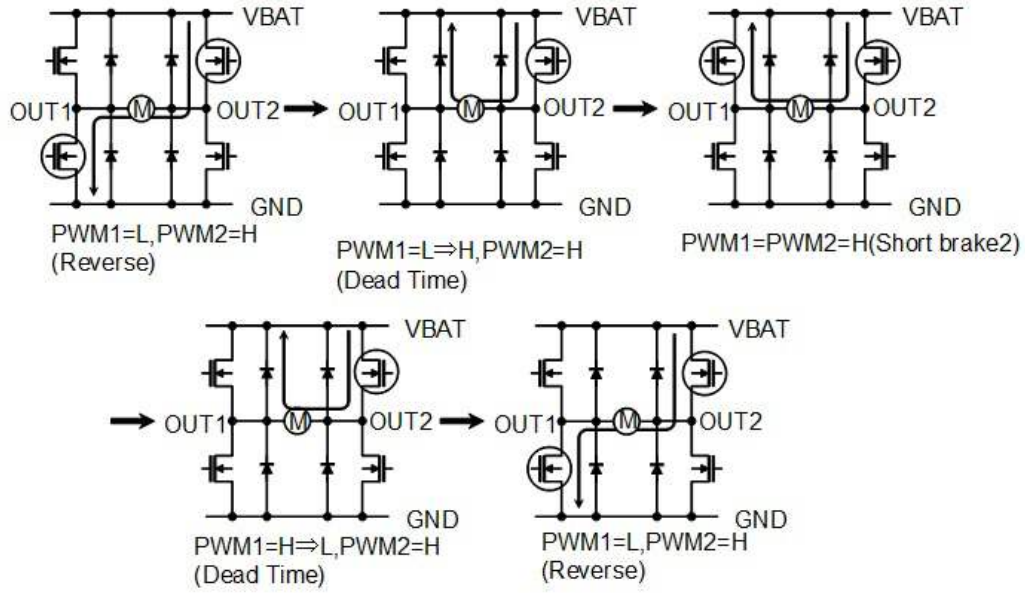
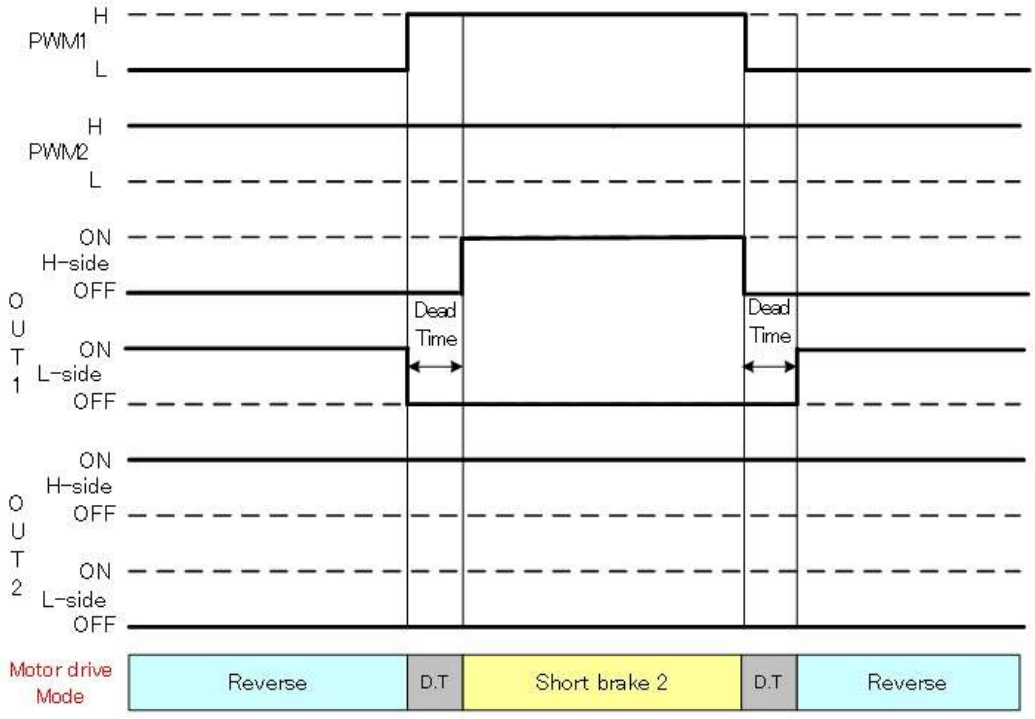


Figure 7.8. Current path for PWM function (reverse rotation, high-side regeneration)

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

7.5.8. PWM function (reverse) timing chart



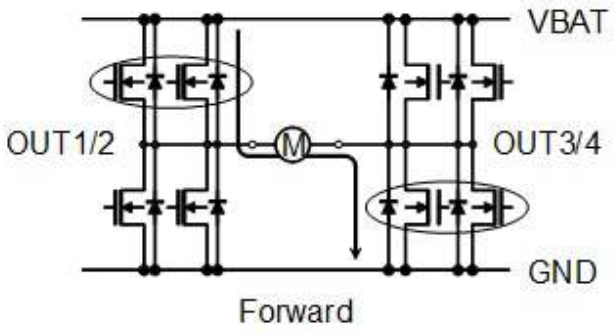
* D.T: Dead time

Figure 7.9. PWM function (reverse rotation, high-side regeneration) timing chart

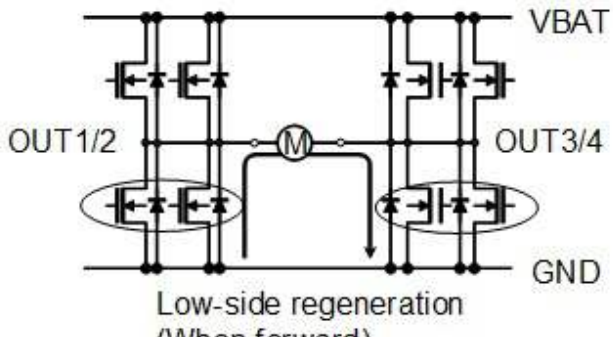
Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.5.9. Combined-Channel Mode (LARGE Mode)

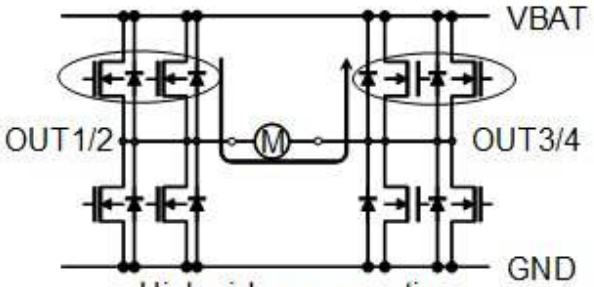
In Combined-Channel Mode (LARGE Mode), the circuit operates as follows.
For operation details, refer to the PWM function above.



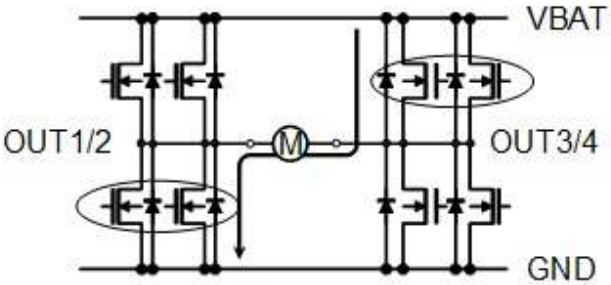
Forward



Low-side regeneration
(When forward)



High-side regeneration
(When forward)



Reverse

7.5.10. Function and SPI CONFIG register setting

Table 7.9. Function and SPI CONFIG register setting

No.	Function	Various setting of SPI registers (except the registers of motor control using SPI)	Pin setting				Pin input								Output				SPI CONFIG register settings	
																			low- or high-side regeneration setting	
			ISEL1	ISEL2	OSEL1	OSEL2	PWM1	PWM2	PWM3	PWM4	EN1 (OUT1&OUT2)	ENB1 (OUT1&OUT2)	EN2 (OUT3&OUT4)	ENB2 (OUT3&OUT4)	OUT1	OUT2	OUT3	OUT4	Ch1 CONFIG1 DATA[20]	Ch2 CONFIG2 DATA[20]
1	Combined-Channel (LARGE) Mode Direct PWM	Not required	L	X	L	L	H/L	H/L	Disable	Disable	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L		H/L		Disable	Disable
2	Combined-Channel (LARGE) Mode Direct PWM+ each setting by SPI	Required	L	X	L	L	H/L	H/L	Disable	Disable	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L		H/L		Disable	Disable
3	Combined-Channel (LARGE) Mode Motor control using SPI	Not required	H	X	L	L	Disable	Disable	Disable	Disable	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L		H/L		low-side regeneration (Initial)	Disable
4	Combined-Channel (LARGE) Mode Motor control using SPI + each setting by SPI	Required	H	X	L	L	Disable	Disable	Disable	Disable	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L		H/L		0: low-side regeneration 1: high-side regeneration	Disable
5	Dual-Channel (SMALL) Mode Ch1/Ch2 direct PWM	Not required	L	L	L	H	H/L	H/L	H/L	H/L	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L	H/L	H/L	H/L	Disable	Disable
6	Dual-Channel (SMALL) Mode Ch1/Ch2 direct PWM + each setting by SPI	Required	L	L	L	H	H/L	H/L	H/L	H/L	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L	H/L	H/L	H/L	Disable	Disable
7	Dual-Channel (SMALL) Mode Ch1/Ch2 motor control using SPI	Not required	H	H	L	H	Disable	Disable	Disable	Disable	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L	H/L	H/L	H/L	low-side regeneration (Initial)	low-side regeneration (Initial)
8	Dual-Channel (SMALL) Mode Ch1/Ch2 motor control using SPI + each setting by SPI	Required	H	H	L	H	Disable	Disable	Disable	Disable	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L	H/L	H/L	H/L	0: low-side regeneration 1: high-side regeneration	0: low-side regeneration 1: high-side regeneration
9	Dual-Channel (SMALL) Mode Ch1 direct PWM Ch2 motor control using SPI	Not required	L	H	L	H	H/L	H/L	Disable	Disable	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L	H/L	H/L	H/L	Disable	low-side regeneration (Initial)
10	Dual-Channel (SMALL) Mode Ch1 direct PWM+ each setting by SPI Ch2 motor control using SPI + each setting by SPI	Required	L	H	L	H	H/L	H/L	Disable	Disable	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L	H/L	H/L	H/L	Disable	0: low-side regeneration 1: high-side regeneration
11	Dual-Channel (SMALL) Mode Ch1 motor control using SPI Ch2 direct PWM	Not required	H	H	L	H	Disable	Disable	H/L	H/L	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L	H/L	H/L	H/L	low-side regeneration (Initial)	Disable
12	Dual-Channel (SMALL) Mode Ch1 motor control using SPI + each setting by SPI Ch2 direct PWM+ each setting bySPI	Required	H	H	L	H	Disable	Disable	H/L	H/L	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L	H/L	H/L	H/L	0: low-side regeneration 1: high-side regeneration	Disable
13	Half Mode Ch1/Ch2 direct PWM	Not required	L	L	H	L	H/L	H/L	H/L	H/L	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L	H/L	H/L	H/L	Disable	Disable
14	Half Mode Ch1/Ch2 direct PWM + each setting by SPI	Required	L	L	H	L	H/L	H/L	H/L	H/L	H:Enable L:Disable	H:Disable L:Enable	H:Enable L:Disable	H:Disable L:Enable	H/L	H/L	H/L	H/L	Disable	Disable

7.6. DIAG output (Table 7.10 and Figure 7.10)

DIAG1 and DIAG2 are open-drain output pins. Insert pull-up resistors between these pins and VDDIO (MCU power supply). If not using SPI communication, connect the VDDIO pin and the external pull-up resistors, that is connected at DIAG1 and DIAG2, to the VCC power supply.
These pins output L when the following abnormalities are detected.

・In the following table, X: Don't care, H: High, L: Low, and Hi-Z: High impedance.

Table 7.10. DIAG functionality (Dual-Channel Mode)

								Motor drive output			
Function	EN1	ENB1	EN2	ENB2	Is EN/ENB pulse input needed when DIAG is cleared?	DIAG1 pin	DIAG2 pin	OUT1	OUT2	OUT3	OUT4
Forward (normal operation)	H	L	H	L	-	H	H	H	L	H	L
Reverse (normal operation)	H	L	H	L	-	H	H	L	H	L	H
Short brake (normal operation)	H	L	H	L	-	H	H	L/H	L/H	L/H	L/H
EN1 Disable	L	X	X	X	No	L	H/L	Hi-Z	Hi-Z	H/L/Hi-Z	H/L/Hi-Z
EN2 Disable	X	X	L	X	No	H/L	L	H/L/Hi-Z	H/L/Hi-Z	Hi-Z	Hi-Z
ENB1 Disable	X	H	X	X	No	L	H/L	Hi-Z	Hi-Z	H/L/Hi-Z	H/L/Hi-Z
ENB2 Disable	X	X	X	H	No	H/L	L	H/L/Hi-Z	H/L/Hi-Z	Hi-Z	Hi-Z
Sleep Mode	X	L/H	X	L/H	-	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Over-temperature detected (TSD)	X	X	X	X	No	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Ch1 over-current detected (ISD)	X	X	X	X	Yes	L	H/L	Hi-Z	Hi-Z	H/L/Hi-Z	H/L/Hi-Z
Ch2 over-current detected (ISD)	X	X	X	X	Yes	H/L	L	H/L/Hi-Z	H/L/Hi-Z	Hi-Z	Hi-Z
VBAT under-voltage detected	X	X	X	X	No	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VCC under-voltage detected	X	X	X	X	No	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VCC under-voltage detected (POR)	X	X	X	X	No	L (*3)	L (*3)	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Ch1 open load during operation detected	X	X	X	X	No	L	H/L	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z
Ch2 open load during operation detected	X	X	X	X	No	H/L	L	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z
Ch1 open load during non-operation detected	X	X	X	X	No	L	H/L	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z
Ch2 open load during non-operation detected	X	X	X	X	No	H/L	L	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z
Initial/restarted diagnosis detects an error (detection of VBAT/VCC under-voltage or over-temperature)	X	X	X	X	No	L	L	(*1)	(*1)	(*1)	(*1)
Initial/restarted diagnosis detects an error (detection of Ch1 over-current or open load during operation/non-operation)	X	X	X	X	No	L	H/L	(*1)	(*1)	(*1)	(*1)
Initial/restarted diagnosis detects an error (detection of Ch2 over-current or open load during operation/non-operation)	X	X	X	X	No	H/L	L	(*1)	(*1)	(*1)	(*1)
Initial/restarted diagnosis is attempted but does not start (detection of VBAT/VCC under-voltage or over-temperature)	X	X	X	X	No	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Function	EN1	ENB1	EN2	ENB2	Is EN/ENB pulse input needed when DIAG is cleared?	DIAG1 pin	DIAG2 pin	Motor drive output			
								OUT1	OUT2	OUT3	OUT4
Initial/restarted diagnosis is attempted but does not start (detection of Ch1 over-current or open load during operation/non-operation)	X	X	X	X	No	L	H/L	Hi-Z	Hi-Z	(*1)	(*1)
Initial/restarted diagnosis is attempted but does not start (detection of Ch2 over-current or open load during operation/non-operation)	X	X	X	X	No	H/L	L	(*1)	(*1)	Hi-Z	Hi-Z
SPI communication disruption detected	X	X	X	X	No	L	L	(*2)	(*2)	(*2)	(*2)
SPI communication CRC error detected	X	X	X	X	No	L	L	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z
Abnormal SPI communication SCLK clock count detected	X	X	X	X	No	L	L	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z
Abnormal SPI communication address detected	X	X	X	X	No	L	L	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z

*1: Operation is similar to Table 7.1. H-bridge motor function 1.
*2: Operation specified in CONFIG1 DATA[8].

Table 7.11. DIAG functionality (Combined-Channel Mode)

Function	EN1	ENB1	EN2	ENB2	Is EN/ENB pulse input needed when DIAG is cleared?	DIAG1 pin	DIAG2 pin	Motor drive output			
								OUT1	OUT2	OUT3	OUT4
Forward (normal operation)	H	L	H	L	-	H	H	H	H	L	L
Reverse (normal operation)	H	L	H	L	-	H	H	L	L	H	H
Short brake (normal operation)	H	L	H	L	-	H	H	L/H	L/H	L/H	L/H
EN1 and EN2 Disable	L	X	L	X	No	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z
ENB1 and ENB2 Disable	X	H	X	H	No	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Sleep Mode	X	L/H	X	L/H	-	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Over-temperature detected (TSD)	X	X	X	X	No	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Ch1 over-current detected (ISD)	X	X	X	X	Yes	L	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Ch2 over-current detected (ISD)	X	X	X	X	Yes	H	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VBAT under-voltage detected	X	X	X	X	No	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VCC under-voltage detected	X	X	X	X	No	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VCC under-voltage detected (POR)	X	X	X	X	No	L (*3)	L (*3)	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Ch1-Ch2 open load during operation detected	X	X	X	X	No	L	L	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z
Ch1-Ch2 open load during non-operation detected	X	X	X	X	No	L	L	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z

Function	EN1	ENB1	EN2	ENB2	Is EN/ENB pulse input needed when DIAG is cleared?	DIAG1 pin	DIAG2 pin	Motor drive output			
								OUT1	OUT2	OUT3	OUT4
Initial/restarted diagnosis detects an error (detection of VBAT/VCC under-voltage or over-temperature)	X	X	X	X	No	L	L	(*1)	(*1)	(*1)	(*1)
Initial/restarted diagnosis detects an error (detection of Ch1-Ch2 over-current or open load during operation/non-operation)	X	X	X	X	No	L	L	(*1)	(*1)	(*1)	(*1)
Initial/restarted diagnosis is attempted but does not start (detection of VBAT/VCC under-voltage or over-temperature)	X	X	X	X	No	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Initial/restarted diagnosis is attempted but does not start (detection of Ch1-Ch2 over-current or open load during operation/non-operation)	X	X	X	X	No	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SPI communication disruption detected	X	X	X	X	No	L	L	(*2)	(*2)	(*2)	(*2)
SPI communication CRC error detected	X	X	X	X	No	L	L	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z
Abnormal SPI communication SCLK clock count detected	X	X	X	X	No	L	L	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z
Abnormal SPI communication address detected	X	X	X	X	No	L	L	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z	H/L/Hi-Z

*1: Operation is similar to Table 7.2. H-bridge motor function 2.
*2: Operation specified in CONFIG1 DATA[8].
Note: In Combined-Channel Mode, externally short-circuit ISEL1/2, EN1/2, ENB1/2, OUT1/2, and OUT3/4.Note that EN2/ENB2 are effective as analog signals to control the output DMOS gates but ineffective as signals supplied to the logic circuit.

■ Even in Combined-Channel Mode (LARGE Mode), each DIAG circuit operates individually.

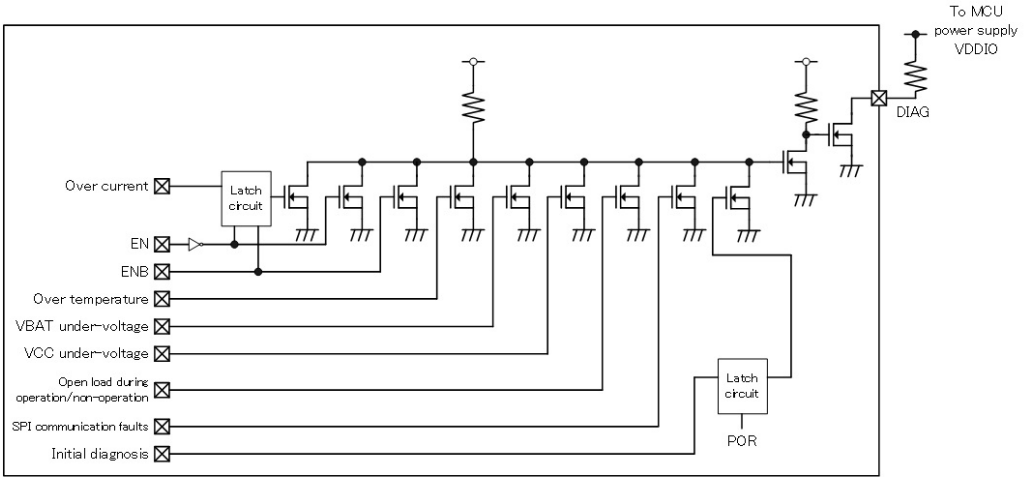


Figure 7.10. Example DIAG output circuit configuration

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

Table 7.12. DIAG functionality when an abnormality is detected (details)

Detection circuit	Motor output when detecting	DIAG	Recovery procedure	SPI
Short-circuit to power supply or ground detected (latched)	Depends on case. See "7.6.2. Over-current detection".			
Short-circuit to power supply or ground detected (automatic recovery)	Depends on case. See "7.6.2. Over-current detection".			
Over-temperature detected	OFF (Hi-Z)	DIAG retains L while over-temperature is detected. When temperature falls below the hysteresis temperature, DIAG cancels L and automatically returns to H.	Automatic recovery at 150°C or below	Automatic recovery
Open load during operation detected	Function operation	DIAG retains L while load is open. When motor is reconnected, DIAG automatically returns to H.	Normal operation is continued with motor re-connection	Automatic recovery
VBAT under-voltage detection	OFF (Hi-Z)	When detected, DIAG outputs L. When the voltage reaches the level at which detection is canceled, DIAG automatically returns to H.	Automatic recovery	Automatic recovery
VCC under-voltage detection 1 (when voltage decreases to the POR voltage or less)	OFF (Hi-Z)	When detected, DIAG outputs L. When voltage recovers (detection voltage + hysteresis voltage), DIAG automatically returns to H.	Automatic recovery	Since a reset signal is input below the POR voltage, settings are initialized at recovery.
VCC under-voltage detection 2 (when voltage decreases but does not reach the POR voltage)	OFF (Hi-Z)	When detected, DIAG outputs L. When voltage recovers (detection voltage + hysteresis voltage), DIAG automatically returns to H.	Automatic recovery	Abnormality flag "1" is maintained until SPI executes 1WC. Execution of 1WC clears the bit.

7.6.1. Abnormal VBAT/VCC voltage

・When the abnormal VBAT/VCC voltage returns to normal, motor operation recovers automatically.
・When the abnormal VBAT/VCC voltage returns to normal, DIAG output also recovers automatically.
The abnormality bit (STATUS1 DATA[10]) for VCC abnormal voltage (VCC under-voltage detection) is latched until SPI clears the bit.

The abnormality bit (STATUS1 DATA[10]) for VCC abnormal voltage (VCC under-voltage detection) is cleared when a single pulse of Disable→Enable in EN or ENB triggers an initial/restarted diagnosis.

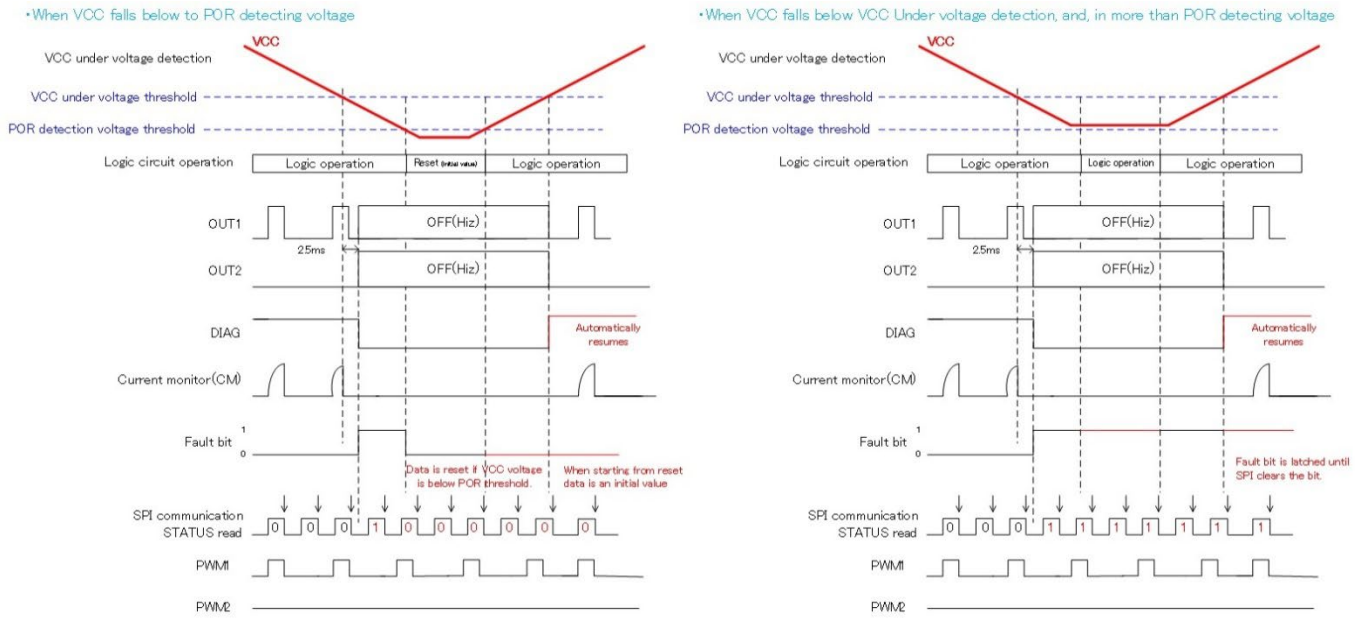


Figure 7.11. VCC under-voltage detection timing chart

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

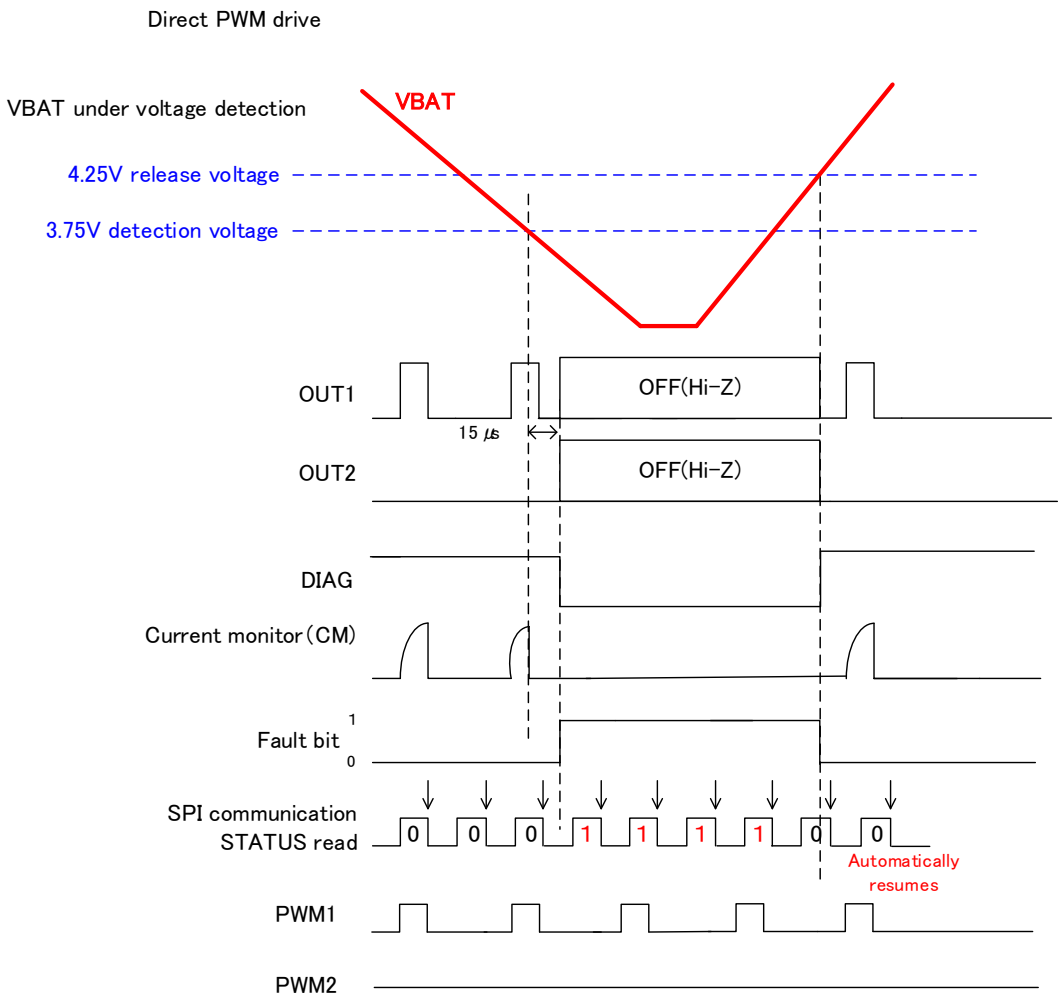


Figure 7.12. VBAT under-voltage detection timing chart

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.6.2. Over-current detection

Either the EN pin rising edge or the ENB pin falling edge clears the latched L output from the DIAG pin.

Table 7.13. OUT1/2, OUT3/4, abnormality bit, and DIAG function when over-current is detected (details)

Table 7.13Condition (1): Over-current detection continues for 1 μs
Condition (2): EN or ENB Disable→Enable timing
Condition (3): Output Hi-Z cancellation setting using SPI communication

No.	Motor drive method	Detection mode	OUT1/2 and OUT3/4	Abnormality bit	DIAG
1	Direct PWM	Automatic recovery	For (1), Hi-Z. For (2) or (3), or when 300 ms elapses, Hi-Z is canceled. (When (2) or (3) is satisfied, the condition of 300 ms is cleared.)	For (1), bit = 1. At 3.25 μs after OUT1/2 (or OUT3/4) output, Hi-Z is canceled. If over-current is not detected, bit = 0. * For the timing when the Hi-Z of OUT is canceled, see Supplements 1 and 2. * EN/ENB Disable does not clear bit = 1.	For (1), low. For (2), return to high.
2		Latched	For (1), Hi-Z. For (2) or (3), Hi-Z is canceled.	Same as above	Same as above
3	Drive using SPI communication	Automatic recovery	For (1), Hi-Z. For (2) or (3), or when 300 ms elapses, Hi-Z is canceled. (When (2) or (3) is satisfied, the condition of 300 ms is cleared.)	Same as above	Same as above
4		Latched	For (1), Hi-Z. For (2) or (3), Hi-Z is canceled.	Same as above	Same as above

Supplement 1: Cancellation timing of Hi-Z for OUT1/2 and OUT3/4

- For SPI_PWM drive: Once the cancellation condition is satisfied, Hi-Z is canceled at the next PWM cycle. The next PWM cycle is as follows.
  (1) PWM duty-ON timing of forward or reverse drive
  (SPI settings for the PWM duty-ON interval: 0% to 100%)
  (2) Brake or output OFF (Hi-Z) ⇒ PWM duty-ON timing of forward or reverse drive (SPI settings for the PWM duty-ON interval: 0% to 100%)
- For direct PWM drive: Once the cancellation condition is satisfied, Hi-Z is immediately canceled.
- However, if EN/ENB = Disable, Hi-Z is canceled at Disable→Enable regardless of the PWM drive method.

Supplement 2: Over-current operation in Half-Bridge Mode (a mode limited to direct PWM drive)

- Only the driver pin for which over-current is detected (OUT1, OUT2, OUT3, or OUT4) is set to Hi-Z.
- Hi-Z is canceled immediately after it receives a Hi-Z cancellation signal from SPI communication, or when EN/ENB changes from Disable to Enable.

Note: Direct PWM drive cancels Hi-Z immediately without synchronizing with PWM instructions regardless of H-Bridge or Half-Bridge Mode.

7.6.3. Over-temperature detection

The latched L output of the DIAG pin is automatically cleared (automatic recovery type).

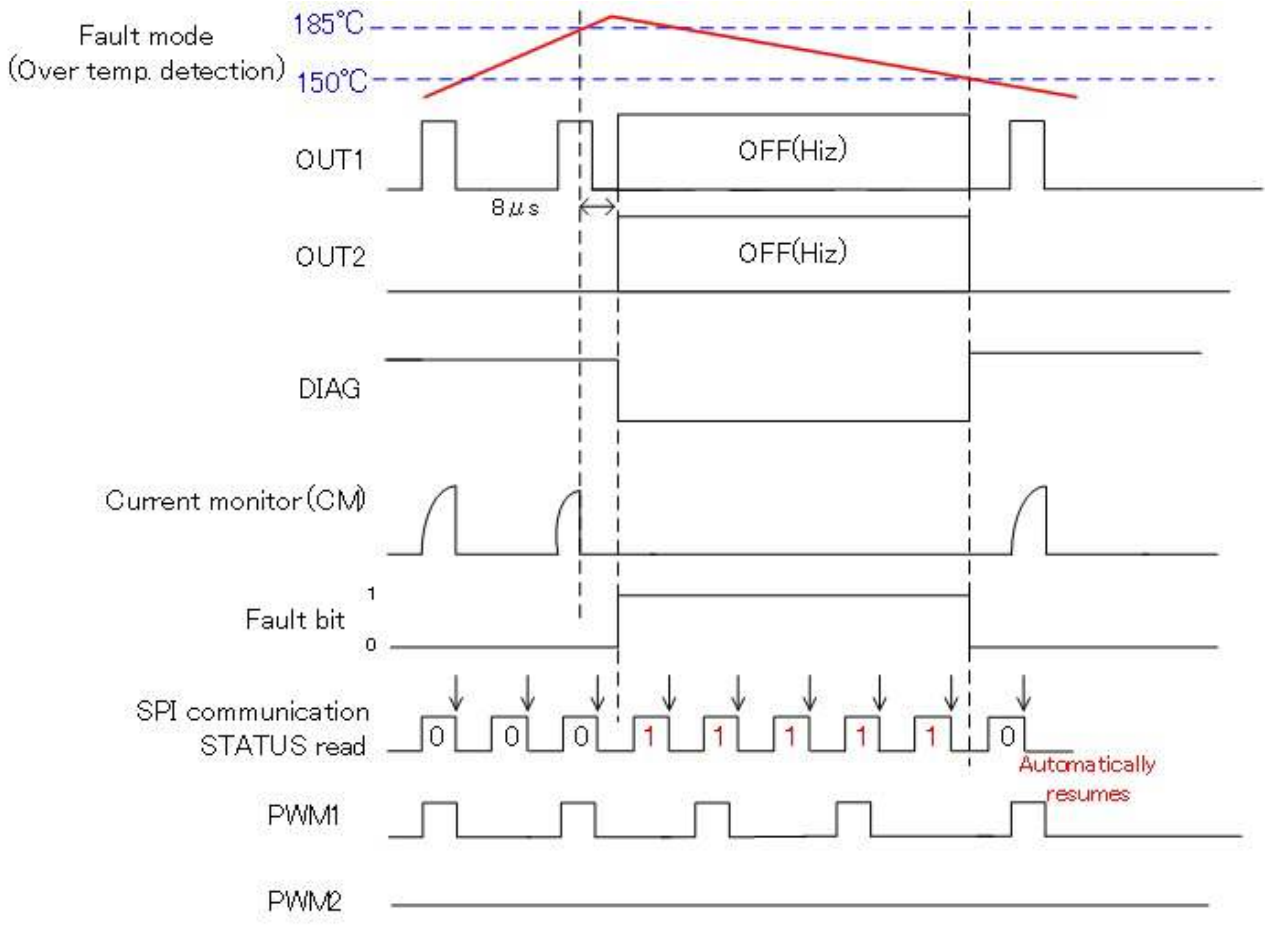


Figure 7.13 Over-temperature detection timing chart

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.7. Current-limit control

This IC adopts a chopper-type current-limit control. When an event causes a large current, such as transient pulses due to high-speed throttle operation or a locked motor due to an immovable motor shaft, the IC activates the current-limit control to protect the actuator and reduce the power dissipation. (An additional over-current protection circuit prepared in another block handles short-circuits to power supply or ground.)

The current-limit comparator is located on the low side. Ilim-H denotes the high threshold, and Ilim-L denotes the low threshold. The low side performs regeneration (slow decay).

A blanking time is set internally, after which current-limit control activates. Ilim-H = 6.5 A (typ.) and Ilim-L = Ilim-H - 0.25 A (typ.)

Two current-limit thresholds are selectable for 16 combinations by SPI registers as following table.

<table>
<tr><th></th><th colspan="2">Ch1 (OUT1/OUT2)</th><th colspan="2">Ch2 (OUT3/OUT4)</th></tr>
<tr><td rowspan="10">Dual-Channel Mode
(drives two motors)</td><td>Ilim-H</td><td>Ilim-L</td><td>Ilim-H</td><td>Ilim-L</td></tr>
<tr><td rowspan="2">6.5 A
(initial value)</td><td>6.5 - 0.25 A
(initial value)</td><td rowspan="2">6.5 A
(initial value)</td><td>6.5 - 0.25 A
(initial value)</td></tr>
<tr><td>6.5 - 0.5 A</td><td>6.5 - 0.5 A</td></tr>
<tr><td rowspan="2">4.6 A</td><td>4.6 - 0.25 A</td><td rowspan="2">6.5 A
(initial value)</td><td>6.5 - 0.25 A
(initial value)</td></tr>
<tr><td>4.6 - 0.5 A</td><td>6.5 - 0.5 A</td></tr>
<tr><td rowspan="2">6.5 A
(initial value)</td><td>6.5 - 0.25 A
(initial value)</td><td rowspan="2">4.6 A</td><td>4.6 - 0.25 A</td></tr>
<tr><td>6.5 - 0.5 A</td><td>4.6 - 0.5 A</td></tr>
<tr><td rowspan="2">4.6 A</td><td>4.6 - 0.25 A</td><td rowspan="2">4.6 A</td><td>4.6 - 0.25 A</td></tr>
<tr><td>4.6 - 0.5 A</td><td>4.6 - 0.5 A</td></tr>
</table>

In Combined-Channel Mode, the following four combinations are selectable:

<table>
<tr><th></th><th colspan="2">Ch1 (OUT1/OUT2), Ch2 (OUT3/OUT4)</th><th colspan="2">Total</th></tr>
<tr><td rowspan="5">Combined-Channel
Mode (drives one motor)</td><td>Ilim-H</td><td>Ilim-L</td><td>Ilim-H</td><td>Ilim-L</td></tr>
<tr><td rowspan="2">6.5 A
(initial value)</td><td>6.5 - 0.25 A
(initial value)</td><td rowspan="2">13 A
(initial value)</td><td>13A- 0.5 A
(initial value)</td></tr>
<tr><td>6.5 - 0.5 A</td><td>13A - 1.0 A</td></tr>
<tr><td rowspan="2">4.6 A</td><td>4.6 - 0.25 A
(initial value)</td><td rowspan="2">9.2 A</td><td>9.2A - 0.5 A
(initial value)</td></tr>
<tr><td>4.6 - 0.5 A</td><td>9.2A- 1.0 A</td></tr>
</table>

7.7.1. Chopper-type current-limit control (basic operation) (Figure 7.14)

The following illustrates the basic operation of the chopper-type current-limit control (when Ilim-H = 6.5 A and Ilim-L = Ilim-H - 0.25 A):

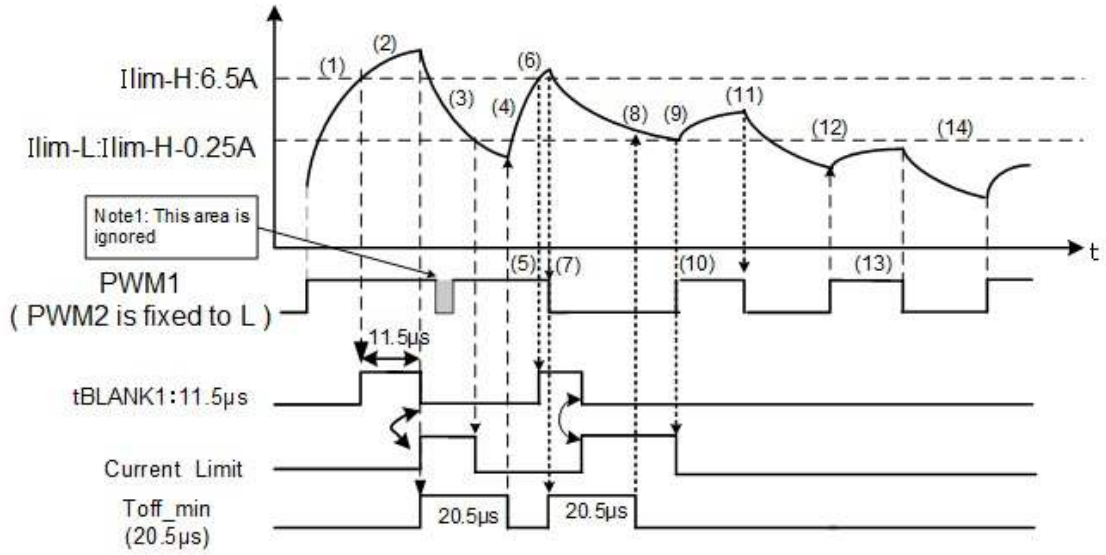


Figure 7.14 Chopper-type current-limit control

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

<Basic operation>

(1) Large current is detected at Ilim-H (6.5 A).
(2) The blanking counter starts counting at the detection. Since a current above Ilim-H (6.5 A) still flows in this case, the current limit signal rises at the falling edge of tBLANK1 after a blanking time (tBLANK1: 11.5 µs).
(3) After the blanking, the motor drive output automatically enters a short-brake mode (low side simultaneous ON) for current regeneration. At the same time, Toff_min rises to H to start counting.
(4) After a Toff_min period (20.5 µs), if the current is below Ilim-L, normal operation (forward rotation) resumes.
(5) Since PWM1 is H, the motor drive current increases.
In this case, the PWM1 signal indicated by Note 1 is ignored (Toff_min is prioritized).

7.7.2. PWM signal input during forward rotation (Case 1) (Figure 7.14)

(6) After the motor operation resumes at the falling edge of Toff_min, large current is detected again at Ilim-H (6.5 A).
Counting by tBLANK1 (11.5 µs) starts.
(7) When PWM changes to L during the blanking time, a short-brake is applied (low side simultaneous ON) along with current regeneration.
(8) Since the current value after Toff_min (20.5 µs) is above Ilim-L, the short brake continues.
(9) Since Ilim-L is detected, current limit changes to L and normal mode resumes.
(10) Since PWM1 is still H, the motor drive current increases.

7.7.3. PWM signal input during forward rotation (Case 2) (Figure 7.14)

(11) At the falling edge of PWM1, short-brake mode begins.
(12) When PWM1 = H, normal mode resumes.
(13) Since PWM1 is still H, the motor drive current increases.
(14) When PWM1 = L, the operation becomes short-brake mode, and the motor drive current decreases.

7.7.4. Current measurement points in current-limit control

The current is detected at the low-side driver of the motor drive output (Figure 7.15).

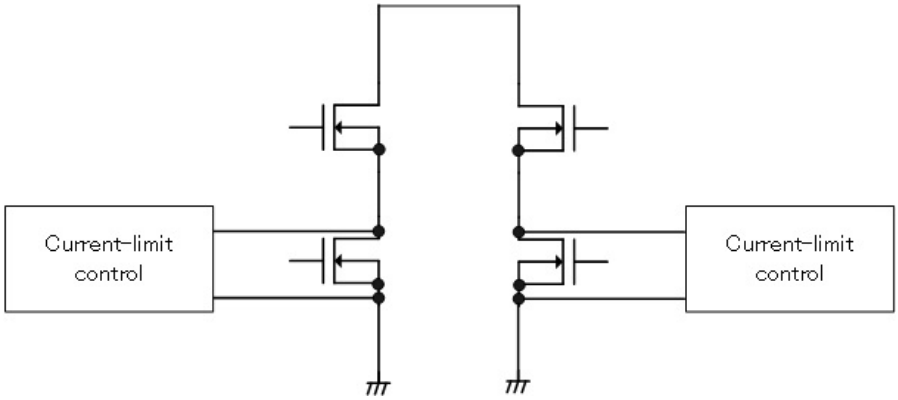


Figure 7.15 Current measurement points in current-limit control

7.7.5. Operation flowchart (Figure 7.16)

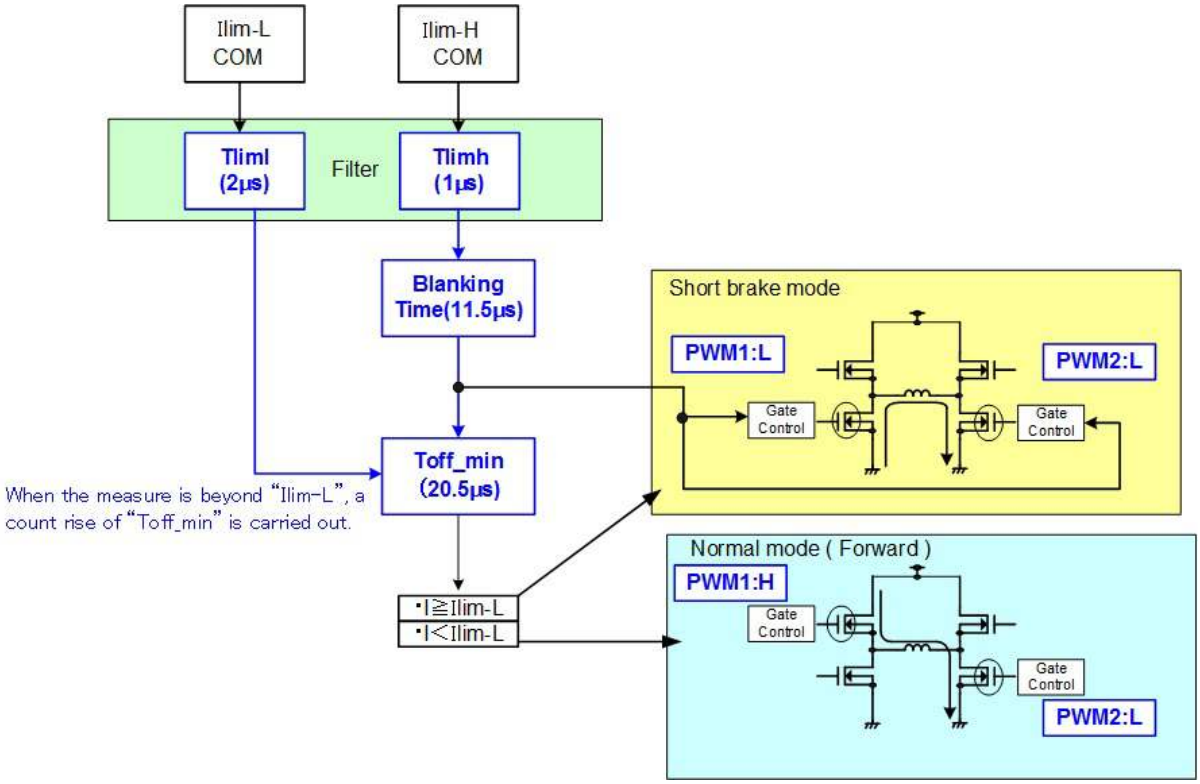


Figure 7.16 Current-limit control circuit operation flowchart

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

7.7.6. Temperature-adjusted current-limit control (Figure 7.17)

When the junction temperature Tj increases to the Twar temperature (150 to 177°C), the current-limit control circuit reduces the current-limit threshold to 2.5 A.
Ilim-L also decreases with Ilim-H.

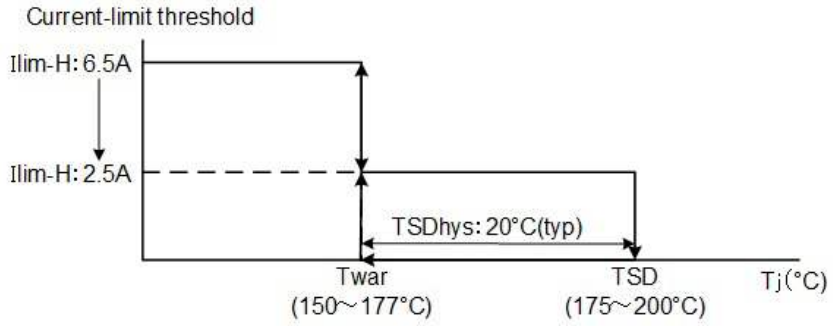


Figure 7.17 Temperature-adjusted current-limit control

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.8. High-side current monitoring: CM pin (Figure 7.18, Figure 7.19,Figure 20,Figure21)

This IC monitors the current value (0 to 6A) flowing through the high side Nch of the H-bridge circuit anytime in active mode. 0.24% of the current is output from CM1(CM2) pin to be converted to voltage with an external resistor(220Ω) connected between CM1(CM2) and GND. The MCU can recognize the motor condition such as the motor rocked or the motor disconnected in active mode with the voltage generated at CM1(CM2) pin.

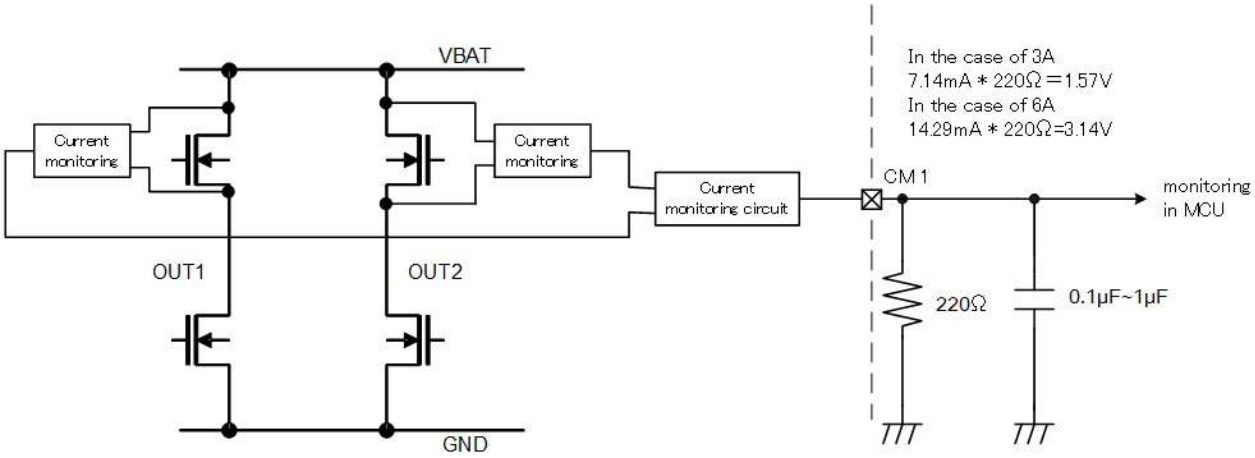


Figure 7.18 High-side current monitoring configuration

For open-load detection during operation, connects an external resistor.
Current monitoring is enabled even when EN/ENB are disabled and the output is OFF.
However, monitoring is disabled in Sleep Mode (SLEEPB = L).

Note: The resistor (220Ω) in the above figure is when the MCU (ADC) power supply is used at 5V. Since this output circuit configuration consists of a 5V power supply circuit, be careful not to exceed the withstand voltage of the MCU pins if the MCU power supply is 5V or lower. (Addition of a zener diode or the like is recommended.)

Also, note that the 220Ω external resistor requires thorough evaluation because variations in the external resistor value will also cause variations in output voltage.

Note: The current monitor on the Hi-side side is also used to detect an open load during operation, so be sure to connect a resistor (220Ω) + capacitor (0.1μF to 1μF). If the resistor and capacitor are not connected, the load open detection during operation will not be detected.

Note: The range of the current monitor is 0 to 6A even when using the Large mode (2-channel coupling mode).

The following shows an example where the current is 3 A.
Note that consecutive forward and reverse operation is prohibited. Always insert a short brake.

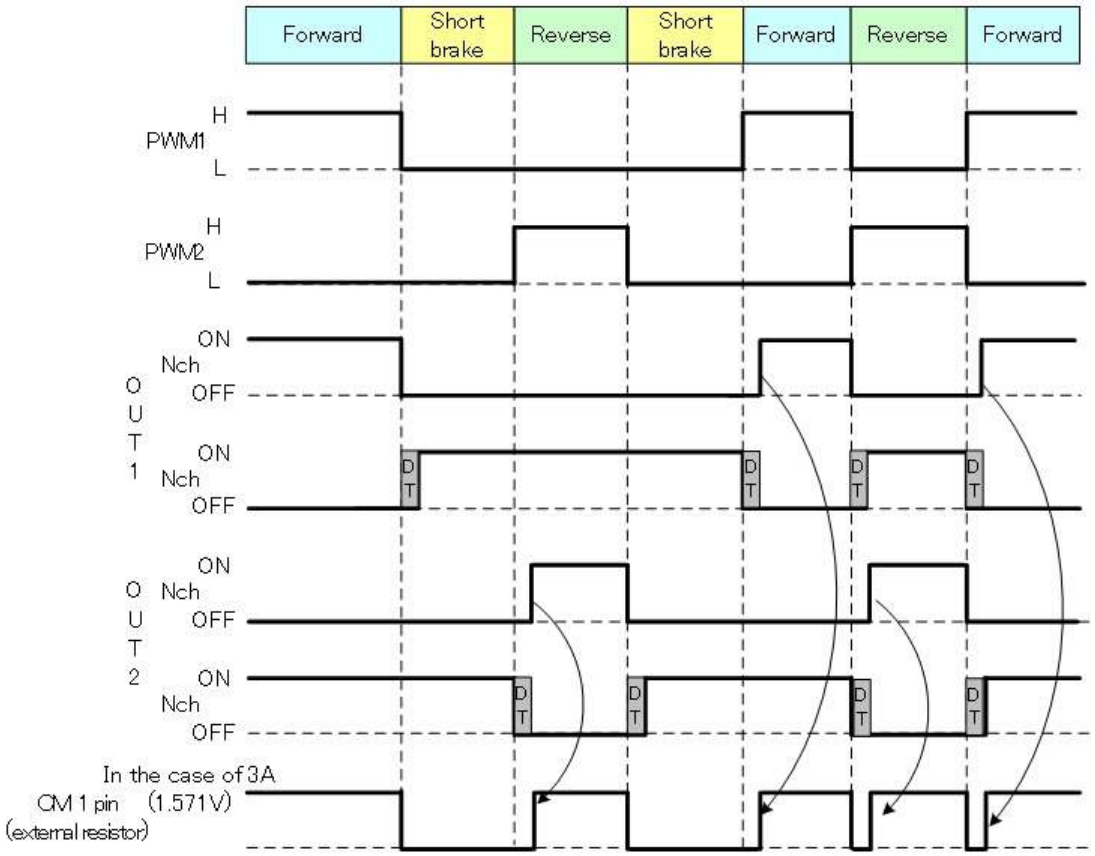


Figure 7.19 High-side current monitoring timing chart

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

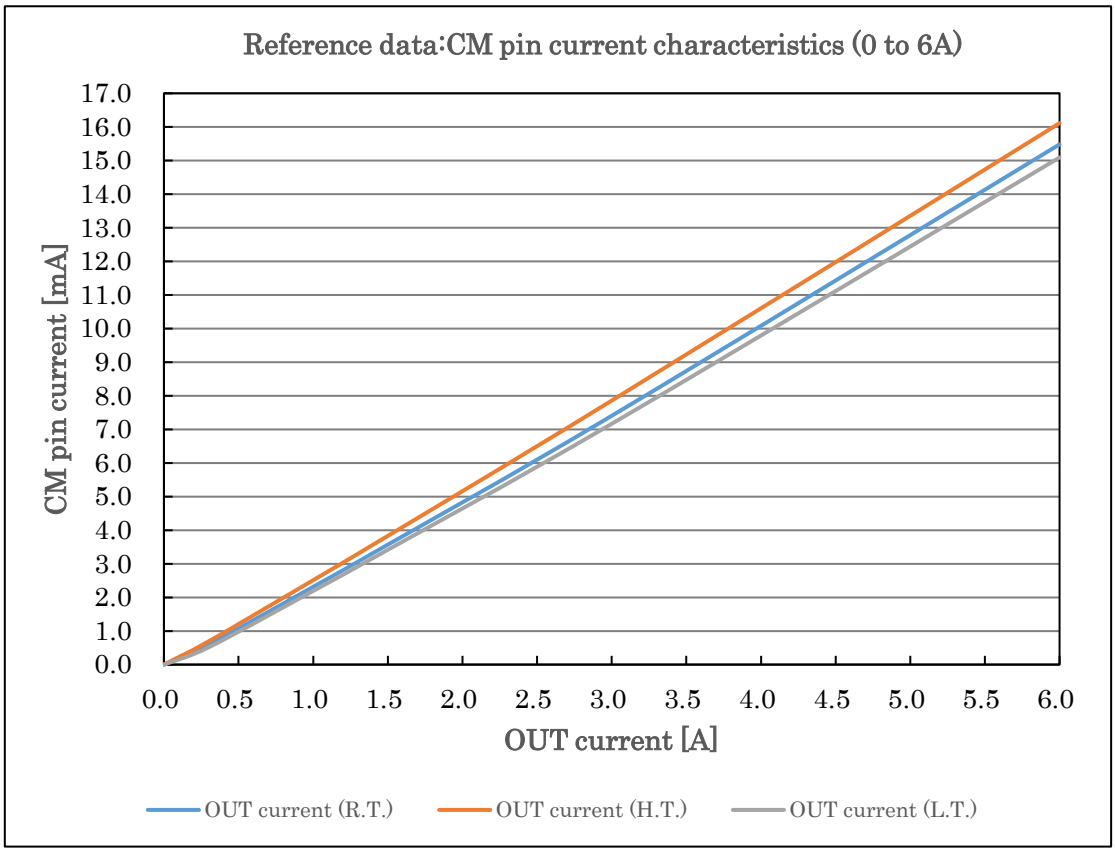


Figure 7.20 CM pin current vs. OUT current characteristics (0 to 6A)

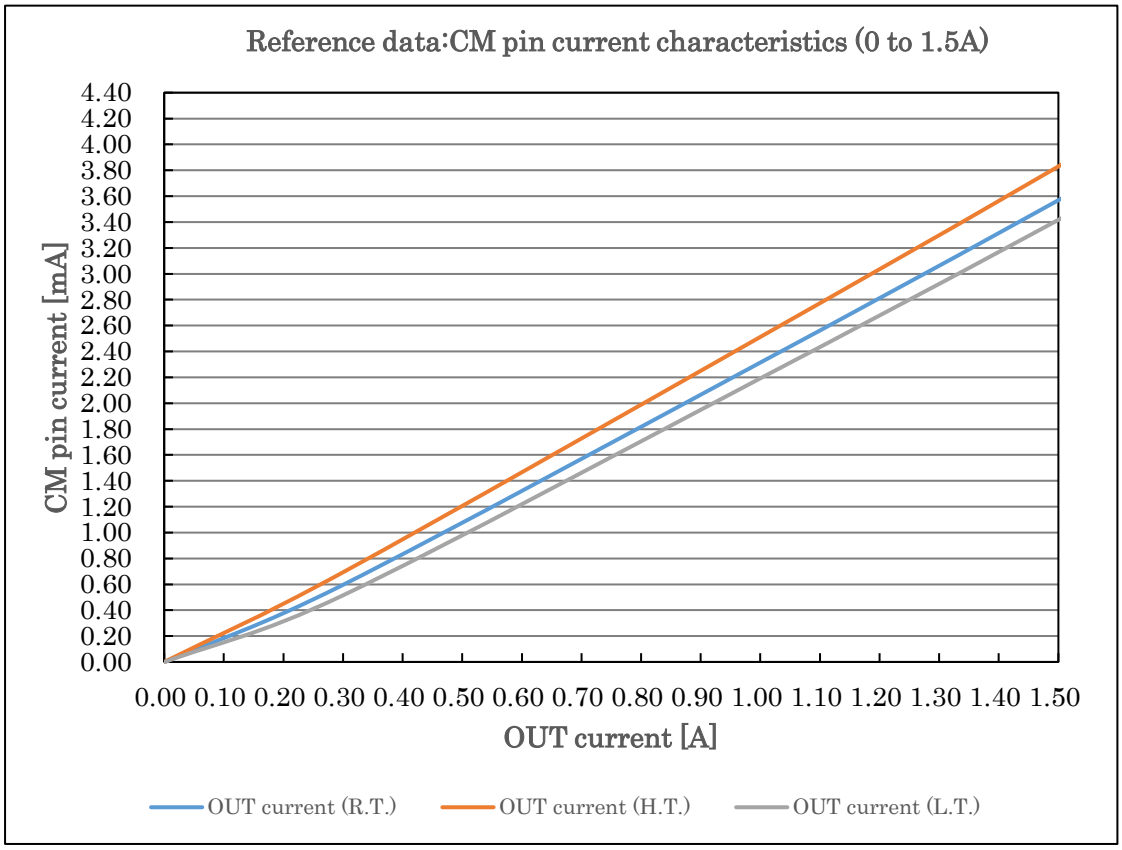


Figure 7.21 CM pin current vs. OUT current characteristics (0 to 1.5A)

7.9. Open-load detection

This IC detects an open load when the motor connection between OUT1 and OUT2 or between OUT3 and OUT4 is open.
Upon detection, the IC changes the DIAG pin to L and performs an operation to notify the SPI register that the load is open. As shown below, an open-load detection can occur in two environments (operation/non-operation).

7.9.1. Open-load detection circuit during operation (output ON)

An open load is identified using the CM (current monitoring) function. So insert a resistor between the CM pin and GND.

The following shows a block diagram (Figure 7.22) and operation waveforms (a load current waveform and internal signals: Figure 7.23) that serve as a design specification for detecting an open load during operation.

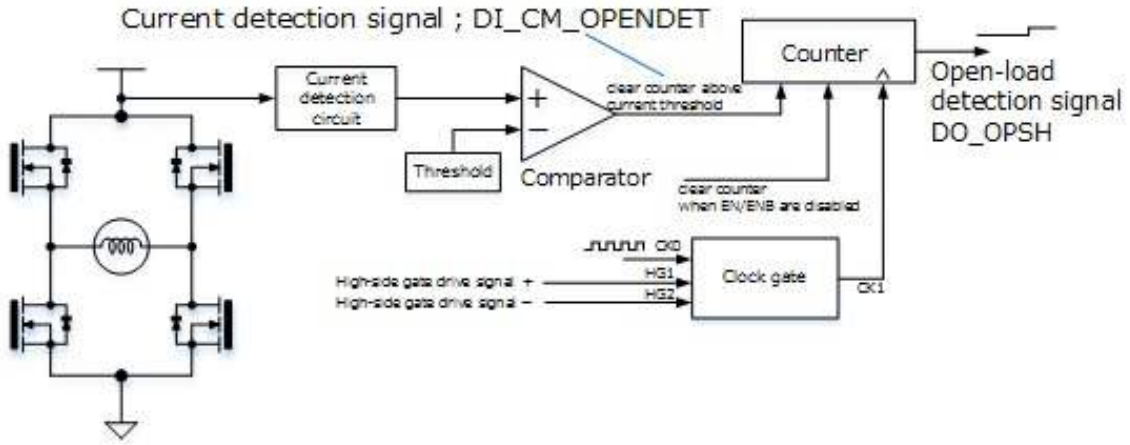


Figure 7.22 Open-load detection during operation: block diagram

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

Detailed specifications of open-load detection signal DO_OPSH

■ Operation specifications of open detection counter

・When monitoring condition (*1) matches
DI_CM_OPENDET = Lo (below current threshold) ⇒increment counter
DI_CM_OPENDET = Hi (above current threshold) ⇒clear counter (cleared state is fixed)

・When monitoring condition (*1) doesn't match
If monitoring masking condition (*2) matches ⇒clear counter (cleared state is fixed)
If monitoring masking condition (*2) doesn't match ⇒suspend counter incrementation (counter value is retained)

■ Operation specifications of open-load detection signal DO_OPSH

・Open detection signal = 1 when counter value reaches 100 ms
・Open detection signal = 0 (automatic recovery) when counter-clear condition is satisfied
* When EN/ENB are disabled or an abnormality is detected, no monitoring occurs, and the state of the detection signal is retained.

■ Handling of open-load detection signal DO_OPSH

・Open-load detection signal is a state-recognition signal and thus has no effect on motor operation
・While the open detection signal is 1, DIAG outputs Lo
・IC constantly writes open detection signal DO_OPSH in SPI register

*1: Condition for monitoring
(OUT1_Hi-side, OUT2_Hi-side) = (ON, OFF) or (OFF, ON)
(OUT3_Hi-side, OUT4_Hi-side) = (ON, OFF) or (OFF, ON)
*2: Condition for masking monitoring (because no output current flows through the IC)
- During initial diagnosis
- While EN or ENB is disabled (since the output is Hi-Z)
  This means that even after initial diagnosis completes, monitoring is masked when the system is disabled.
- When a detected abnormality forces the output to be Hi-Z
- During Sleep Mode (nothing can be monitored, because logic operations are disabled)

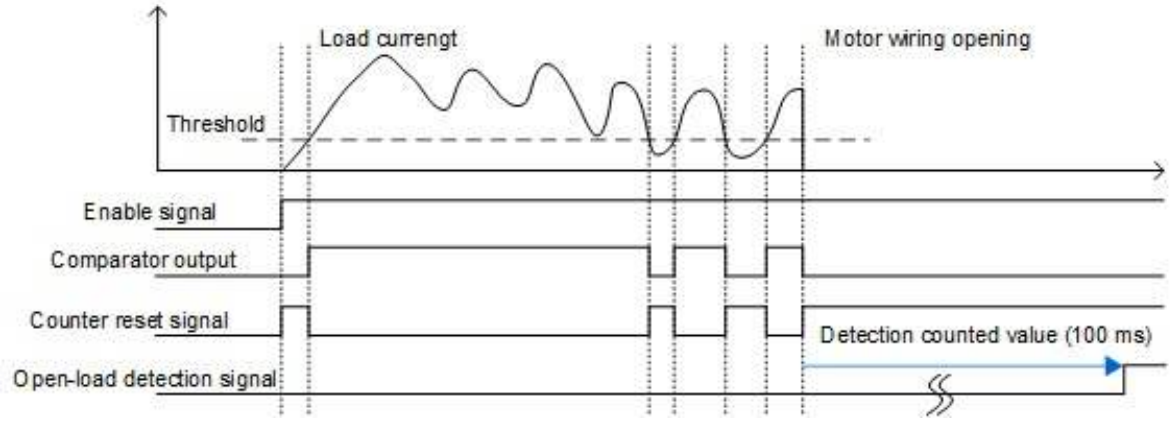


Figure 7.23 Open-load detection during operation: operation waveform

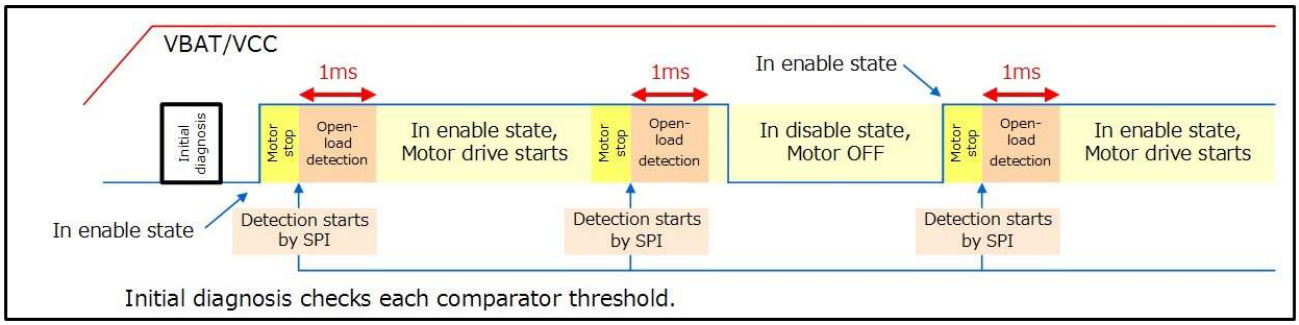
When the motor is operating and the load current falls below the threshold, the counter reset state is cancelled and counter incrementation starts. When the counter reaches the value where detection is recognized, the circuit outputs an open detection signal.

7.9.2. Open-load detection circuit during non-operation (output OFF)

・Open-load detection during non-operation performs as follows:
- Initial diagnosis does not execute open-load detection during non-operation. The initial diagnosis only tests the comparator circuit to be used for open-load detection during non-operation.
- After the initial diagnosis completes, start the open-load detection during non-operation function using an SPI signal whenever the user deems it necessary.
- Select a detection duration depending on the load conditions using SPI communication.
- Open-load detection during non-operation detects an open load when the motor is stopped (braked or output OFF (Hi-Z) due to SPI control). When the IC is enabled and the motor is stopped (braked or output OFF (Hi-Z) due to SPI control), send CONFIG7 DATA[30]/[27]=1 (execution of open-load detection while Ch1/Ch2 is not operating) using SPI communication to execute the detection operation.
- The threshold to detect output voltage swiched is set 1/2×VBAT [V] (typ.)

・Output states before starting open-load detection during non-operation (motor is stopped):
The output is braked (low or high side) by PWM input (duty-ON period is 0%).
The output is braked or in an OFF (Hi-Z) state due to a motor operation setting from SPI control.

Note: Even when VBAT/VCC under-voltage detection activates, the output is OFF (Hi-Z). Since the supply voltage is out of the operating range, however, open-load detection does not work.
Note: VBAT/VCC under-voltage detection and over-current detection, over-temperature detection and initial diagnosis operation are prioritized over open-load detection during non-operation.
Note:, When abnormal conditons (VBAT/VCC under-voltage detection / over-current detection / over-temperature detection) and initial diagnosis operation are detected under an open-load detection condition during non-operation, an open-load detection is interruptted and the outputs turn OFF (Hi-Z) by these anomaly detection or initial diagnosis operation.
Note: When an open-load detection interrupts operation by fault detections (VBAT/VCC under-voltage detection and over-current detection, over-temperature detection) and initial diagnosis operation, abnormality bit (STATUS1 DATA [18] / [17]) of an open-load detection during non-operation is still "0" (undetected).



Open-load detection during non-operation: conceptual timing chart

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

7.9.3. Output short detection to power supply or ground during non-operation

The open-load detection circuit shown above can also detect a output short to power supply or ground. For detection, when a single high-side/low-side DMOS is turned ON, check the output voltage while monitoring the voltage of the other side.
Note that if the detection takes too much time, a output short to power supply or ground may cause over-current through the DMOS.
Over-current detection (detection of output short to power supply or ground) is prioritized over open-load detection during non-operation. When over-current condition (detection of output short to power supply or ground) is detected under an open-load detection condition during non-operation, an open-load detection is interruptted and over-current detection performs.Also, when an open-load detection during non-operation is interruptted by detection over-current, abnormality bit (STATUS1 DATA [18] / [17]) of an open-load detection during non-operation is still "0" (undetected).

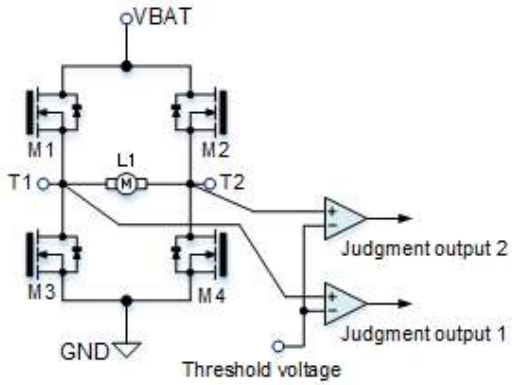


Figure 7.24 Output short detection to power supply or ground during non-operation : block diagram

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

7.10. Sleep function

The IC has a sleep function. When the SLEEPB pin is L, the IC enters Sleep Mode, which reduces power consumption.

SLEEPB pin	Function
H	Normal operation
L	All major circuits are OFF

Note: When the IC recovers (restarts) from Sleep Mode, since the OSC and charge-pump circuits are OFF, a wake-up time is required. Design your system to accommodate the time needed for the restart.

Each internal block follows below table in Sleep Mode.

Table 7.14

	Circuit block											
Mode	Input circuit (SLEEPB terminal)	Input circuit (except SLEEPB terminal)	Power supply monitoring	Over-temperature detection	Current limit	Over-current detection	Current monitoring	DIAG circuit	Internal OSC circuit	SPI circuit	CP circuit	Motor output circuit
Normal	●	●	●	●	●	●	●	●	●	●	●	●
Half-Bridge	●	●	●	●	×	●	● (*)	●	●	●	●	●
Disable	●	●	●	●	●	●	●	●	●	●	●	● (output OFF)
Sleep Mode	●	×	×	×	×	×	×	×	×	×	×	×

●: Operating, ×: Disabled

*: In Half-Bridge Mode, it becomes invalid since current monitoring monitors the sum of the high side current of OUT1/2 and OUT3/4 which flows into CM1/2 terminal.

7.11. OSC circuit (oscillation circuit) (Figure 7.25)

The IC has the oscillation circuit with 16 MHz.
The oscillation circuit automatically starts when VCC rises without any trigger signals.

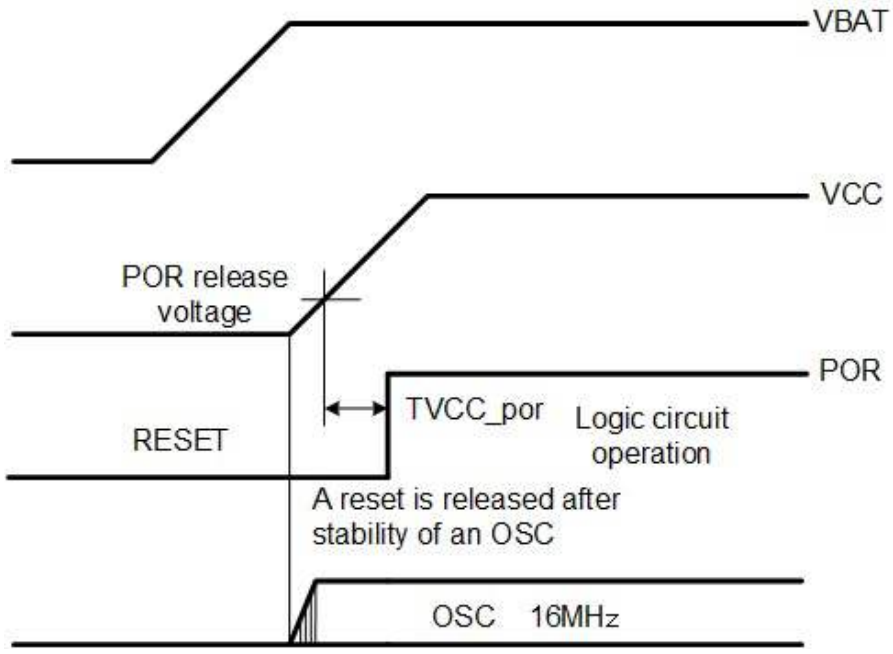


Figure 7.25 OSC circuit starting operation

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.12. SPI communication circuit

This IC incorporates an SPI communication circuit for bidirectional communication between this IC and an external MCU. This IC is the Slave and the external MCU is the Master in the communication. Using SPI communication, this IC and the external MCU can transmit and receive information to set various motor control parameters, monitor various abnormality detections, and control the motor drive circuit (drive mode and PWM duty ratio).
Both parallel and daisy-chain connections can be used to connect this IC and the external MCU.

7.12.1. SPI communication operation

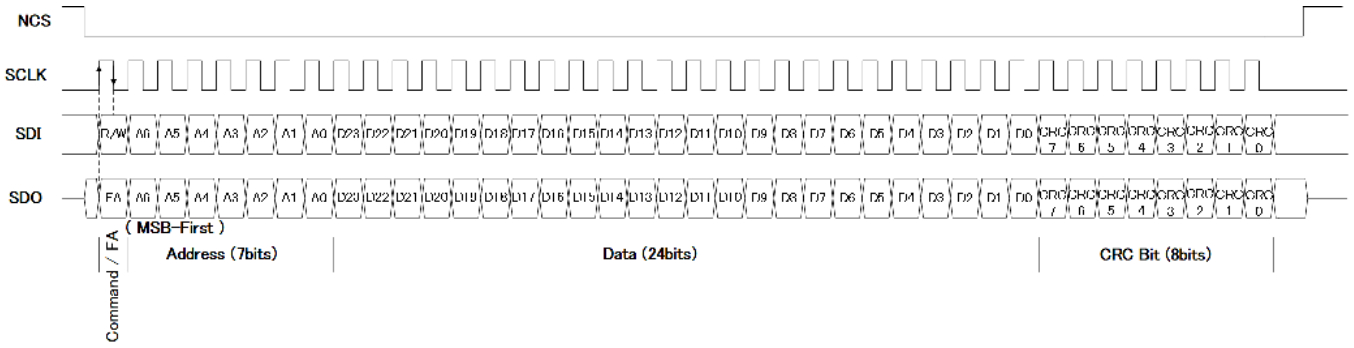


Figure 7.26 SPI communication format

NCS is a chip-select input. When NCS is low, communication with an external MCU is enabled (low active). The IC determines the received command at the rising edge of NCS. When NCS is low, serial data is transmitted and received, synchronized with SCLK. When NCS is high, SDO is in a high-impedance (Hi-Z) state.

SCLK is a clock input to synchronize communication between this IC and an external MCU. The external MCU, synchronized with the rising edge of SCLK, outputs transmission data to SDI of this IC. This IC, synchronized with the falling edge of SCLK, reads the received data. Similarly, this IC, synchronized with the rising edge of SCLK, outputs transmission data from SDO to the external MCU or to the next IC in the daisy chain. The external MCU or next IC in the daisy chain, synchronized with the falling edge of SCLK, reads the received data.

SDI (Serial Data In) allows this IC to receive serial data. It receives serial data in order from MSB to LSB. SDI reads data, synchronizing with the falling edge of SCLK. The external MCU outputs transmission data, synchronized with the rising edge of SCLK.

SDO (Serial Data Out) allows this IC to transmit serial data. It transmits serial data in order from MSB to LSB. SDO outputs data, synchronized with the rising edge of SCLK. When NCS is high, SDO is in a high-impedance (Hi-Z) state.

As shown in Figure 7.26, the length of serial data is 40 bits, which is defined as 1 frame. There are two communication operations: READ and WRITE. The external MCU selects READ/WRITE using the command bit (R/W bit) of the serial data.

For a parallel connection between the external MCU and this IC, NCS must be turned to low for each frame. For a daisy-chain connection, the MCU can communicate consecutively with multiple ICs (up to 8) after turning NCS to low. For example, if 8 ICs are connected in a daisy chain, 8 frames (40 bits * 8 = 320 bits) can be communicated consecutively while NCS is low.

7.12.1.1. SPI communication READ operation

READ operation
Table 7.15 and Table 7.16 show the data configuration for the READ operation.

Table 7.15. READ command data configuration

	40 bits			
	bit39	bit38 to bit32	bit31 to bit8	bit7 to bit0
MCU transmits; IC receives (SDI)	Command RW[39]	Address ADR[38:32]	Blank Dummy[31:8]	CRC data CRC[7:0]

- bit39 selects READ/WRITE operation. Command RW[39] = 0x0 specifies READ.
- bit38-32 specifies READ address. ADR[38:32] specifies the address that the external MCU reads.
- bit31-8: Blank bits. READ command does not use the bits.
- bit7-0: CRC data bits. The external MCU calculates the CRC data. The range of CRC operands is bit39-bit8 (RW, ADR, and Dummy).
- This IC transmits (replies with) DATA[31:8] that corresponds to the address ADR[38:32] specified by the READ command in the next frame.
- The range of CRC operands in READ command data received by this IC is bit39-bit8 (RW, ADR, and Dummy). When CRC identifies an error, the READ command is not executed.

Table 7.16. READ (reply) data configuration

	40 bits			
	bit39	bit38 to bit32	bit31 to bit8	bit7 to bit0
IC transmits (SDO); MCU receives	SPI error flag FA[39]	Address ADR[38:32]	Data DATA[31:8]	CRC data CRC[7:0]

- bit39: Error flag for the previous frame. When an error is detected, SPI communication error flag FA[39] = 0x1 is output.
- bit38-32: Address specified by the external MCU.
- bit31-8: Transmitted data DATA[31:8]. For a READ command, the IC transmits (replies with) data to the external MCU. The data to be transmitted is located in this IC's register corresponding to the address specified by the external MCU.
- bit7-0: CRC data. The IC calculates the CRC data. The range of CRC operands is bit39-bit8 (FA, ADR, and DATA).

7.12.1.2. SPI communication WRITE operation

WRITE operation
Table 7.17 and Table 7.18 show the data configuration in the WRITE operation.

Table 7.17. WRITE command data configuration

	40 bits			
	bit39	bit38 to bit32	bit31 to bit8	bit7 to bit0
MCU transmits; IC receives (SDI)	Command RW[39]	Address ADR[38:32]	Data DATA[31:8]	CRC data CRC[7:0]

- bit39 selects READ/WRITE operation. Command RW[39] = 0x1 specifies WRITE.
- bit38-32 specifies WRITE address. ADR[38:32] specifies the address in which the IC writes data.
- bit31-8: Transmitted data DATA[31:8] (data to be written to the IC).
- bit7-0: CRC data bits. The external MCU calculates the CRC data. The range of CRC operands is bit39-bit8 (RW, ADR, and DATA).
- The IC writes DATA[31:8] in the register that corresponds to the address ADR[38:32] specified by the WRITE command.

・The range of CRC operands in WRITE command data received by the IC is bit39-bit8 (RW, ADR, and DATA). When CRC identifies an error, the WRITE command is not executed.

Table 7.18. READ after WRITE (reply) data configuration

	40 bits			
	bit39	bit38 to bit32	bit31 to bit8	bit7 to bit0
IC transmits (SDO); MCU receives	SPI error flag FA[39]	Address ADR[38:32]	Data DATA[31:8]	CRC data CRC[7:0]

・bit39: Error flag for the previous frame. When an error is detected, SPI communication error flag FA[39] = 0x1 is output.
・bit38-32: Address specified by the external MCU.
・bit31-8: Transmitted data DATA[31:8]. For a WRITE command, the IC transmits (replies with) data to the external MCU. The transmitted data is the data written in this IC's register corresponding to the address specified by the external MCU.
・bit7-0: CRC data. The IC calculates the CRC data. The range of CRC operands is bit39-bit8 (FA, ADR, and DATA).
・The IC transmits the READ-after-WRITE (reply) data to the external MCU to allow the MCU to verify whether the WRITE is correct.

7.12.1.3. SPI communication error

SPI communication error
For the following cases of (1), (2), or (3) in SPI communication, the IC detects a communication error. When this occurs, the IC does not execute commands or register writes, and it outputs SPI communication error flag FA[0] = 0x1. The communication error in the current frame is reflected in the SPI communication error flag of the next frame.
For SPI communication error (1), (2), or (3), the DIAG pin outputs L. When SPI communication resumes normal operation, the DIAG pin automatically returns from L to H.

(1) CRC error
・An error in the received data is detected.

(2) Abnormal SCLK clock count
・While NCS = L, the SCLK clock count is less than or more than the specification.

(3) Abnormal address detected
・Access was specified to an address where no register exists.

CRC error (CRC calculation)
Each piece of transmitted/received data in SPI communication includes CRC check bits. CRC check bits are bit7-bit0 in a frame (40 bits). If data received by the IC from an external MCU contains a CRC error, the data is not accepted and is discarded. For data transmitted from this IC, use the external MCU to detect and properly handle a CRC error.

CRC calculation parameters used in this IC are as follows:
Generating polynomial: $X^8+X^4+X^3+X^2+1$
Bit-shift direction: Normal (left bit shift)
Initial value: 0x00 (All "0")

7.12.2. SPI connection method

7.12.2.1. SPI parallel connection

SPI parallel connection

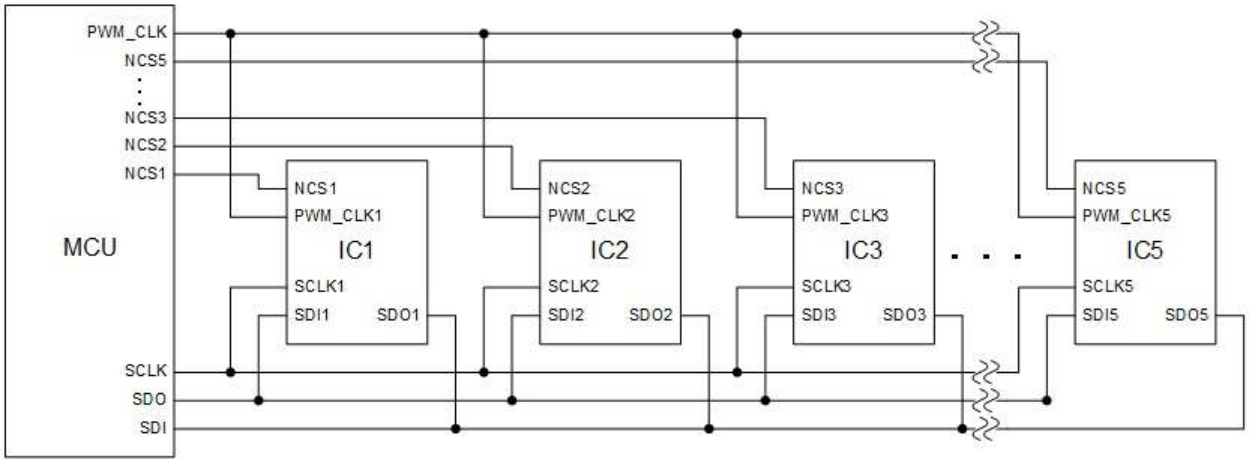


Figure 7.27 Example SPI parallel connection (five connected ICs)

In the example SPI parallel connection (Figure 7.), a communication clock (SCLK), a data output (SDO), and a data input (SDI) are connected in parallel. The external MCU (Master) assigns an independent chip-select signal to each IC (Slaves: IC1 to IC5) to enable individual access. Since all ICs (Slaves: IC1 to IC5) share one communication clock (SCLK) and two data lines (SDO and SDI), only the IC (Slave) whose chip-select signal (NCS) is low receives the communication clock and the data, and only it replies.

7.12.2.2. SPI daisy-chain connection

SPI daisy-chain connection

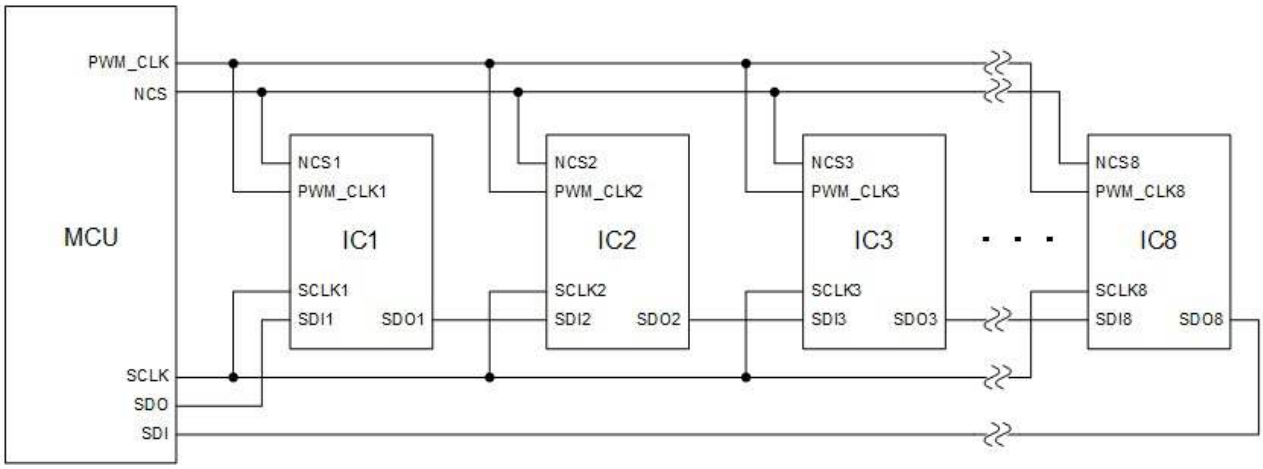


Figure 7.28 Example SPI daisy-chain connection (eight connected ICs)

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

A single chip-select signal (NCS) from the external MCU (Master) controls the NCS inputs of all ICs (Slaves). All ICs (Slaves) operate with the same clock signal. Only the first IC (Slave: IC1) connected to the daisy chain directly receives data from the external MCU (Master). Every other IC (Slave: IC2 to IC8) receives data with its SDI from the SDO of the IC located before it in the daisy chain.

In the example SPI daisy-chain connection (Figure 7.2828), IC1 receives data directly from the external MCU while the chip-select signal (NCS) is low and captures the data in an internal shift register in IC1. While the external MCU keeps NCS low, the data is propagated to the SDO1 output of IC1 as is. Since SDO1 of IC1 is connected to SDI2 of IC2, the output data from SDO1 of IC1 is sent to an internal shift register in IC2. While IC2 is receiving data from IC1, the external MCU can simultaneously transmit another command to IC1. The new command overwrites the previous data in the shift register of IC1. While NCS is low and until every IC (IC1 to IC8) receives a command directed to it, sets of data propagate through the daisy-chain connection. A command stored in the shift register of each IC is executed at the rising edge of NCS.
If eight ICs are connected in a daisy chain, the low period of NCS has a duration of eight frames.

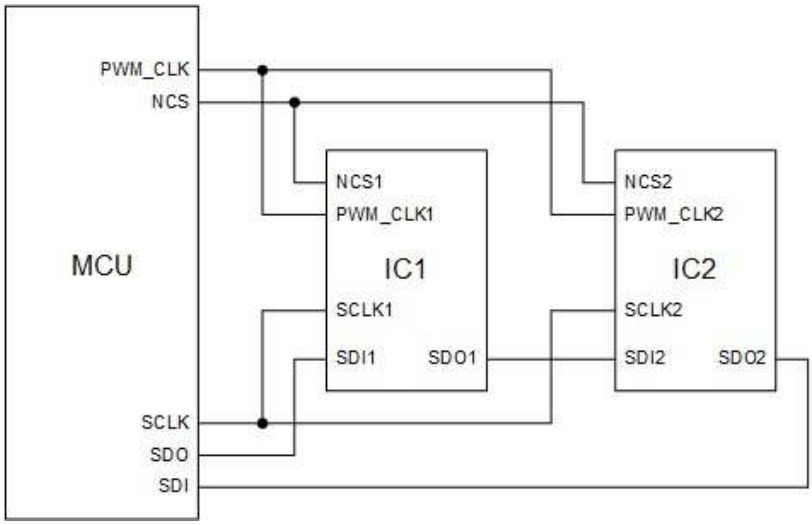


Figure 7.29 Example SPI daisy-chain connection for two ICs

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

- READ command communication timing for 2-IC serial (daisy-chain) connection
  - Commands for the two ICs are determined at the rising edge of NCS.
  - When the communication clock (SCLK) inputs more than 40 clocks to IC1 and IC2, the data input to IC1 shifts out from SDO of IC1 and enters SDI of IC2. When the MCU inputs 80 bits, READ commands are stored in IC1 (*2) and IC2 (*1), which are determined at the rising edge of NCS.
  - When the MCU transmits the next command (Command N+1), the ICs transmit 80 bits of READ data corresponding to the READ command (Command N) from the external MCU. The response to (*1) is (*3), and the response to (*2) is (*4).

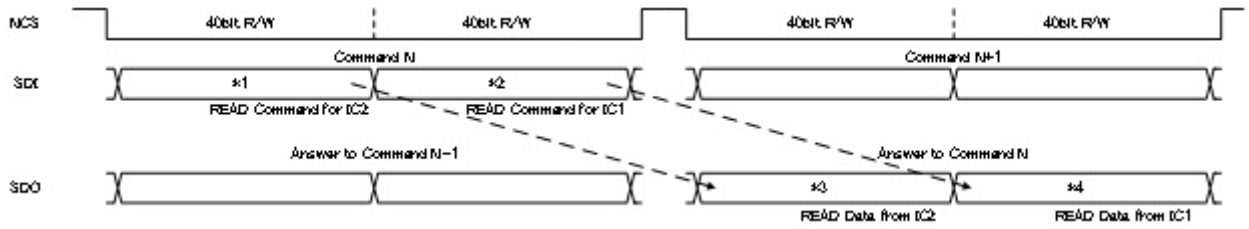


Figure 7.30 2-IC daisy-chain connection READ timing

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

- WRITE command communication timing for 2-IC serial (daisy-chain) connection
  - Commands for the two ICs are determined at the rising edge of NCS.
  - When the communication clock (SCLK) inputs more than 40 clocks to IC1 and IC2, the data input to IC1 shifts out from SDO of IC1 and enters SDI of IC2. When the MCU inputs 80 bits, WRITE commands are stored in IC1 (*2) and IC2 (*1). The commands for the two ICs are determined at the rising edge of NCS, and the data is written.
  - When the MCU transmits the next command (Command N+1), the ICs transmit 80 bits of data (including written data) corresponding to the WRITE command (Command N) from the external MCU. The response to (*1) is (*3) and the response to (*2) is (*4).

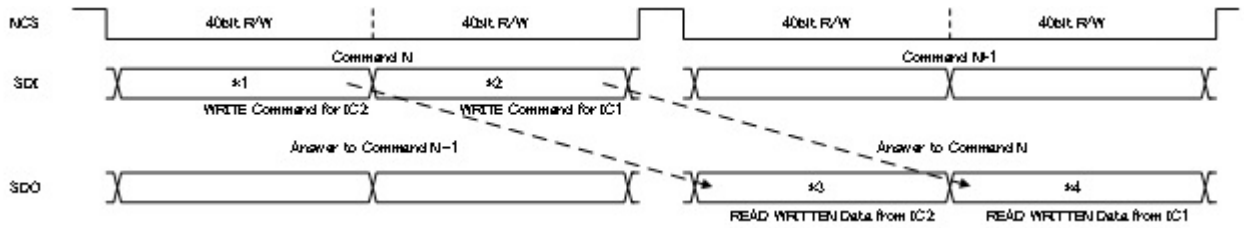


Figure 7.31 2-IC daisy-chain connection WRITE timing

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.12.3. Motor control operation using SPI communication

Setting the ISEL1/ISEL2 pin to H (connected to VCC) to set SPI motor drive mode also enables motor control using SPI communication.
The settings of the ISEL1 and ISEl2 pins (H or L) can be read from the STATUS1 register, whose address is ADR[38:32] = 0x01.

7.12.3.1. Operation when ISEL1/ISEL2 = H

- Motor control using SPI communication: Enabled
  The data written in the CONFIG3/4/5/6 registers, whose addresses are ADR[38:32] = 0x06, 0x07, 0x08, and 0x09, drive the motor.See Table 7.19.
- PWM1/2/3/4 pin input: Disabled
  No input signals are accepted.
- Clock for output Dr circuit (IC internal circuit): Enabled
  Select the external input clock (input to the PWM_CLK pin). Use an internal clock for various abnormality detection circuits to avoid the filtering time variations that an external clock may cause.
- PWM_CLK pin input clock abnormality detection: Enabled
  When the PWM_CLK pin input clock is stopped, the IC uses an internal clock as an alternative. The IC notifies the MCU using SPI when the PWM_CLK pin input clock is abnormal. When using an internal clock instead of an external clock, the IC drives the outputs (OUT1/2 and OUT3/4) with a 2MHz clock, which it generates by dividing the original oscillation 16 MHz by 8, as retaining the CONFIG3/4/5/6 register settings.

7.12.3.2. Operation when ISEL1/ISEL2 = L

- Motor control using SPI communication: Disabled
  The data written in the CONFIG3/4/5/6 registers, whose addresses are ADR[38:32] = 0x06, 0x07, 0x08, and 0x09, are ineffective.
  The IC discards data from WRITE attempts to prevent overwriting.
  The initial value (all "0") is retained.
- PWM1/2/3/4 pin input: Enabled
  The IC drives the outputs (OUT1/2 and OUT3/4) according to the input signals.
- Clock for output Dr circuit (IC internal circuit): Disabled
  The external input clock (input to the PWM_CLK pin) is not used.
- PWM_CLK pin input clock abnormality detection: Enabled
  PWM_CLK pin input clock suspension is monitored. However, the PWM_CLK pin input clock fault is ignored.
  When ISEL1/ISEL2 = L, connect the PWM_CLK pin to GND.

7.12.3.3. External clock supply by PWM_CLK pin

An external MCU supplies a reference clock of the PWM frequency to the PWM_CLK pin.
Each IC connected using SPI communication (parallel or daisy chain) generates its PWM control clock frequency from the reference clock of the PWM frequency externally supplied to the PWM_CLK pin.
The PWM control clock frequency of each IC (for Ch1 and Ch2) can be selected with the CONFIG register setting using SPI communication.

7.12.3.4. Motor operation setting using SPI communication

Write the settings of motor operation (forward/reverse/brake/output OFF (Hi-Z)), drive cycle period, and duty-ON period (PWM duty-ON interval) in address ADR[38:32] = 0x08 and 0x09.
Setting CONFIG5/6 data: DATA[31:30] selects a motor operation.
Setting CONFIG5/6 data: DATA[29:19] specifies a PWM drive cycle period.
Setting CONFIG5/6 data: DATA[18:8] specifies a duty-ON period within the PWM drive cycle period set by data DATA[29:19]. The period is defined as a "PWM duty-ON interval".

Write a setting to determine whether to apply low- or high-side regeneration during PWM duty-OFF intervals in address ADR[6:0] = 0x04/0x05.
Setting CONFIG1/2 data: DATA[20] selects either low- or high-side regeneration during PWM duty-OFF intervals.

7.12.3.5. Update timing for each motor operation control setting using SPI communication

・SPI settings updated at the next PWM cycle after receiving SPI:
- Base frequency
- ON delay time
- Duty-ON period
- Drive cycle period
- Motor operation
  - ・Forward ⇔reverse
  - ・Forward/reverse ⇒brake

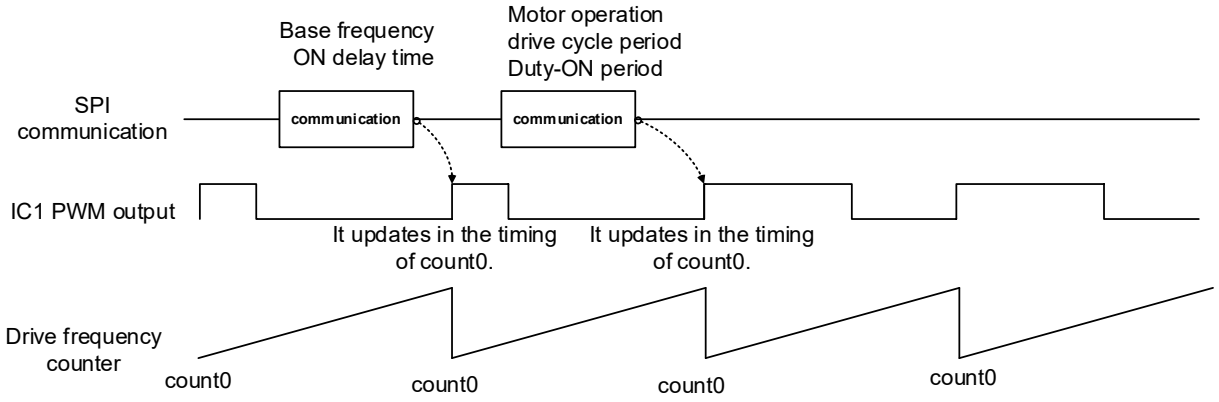


Figure 7.32 Motor operation control using SPI communication: SPI setting update timing 1

Note: The IC updates the operation settings of brake/output OFF (Hi-Z) ⇒forward/reverse and any state ⇒ output OFF (Hi-Z) after SPI reception, i.e., within 1,000 ns after the rising edge of NCS (see Table 10.11. SPI communication: Electrical characteristics). Updates are reflected in the PWM output before the next PWM cycle.

7.12.3.6. ON delay time when using multiple H-bridges (daisy-chain connection)

When using multiple H-bridges in a daisy-chain connection for motor control using SPI communication, set an ON delay time using SPI communication to prevent simultaneous PWM duty ON.

ON delay time is calculated as follows:

ON delay time = (1/fdiv) * ON delay time setting register value (7.1)
fdiv: Base frequency

= external clock frequency * base frequency register setting (frequency division ratio)

1) ON delay time setting register value ≤ drive frequency setting register value
2) If ON delay time setting register value = drive frequency setting register value, the delay time is one drive cycle period

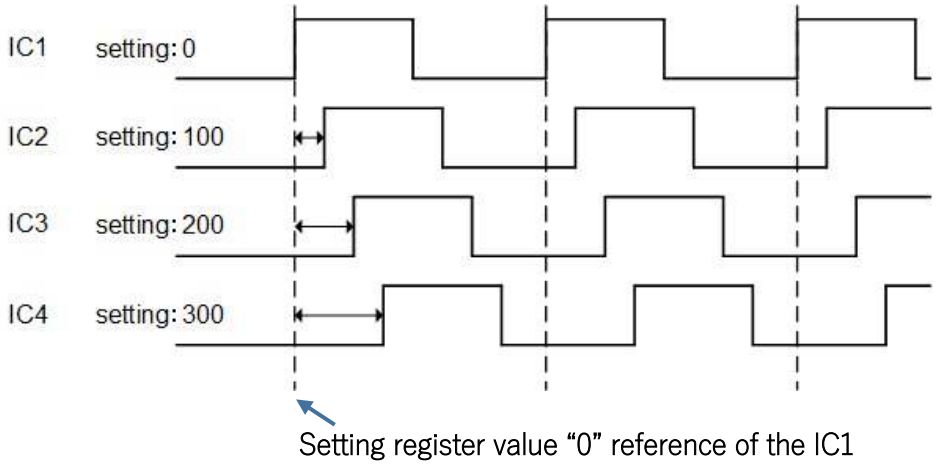


Figure 7.33 ON delay time when using multiple H-bridges

7.12.4. PWM_CLK pin input clock abnormality detection

This IC incorporates a function to monitor the suspension of the external clock input to the PWM_CLK pin. When PWM_CLK (2 MHz) is suspended for 8 µs (typ.), the function determines that the external clock is suspended. This function starts monitoring once the IC invokes the VCC power supply and cancels the reset of internal logic.
When PWM_CLK is not used (i.e., no external clock (2 MHz) is input to the PWM_CLK pin, even during normal motor operation) the abnormality detection flag "1" is set in the SPI register (STATUS1 DATA[12]).

7.12.5. SPI communication disruption detection

This IC has a function to monitor SPI communication disruptions. SPI sets the threshold for SPI communication-disruption duration, and the IC monitors it. For an IC operation after it detects an SPI communication disruption, SPI settings can specify "to continue the operation immediately before the disruption" or "to turn the outputs (OUT1/2 and OUT3/4) OFF (Hi-Z)".
For the settings of SPI communication-disruption threshold and of IC operation selection after SPI communication disruption, see Table 7.19. SPI register map.
When the IC detects an SPI communication disruption, the DIAG pin outputs L. When SPI communication resumes normal operation, the DIAG pin automatically returns from L to H.
However, when it detects an SPI communication disruption, the abnormality bit of SPI is latched (1WC).

7.12.6. Daisy-chain connection containing both PWM input motor drive and SPI motor drive

A daisy-chain connection for motor control may contain both ICs using PWM input motor drive and ICs using SPI motor drive. When this occurs, set the ISEL1/ISEL2 pins and arrange the PWM_CLK pin as shown in Figure 7.3434.

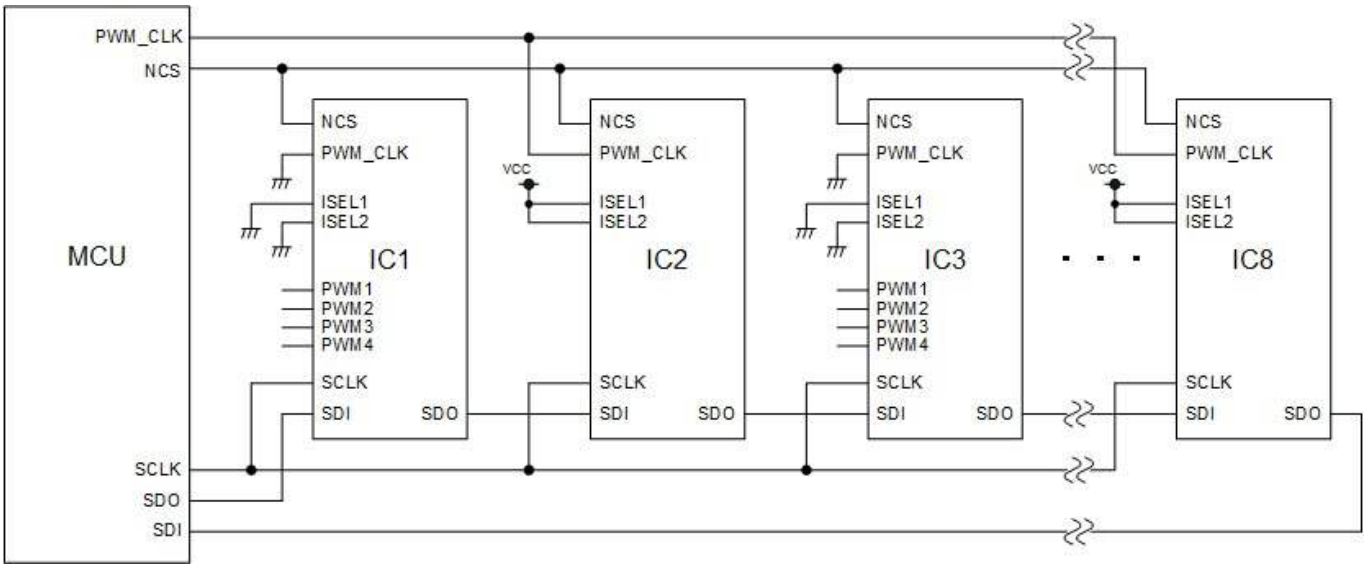


Figure 7.34 Example daisy-chain connection containing both PWM input motor drive and SPI motor drive ICs

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

- A daisy-chain connection containing both motor operation controls, PWM1/2 and SPI (Figure 7.34).
- Motor operation control with ISEL1 = L: PWM1/2 control and ISEL1 = H: SPI control
- For ICs with PWM1/2/3/4 control (ISEL1/ISEL2 = L), connect the PWM_CLK pins to GND, where the PWM_CLK wire skips these pins.

7.12.7. SPI register map

Table 7.19. SPI register map

NAME	R/W	Address	Data bit																						CRC bit
	[39]	[38:32]	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
STATUS1	R (1WC)	0x01	ISEL1 pin state detection (automatic recovery)	ISEL2 pin state detection (automatic recovery)	OSEL1/OSEL2 pin state detection (automatic recovery)		Initial/restarted diagnosis error (VBAT under-voltage)	Initial/restarted diagnosis start abnormality (VBAT under-voltage)	Initial/restarted diagnosis error (VCC under-voltage)	Initial/restarted diagnosis start abnormality (VCC under-voltage)	Initial/restarted diagnosis error (over-temperature detection)	Initial/restarted diagnosis start abnormality (over-temperature detection)	Initial/restarted diagnosis Ch1 diagnosis result	Initial/restarted diagnosis Ch2 diagnosis result	Over-temperature detection (automatic recovery)	Ch1 open-load detection during non-operation	Ch2 open-load detection during non-operation	SPI communication disruption detection (1WC_Flag)	SPI communication CRC error detection (1WC_Flag)	SPI communication SCLK clock count abnormality detection (1WC_Flag)	SPI communication abnormal address detection (1WC_Flag)	External clock abnormality detection (PWM_CLK input) (1WC_Flag)	VBAT under-voltage detection (automatic recovery)	VCC under-voltage detection (1WC_Flag)	Ch1 state (*1) (automatic recovery)	Ch2 state (*1) (automatic recovery)	CRC calculation result of bit[39:8]
STATUS2	R (1WC)	0x02	-	-	-	-	Initial/restarted diagnosis error (Ch1 over-current detection)	Initial/restarted diagnosis start abnormality (Ch1 over-current detection)	-	-	Initial/restarted diagnosis error (Ch1 open-load detection during operation)	Initial/restarted diagnosis start abnormality (Ch1 open-load detection during operation)	Initial/restarted diagnosis error (Ch1 open-load detection during non-operation)	Initial/restarted diagnosis start abnormality (Ch1 open-load detection during non-operation)	OUT1 high-side over-current detection (short-circuit to ground) (automatic recovery)	OUT2 high-side over-current detection (short-circuit to ground) (automatic recovery)	OUT1 low-side over-current detection (short-circuit to power supply) (automatic recovery)	OUT2 low-side over-current detection (short-circuit to power supply) (automatic recovery)	Ch1 open-load detection during operation (automatic recovery)	-	-	-	-	-	-	-	CRC calculation result of bit[39:8]
STATUS3	R (1WC)	0x03	-	-	-	-	Initial/restarted diagnosis error (Ch2 over-current detection)	Initial/restarted diagnosis start abnormality (Ch2 over-current detection)	-	-	Initial/restarted diagnosis error (Ch2 open-load detection during operation)	Initial/restarted diagnosis start abnormality (Ch2 open-load detection during operation)	Initial/restarted diagnosis error (Ch2 open-load detection during non-operation)	Initial/restarted diagnosis start abnormality (Ch2 open-load detection during non-operation)	OUT3 high-side over-current detection (short-circuit to ground) (automatic recovery)	OUT4 high-side over-current detection (short-circuit to ground) (automatic recovery)	OUT3 low-side over-current detection (short-circuit to power supply) (automatic recovery)	OUT4 low-side over-current detection (short-circuit to power supply) (automatic recovery)	Ch2 open-load detection during operation (automatic recovery)	-	-	-	-	-	-	-	CRC calculation result of bit[39:8]

R: Read, R (1WC): Write "1" to clear flag, W: Write

*1: Even in Combined-Channel Mode (LARGE Mode), an abnormality flag is set in the channel that detects the abnormality.

NAME	R/W	Address	Data bit																						CRC bit
	[39]	[38:32]	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
CONFIG1	R/W	0x04	-	-	-	-	-	-	-	-	-	Ch1 open-load detection during non-operation time setting		Ch1 PWM duty-OFF interval low- or high-side regeneration setting	VBAT under-voltage cancellation delay time (common to Ch1 and Ch2) (digital filter)	Ch1 current limit threshold: upper limit setting	Ch1 (OUT1/2) current limit threshold: lower limit setting	Ch1 open-load detection during operation threshold setting		Ch1 SR mode SR2, SR1, SR0			Ch1 over-current detection mode (latched or automatic recovery)	SPI communication-disruption determination threshold setting (common to Ch1 and Ch2)		Operation mode setting when SPI communication is disrupted (common to Ch1 and Ch2)	CRC calculation result of bit[39:8]
CONFIG2	R/W	0x05	-	-	-	-	-	-	-	-	-	Ch2 open-load detection during non-operation time setting		Ch2 PWM duty-OFF interval low- or high-side regeneration setting	-	Ch2 current limit threshold: upper limit setting	Ch2 (OUT3/4) current limit threshold: lower limit setting	Ch2 open-load detection during operation threshold setting		Ch2 SR mode SR2, SR1, SR0			Ch2 over-current detection mode (latched or automatic recovery)	-	-	-	CRC calculation result of bit[39:8]
CONFIG3	R/W	0x06	Ch1 base frequency setting		-	-	-	-	-	-	-	-	-	-	-	Ch1 ON delay time setting (counter value: 0 to 2047)										CRC calculation result of bit[39:8]
CONFIG4	R/W	0x07	Ch2 base frequency setting		-	-	-	-	-	-	-	-	-	-	-	Ch2 ON delay time setting (counter value: 0 to 2047)										CRC calculation result of bit[39:8]

R: Read, R (1WC): Write "1" to clear flag, W: Write

NAME	R/W	Address	Data bit																							CRC bit
	[39]	[38:32]	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
CONFIG5	R/W	0x08	Ch1 motor operation setting (forward/reverse/brake/output OFF (Hi-Z))		Ch1 drive frequency setting (counter value: 0 to 2047)											Ch1 duty-ON period setting (PWM duty) (counter value: 0 to 2047)											CRC calculation result of bit[39:8]
CONFIG6	R/W	0x09	Ch2 motor operation setting (forward/reverse/brake/output OFF (Hi-Z))		Ch2 drive frequency setting (counter value: 0 to 2047)											Ch2 duty-ON period setting (PWM duty) (counter value: 0 to 2047)											CRC calculation result of bit[39:8]
CONFIG7	W	0x0A	Ch1 over-current detection output OFF cancellation for short-circuit to power supply or ground	Ch1 open-load diagnosis execution during non-operation	Ch1 CONFIG3/CONFIG5 setting update	Ch2 over-current detection output OFF cancellation for short-circuit to power supply or ground	Ch2 open-load diagnosis execution during non-operation	Ch2 CONFIG4/CONFIG6 setting update	OUT1 over-current detection output OFF cancellation for short-circuit to power supply or ground (effective only in Half Mode)	OUT2 over-current detection output OFF cancellation for short-circuit to power supply or ground (effective only in Half Mode)	OUT3 over-current detection output OFF cancellation for short-circuit to power supply or ground (effective only in Half Mode)	OUT4 over-current detection output OFF cancellation for short-circuit to power supply or ground (effective only in h Half Mode)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC calculation result of bit[39:8]

R: Read, R (1WC): Write "1" to clear flag, W: Write

7.12.7.1. List of SPI DATA[31:8]

Table 7.20. STATUS1 (ADR[38:32]: 0x01)

Bit	NAME	INIT (initial value)	Command (R/W)	Description
31	ISEL1 pin state detection	0	R	ISEL1 pin state read-out 0: L (connected to GND), 1: H (connected to VCC)
30	ISEL2 pin state detection	0	R	ISEL2 pin state read-out 0: L (connected to GND), 1: H (connected to VCC)
29 28	OSEL1/OSEL2 pin state detection	0 0	R R	OSEL1/OSEL2 pin state read-out 00: OSEL1/2 = L/L (Combined-Channel Mode: both OSEL1/2 are connected to GND) 01: OSEL1/2 = L/H (Dual-Channel Mode: OSEL1 = GND, OSEL2 = VCC) 10: OSEL1/2 = H/L (Half Mode: OSEL1 = VCC, OSEL2 = GND) 11: OSEL1/2 = H/H (Prohibited Mode: all outputs are latched to OFF (Hi-Z))
27	Initial/restarted diagnosis error (VBAT under-voltage)	1	R	Initial/restarted diagnosis error detected in VBAT under-voltage detection circuit (threshold of VBAT under-voltage detection circuit is abnormal) 0: Undetected, 1: Detected
26	Initial/restarted diagnosis start abnormality (VBAT under-voltage)	1	R	Initial/restarted diagnosis start abnormality detected in VBAT under-voltage detection circuit (VBAT under-voltage detection circuit cannot start because it is not reset to the normal value (undetected state)) 0: Undetected, 1: Detected
25	Initial/restarted diagnosis error (VCC under-voltage)	1	R	Initial/restarted diagnosis error detected in VCC under-voltage detection circuit (threshold of VCC under-voltage detection circuit is abnormal) 0: Undetected, 1: Detected
24	Initial/restarted diagnosis start abnormality (VCC under-voltage)	1	R	Initial/restarted diagnosis start abnormality detected in VCC under-voltage detection circuit (VCC under-voltage detection circuit cannot start because it is not reset to the normal value (undetected state)) 0: Undetected, 1: Detected
23	Initial/restarted diagnosis error (over-temperature detection)	1	R	Initial/restarted diagnosis error detected in over-temperature detection circuit (threshold of the over-temperature detection circuit is abnormal) 0: Undetected, 1: Detected
22	Initial/restarted diagnosis start abnormality (over-temperature detection)	1	R	Initial/restarted diagnosis start abnormality detected in over-temperature detection circuit (over-temperature detection circuit cannot start because it is not reset to the normal value (undetected state)) 0: Undetected, 1: Detected
21	Initial/restarted diagnosis Ch1 diagnosis result	1	R	Results of initial/restarted diagnosis and diagnosis start abnormality (diagnosis results of detection circuits for over-current and open load during operation/non-operation) for Ch1 (OUT1/2) 0: Undetected 1: A bit of STATUS2 diagnosis results is abnormal
20	Initial/restarted diagnosis Ch2 diagnosis result	1	R	Results of initial/restarted diagnosis and diagnosis start abnormality (diagnosis results of detection circuits for over-current and open load during operation/non-operation) for Ch2 (OUT3/4) 0: Undetected 1: A bit of STATUS3 diagnosis results is abnormal
19	Over-temperature detection	0	R	IC over-temperature detected 0: Undetected, 1: Detected
18	Ch1 open-load detection during non-operation	0	R	Ch1 (OUT1/2) open load during non-operation detected 0: Undetected, 1: Detected
17	Ch2 open-load detection during non-operation	0	R	Ch2 (OUT3/4) open load during non-operation detected 0: Undetected, 1: Detected
16	SPI communication disruption detection	0	R (1WC)	SPI communication disruption detected 0: Undetected, 1: Detected
15	SPI communication CRC error detection	0	R (1WC)	SPI communication CRC error detected 0: Undetected, 1: Detected
14	SPI communication SCLK clock count abnormality detection	0	R (1WC)	SPI communication SCLK clock count abnormality detected 0: Undetected, 1: Detected

13	SPI communication abnormal address detection	0	R (1WC)	SPI communication abnormal address detected 0: Undetected, 1: Detected
12	External clock abnormality detection (PWM_CLK input)	0	R (1WC)	External clock abnormality (suspension) detected 0: Undetected, 1: Detected
11	VBAT under-voltage detection	0	R	VBAT under-voltage abnormality detected 0: Undetected, 1: Detected
10	VCC under-voltage detection	0	R (1WC)	VCC under-voltage abnormality detected 0: Undetected, 1: Detected
9	Ch1 state	0	R	Ch1 (OUT1/2) state (detection status of detection circuits for over-current and open load during operation) 0: Undetected, 1: A bit of STATUS2 [19:15] indicates an abnormality
8	Ch2 state	0	R	Ch2 (OUT3/4) state (detection status of detection circuits for over-current and open load during operation) 0: Undetected, 1: A bit of STATUS3 [19:15] indicates an abnormality

Table 7.21. STATUS2 (ADR[38:32]: 0x02)

Bit	NAME	INIT (initial value)	Command (R/W)	Description
31	-	0	R	-
30	-	0	R	-
29	-	0	R	-
28	-	0	R	-
27	Initial/restarted diagnosis error (Ch1 over-current detection)	1	R	Initial/restarted diagnosis error in over-current detection circuit on Ch1 (OUT1/2) side detected (when threshold of over-current detection circuit is abnormal) 0: Undetected, 1: Detected
26	Initial/restarted diagnosis start abnormality (Ch1 over-current detection)	1	R	Initial/restarted diagnosis start abnormality in over-current detection circuit on Ch1 (OUT1/2) side detected (over-current detection circuit cannot start because it is not reset to the normal value (undetected state)) 0: Undetected, 1: Detected
25	-	0	R	-
24	-	0	R	-
23	Initial/restarted diagnosis error (Ch1 open-load detection during operation)	1	R	Initial/restarted diagnosis error in the detection circuit for open load during operation on Ch1 (OUT1/2) side detected (when threshold of detection circuit for open load during operation is abnormal) 0: Undetected, 1: Detected
22	Initial/restarted diagnosis start abnormality (Ch1 open-load detection during operation)	1	R	Initial/restarted diagnosis start abnormality in the detection circuit for open load during operation on Ch1 (OUT1/2) side (circuit that detects open load during operation cannot start because it is not reset to the normal value (undetected state)) 0: Undetected, 1: Detected
21	Initial/restarted diagnosis error (Ch1 open-load detection during non-operation)	1	R	Initial/restarted diagnosis error in the detection circuit for open load during non-operation on Ch1 (OUT1/2) side detected (when threshold of detection circuit for open load during non-operation is abnormal) 0: Undetected, 1: Detected
20	Initial/restarted diagnosis start abnormality (Ch1 open-load detection during non-operation)	1	R	Initial/restarted diagnosis start abnormality in the detection circuit for open load during non-operation on Ch1 (OUT1/2) side (circuit that detects open load during non-operation cannot start because it is not reset to the normal value (undetected state)) 0: Undetected, 1: Detected
19	OUT1 high-side over-current detection (short-circuit to ground detection)	0	R	OUT1 high-side over-current (short-circuit to ground) detected 0: Undetected, 1: Detected
18	OUT2 high-side over-current detection (short-circuit to ground detection)	0	R	OUT2 high-side over-current (short-circuit to ground) detected 0: Undetected, 1: Detected
17	OUT1 low-side over-current detection (short-circuit to power supply detection)	0	R	OUT1 low-side over-current (short-circuit to power supply) detected 0: Undetected, 1: Detected
16	OUT2 low-side over-current detection (short-circuit to power supply detection)	0	R	OUT2 low-side over-current (short-circuit to power supply) detected 0: Undetected, 1: Detected
15	Ch1 open-load detection during operation	0	R	Ch1 (OUT1/2) open load during operation detected 0: Undetected, 1: Detected
14	-	0	R	-
13	-	0	R	-
12	-	0	R	-
11	-	0	R	-
10	-	0	R	-
9	-	0	R	-
8	-	0	R	-

Table 7.22. STATUS3 (ADR[38:32]: 0x03)

Bit	NAME	INIT (initial value)	Command (R/W)	Description
31	-	0	R	-
30	-	0	R	-
29	-	0	R	-
28	-	0	R	-
27	Initial/restarted diagnosis error (Ch2 over-current detection)	1	R	Initial/restarted diagnosis error in over-current detection circuit on Ch2 (OUT3/4) side detected (when threshold of over-current detection circuit is abnormal) 0: Undetected, 1: Detected
26	Initial/restarted diagnosis start abnormality (Ch2 over-current detection)	1	R	Initial/restarted diagnosis start abnormality in over-current detection circuit on Ch2 (OUT3/4) side detected (over-current detection circuit cannot start because it is not reset to the normal value (undetected state)) 0: Undetected, 1: Detected
25	-	0	R	-
24	-	0	R	-
23	Initial/restarted diagnosis error (Ch2 open-load detection during operation)	1	R	Initial/restarted diagnosis error in detection circuit for open load during operation on Ch2 (OUT3/4) side detected (when threshold of detection circuit for open load during operation is abnormal) 0: Undetected, 1: Detected
22	Initial/restarted diagnosis start abnormality (Ch2 open-load detection during operation)	1	R	Initial/restarted diagnosis start abnormality in detection circuit for open load during operation on Ch2 (OUT3/4) side (circuit that detects open load during operation cannot start because it is not reset to the normal value (undetected state)) 0: Undetected, 1: Detected
21	Initial/restarted diagnosis error (Ch2 open-load detection during non-operation)	1	R	Initial/restarted diagnosis error in detection circuit for open load during non-operation on Ch2 (OUT3/4) side detected (when threshold of detection circuit for open load during non-operation is abnormal) 0: Undetected, 1: Detected
20	Initial/restarted diagnosis start abnormality (Ch2 open-load detection during non-operation)	1	R	Initial/restarted diagnosis start abnormality in detection circuit for open load during non-operation on Ch2 (OUT3/4) side (circuit that detects open load during non-operation cannot start because it is not reset to the normal value (undetected state)) 0: Undetected, 1: Detected
19	OUT3 high-side over-current detection (short-circuit to ground detection)	0	R	OUT3 high-side over-current (short-circuit to ground) detected 0: Undetected, 1: Detected
18	OUT4 high-side over-current detection (short-circuit to ground detection)	0	R	OUT4 high-side over-current (short-circuit to ground) detected 0: Undetected, 1: Detected
17	OUT3 low-side over-current detection (short-circuit to power supply detection)	0	R	OUT3 low-side over-current (short-circuit to power supply) detected 0: Undetected, 1: Detected
16	OUT4 low-side over-current detection (short-circuit to power supply detection)	0	R	OUT4 low-side over-current (short-circuit to power supply) detected 0: Undetected, 1: Detected
15	Ch2 open-load detection during operation	0	R	Ch2 (OUT3/4) open load during operation detected 0: Undetected, 1: Detected
14	-	0	R	-
13	-	0	R	-
12	-	0	R	-
11	-	0	R	-
10	-	0	R	-
9	-	0	R	-
8	-	0	R	-

Table 7.23. CONFIG1 (ADR[38:32]: 0x04)

Bit	NAME	INIT (initial value)	Command (R/W)	Description
31	-	0	R	-
30	-	0	R	-
29	-	0	R	-
28	-	0	R	-
27	-	0	R	-
26	-	0	R	-
25	-	0	R	-
24	-	0	R	-
23	-	0	R	-
22 21	Ch1 open-load during non-operation detection time setting	0 0	R/W R/W	Detection time setting for Ch1 (OUT1/2) open load during non-operation 00: 100 µs, 01: 50 µs, 10: 500 µs, 11: -
20	Ch1 PWM duty-OFF interval low- or high-side regeneration setting	0	R/W	Low- or high-side regeneration setting during PWM duty-OFF interval on Ch1 (OUT1/2) side 0: Low-side regeneration, 1: High-side regeneration
19	VBAT under-voltage cancellation delay time (common to Ch1 and Ch2)	0	R/W	VBAT under-voltage cancellation delay time (digital filter) setting (common to Ch1 (OUT1/2) and Ch2 (OUT3/4)) 0: 0 µs (no filtering), 1: 100 µs
18	Ch1 current limit threshold upper limit	0	R/W	Ch1 (OUT1/2) current limit threshold upper limit setting 0: 6.5 A, 1: 4.6 A
17	Ch1 current limit threshold lower limit	0	R/W	Ch1 (OUT1/2) current limit threshold lower limit setting 0: Upper limit - 0.25 A, 1: Upper limit - 0.5 A
16 15	Ch1 open load during operation detection threshold setting	0 0	R/W R/W	Detection threshold setting for Ch1 (OUT1/2) open load during operation 00: 200 mA, 01: 100 mA 10: 300 mA, 11: 200 mA
14 13 12	Ch1 SR mode SR2 SR1 SR0	0 0 0	R/W R/W R/W	Ch1 (OUT1/2) SR mode setting 000: Voltage SR Normal (Control OFF, 17.50 V/µs(design data)) 001: Voltage SR Slow1 (1.09 V/µs(design data)) 010: Voltage SR Slow2 (2.19V/µs(design data)) 011: Voltage SR Slow3 (4.38V/µs(design data)) 100: Voltage SR Slow4 (8.75V/µs(design data)) 101: Voltage SR Fast2 (21.88V/µs(design data)) 110: Voltage SR Fast1 (26.25V/µs(design data)) 111: Voltage SR Normal (Control OFF, 17.50 V/µs(design data))
11	Ch1 over-current detection mode (latched or automatic recovery)	0	R/W	Ch1 (OUT1/2) over-current detection mode setting 0: Over-current detection latch mode, 1: Automatic recovery mode
10 9	SPI communication disruption determination threshold time setting (common to Ch1 and Ch2)	0 0	R/W R/W	Ch1 (OUT1/2) & Ch2 (OUT3/4) SPI communication-disruption determination threshold time setting 00: 10 ms, 01: 100 ms, 10: 1 s, 11: Disruption determination disabled
8	Operation mode setting when SPI communication is disrupted (common to Ch1 and Ch2)	0	R/W	Operation mode setting when Ch1 (OUT1/2) & Ch2 (OUT3/4) SPI communication disruption is detected 0: Output (OUT1/2, OUT3/4) OFF (Hi-Z), 1: Continue operation immediately before disruption

Table 7.24. CONFIG2 (ADR[38:32]: 0x05)

Bit	NAME	INIT (initial value)	Command (R/W)	Description
31	-	0	R	-
30	-	0	R	-
29	-	0	R	-
28	-	0	R	-
27	-	0	R	-
26	-	0	R	-
25	-	0	R	-
24	-	0	R	-
23	-	0	R	-
22 21	Ch2 open load during non-operation detection time setting	0 0	R/W R/W	Detection time setting for Ch2 (OUT3/4) open load during non-operation 00: 100 µs, 01: 50 µs, 10: 500 µs, 11: -
20	Ch2 PWM duty-OFF interval low- or high-side regeneration setting	0	R/W	Low- or high-side regeneration setting during PWM duty-OFF interval on Ch2 (OUT3/4) side 0: Low-side regeneration, 1: High-side regeneration
19	-	0	R	-
18	Ch2 current limit threshold upper limit	0	R/W	Ch2 (OUT3/4) current limit threshold upper limit setting 0: 6.5 A, 1: 4.6 A
17	Ch2 current limit threshold lower limit	0	R/W	Ch2 (OUT3/4) current limit threshold lower limit setting 0: Upper limit - 0.25 A, 1: Upper limit - 0.5 A
16 15	Ch2 open load during operation detection threshold setting	0 0	R/W R/W	Detection threshold setting for Ch2 (OUT3/4) open load during operation 00: 200 mA, 01: 100 mA 10: 300 mA, 11: 200 mA
14 13 12	Ch2 SR mode SR2 SR1 SR0	0 0 0	R/W R/W R/W	Ch2 (OUT3/4) SR mode setting 000: Voltage SR Normal (Control OFF, 17.50 V/µs(design data)) 001: Voltage SR Slow1 (1.09 V/µs(design data)) 010: Voltage SR Slow2 (2.19V/µs(design data)) 011: Voltage SR Slow3 (4.38V/µs(design data)) 100: Voltage SR Slow4 (8.75V/µs(design data)) 101: Voltage SR Fast2 (21.88V/µs(design data)) 110: Voltage SR Fast1 (26.25V/µs(design data)) 111: Voltage SR Normal (Control OFF, 17.50 V/µs(design data))
11	Ch2 over-current detection mode (latched or automatic recovery)	0	R/W	Ch2 (OUT3/4) over-current detection mode setting 0: Over-current detection latch mode, 1: Automatic recovery mode
10 9	-	0 0	R R	-
8	-	0	R	-

Table 7.25. CONFIG3 (ADR[38:32]: 0x06)

Bit	NAME	INIT (initial value)	Command (R/W)	Description
31 30	Ch1 base frequency setting	0 0	R/W R/W	Ch1 (OUT1/2) base frequency setting; frequency division ratio setting for external input clock 00: 1/1 division, 01: 1/2 division, 10: 1/4 division, 11: 1/20 division
29	-	0	R	-
28	-	0	R	-
27	-	0	R	-
26	-	0	R	-
25	-	0	R	-
24	-	0	R	-
23	-	0	R	-
22	-	0	R	-
21	-	0	R	-
20	-	0	R	-
19	-	0	R	-
18 17 16 15 14 13 12 11 10 9 8	Ch1 ON delay time setting (counter value: 0 to 2047)	0 0 0 0 0 0 0 0 0 0 0	R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W	Ch1 (OUT1/2) ON delay time setting for motor drive with SPI control

Table 7.26. CONFIG4 (ADR[38:32]: 0x07)

Bit	NAME	INIT (initial value)	Command (R/W)	Description
31 30	Ch2 base frequency setting	0 0	R/W R/W	Ch2 (OUT3/4) base frequency setting; frequency division ratio setting for external input clock 00: 1/1 division, 01: 1/2 division 10: 1/4 division, 11: 1/20 division
29	-	0	R	-
28	-	0	R	-
27	-	0	R	-
26	-	0	R	-
25	-	0	R	-
24	-	0	R	-
23	-	0	R	-
22	-	0	R	-
21	-	0	R	-
20	-	0	R	-
19	-	0	R	-
18 17 16 15 14 13 12 11 10 9 8	Ch2 ON delay time setting (counter value: 0 to 2047)	0 0 0 0 0 0 0 0 0 0 0	R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W	Ch2 (OUT3/4) ON delay time setting for motor drive with SPI control

Table 7.27. CONFIG5 (ADR[38:32]: 0x08)

Bit	NAME	INIT (initial value)	Command (R/W)	Description
31 30	Ch1 motor operation setting (forward/reverse/brake/output OFF (Hi-Z))	0 0	R/W R/W	Ch1 (OUT1/2) motor operation setting 00: Output OFF (Hi-Z), 01: Forward, 10: Reverse, 11: Brake (low- or high-side is determined in combination with bit20 of CONFIG1)
29 28 27 26 25 24 23 22 21 20 19	Ch1 drive cycle period setting (counter value: 0 to 2047)	0 0 0 0 0 0 0 0 0 0 0	R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W	Ch1 (OUT1/2) drive cycle period setting for motor drive with SPI control Drive frequency fpwm is calculated as follows: fpwm = fdiv / (drive frequency setting register value + 1) fdiv: Base frequency = external input clock frequency * base frequency set value (frequency division ratio)
18 17 16 15 14 13 12 11 10 9 8	Ch1 duty-ON period setting (counter value: 0 to 2047)	0 0 0 0 0 0 0 0 0 0 0	R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W	Ch1 (OUT1/2) PWM duty-ON period setting for motor drive with SPI control PWM_Duty = duty-ON period setting (counter value) / (drive frequency setting (counter value) + 1) Set the registers so that duty-ON period setting register value ≤ drive frequency setting register value. 1) If duty-ON period setting register value = drive frequency setting register value, PWM duty-ON interval is 100%. 2) If duty-ON period setting register value > drive frequency setting register value, PWM duty-ON interval is still 100%. 3) If duty-ON period setting register value = 0, PWM duty-ON interval is 0%.

Table 7.28. CONFIG6 (ADR[38:32]: 0x09)

Bit	NAME	INIT (initial value)	Command (R/W)	Description
31 30	Ch2 motor operation setting (forward/reverse/brake/output OFF (Hi-Z))	0 0	R/W R/W	Ch2 (OUT3/4) motor operation setting 00: Output OFF (Hi-Z), 01: Forward, 10: Reverse, 11: Brake (low- or high-side is determined in combination with bit20 of CONFIG2)
29 28 27 26 25 24 23 22 21 20 19	Ch2 drive cycle period setting (counter value: 0 to 2047)	0 0 0 0 0 0 0 0 0 0 0	R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W	Ch2 (OUT3/4) drive cycle period setting for motor drive with SPI control Drive frequency fpwm is calculated as follows: fpwm = fdiv / (drive frequency setting register value + 1) fdiv: Base frequency = external input clock frequency * base frequency set value (frequency division ratio)
18 17 16 15 14 13 12 11 10 9 8	Duty-ON period setting (counter value: 0 to 2047)	0 0 0 0 0 0 0 0 0 0 0	R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W	Ch2 (OUT3/4) PWM duty-ON period setting for motor drive with SPI control PWM_Duty = duty-ON period setting (counter value) / (drive frequency setting (counter value) + 1) Set the registers so that duty-ON period setting register value ≤ drive frequency setting register value. 1) If duty-ON period setting register value = drive frequency setting register value, PWM duty-ON interval is 100%. 2) If duty-ON period setting register value > drive frequency setting register value, PWM duty-ON interval is still 100%. 3) If duty-ON period setting register value = 0, PWM duty-ON interval is 0%.

Table 7.29. CONFIG7 (ADR[38:32]: 0x0A)

Bit	NAME	INIT (initial value)	Command (R/W)	Description
31	Output OFF cancellation when Ch1 over-current (short-circuit to power supply or ground) is detected	0	W	Command to cancel output OFF (latched) when Ch1 (OUT1/2) over-current (short-circuit to power supply or ground) is detected 0: Output OFF is not canceled, 1: Output OFF is canceled (one-shot pulse)
30	Ch1 open-load detection during non-operation	0	W	Command to execute Ch1 (OUT1/2) open-load detection during non-operation 0: Detection is not executed, 1: Detection is executed (one-shot pulse)
29	Ch1 CONFIG3/CONFIG5 setting update	0	W	Command to update Ch1 (OUT1/2) CONFIG3/CONFIG5 setting 0: A WRITE attempt updates CONFIG3/CONFIG5 registers, and the PWM operation reflects it 1: CONFIG3/CONFIG5 registers under WRITE attempt are retained; the next "0" WRITE in this bit updates the registers, and the PWM operation reflects it. Note that when CONFIG7 is enable CONFIG3 and CONFIG5 registers need to be set. (refer to below timing chart)
28	Output OFF cancellation when Ch2 over-current (short-circuit to power supply or ground) is detected	0	W	Command to cancel output OFF (latched) when Ch2 (OUT3/4) over-current (short-circuit to power supply or ground) is detected 0: Output OFF is not canceled, 1: Output OFF is canceled (one-shot pulse)
27	Ch2 open-load detection during non-operation	0	W	Command to execute Ch2 (OUT3/4) open-load detection during non-operation 0: Detection is not executed, 1: Detection is executed (one-shot pulse)
26	Ch2 CONFIG4/CONFIG6 setting update	0	W	Command to update Ch2 (OUT3/4) CONFIG4/CONFIG6 setting 0: A WRITE attempt updates CONFIG4/CONFIG6 registers, and the PWM operation reflects it 1: CONFIG4/CONFIG6 registers under WRITE attempt are retained; the next "0" WRITE in this bit updates the registers, and the PWM operation reflects it Note that when CONFIG7 is enable CONFIG4 and CONFIG6 registers need to be set. (refer to below timing chart)
25	Output OFF cancellation when OUT1 over-current (short-circuit to power supply or ground) is detected (effective only in Half Mode)	0	W	Command to cancel output OFF (latched) when OUT1 over-current (short-circuit to power supply or ground) is detected during Half Mode 0: Output OFF is not canceled, 1: Output OFF is canceled (one-shot pulse)
24	Output OFF cancellation when OUT2 over-current (short-circuit to power supply or ground) is detected (effective only in Half Mode)	0	W	Command to cancel output OFF (latched) when OUT2 over-current (short-circuit to power supply or ground) is detected during Half Mode 0: Output OFF is not canceled, 1: Output OFF is canceled (one-shot pulse)
23	Output OFF cancellation when OUT3 over-current (short-circuit to power supply or ground) is detected (effective only in Half Mode)	0	W	Command to cancel output OFF (latched) when OUT3 over-current (short-circuit to power supply or ground) is detected during Half Mode 0: Output OFF is not canceled, 1: Output OFF is canceled (one-shot pulse)
22	Output OFF cancellation when OUT4 over-current (short-circuit to power supply or ground) is detected (effective only in Half Mode)	0	W	Command to cancel output OFF (latched) when OUT4 over-current (short-circuit to power supply or ground) is detected during Half Mode 0: Output OFF is not canceled, 1: Output OFF is canceled (one-shot pulse)
21	-	0	R	-
20	-	0	R	-
19	-	0	R	-
18	-	0	R	-
17	-	0	R	-
16	-	0	R	-
15	-	0	R	-
14	-	0	R	-
13	-	0	R	-
12	-	0	R	-
11	-	0	R	-
10	-	0	R	-
9	-	0	R	-
8	-	0	R	-

7.12.7.2. SPI setting register (effective/ineffective) in Combined-Channel Mode (LARGE Mode)

In Combined-Channel Mode (LARGE Mode), the Ch1 settings of SPI setting registers are effective for controlling the outputs (OUT1/2 and OUT3/4). The following table shows the details:

	NAME	Ch	Motor drive using SPI communication ISEL1 = H (Enabled), ISEL2 = Don't care (disabled)	Direct PWM motor drive ISEL1 = L (Enabled), ISEL2 = Don't care (Disabled)
Analog parameter setting	CONFIG1	Ch1	Enabled	Enabled
Analog parameter setting	CONFIG2	Ch2	Disabled	Disabled
Logic parameter setting	CONFIG3	Ch1	Enabled	Disabled
Logic parameter setting	CONFIG4	Ch2	Disabled	Disabled
Motor operation instruction	CONFIG5	Ch1	Enabled	Disabled
Motor operation instruction	CONFIG6	Ch2	Disabled	Disabled
Command execution setting	CONFIG7	Ch1	Enabled	Enabled
Command execution setting	CONFIG7	Ch2	Disabled	Disabled

Note: In Combined-Channel Mode (LARGE Mode), a WRITE operation of SPI communication can write a Ch2 SPI setting normally, but the Ch2 setting is disabled for IC operation (output control).

Note: In Combined-Channel Mode (LARGE Mode), only ISEL1 selects a drive mode (SPI drive or direct PWM drive), and ISEL2 is disabled.

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7.13. Power supply monitoring function

This IC has a power supply monitoring function.

7.13.1. VBAT under-voltage detection circuit (see Figure 7.35 and Figure 7.36)

・When VBAT voltage decreases below the under-voltage detection threshold, OUT1/2 and OUT3/4 turns OFF (Hi-Z state).
The IC has a filter (TVBAT_uv: approximately 10.0 μs (typ.)) to prevent chattering.
Even while the H-bridge circuit is OFF (Hi-Z) due to VBAT under-voltage detection, logic circuits can operate if the VCC voltage is above the VCC under-voltage POR voltage.

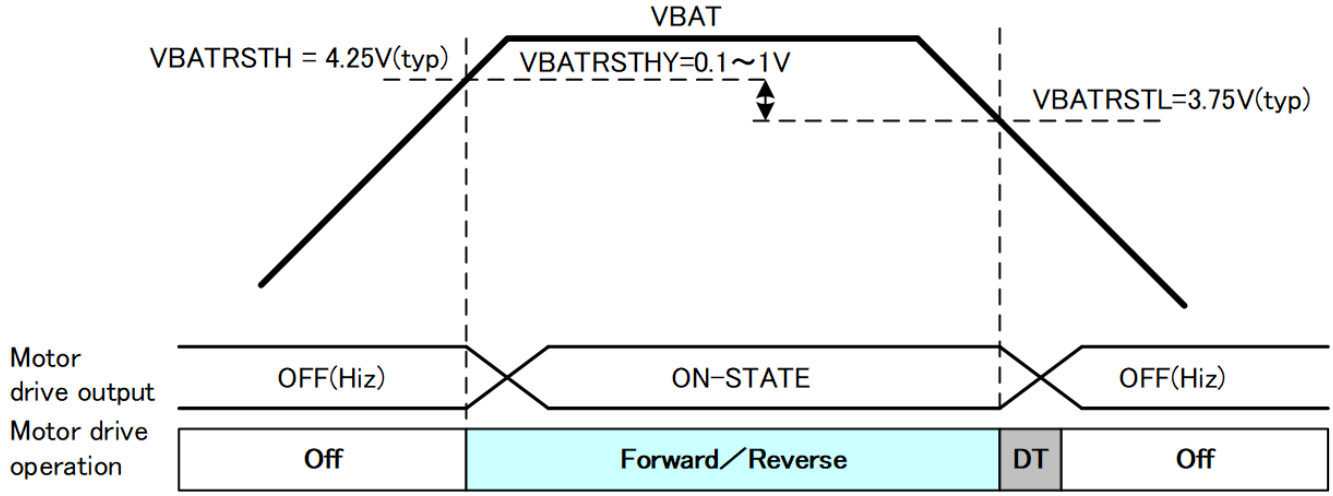


Figure 7.35 VBAT under-voltage detection threshold characteristics

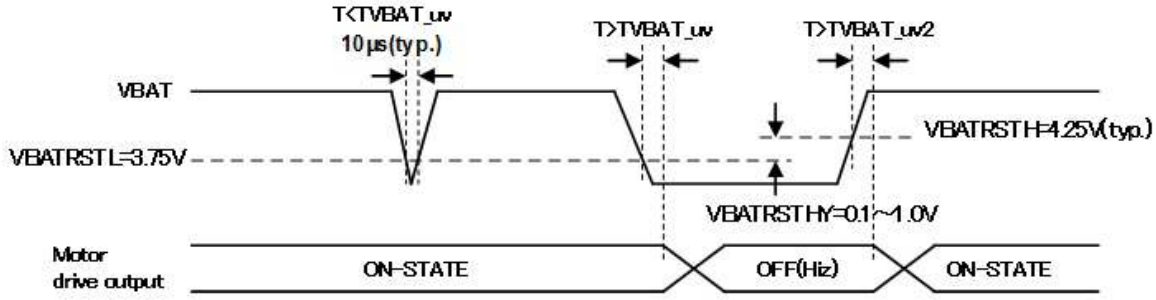


Figure 7.36 VBAT under-voltage detection timing chart 1

・The detection signal of the over-temperature detection circuit retains its state immediately before VBAT under-voltage is detected (TSD detected or TSD undetected) when VBAT falls below the under-voltage detection voltage. Since the detection signal of the over-temperature detection circuit is retained while VBAT under-voltage is detected, the detection signal of the over-temperature detection circuit does not change (detected→undetected or undetected→detected) until the VBAT under-voltage detection is canceled.

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.13.2. VCC under-voltage detection circuit (see Figure 7.37 to Figure 7.39)

When VCC voltage decreases below the under-voltage detection threshold, OUT1/2 and OUT3/4 turns OFF (Hi-Z state). The IC has a filter (2.5 ms (typ.)) to prevent chattering.
The abnormality bit of SPI latches a flag showing that VCC under-voltage is detected.
The logic circuit is reset if VCC voltage is below VCCRHL (3.07 V (typ.)). Moreover, the IC has a filter (13.0 μs (typ.)) to prevent chattering.

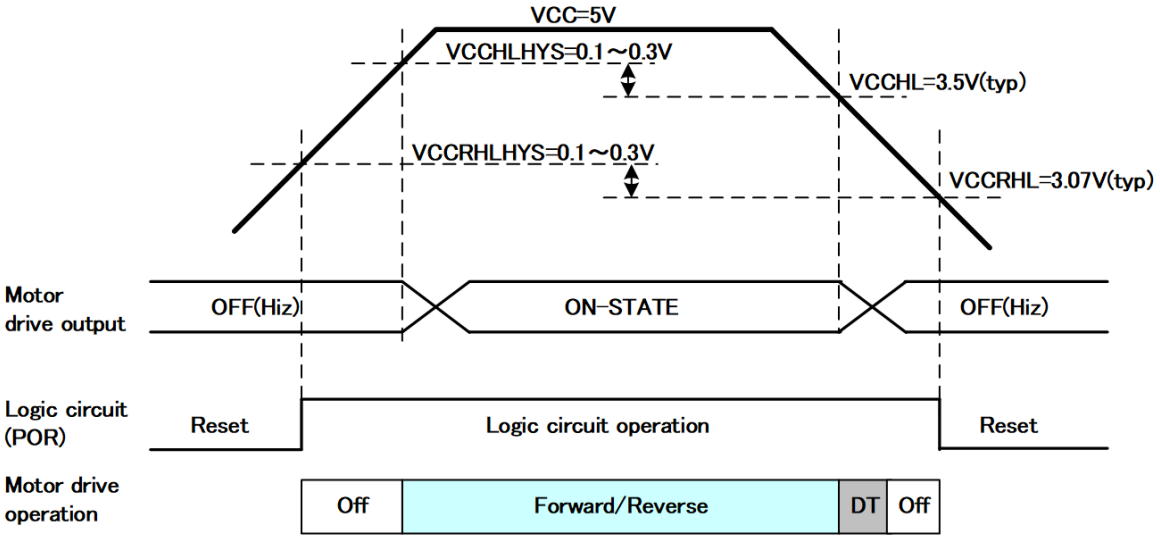


Figure 7.37 VCC under-voltage detection and POR threshold characteristics

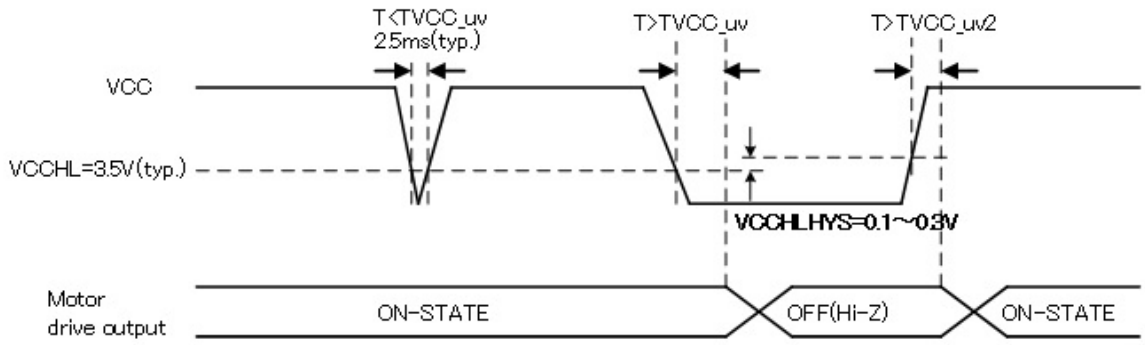


Figure 7.38 VCC under-voltage detection timing chart 1

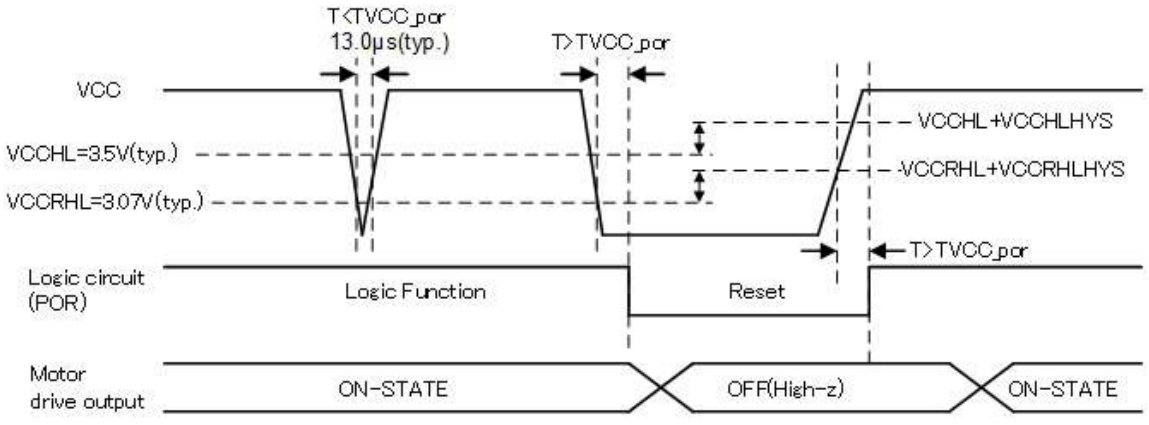


Figure 7.39 VCC under-voltage POR timing chart 1

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.14. Over-temperature detection circuit (Figure 7.40 and Figure 7.41)

(1) This IC has an over-temperature detection circuit. At a temperature above TSD, the IC turns the motor drive output OUT1/2 and OUT3/4 to Hi-Z to protect the IC.
(2) Simultaneously, the DIAG pin outputs L.
(3) When the temperature decreases below to the TSD – TSDhys by operation of over-temperature detection circuit, normal operation automatically resumes.
(The output automatically resumes from Hi-Z when the temperature is below TSD - TSDhys.)
(4) The DIAG pin output automatically resumes from L output when the temperature is below TSD - TSDhys.

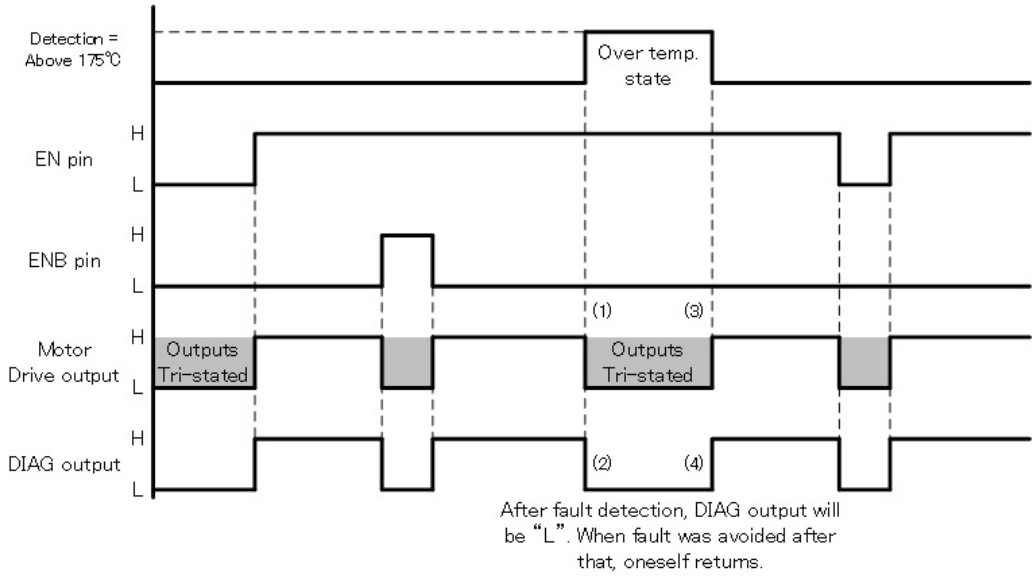


Figure 7.40 Over-temperature detection timing chart

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

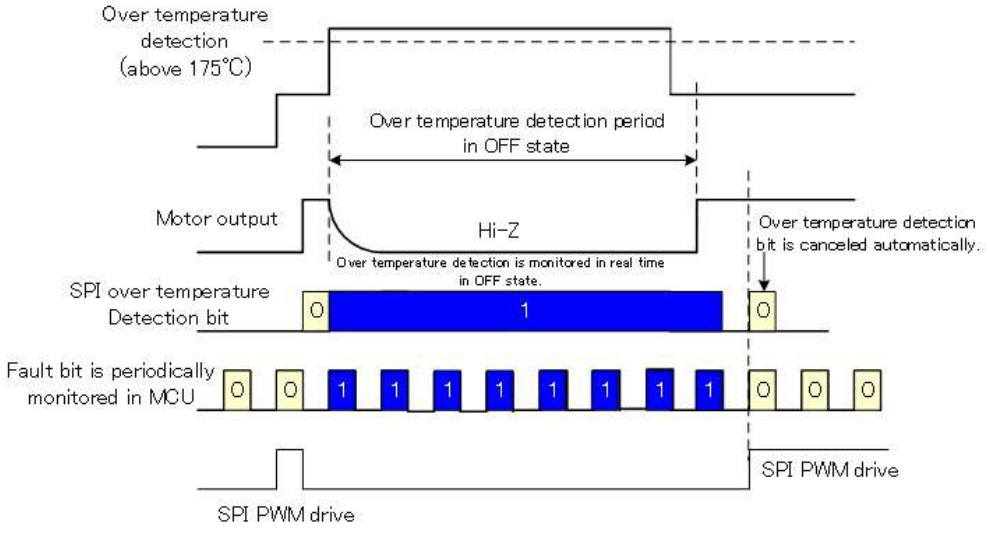


Figure 7.41 Over-temperature detection detailed timing chart

- The detection signal of the over-temperature detection circuit retains its state even when VBAT falls below the under-voltage detection voltage.
- The detection signal of the over-temperature detection circuit is forced into an undetected state during initial diagnosis.

- When TSD arises, PWM input is disabled.

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

Note: According to the absolute maximum ratings of this product, product integrity is guaranteed for storage temperatures below 150°C. If the IC is stored or used in conditions exceeding this temperature, subsequent normal operations are not guaranteed. Moreover, it may cause smoke and/or fire. Do not under any circumstances store or use this IC in conditions exceeding this temperature.

Although this IC incorporates an over-temperature detection function as shown above, the function does not maintain the temperature of the IC below the over-temperature detection shutdown temperature (TSD), and works outside the guaranteed operating range. Treat this function as an auxiliary function.
(This function is not individually tested in an actual high-temperature environment. Rather, a test function simulates the detection circuit operation.)

7.15. Circuit to detect over-current caused by short-circuit to power supply or ground, or short-circuited load (Figure 7.42, Figure 7., and Figure 7.)

This IC incorporates over-current detection circuits for high- and low-side drivers of the motor drive outputs.
When a motor drive output pin is short-circuited to power supply or ground, or a load is short circuited, if the current exceeds the over-current threshold (11 A (typ.)), the over-current detection circuit operates to turn the motor drive output OFF. All Hi- and Lo-side drivers of OUT1/2 and OUT3/4 pins turn OFF. Simultaneously, the DIAG pin outputs L.
The over-current detection function has two modes: one mode turns the output OFF and the other mode recovers automatically after over-current is detected. Use SPI settings to switch between modes.
Note that in Half-Bridge Mode, the automatic recovery mode is disabled. Only a half-bridge output where over-current occurs is latched to OFF.

SPI settings: Over-current detection mode CONFIG1/2 DATA[11] = 0 or 1 (latch or automatic recovery mode)

When one of the over-current detection circuits (Ch1: 4 circuits, Ch2: 4 circuits) detects over-current and enters an over-current abnormality detection state, over-current detection signals from other circuits are not accepted until the abnormality detection state is canceled.
Consequently, an abnormality flag is only set for the over-current detection circuit that detects over-current (short-circuit to power supply or ground) first.

7.15.1. SPI settings: Over-current detection in automatic recovery mode (see Figure 7.4242 and Figure 7.43)

This function is disabled in Half-Bridge Mode. Therefore, an over-current detection mode setting to automatic recovery (SPI setting: CONFIG1/2 DATA[11] = 1) is ignored.

・When motor drive output is short-circuited to power supply or ground, the output turns OFF when a current above the over-current threshold (Iovc) flows for tBLANK2 = 1 μs (Tovc). This prevents incorrect operation caused by factors such as noise.

After 300 ms (typ.), the IC attempts automatic recovery, which is repeated until the external MCU issues an instruction.
If the output current is in the normal range at an automatic recovery, the OUT1/2 and OUT3/4 outputs resume normal operation.

・An instruction from the MCU turns the output OFF.
The MCU sends EN/ENB signals to turn the output OFF.

・Another instruction from the MCU cancels the OFF state and restarts various functions.

One pulse of EN fall or ENB rise restarts the functions.

・When tBLANK2 is enabled, tBLANK1 is ignored and tBLANK2 is prioritized.

- The detection signal of the over-current detection circuit is forced into an undetected state during initial/restarted diagnosis.

SPI settings: Over-current detection in automatic recovery mode 1 (example: low-side)

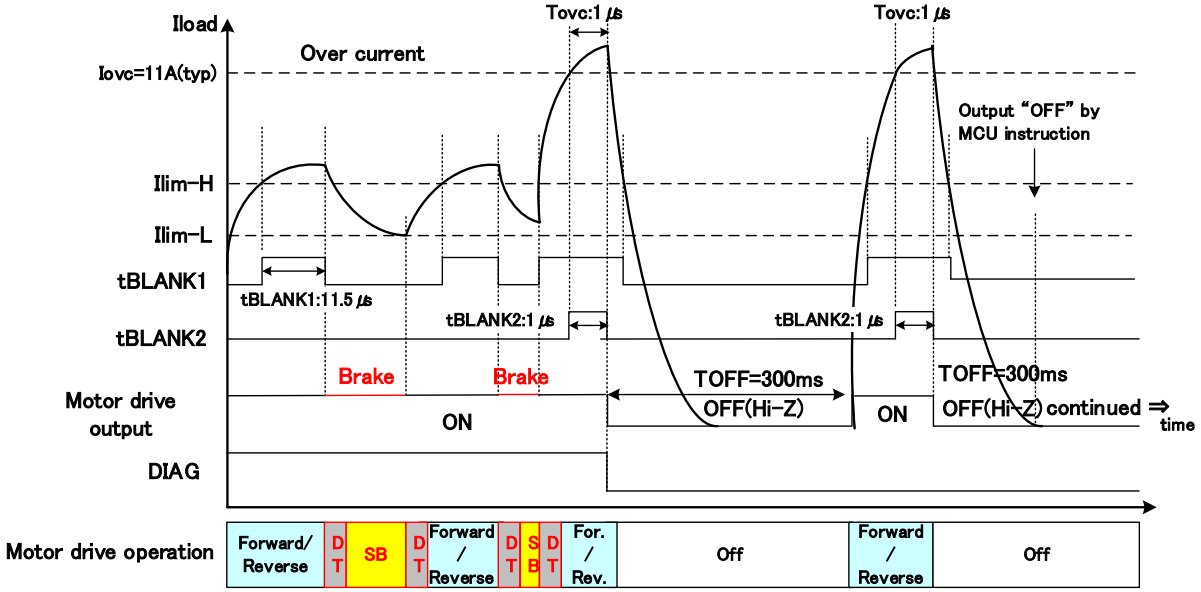


Figure 7.42 Over-current detection operation for short-circuit to power supply or ground, and short-circuited load: timing chart 1

SPI settings: Over-current detection in automatic recovery mode 2 (example: low-side)

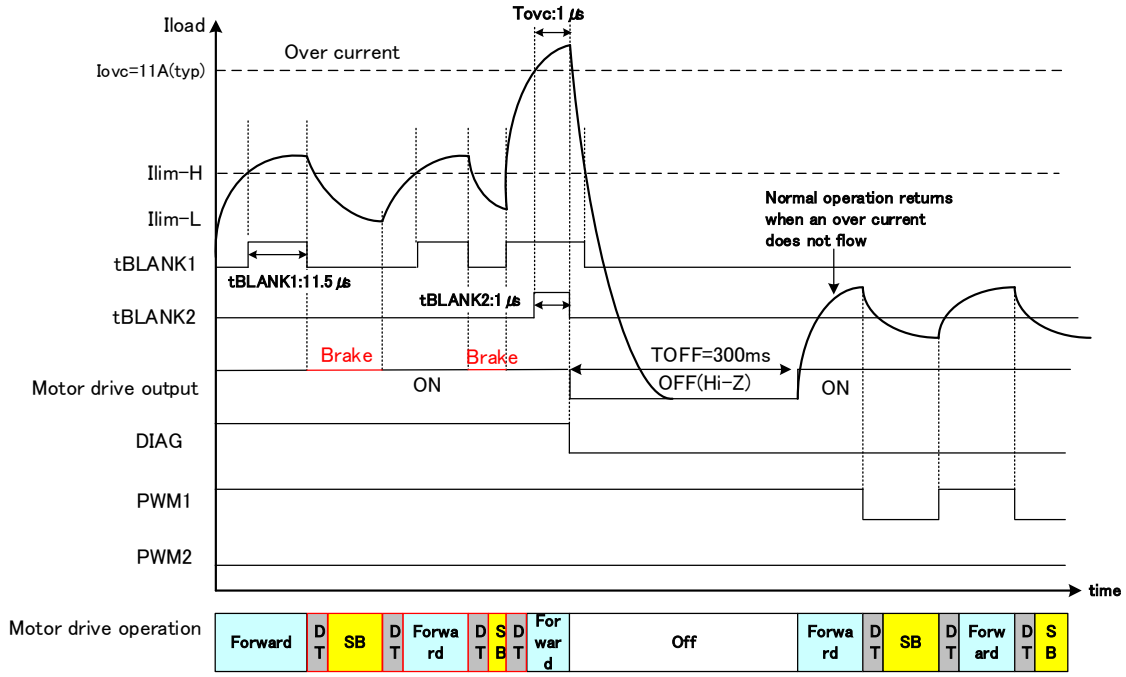
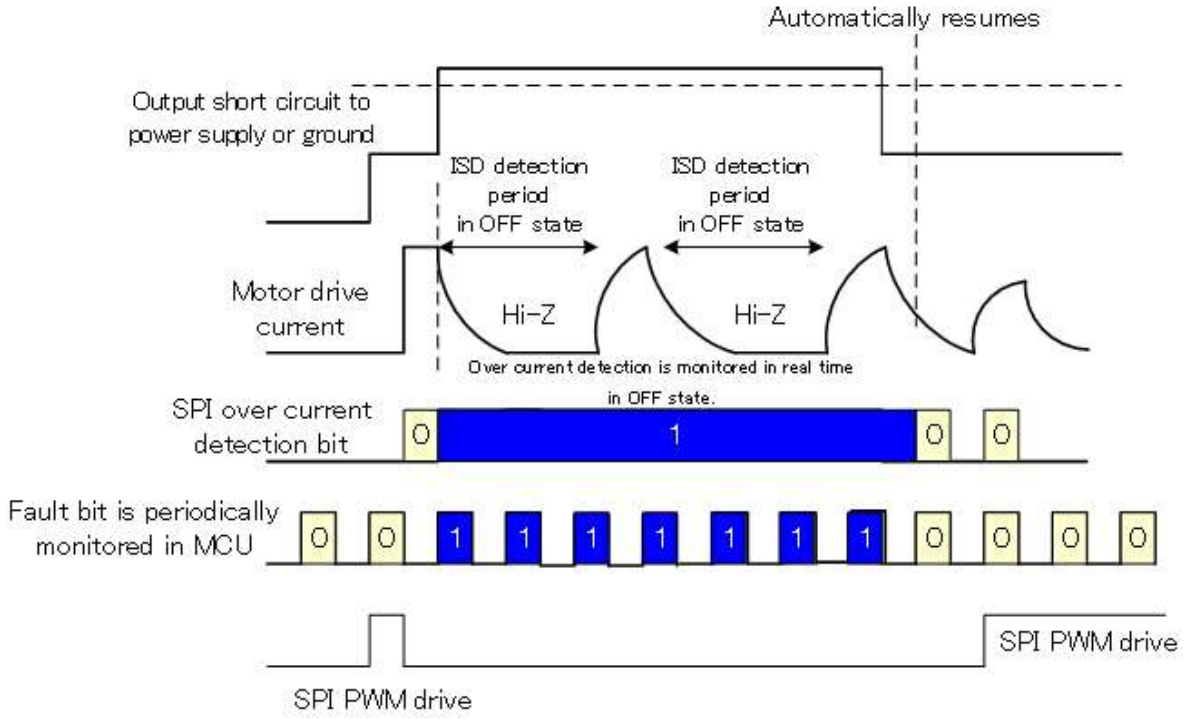


Figure 7.43 Over-current detection operation for short-circuit to power supply or ground, and short-circuited load: timing chart 2

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

・Automatic recovery mode



Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.15.2. SPI settings: Over-current detection in latch mode (see Figure 7.44)

- When a motor drive output is short-circuited to power supply or ground, the output automatically turns OFF if a current above the over-current threshold (Iovc) is detected and the current above the threshold still flows after tBALNK2 = 1 µs (which prevents incorrect operation caused by factors such as noise).

- An instruction from the MCU cancels the OFF state and restarts various functions.
  One pulse of EN fall or ENB rise restarts the functions.

- If tBLANK2 is enabled, tBLANK1 is canceled.

SPI settings: Over-current detection in latch mode (example: low-side)

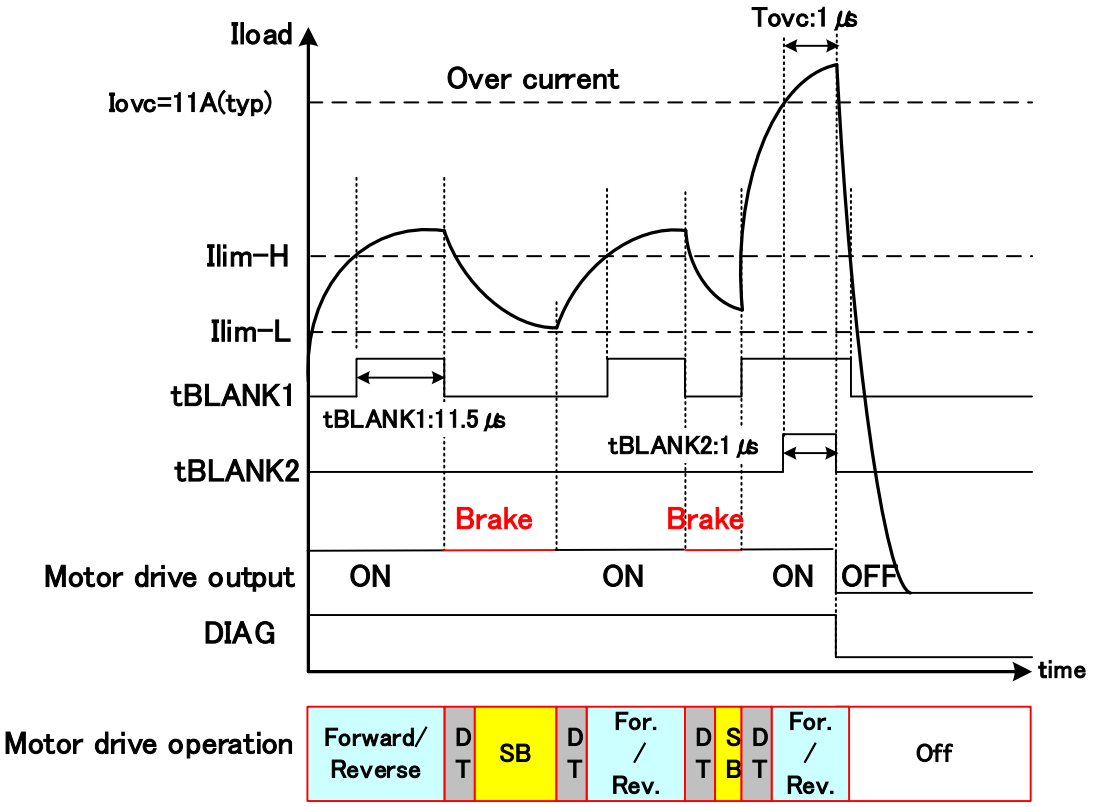
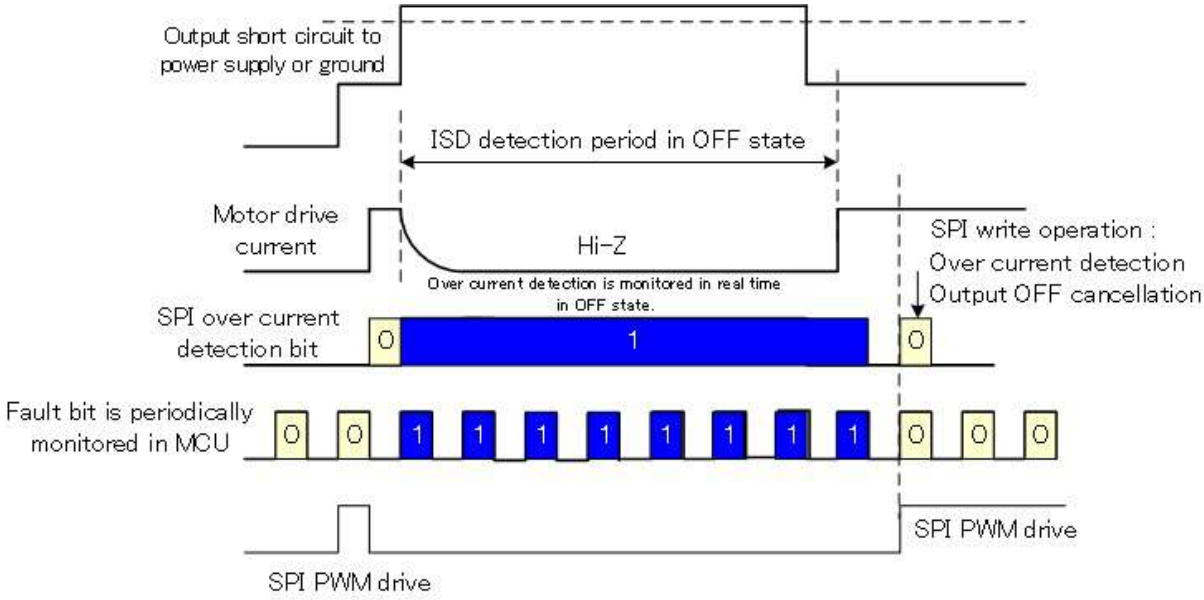


Figure 7.44 Over-current detection operation for short-circuit to power supply or ground, and short-circuited load: timing chart 3

・SPI communication cancels output OFF (latched) for recovery.



Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

7.15.3. Recovery from OFF state: timing chart (when short-circuit to power supply or ground is detected)

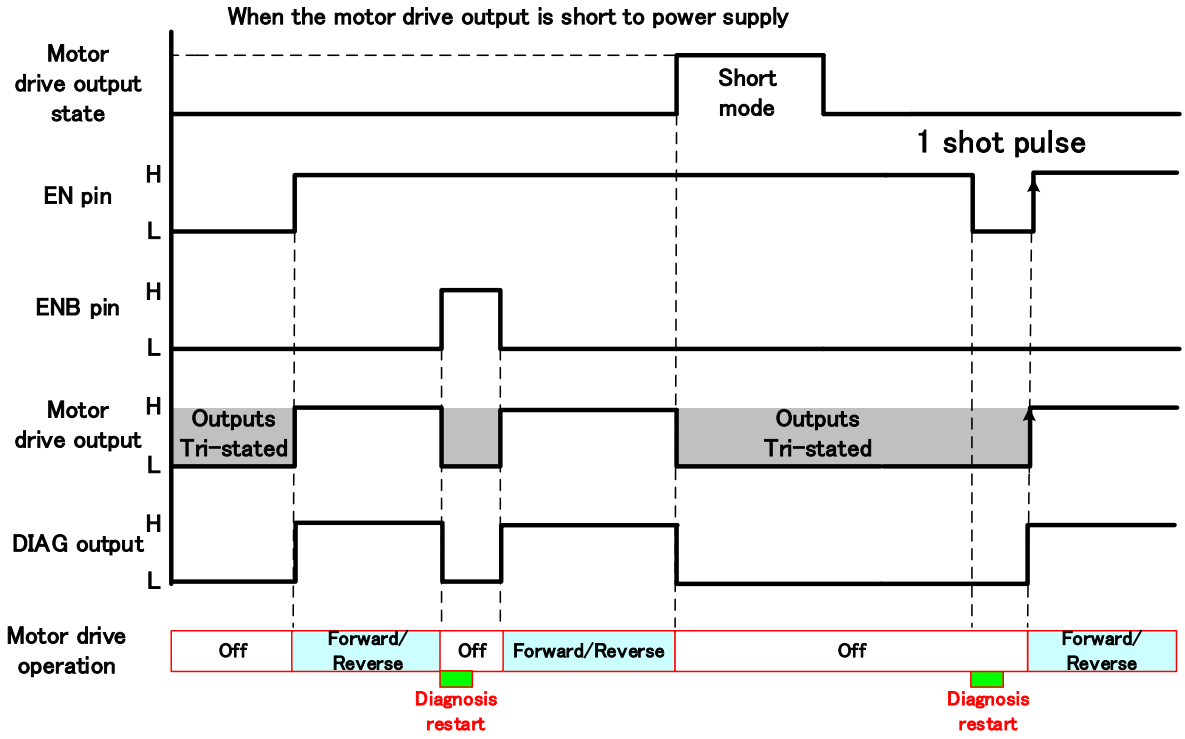


Figure 7.45 Recovery from OFF state for short-circuit to power supply or ground, and short-circuited load: timing chart

Either the EN pin rising edge or the ENB pin falling edge clears the latched L output from the DIAG pin.

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

Note: This detection circuit helps prevent abnormal states such as short-circuited output, but it will not necessarily prevent IC breakdown. Therefore, when an output pin is short-circuited to another output pin, power supply, or ground, the IC may break down. As such, design the output, VBAT, VCC, and GND lines carefully.

7.16. Initial diagnosis

The IC has an initial diagnosis function to check the operation of comparators in advance for power-supply monitoring, over-temperature detection, over-current detection, and open-load detection during operation/non-operation.

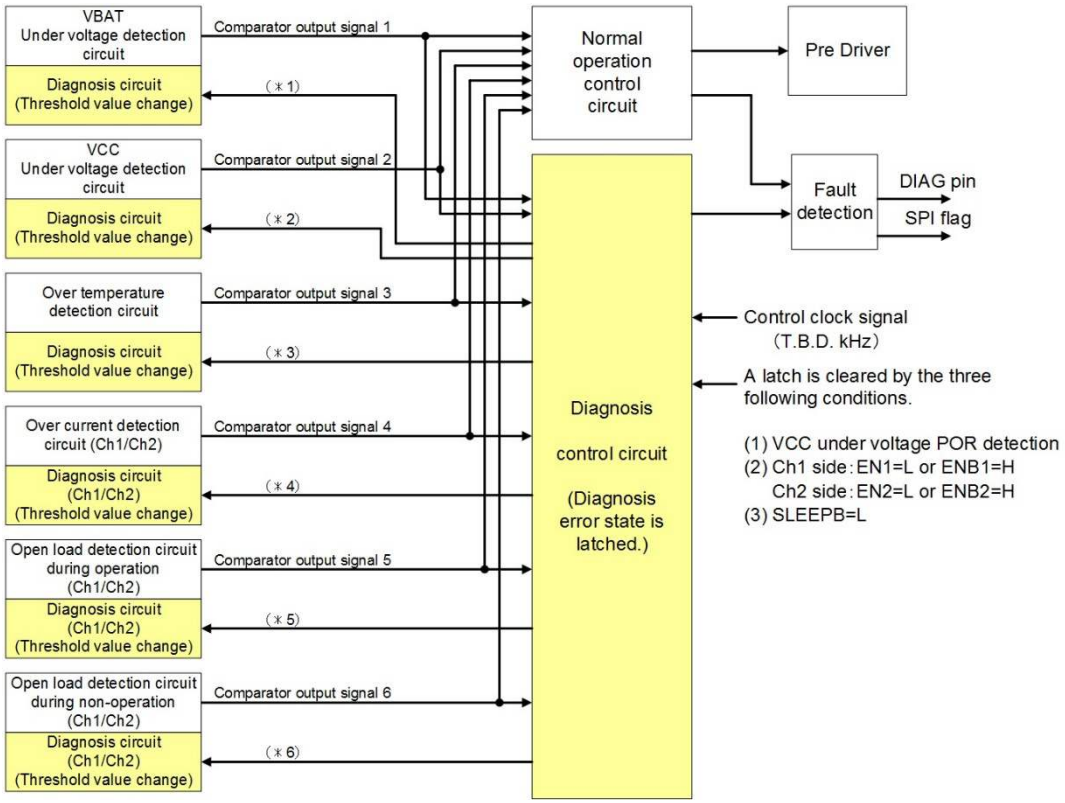


Figure 7.46 Initial diagnosis block diagram

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

*1 to 6: Initial diagnosis/ normal operation threshold value switching signal
H: Threshold value for initial diagnosis: For normal voltage and current, VBAT, VCC, over-temperature, over-current, and open load during operation/non-operation are "detected".
L: Threshold value for normal operation: For normal voltage and current, VBAT, VCC, over-temperature, over-current, and open load during operation/non-operation are "undetected".

◆Table7.30. Operation summary of initial diagnosis

Condition	Each detector	Start-after POR formation conditions	The state where it does not detect Test 1 (Normal threshold)	The state where it does not detect Test 2 (A threshold is changed)	The state where it does not detect Test 3 (Normal threshold)	Diagnostic result	Under diagnostic operation		After termination of initial diagnosis		memo
							DIAG1, DIAG2 PIN	OUT1/2, OUT3/4 PIN	DIAG1, DIAG2 PIN	OUT1/2, OUT3/4 PIN	
1	CP voltage starting	○	–	–	–	Normal	L	Hiz	H	Output Function	
	VBAT under voltage	○	○	○	○						
	VCC under voltage	○	○	○	○						
	Over temperature	○	○	○	○						
	Over current	○	○	○	○						
	Open load during operation	○	○	○	○						
	Open load during non-operation	○	○	○	○						
2	CP voltage starting	○	–	–	–	Fault	L	Hiz	L	Output Function	
	VBAT under voltage	○	In the case of NG, it is also at any 1 condition	○	○						
	VCC under voltage	○		○	○						
	Over temperature	○		○	○						
	Over current	○		○	○						
	Open load during operation	○		○	○						
	Open load during non-operation	○		○	○						
3	CP voltage starting	○	–	–	–	Fault	L	Hiz	L	Output Function	
	VBAT under voltage	○	○	In the case of NG, it is also at any 1 condition	○						
	VCC under voltage	○	○		○						
	Over temperature	○	○		○						
	Over current	○	○		○						
	Open load during operation	○	○		○						
	Open load during non-operation	○	○		○						
4	CP voltage starting	○	–	–	–	Fault	L	Hiz	L	Output Function	
	VBAT under voltage	○	○	○	In the case of NG, it is also at any 1 condition						
	VCC under voltage	○	○	○							
	Over temperature	○	○	○							
	Over current	○	○	○							
	Open load during operation	○	○	○							
	Open load during non-operation	○	○	○							
5	CP voltage starting	When at least one condition continues the state where it detects	–	–	–	Fault	L	Hiz	L	Hiz	Initial diagnosis does not start.
	VBAT under voltage		–	–	–						
	VCC under voltage		–	–	–						
	Over temperature		–	–	–						
	Over current		–	–	–						
	Open load during operation		–	–	–						
	Open load during non-operation		–	–	–						

Note: The CP voltage-rise detection circuit is used as a condition for startup but is not diagnosed.

Note: In case 5, the IC keeps waiting until six detection circuits output normal values (undetected state). When they output normal values, initial diagnosis starts and lasts for 57 µs (if 32 µs have elapsed after POR is canceled).

Note: In Half Mode, open-load detection circuits during operation/non-operation are not diagnosed.

Note: When VBAT voltage is in the range of VBAT under-voltage detecting voltage - VBAT under-voltage cancellation voltage, initial diagnosis is NG. Since DAIG output = L and initial-diagnosis NG (fault flag: "1") of STATUS1 register of SPI is output, set the VBAT voltage as the voltage more than VBAT under-voltage cancellation voltage.

Note: When VCC voltage is in the range of VCC under-voltage detecting voltage and VCC under-voltage cancellation voltage, initial diagnosis results in No-Good with DAIG output = L and initial-diagnosis NG (fault flag: "1") of STATUS1 register of SPI is output. Therefore, set the VCC voltage as the voltage more than VCC under-voltage cancellation voltage.

Note: "-" indicates to be not tested (not diagnosed) .

◆Table7.31. Operation summary of restarted diagnosis

Condition	Each detector	Initial diagnositic restart formation conditions	The state where it does not detect Test 1 (Normal threshold)	The state where it does not detect Test 2 (A threshold is changed)	The state where it does not detect Test 3 (Normal threshold)	Diagnostic result	Under diagnostic operation		After termination of a restart		memo
							DIAG1, DIAG2 PIN	OUT1/2, OUT3/4 PIN	DIAG1, DIAG2 PIN	OUT1/2, OUT3/4 PIN	
1	CP voltage starting	○	–	–	–	Normal	L	Hiz	H	Output Function	
	VBAT under voltage	○	○	○	○						
	VCC under voltage	○	○	○	○						
	Over temperature	○	○	○	○						
	Over current	○	○	○	○						
	Open load during operation	○	○	○	○						
	Open load during non-operation	○	○	○	○						
2	CP voltage starting	○	–	–	–	Fault	L	Hiz	L	Output Function	
	VBAT under voltage	○	–	–	–						
	VCC under voltage	○	–	–	–						
	Over temperature	○	–	–	–						
	Over current	○	In the case of NG, it is also at any 1 condition	○	○						
	Open load during operation	○		○	○						
	Open load during non-operation	○		○	○						
3	CP voltage starting	○	–	–	–	Fault	L	Hiz	L	Output Function	
	VBAT under voltage	○	–	–	–						
	VCC under voltage	○	–	–	–						
	Over temperature	○	–	–	–						
	Over current	○	○	In the case of NG, it is also at any 1 condition	○						
	Open load during operation	○	○		○						
	Open load during non-operation	○	○		○						
4	CP voltage starting	○	–	–	–	Fault	L	Hiz	L	Output Function	
	VBAT under voltage	○	–	–	–						
	VCC under voltage	○	–	–	–						
	Over temperature	○	–	–	–						
	Over current	○	○	○	In the case of NG, it is also at any 1 condition						
	Open load during operation	○	○	○							
	Open load during non-operation	○	○	○							
5	CP voltage starting	When at least one condition continues the state where it detects	–	–	–	Fault	L	Hiz	L	Hiz	Diagnosis does not restart.
	VBAT under voltage		–	–	–						
	VCC under voltage		–	–	–						
	Over temperature		–	–	–						
	Over current		–	–	–						
	Open load during operation		–	–	–						
	Open load during non-operation		–	–	–						

Note: The CP voltage-rise detection circuit is used as a condition for restart but is not diagnosed.
Note: In case 5, the IC keeps waiting until six detection circuits output normal values (undetected state). When they output normal values, restarted diagnosis starts and lasts for 57 μs (if 32 μs have elapsed after EN/ENB are disabled).
Note: "-" indicates to be not tested (not diagnosed).
Note: The diagnosis does not work if VCC is below the under-voltage POR detection voltage.
Note: In Half Mode, open-load detection circuits during operation/non-operation are not diagnosed.
Note:When the EN or ENB signal sets a Disable state, diagnosis restarts.

8. Absolute maximum ratings

Table 8.1. Absolute maximum ratings

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applicable pin	Condition	Rating	Unit
Power supply voltage 1	VBAT	VBAT	DC	-0.3 to +28.0	V
Power supply voltage 2	VBAT	VBAT	Transient: 0.5 s	-0.3 to +40.0 (*5)	V
Power supply voltage 3	VCC VDD VDDIO	VCC VDD VDDIO	DC (*3)	-0.3 to +6.0 (*6)	V
Input voltage 1	VIN	PWM1, PWM2, PWM3, PWM4, EN1, ENB1, EN2, ENB2, ISEL1, ISEL2, SDI, NCS, SCLK, PWM_CLK, SLEEPB	DC	-0.3 to VCC, VDD, VDDIO+VF and VCC, VDD, VDDIO+VF ≤ +6.0 (*6)	V
Input voltage 2	VIN	OSEL1, OSEL2	DC	-0.3 to VCC, VDD, VDDIO+VF and VCC, VDD, VDDIO+VF ≤ +6.0 (*6)	V
Output voltage 1	VOUT	DIAG1, DIAG2	DC	-0.3 to +6.0 (*6)	V
Output voltage 2	VOUT	CM1, CM2	DC	-0.3 to VCC	V
Output voltage 3	VOUT	SDO	DC	-0.3 to VCC, VDD, VDDIO+VF and VCC, VDD, VDDIO+VF ≤ +6.0 (*6)	V
Output voltage 4	VOUT	OUT1, OUT2, OUT3, OUT4	DC (*4)	-VF to VBAT+VF and VBAT+VF ≤ +40.0 (*5)	V
Output voltage 5	VOUT	OUT1, OUT2, OUT3, OUT4	DC, VBAT-OUT1/2, VBAT-OUT3/4 (*4)	-VF to +40.0	V
Output current 1	IOUT	OUT1, OUT2, OUT3, OUT4	(*2)	Over-current detection value	A
Output current 2	IOUT	DIAG1, DIAG2	DC	+2.5	mA
Output current 3	IOUT	CM1, CM2	DC	-25.0	mA
Output current 4	IOUT	SDO	DC	3.0	mA
Storage temperature	Tstg	-	-	-55 to +150	°C
Lead temperature and time	Tsol	-	Manual soldering	260 (10 s)	
Power dissipation	PD	-	-	6.07 (TB9053) 5.18 (TB9054)	W

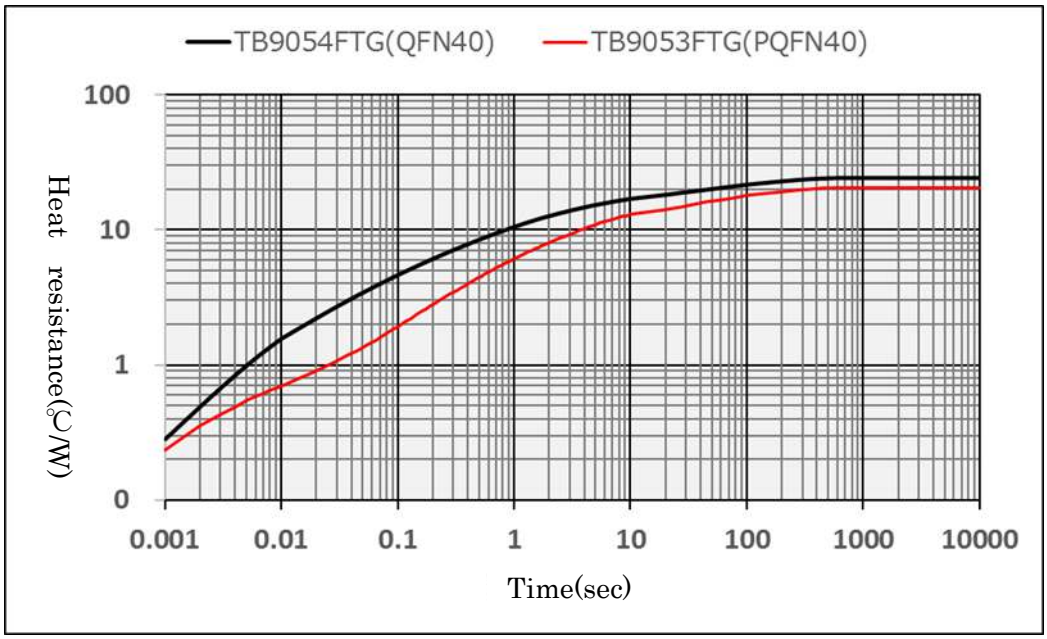
Note: Sink current of IC is indicated as positive"+" and source current as negative "-".

Absolute maximum ratings:

The absolute maximum ratings are a set of ratings that must not be exceeded even momentarily. Exceeding the rating(s) may cause IC breakdown, deterioration, or damage, and may also damage other devices. Regardless of the operating conditions, design your system so that the absolute maximum ratings are never exceeded. Use the IC within the specified operating range.

*1: Do not exceed the absolute maximum ratings, including voltage caused by counter electromotive force.
*2: When using the IC with continuous output current, carefully review and evaluate your board's thermal design and ensure that the junction temperature is less than 150°C.
*3: 5V applied for VCC should be used the power supply generated on ECU board to prevend the IC from surges through the connetor for ECU.
*4: The assumed VF value is the voltage generated by regeneration current flowing through the body diode of DMOS output after the load is short-circuited and the output turns OFF.
*5: The voltage difference between PGND and VBAT must be within 40 V.
*6: The voltage difference between AGND and VCC must be within 6 V.

8.1. Thermal resistance information



To be described based on the thermal resistance evaluation results of actual package samples.

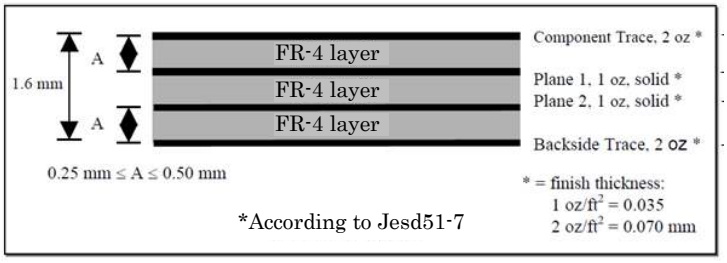
Figure 8.1. Junction to ambient transient thermal resistance

<Test condition>

- Board size : 114.3mm x 76.2mm x 1.6mm (JDEC standard : Jesd51-)
- Layer : Multi-Layer (Cu 4 layers)
- Cu layer thickness : 35 μ m (1/4 layer), 70 μ m (2/3 layer)
- Cu layer area size : 74 x 74mm2
- Number of Cu Via : 16 (4mm x 4mm)
- Ambient temperature 125°C

<Data>

- TB9053FTG : θja = 20.6 °C/W, θjc = 0.67 °C/W (Junction – E-Pad)
- TB9054FTG : θja = 24.1 °C/W, θjc = 2.6 °C/W (Junction – E-Pad)



9. Operation range

9.1. Power supply

Three power supplies (VBAT, VCC, and VDDIO) are externally supplied to this IC.

(1) VBAT power supply
Connect a battery power supply to VBAT, which is used for motor drive output.
The IC has a function to detect VBAT under-voltage.

(2) VCC power supply
Externally supply 5 V to VCC, which serves as a power supply for digital I/O in the IC.
VCC also serves as a power supply for internal analog circuits, which perform various monitoring functions.
The IC has a monitoring function to detect VCC under-voltage.

(3) VDDIO power supply
Externally supply the same power supply as for the I/O of the MCU to VDDIO, which serves as a power supply for the digital I/O of the SPI communication circuit in the IC.
The IC has no functions to monitor VDDIO power supply.

Table 9.1. Operating range

Item	Symbol	Rating	Unit	Remarks
Power supply voltage 1	VBAT	4.5 to 28.0	V	Note that until VBAT or VCC falls below each under-voltage detection voltage, the motor still functions.
Power supply voltage 2	VCC	4.5 to 5.5	V	Note that until VBAT or VCC falls below each under-voltage detection voltage, the motor still functions.
Power supply voltage 3	VDDIO	3.0 to 5.5	V	-
Operating temperature	Tj	-40 to 150	°C	-

Table 9.2. Power supply slew rate

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Power supply slew rate	VBSLEW	VBAT, VCC, VDD, VDDIO		-2	-	2	V/µs

10. Electrical characteristics

10.1. Input circuit

Table 10.1. Input circuit electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Input voltage	VIH1	PWM1/PWM2/ PWM3/PWM4, EN1/ENB1/EN 2/ENB2, ISEL1/ISEL2, PWM_CLK, SLEEPB, OSEL1/OSEL2		2.0	-	VCC	V
	VIL1			-0.3	-	0.8	V
	Vhys1			0.1	0.35	1.0	V
Input current	IIH1	PWM1/PWM2/ PWM3/PWM4, EN1/EN2/ ISEL1/ISEL2, PWM_CLK, SLEEPB, OSEL1/OSEL2	VIN = VCC = 5 V	25	50	100	µA
	IIH2	ENB1/ENB2		-5	0	5	µA
	IIL1	ENB1/ENB2	VIN = GND	-30	-14	-5	µA
	IIL2	PWM1/PWM2/ PWM3/PWM4, EN1/EN2/ ISEL1/ISEL2, PWM_CLK, SLEEPB, OSEL1/OSEL2		-5	0	5	µA
Sleep start time	tsleep (on)	SLEEPB		1,6	2.3	3.0	ms
Sleep cancellation time	tsleep (off)	SLEEPB		10	32	50	µs
PWM input maximum frequency	PWMMAX	PWM1/PWM2 PWM3/PWM4		-	-	20	kHz
EN/ENB logic determination time	TEN_ENB	EN1, ENB1 EN2, ENB2	Logic determination time, when the logic determined by the EN1/2 and ENB1/2 pins is changed	-	3.8	6.0	µs
Input pin noise filter	VI (noise)	EN1, ENB1, EN2, ENB2,		0.2	0.4	1.0	µs
Current consumption	ICC	VCC	VCC = 5 V; see Figure 11.1	-	5.4	8.5	mA
	ICC (sleep)	VCC	VCC = 5 V, Iout=0A, Sleep Mode	-	-	15	µA
	IDDIO	VDDIO	VDDIO = 5 V; see Figure 11.1	-	0.2	10	µA
	IBAT	VBAT	VBAT = 14 V; see Figure 11.1	-	1.0	2.0	mA
	IBAT (sleep)	VBAT	VBAT = 14V, Iout=0A, Sleep Mode	-	0.3	30	µA

Note: PWM1/2/3/4 have internal pull-down resistors.
Note: EN1/2 have internal pull-down resistors, and ENB1/2 have pull-up resistors.

10.2. Power supply monitoring function

Table 10.2. Power supply monitoring function electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
VBAT under-voltage detection voltage	VBATRSTL	VBAT	Figure 7.35	3.4	3.75	4.0	V
VBAT under-voltage cancellation voltage	VBATRSTH	VBAT	Figure 7.35	3.9	4.25	4.5	V
VCC under-voltage detection voltage	VCCHL	VCC	Figure 7.37	3.3	3.5	3.7	V
VCC under-voltage POR detection voltage	VCCRHL	VCC	Figure 7.37	2.85	3.07	3.25	V

10.3. Motor drive output circuit

Table 10.3. Motor drive output circuit electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition		Min.	Typ.	Max.	Unit
H-bridge output ON-resistance (high side + low side)	Ron (H + L)	OUT1, OUT2, OUT3, OUT4	Tj = +25°C, Iout = 3 A, VBAT = 8 V		-	200	250	mΩ
	Ron (H + L)	OUT1, OUT2, OUT3, OUT4	Tj = +150°C, Iout = 3 A, VBAT = 8 V		-	280	350	mΩ
	Ron (H + L)	OUT1, OUT2, OUT3, OUT4	Tj = +150°C, Iout = 3 A, VBAT = 4.5 V		-	300	370	mΩ
Output leak current	I outleak	OUT1, OUT2, OUT3, OUT4	OUT1/2: OFF (Hi-Z) OUT3/4: OFF (Hi-Z) Vout = VBAT = 28 V		-	85	110	μA
	I outleak	OUT1, OUT2, OUT3, OUT4	OUT1/2: OFF (Hi-Z) OUT3/4: OFF (Hi-Z) Vout = GND		-100	-3	-	μA
Output SR	trD/tfD	OUT1, OUT2, OUT3, OUT4	RL = 3 Ω, VBAT = 14 V; see Figure 10.1	DATA[14:12] =001	-	1.2	-	V/μs
	trD/tfD			DATA[14:12] =010	-	2.7	-	V/μs
	trD/tfD			DATA[14:12] =011	-	4.5	-	V/μs
	trD/tfD			DATA[14:12] =100	-	8.7	-	V/μs
	trD/tfD			DATA[14:12] =000	-	17.7	-	V/μs
	trD/tfD			DATA[14:12] =101	-	22.5	-	V/μs
	trD/tfD			DATA[14:12] =110	-	25.7	-	V/μs
Driver output delay time	tD(on)	PWM1/2, PWM3/4 OUT1/2, OUT3/4	VBAT = 14 V, Output SR = 17.50V/μs Figure 10.2 Measurement circuit: Figure 11.2		-	8.0	13	μs
	tD(off)				-	8.0	13	μs
	ΔtD		tD(on) - tD(off)		-	0	5	μs

EN/ENB Disable delay time	tDEN	EN1/2, ENB1/2 OUT1/2, OUT3/4	Figure 10.3 Output SR = 17.50V/μs Measurement circuit: Figure 11.2	-	8	13	μs

10.4. Current limit control

Table 10.4. Current limit control electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Current limit H-side threshold	Ilim-H	OUT1/2, OUT3/4	CONFIG1/2 DATA[18] = 0	5.0	6.5	8.2	A
	Ilim-H	OUT1/2, OUT3/4	CONFIG1/2 DATA[18] = 1	3.2	4.6	5.8	A
Current limit time	Toff_min	OUT1/2, OUT3/4	Figure 7.1414	15.0	20.5	32.0	μs
Current limit L-side threshold	Ilim-L	OUT1/2, OUT3/4	Figure 7.1414 CONFIG1/2 DATA[17] = 0	Ilim-H -0.10	Ilim-H -0.25	Ilim-H -0.40	A
	Ilim-L	OUT1/2, OUT3/4	Figure 7.1414 CONFIG1/2 DATA[17] = 1	Ilim-H -0.32	Ilim-H -0.5	Ilim-H -0.7	A

* This IC has an internal filter.

Table 10.5. Current limit control electrical characteristics (when temperature requiring current limitation is detected)

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Current limit H-side threshold	Ilim-H	OUT1/2, OUT3/4		1.8	2.5	3.5	A
Current limit temperature	Twar	-	*	150	166	177	°C

Note: * is a design value for which no mass-production test is applicable.

10.5. Over-temperature detection circuit

Table 10.6. Over-temperature detection circuit electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Over-temperature detection shutdown temperature	TSD	-	*	175	-	200	°C
Over-temperature detection recovery temperature	TSDL		*	150	-	-	°C

Note: * is a design value for which no mass-production test is applicable.

10.6. Detection circuit for over-current caused by short-circuit to power supply or ground, or short-circuited load

Table 10.7. Detection circuit for over-current caused by short-circuit to power supply or ground, or by short-circuited load: electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Over-current circuit threshold	Iovc(H)	OUT1/2, OUT3/4	High side	8.0	11.0	16.0	A
	Iovc(L)		Low side	8.5	13.0	17.0	
OFF time	TOFF	OUT1/2, OUT3/4	Automatic recovery mode, Figure 7.43	200	300	400	ms

10.7. DIAG output

Table 10.8 DIAG output electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
DIAG output leak current	Idiag (leak)	DIAG1/2	Vdiag = 5 V	-	0	5.0	μA
L level output voltage	Vdiag	DIAG1/2	RL = 5.1 kΩ, VCC = 1.5 to 5.5 V (L-retention circuit)	-	0.02	0.4	V

10.8. High-side current monitoring

Table 10.9. Output (high-side) current monitoring electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
CM1/2 output current 1	VCM	CM1, CM2	R = 220 Ω, Iout = 0 mA	-	0	90	μA
CM1/2 output current 2			R = 220 Ω, Iout = 300 mA	105	610	1100	μA
CM1/2 output current 3			R = 220 Ω, Iout = 1 A	1.4	2.3	3.4	mA
CM1/2 output current 4			R = 220 Ω, Iout = 1.5 A	2.6	3.6	4.6	mA
CM1/2 output current 5			R = 220 Ω, Iout = 3.0 A	6.0	7.4	9.0	mA
CM1/2 output current 6			R = 220 Ω, Iout = 6.0 A	10.0	15.5	18.0	mA

Note: Since the VCC voltage (min.) is 4.5 V, the voltage is limited even with an external resistance greater than 220 Ω.

10.9. Driver output AC characteristics

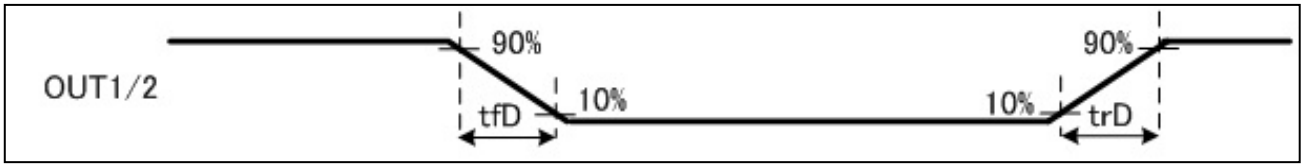


Figure 10.1. Driver output slew rate (SR)

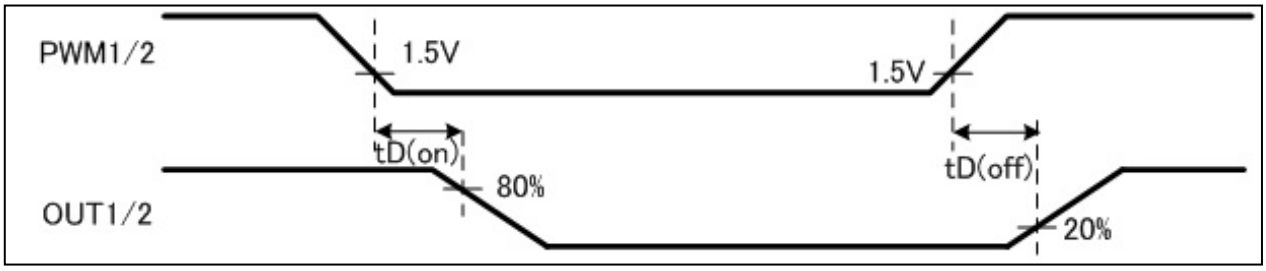


Figure 10.2. Driver output delay time

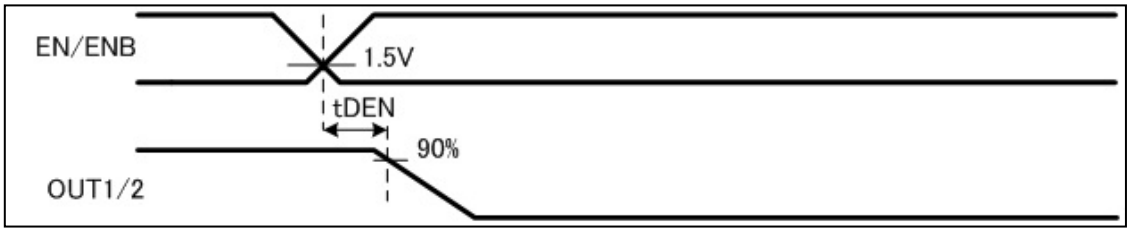


Figure 10.3. Driver output Enable delay time

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

10.10. OSC circuit (oscillation circuit)

Table 10.10. OSC circuit (oscillation circuit) electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Internal oscillation clock frequency	fosc			12.8	16.0	19.2	MHz

10.11. SPI communication

Table 10.11. SPI communication electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Input voltage	VIH3	SDI, SCLK, NCS	VDDIO = 4.5 to 5.5 V	3.6	-	VDDIO	V
	VIL3		VDDIO = 4.5 to 5.5 V	-0.3	-	0.8	V
	Vhys3		VDDIO = 4.5 to 5.5 V	0.1	-	1	V
Input voltage	VIH4	SDI, SCLK, NCS	VDDIO = 3.0 to 3.6 V	2.4	-	VDDIO	V
	VIL4		VDDIO = 3.0 to 3.6 V	-0.3	-	0.8	V
	Vhys4		VDDIO = 3.0 to 3.6 V	0.1	-	1	V
Input current	IIH3	NCS	VIN = VDDIO = 5 V	-5	0	5	μA
	IIH4	SDI, SCLK		25	50	100	μA
	IIL3	SDI, SCLK	VDDIO = 5 V, VIN = GND	-5	0	5	μA
	IIL4	NCS		-30	-14	-5	μA
Output voltage	VOH (SDO)	SDO	IOH = -2 mA	0.9 * VDDIO	-	-	V
	VOL (SDO)	SDO	IOL = 2 mA	-	-	0.1 * VDDIO	V
AC characteristics	Td (SDO1)	NCS → SDO		-	-	100	ns
	Td (SCLK)	NCS → SCLK		100	-	-	ns
	Td (NCS)	SCLK → NCS		100	-	-	ns
	Tsu (SDI)	SCLK → SDI		50	-	-	ns
	Th (SDI)	SCLK → SDI		50	-	-	ns
	Tvalid	SCLK → SDO	CL = 100 pF	-	-	50	ns
	Ttrans	NCS↑ → NCS↓		1000	-	-	ns
	Td (SDO2)	NCS → SDO (OFF)	CL = 100 pF	-	-	300	ns
	fSPI	SCLK		-	-	5	MHz

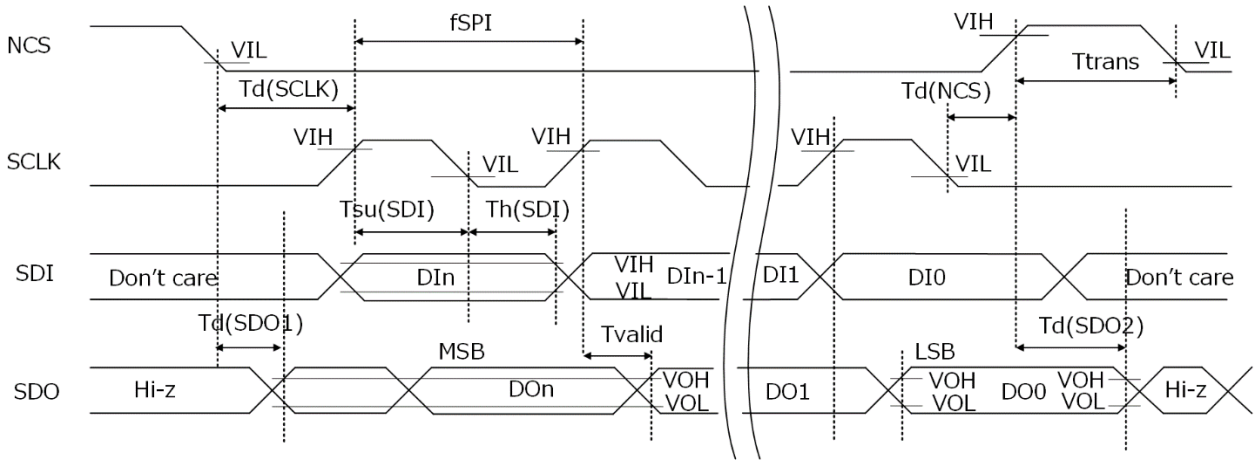


Figure 10.4. SPI communication timing chart

Note: Parts of each timing chart shown in this specification document may be omitted or simplified for explanatory purposes.

Table 10.12. SPI communication disruption detection electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
SPI communication disruption duration	Tstop (NCS)	NCS	CONFIG1 DATA[10:9] = 00	-	10	-	ms
			CONFIG1 DATA[10:9] = 01	-	100	-	ms
			CONFIG1 DATA[10:9] = 10	-	1000	-	ms
			CONFIG1 DATA[10:9] = 11	-	Not applicable	-	ms

Table 10.13. PWM_CLK pin input clock abnormality detection electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
PWM_CLK suspension determination time	Tstop (PWM_CLK)	PWM_CLK		-	8	-	μs

Table 10.14. PWM_CLK pin input clock Input range electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
PWM_CLK Input range	f(PWM_CLK)	PWM_CLK		1.0	2.0	4.0	MHz

11. Measurement circuit diagram

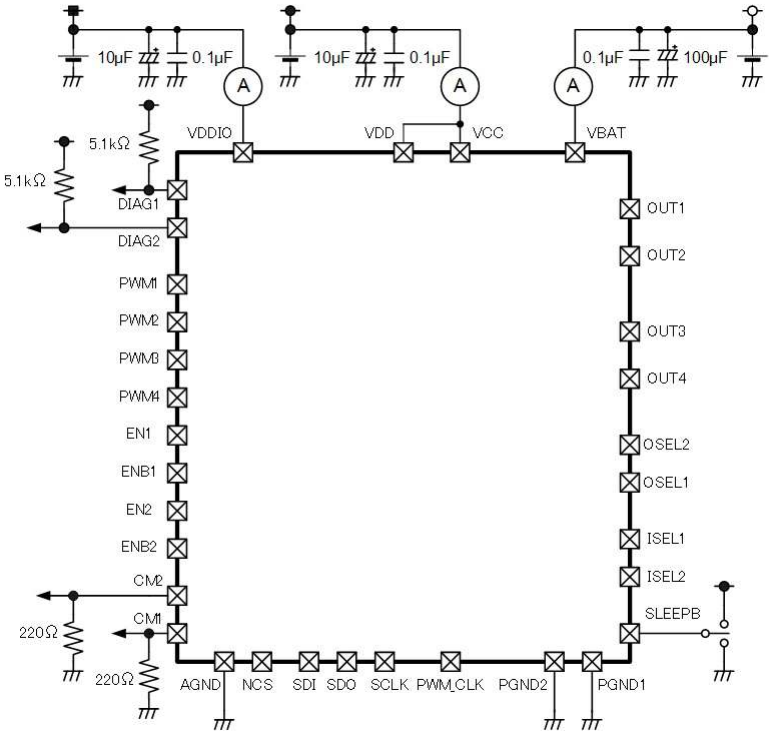


Figure 11.1. Current consumption measurement circuit diagram

Note: The parts in the measurement circuit are used to test characteristics, but are not intended to guarantee that no malfunction or failure occurs in your application.

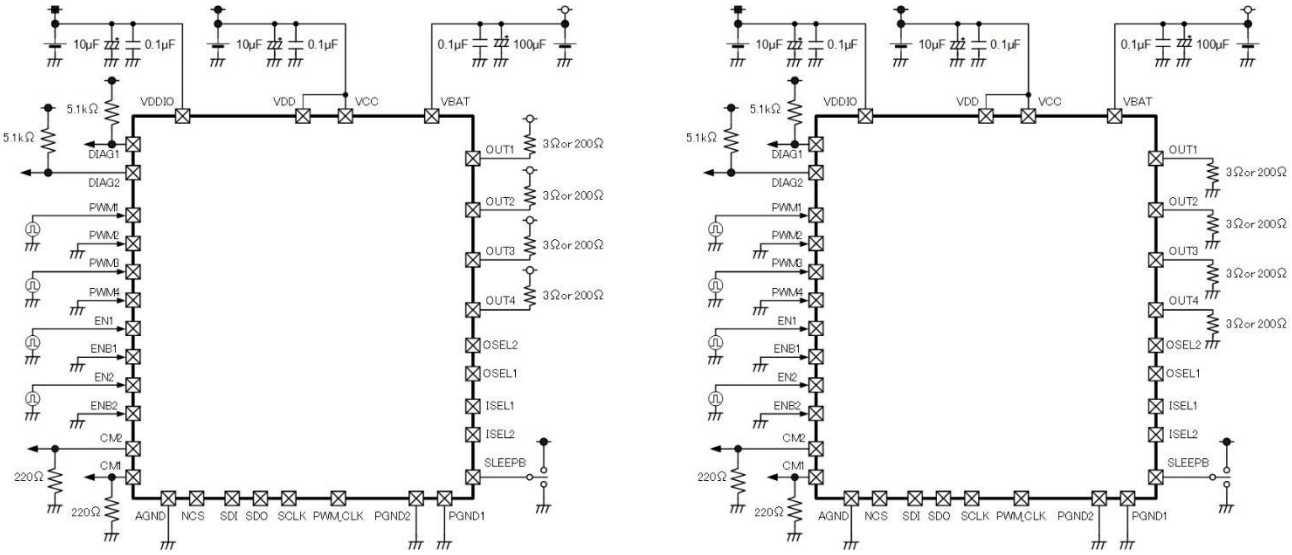
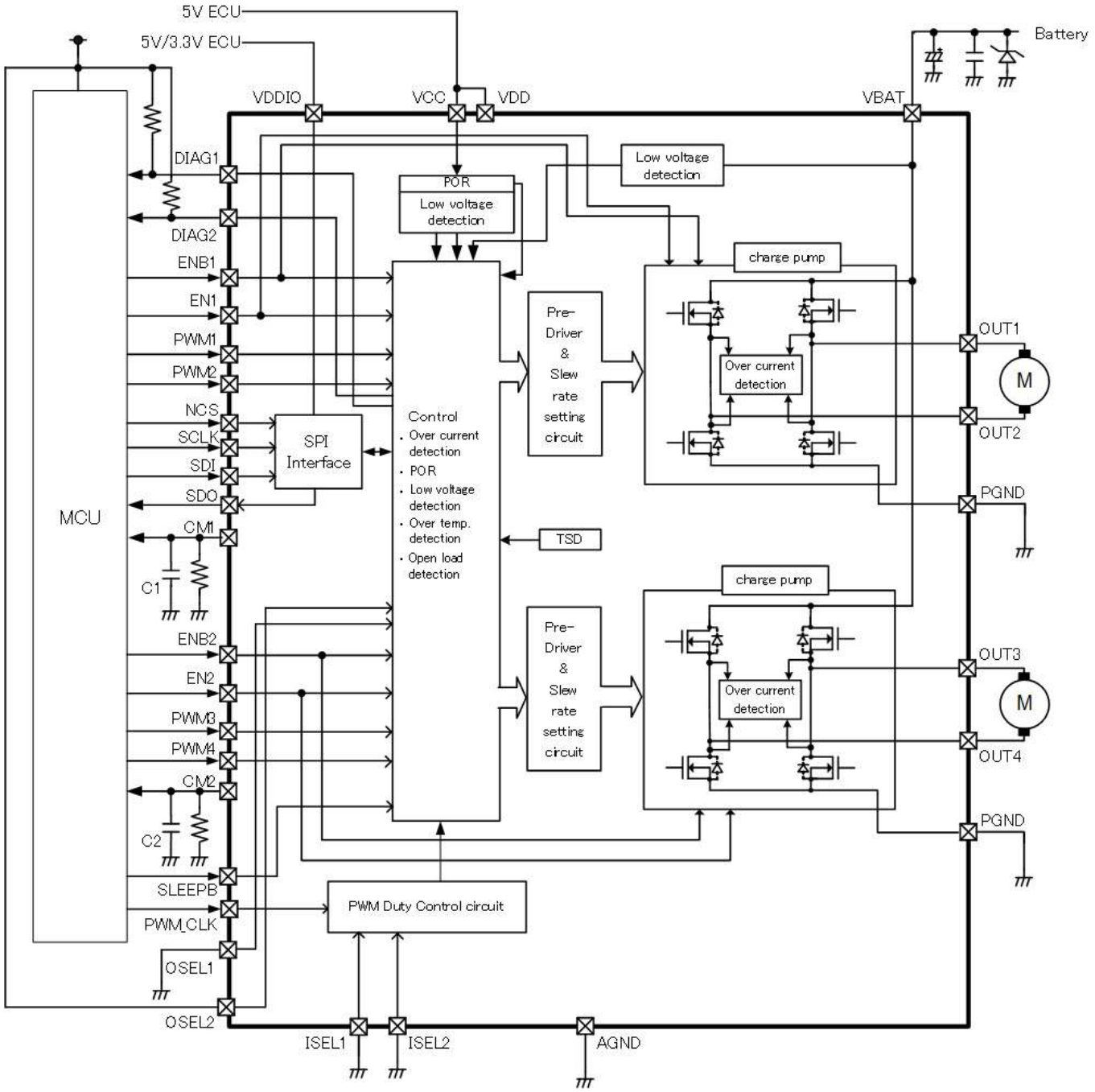


Figure 11.2. OUT pins output delay time measurement circuit diagram

Note: The parts in the measurement circuit are used to test characteristics, but are not intended to guarantee that no malfunction or failure occurs in your application.

12. Example application circuit



C1,C2 capacitance value: 0.1μF to 1μF

Figure 12.1. Example application circuit

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

Note: Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause device breakdown, damage, and/or deterioration.

Note: The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass-production design stage. Toshiba does not grant any license to any industrial property rights by providing examples of application circuits.

Note: When an output pin is short-circuited to another output pin, power supply, or ground, the IC may break down. As such, design the output, VBAT, VCC, and GND lines carefully.

Note: For the board design, use solid patterns for AGND and PGND.

Note: The CM1/CM2 pins are configured with a 5V power supply circuit. In this case, be careful not to exceed the withstand voltage of the MCU pins.

Counter electromotive force:

When power-regeneration starts during motor rotation, the motor current is fed back to the power supply due to motor counter electromotive force.

If the power supply does not have enough sink capability, the power supply and output pins of the IC may exceed the rated voltages.

The magnitude of the motor counter electromotive force varies with use conditions and motor characteristics. Thoroughly verify that the counter electromotive force does not cause any malfunctions or breakdown of the IC or other parts of the system, such as peripheral circuits.

13. Package drawings

13.1. Package dimensions TB9053FTG (P-LQFN40-0606-0.50-001)

Weight: 193mg (typical)
Unit:mm

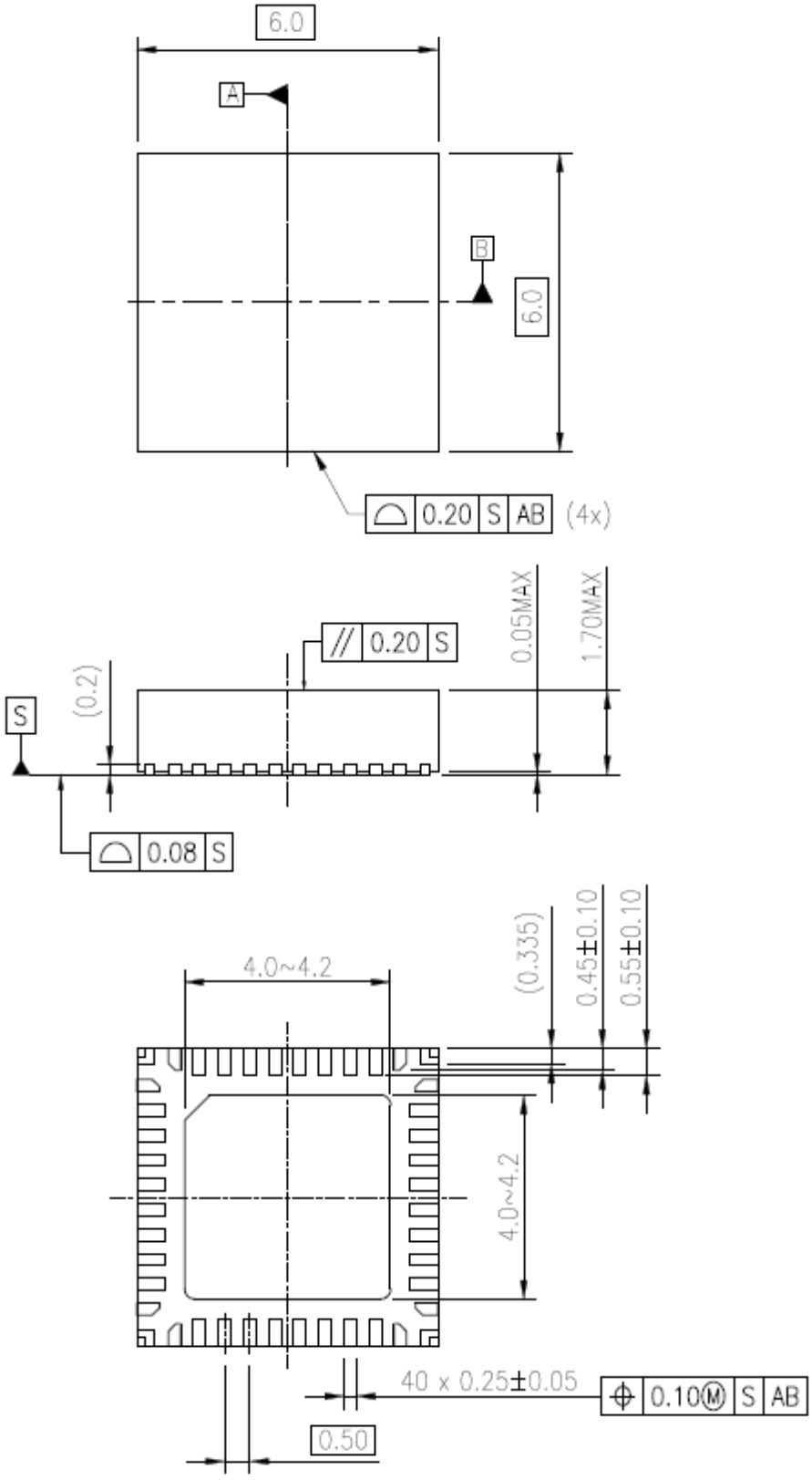


Figure 13.1. Package dimensions TB9053FTG

13.2. Package dimensions TB9054FTG (P-VQFN40-0606-0.50-004)

Weight: 94.4mg (typical)
Unit:mm

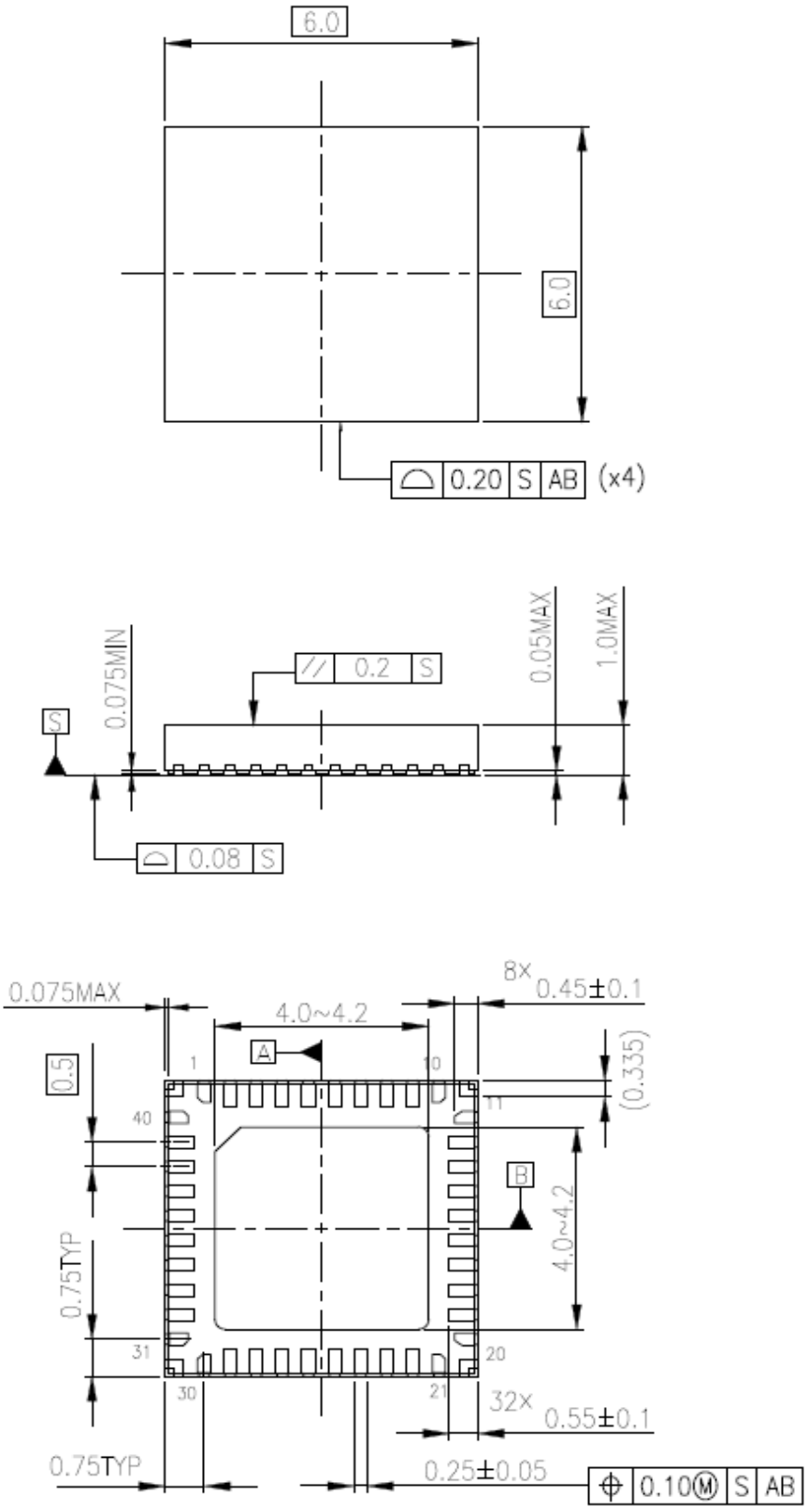
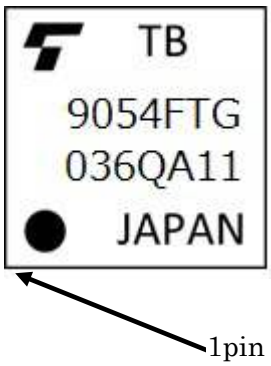


Figure 13.2. Package dimensions TB9054FTG

13.3. Marking



1. Toshiba logo mark
2. Product name (Part number: TB9054FTG)
3. Lot code (e.g. 036QA11)
4. Country/Region of origin (JAPAN)

Note: Lot code description
Example : 0 (1) 36 (2) Q (3) A11 (4)

(1) Last number of calendar year (Example shows “0” of 2020)
(2) Week code (Example shows 36th week)
(3) Product sight code (Q)
(4) Toshiba management code (3 digits at maximum)

14. IC Usage Considerations

14.1. Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.
Do not exceed any of these ratings.
Exceeding the ratings may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

14.2. Points to remember on handling of ICs

(1) Over-current protection circuit
An over-current limiting circuit does not necessarily protect an IC under all circumstances. When it is activated, promptly eliminate the over-current state. Depending on the method of use and/or usage conditions such as exceeding absolute maximum ratings, an over-current detection circuit may not operate properly or the IC is broken down before the circuit is activated. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal shutdown circuit
A thermal shutdown circuit does not necessarily protect an IC under all circumstances. When it is activated, promptly eliminate the over-temperature state. Depending on the method of use and/or usage conditions such as exceeding absolute maximum ratings, a thermal shutdown circuit may not operate properly or the IC is broken down before the circuit is activated.

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