

## SNx4AHC14 Hex Schmitt-Trigger Inverters

### 1 Features

- ESD protection exceeds JESD 22:
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Operating range: 2 V to 5.5 V
- ±8-mA output drive at 5 V
- Schmitt-Trigger inputs enable input noise resistance
- Low power consumption: 20  $\mu$ A maximum  $I_{CC}$
- Latch-up performance exceeds 250 mA per JESD 17

### 2 Applications

- UPS
- White goods
- Computer peripherals
- Printers
- AC servo drives
- Desktop computers

### 3 Description

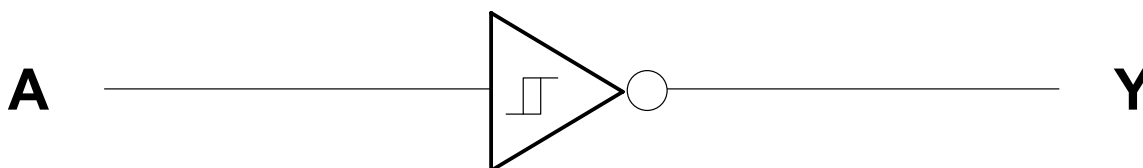
The SNx4AHC14 devices contain six independent inverters. These devices perform the boolean function  $Y = \bar{A}$ .

Each circuit functions as an independent inverter, but, because of the Schmitt-Trigger action, the inverters have different input threshold levels for positive-going ( $V_{T+}$ ) and negative-going ( $V_{T-}$ ) signals.

#### Device Information

PART NUMBER	RATING	PACKAGE <sup>(1)</sup>
SN54AHC14	Military	J (CDIP, 14)
		W (CFP, 14)
		FK (LCCC, 20)
		BQA (WQFN, 14)
SN74AHC14	Commercial	D (SOIC, 14)
		DB (SSOP, 14)
		N (PDIP, 14)
		NS (SO, 14)
		PW (TSSOP, 14)
		DGV (TVSOP, 14)
		RGY (VQFN, 14)
		BQA (WQFN, 14)

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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Logic Diagram (Positive Logic)



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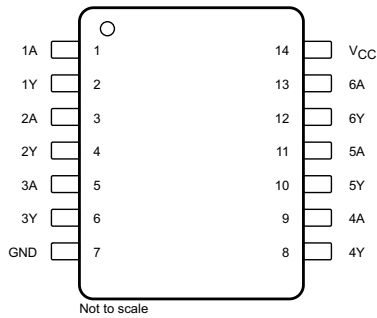
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## 4 Revision History

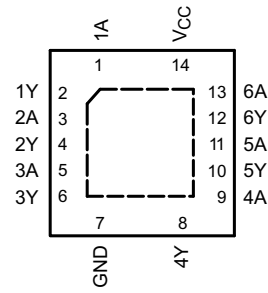
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision M (March 2017) to Revision N (June 2023)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated the <i>Device Information</i> table to include channel count.....	1
• Added the <i>BQA</i> package to the data sheet.....	1
<b>Changes from Revision L (September 2016) to Revision M (March 2017)</b>	<b>Page</b>
• Added $t_{PLH}$ MIN and MAX specification for SN74AHC14 in <i>Switching Characteristics – 5 V</i> .....	7
<b>Changes from Revision K (June 2013) to Revision L (September 2016)</b>	<b>Page</b>
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Changed $R_{\theta JA}$ values in the <i>Thermal Information</i> table from 86 to 99.3 (D), from 96 to 112.4 (DB), from 127 to 141.9 (DGV), from 80 to 61.9 (N), from 76 to 94.7 (NS), from 113 to 128.8 (PW), and from 47 to 63.8 (RGY).....	5
<b>Changes from Revision J (October 2010) to Revision K (June 2013)</b>	<b>Page</b>
• Extended operating temperature range to 125°C.....	1

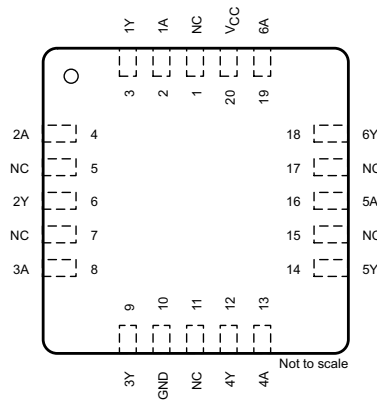
## 5 Pin Configuration and Functions



**Figure 5-1. D, DB, DGV, J, N, NS, PW, or W Package, 14-Pin SOIC, SSOP, TVSOP, CDIP, PDIP, SO, TSSOP, or CFP (Top View)**



**Figure 5-2. RGY or BQA Package, 14-Pin VQFN or WQFN (Top View)**



**Figure 5-3. FK Package, 20-Pin LCCC (Top View)**

**Table 5-1. Pin Functions**

NAME	PIN		TYPE <sup>(1)</sup>	DESCRIPTION
	SOIC, SSOP, TVSOP, CDIP, PDIP, SO, TSSOP, CFP, VQFN	LCCC		
1A	1	2	I	Channel 1 Input
1Y	2	3	O	Channel 1 Output
2A	3	4	I	Channel 2 Input
2Y	4	6	O	Channel 2 Output
3A	5	8	I	Channel 3 Input
3Y	6	9	O	Channel 3 Output
4A	9	13	I	Channel 4 Input
4Y	8	12	O	Channel 4 Output
5A	11	16	I	Channel 5 Input
5Y	10	14	O	Channel 5 Output
6A	13	19	I	Channel 6 Input
6Y	12	18	O	Channel 6 Output
GND	7	10	—	Ground
NC	—	1, 5, 7, 11, 15, 17	—	No internal connection
V <sub>CC</sub>	14	20	—	Power supply

(1) I = input, O = output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage, $V_{CC}$	-0.5	7	V
Input voltage, $V_I$ <sup>(2)</sup>	-0.5	7	V
Output voltage, $V_O$ <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
Input clamp current, $I_{IK}$	$V_I < 0$	-20	mA
Output clamp current, $I_{OK}$	$V_O < 0$ or $V_O > V_{CC}$	$\pm 20$	mA
Continuous output current, $I_O$	$V_O = 0$ to $V_{CC}$	$\pm 25$	mA
Continuous current through $V_{CC}$ or GND		$\pm 50$	mA
Virtual operating junction temperature, $T_J$		150	°C
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 2000$
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	$\pm 1000$
	Machine Model (MM), A115-A	200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	2	5.5	V
$V_I$ Input voltage	0	5.5	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current	$V_{CC} = 2$ V	-50	$\mu$ A
	$V_{CC} = 3.3$ V $\pm 0.3$ V	-4	mA
	$V_{CC} = 5$ V $\pm 0.5$ V	-8	
$I_{OL}$ Low-level output current	$V_{CC} = 2$ V	50	$\mu$ A
	$V_{CC} = 3.3$ V $\pm 0.3$ V	4	mA
	$V_{CC} = 5$ V $\pm 0.5$ V	8	
$T_A$ Operating free-air temperature	SN54AHC14	-55	°C
	SN74AHC14	-40	

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. See TI application report, [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHC14								UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	99.3	112.4	141.9	61.9	94.7	128.8	63.8	88.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	59.1	64.3	61.1	49.5	52.5	57.2	76.6	90.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	53.6	59.8	71.3	41.7	53.4	70.6	39.9	56.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	24.8	28.5	9.7	34.7	21.3	9.6	5.2	9.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	53.3	59.3	70.6	41.7	53.1	70	40	56.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	20	33.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V <sub>T+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 3 V			1.2		2.2	V
		V <sub>CC</sub> = 4.5 V			1.75		3.15	
		V <sub>CC</sub> = 5.5 V			2.15		3.85	
V <sub>T-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 3 V			0.9		1.9	V
		V <sub>CC</sub> = 4.5 V			1.35		2.75	
		V <sub>CC</sub> = 5.5 V			1.65		3.35	
ΔV <sub>T</sub>	Hysteresis (V <sub>T+</sub> – V <sub>T-</sub> )	V <sub>CC</sub> = 3 V			0.3		1.2	V
		V <sub>CC</sub> = 4.5 V			0.4		1.4	
		V <sub>CC</sub> = 5.5 V			0.5		1.6	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	V <sub>CC</sub> = 2 V			1.9		2	V
		V <sub>CC</sub> = 3 V			2.9		3	
		V <sub>CC</sub> = 4.5 V			4.4		4.5	
	I <sub>OH</sub> = –4 mA, V <sub>CC</sub> = 3 V			T <sub>A</sub> = 25°C			2.58	
				SNx4AHC14			2.48	
	I <sub>OL</sub> = –8 mA, V <sub>CC</sub> = 4.5 V			T <sub>A</sub> = 25°C			3.94	
SNx4AHC14				3.8				

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$V_{OL}$	$I_{OH} = 50 \mu A$	$V_{CC} = 2 V$			0.1	V	
		$V_{CC} = 3 V$			0.1		
		$V_{CC} = 4.5 V$			0.1		
	$I_{OH} = 4 mA, V_{CC} = 3 V$	$T_A = 25^\circ C$					0.36
		SN54AHC14					0.5
		SN74AHC14	$T_A = -40^\circ C$ to $85^\circ C$				0.44
			$T_A = -40^\circ C$ to $125^\circ C$				0.5
	$I_{OL} = 8 mA, V_{CC} = 4.5 V$	$T_A = 25^\circ C$					0.36
		SN54AHC14					0.5
SN74AHC14		$T_A = -40^\circ C$ to $85^\circ C$			0.44		
		$T_A = -40^\circ C$ to $125^\circ C$			0.5		
$I_I$	$V_I = 5.5 V$ or GND, $V_{CC} = 0 V$ to $5.5 V$	$T_A = 25^\circ C$			$\pm 0.1$	$\mu A$	
		SNx4AHC14			$\pm 1^{(1)}$		
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$ , $V_{CC} = 5.5 V$	$T_A = 25^\circ C$			1	$\mu A$	
		SNx4AHC14			20		
$C_I$	$V_I = V_{CC}$ or GND, $V_{CC} = 5 V$	$T_A = 25^\circ C$			2	pF	
		SN74AHC14			10		
$C_{pd}$	Power dissipation capacitance	No load, $f = 1 MHz, V_{CC} = 5 V$			9	pF	
<b>NOISE<sup>(2)</sup></b>							
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$	$V_{CC} = 5 V, C_L = 50 pF, T_A = 25^\circ C$			0.8	V	
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$	$V_{CC} = 5 V, C_L = 50 pF, T_A = 25^\circ C$			-0.4	V	
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$	$V_{CC} = 5 V, C_L = 50 pF, T_A = 25^\circ C$			4.6	V	
$V_{IH(D)}$	High-level dynamic input voltage	$V_{CC} = 5 V, C_L = 50 pF, T_A = 25^\circ C$			3.5	V	
$V_{IL(D)}$	Low-level dynamic input voltage	$V_{CC} = 5 V, C_L = 50 pF, T_A = 25^\circ C$			1.5	V	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at  $V_{CC} = 0 V$ .

(2) Characteristics are for surface-mount packages only.

## 6.6 Switching Characteristics – 3.3 V

$V_{CC} = 3.3 V \pm 0.3 V$  and over operating free-air temperature range (unless otherwise noted; see [Parameter Measurement Information](#))

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$	From A (input) to Y (output), $C_L = 15 pF$	$T_A = 25^\circ C$	8.3 <sup>(1)</sup>		12.8 <sup>(1)</sup>	ns
		SN54AHC14	1 <sup>(1)</sup>		15 <sup>(1)</sup>	
		SN74AHC14	1		16	
$t_{PHL}$	From A (input) to Y (output), $C_L = 15 pF$	$T_A = 25^\circ C$	8.3 <sup>(1)</sup>		12.8 <sup>(1)</sup>	ns
		SN54AHC14	1 <sup>(1)</sup>		15 <sup>(1)</sup>	
		SN74AHC14	1		16	
$t_{PLH}$	From A (input) to Y (output), $C_L = 50 pF$	$T_A = 25^\circ C$	10.8		16.3	ns
		SN54AHC14	1		18.5	
		SN74AHC14	1		19.5	

### 6.6 Switching Characteristics – 3.3 V (continued)

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  and over operating free-air temperature range (unless otherwise noted; see [Parameter Measurement Information](#))

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{PHL}$	From A (input) to Y (output), $C_L = 50\text{ pF}$	$T_A = 25^\circ\text{C}$		10.8	16.3	ns
		SN54AHC14		1	18.5	
		SN74AHC14		1	19.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

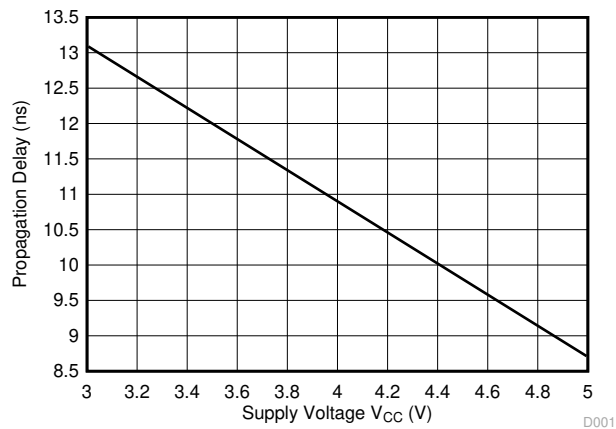
### 6.7 Switching Characteristics – 5 V

$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  and over operating free-air temperature range (unless otherwise noted; see [Parameter Measurement Information](#))

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{PLH}$	From A (input) to Y (output), $C_L = 15\text{ pF}$	$T_A = 25^\circ\text{C}$		5.5 <sup>(1)</sup>	8.6 <sup>(1)</sup>	ns
		SN54AHC14		1 <sup>(1)</sup>	10 <sup>(1)</sup>	
		SN74AHC14		1	10	
$t_{PHL}$	From A (input) to Y (output), $C_L = 15\text{ pF}$	$T_A = 25^\circ\text{C}$		5.5 <sup>(1)</sup>	8.6 <sup>(1)</sup>	ns
		SN54AHC14		1 <sup>(1)</sup>	10 <sup>(1)</sup>	
		SN74AHC14		1	10	
$t_{PLH}$	From A (input) to Y (output), $C_L = 50\text{ pF}$	$T_A = 25^\circ\text{C}$		7	10.6	ns
		SNx4AHC14		1	12	
$t_{PHL}$	From A (input) to Y (output), $C_L = 50\text{ pF}$	$T_A = 25^\circ\text{C}$		7	10.6	ns
		SNx4AHC14		1	12	

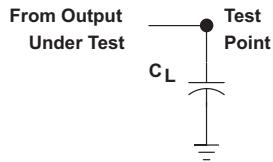
### 6.8 Typical Characteristics

$C_L = 50\text{ pF}$  (unless otherwise noted)

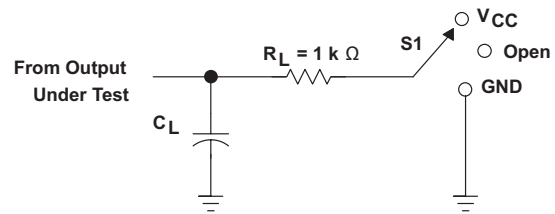


**Figure 6-1. Propagation Delay vs Supply Voltage**

## 7 Parameter Measurement Information



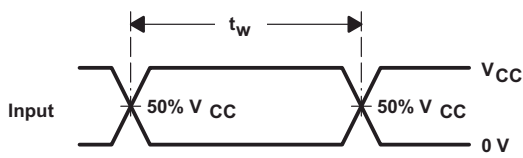
**Figure 7-1. Load Circuit For Totem-Pole Outputs**



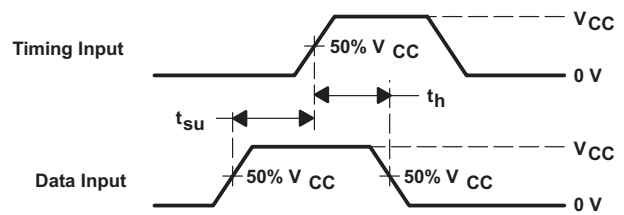
**Figure 7-2. Load Circuit For 3-State and Open-Drain Outputs**

**Table 7-1. Measurement Information**

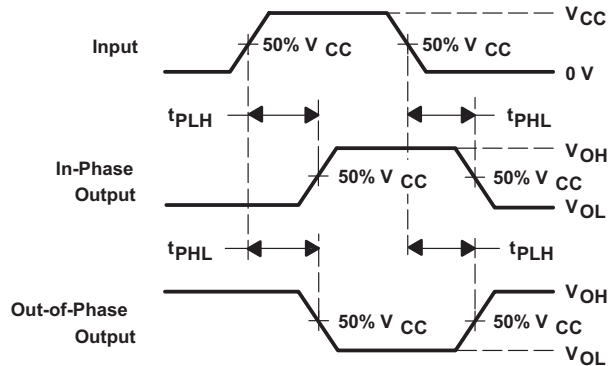
TEST	S1
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PLZ}$ , $t_{PZL}$	$V_{CC}$
$t_{PHZ}$ , $t_{PZH}$	GND
Open drain	$V_{CC}$



**Figure 7-3. Voltage Waveforms Pulse Duration**

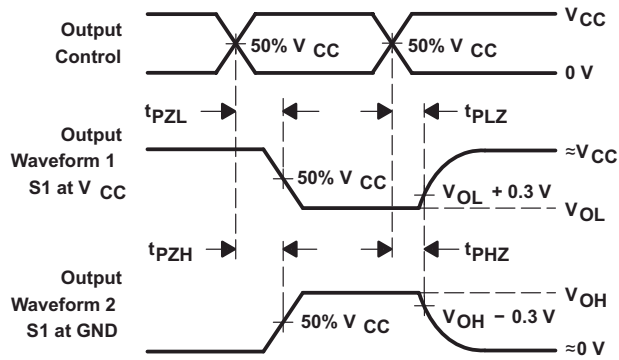


**Figure 7-4. Voltage Waveforms Setup and Hold Times**



**Figure 7-5. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs**





- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 7-6. Voltage Waveforms Enable and Disable Times Low- and High-Level Enabling**

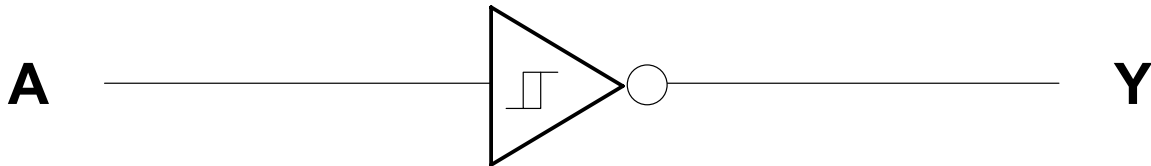
## 8 Detailed Description

### 8.1 Overview

The SNx4AHC14 Schmitt-Trigger devices contain six independent inverters. They perform the Boolean function  $Y = \bar{A}$  in positive logic.

Schmitt-Trigger inputs are designed to provide a minimum separation between positive and negative switching thresholds. This allows for noisy or slow inputs that would cause problems such as oscillation or excessive current draw with normal CMOS inputs.

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

The wide operating range of the device allows it to be used in a variety of systems that use different logic levels. The output can drive up to 10 LSTTL loads each. The balanced drive outputs can source or sink 8 mA at 5-V  $V_{CC}$ .

### 8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SNx4AHC14.

**Table 8-1. Function Table**

INPUT A	OUTPUT Y
H	L
L	H

## 9 Application and Implementation

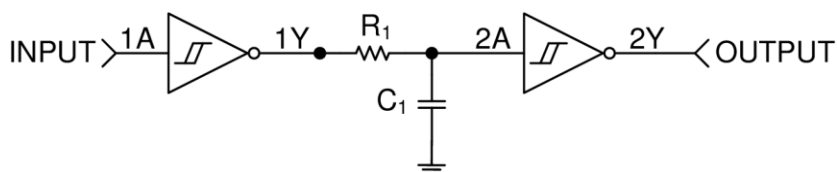
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74AHC14 device is a Schmitt-Trigger input CMOS device that can be used for a multitude of inverting buffer type functions. The application shown here takes advantage of the Schmitt-Trigger inputs to produce a delay for a logic input.

### 9.2 Typical Application



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**Figure 9-1. Simplified Application Schematic**

#### 9.2.1 Design Requirements

This device uses CMOS technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Parallel output drive can create fast edges into light loads so consider routing and load conditions to prevent ringing.

#### 9.2.2 Detailed Design Procedure

This circuit is designed around an RC network that produces a slow input to the second inverter. The RC time constant,  $\tau$ , is calculated from:  $\tau = RC$ .

The delay time for this circuit is from  $t_{\text{delay}(\text{min})} = -\ln |1 - V_{T+(\text{min})} / V_{CC}| \tau$  to  $t_{\text{delay}(\text{max})} = -\ln |1 - V_{T+(\text{max})} / V_{CC}| \tau$ . It must be noted that the delay is consistent for each device, but because the switching threshold is only ensured between the minimum and maximum value, the output pulse length varies between devices. These values must be calculated by using the minimum and maximum  $V_{T+}$  values in the [Electrical Characteristics](#).

The resistor value must be chosen such that the maximum current to and from the SN74AHC14 is 8 mA at  $5-V V_{CC}$ .

### 9.2.3 Application Curve

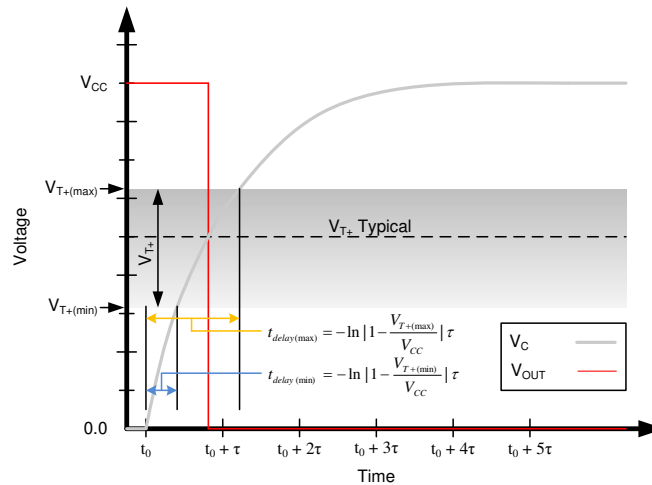


Figure 9-2. Ideal Capacitor Voltage and Output Voltage With Positive Switching Threshold

### 9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#). The  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. TI recommends using a 0.1- $\mu\text{F}$  capacitor on the  $V_{CC}$  terminal, and must be placed as close as possible to the pin for best results.

### 9.4 Layout

#### 9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such inputs must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. Floating outputs are generally acceptable, unless the part is a transceiver.

#### 9.4.2 Layout Example

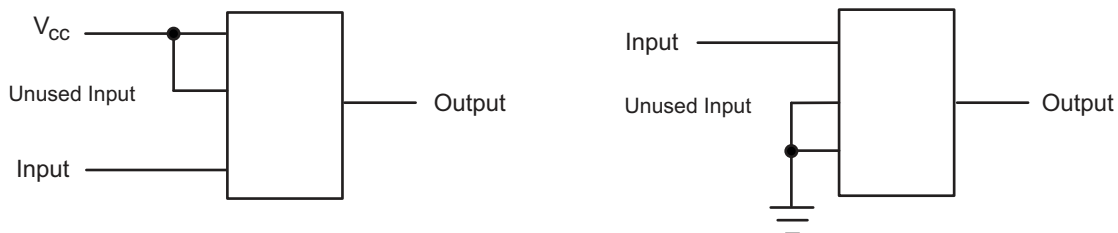


Figure 9-3. Layout Diagram

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application report](#)

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9680201Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680201Q2A SNJ54AHC14FK	<a href="#">Samples</a>
5962-9680201QCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680201QCA SNJ54AHC14J	<a href="#">Samples</a>
5962-9680201QDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680201QDA SNJ54AHC14W	<a href="#">Samples</a>
5962-9682001QCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682001QCA SNJ54AHC08J	<a href="#">Samples</a>
5962-9682001QDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682001QDA SNJ54AHC08W	<a href="#">Samples</a>
SN74AHC14BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC14	<a href="#">Samples</a>
SN74AHC14DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14	<a href="#">Samples</a>
SN74AHC14DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14	<a href="#">Samples</a>
SN74AHC14DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	AHC14	<a href="#">Samples</a>
SN74AHC14DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC14	<a href="#">Samples</a>
SN74AHC14DRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AHC14	<a href="#">Samples</a>
SN74AHC14DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC14	<a href="#">Samples</a>
SN74AHC14N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC14N	<a href="#">Samples</a>
SN74AHC14NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC14	<a href="#">Samples</a>
SN74AHC14PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HA14	<a href="#">Samples</a>
SN74AHC14PWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC14PWRG3	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	HA14	<a href="#">Samples</a>
SN74AHC14PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA14	<a href="#">Samples</a>
SN74AHC14RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA14	<a href="#">Samples</a>
SNJ54AHC08J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682001QC A SNJ54AHC08J	<a href="#">Samples</a>
SNJ54AHC08W	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682001QD A SNJ54AHC08W	<a href="#">Samples</a>
SNJ54AHC14FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9680201Q2A SNJ54AHC 14FK	<a href="#">Samples</a>
SNJ54AHC14J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680201QC A SNJ54AHC14J	<a href="#">Samples</a>
SNJ54AHC14W	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680201QD A SNJ54AHC14W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54AHC14, SN74AHC14 :**

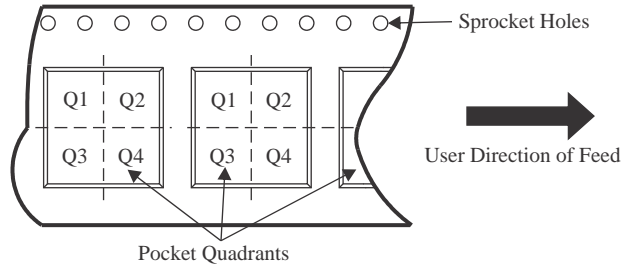
- Catalog : [SN74AHC14](#)
- Enhanced Product : [SN74AHC14-EP](#), [SN74AHC14-EP](#)
- Military : [SN54AHC14](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC14BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC14DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC14DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC14DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74AHC14DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74AHC14DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC14NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC14PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC14PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC14RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC14BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC14DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHC14DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHC14DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74AHC14DR	SOIC	D	14	2500	364.0	364.0	27.0
SN74AHC14DRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74AHC14DRG4	SOIC	D	14	2500	340.5	336.1	32.0
SN74AHC14NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHC14PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC14PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74AHC14PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC14RGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

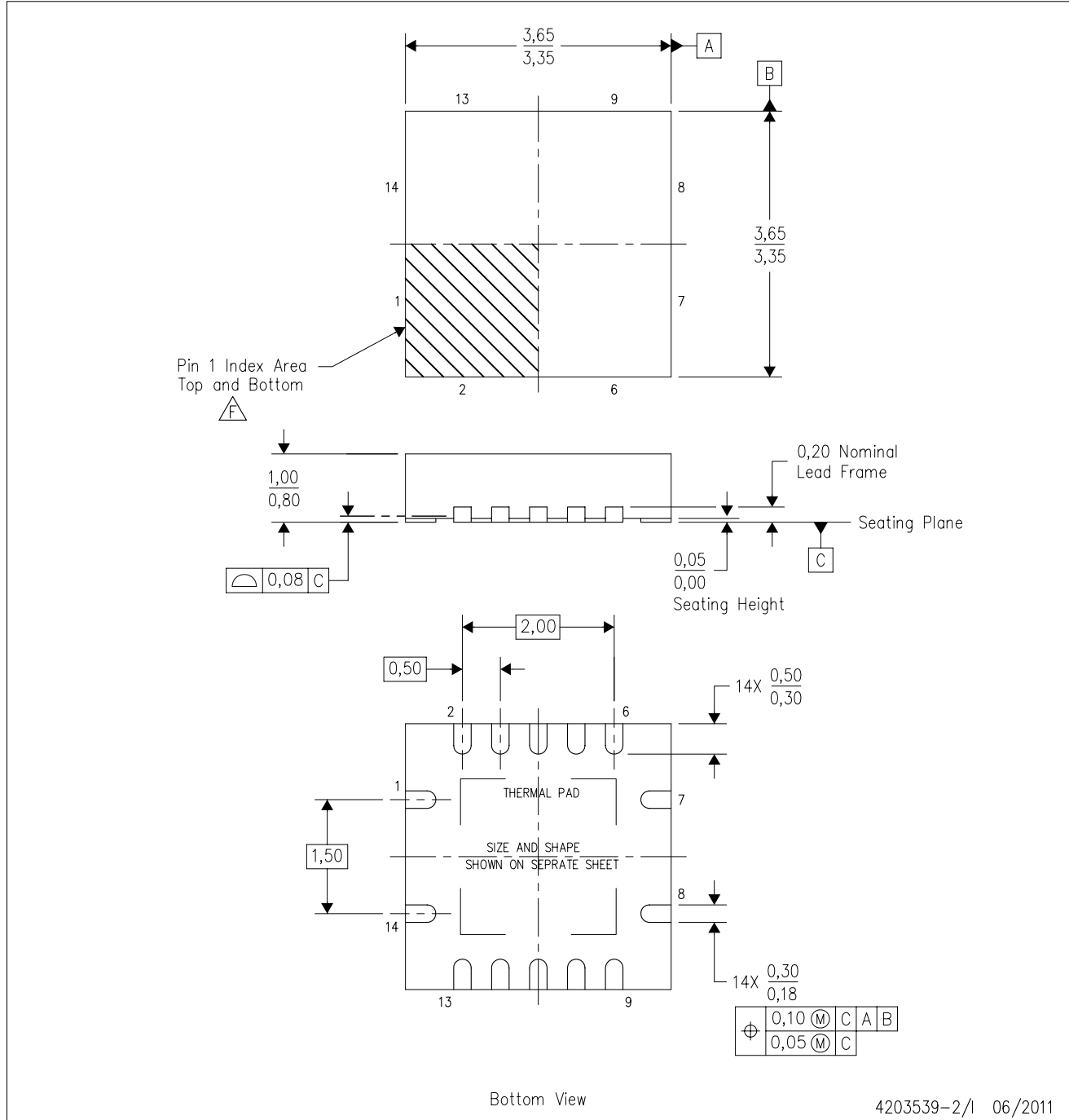
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9680201Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9680201QDA	W	CFP	14	1	506.98	26.16	6220	NA
5962-9682001QDA	W	CFP	14	1	506.98	26.16	6220	NA
SN74AHC14N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC14N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC08W	W	CFP	14	1	506.98	26.16	6220	NA
SNJ54AHC14FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54AHC14W	W	CFP	14	1	506.98	26.16	6220	NA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

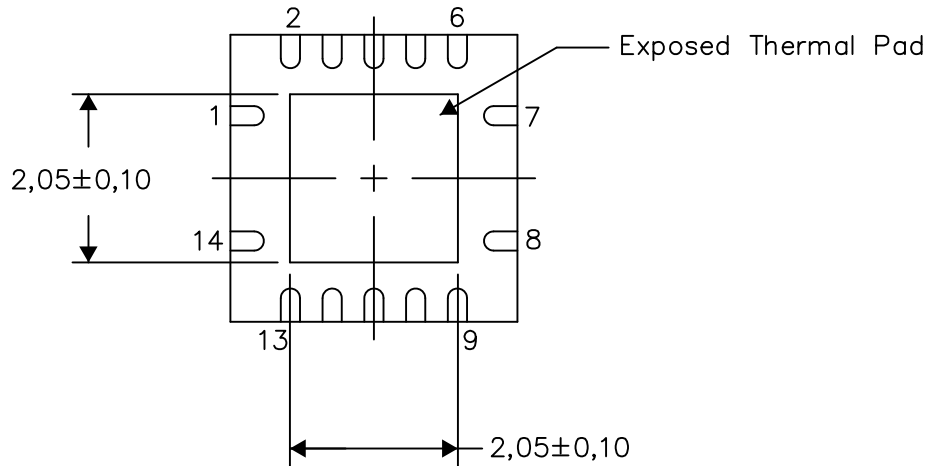
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

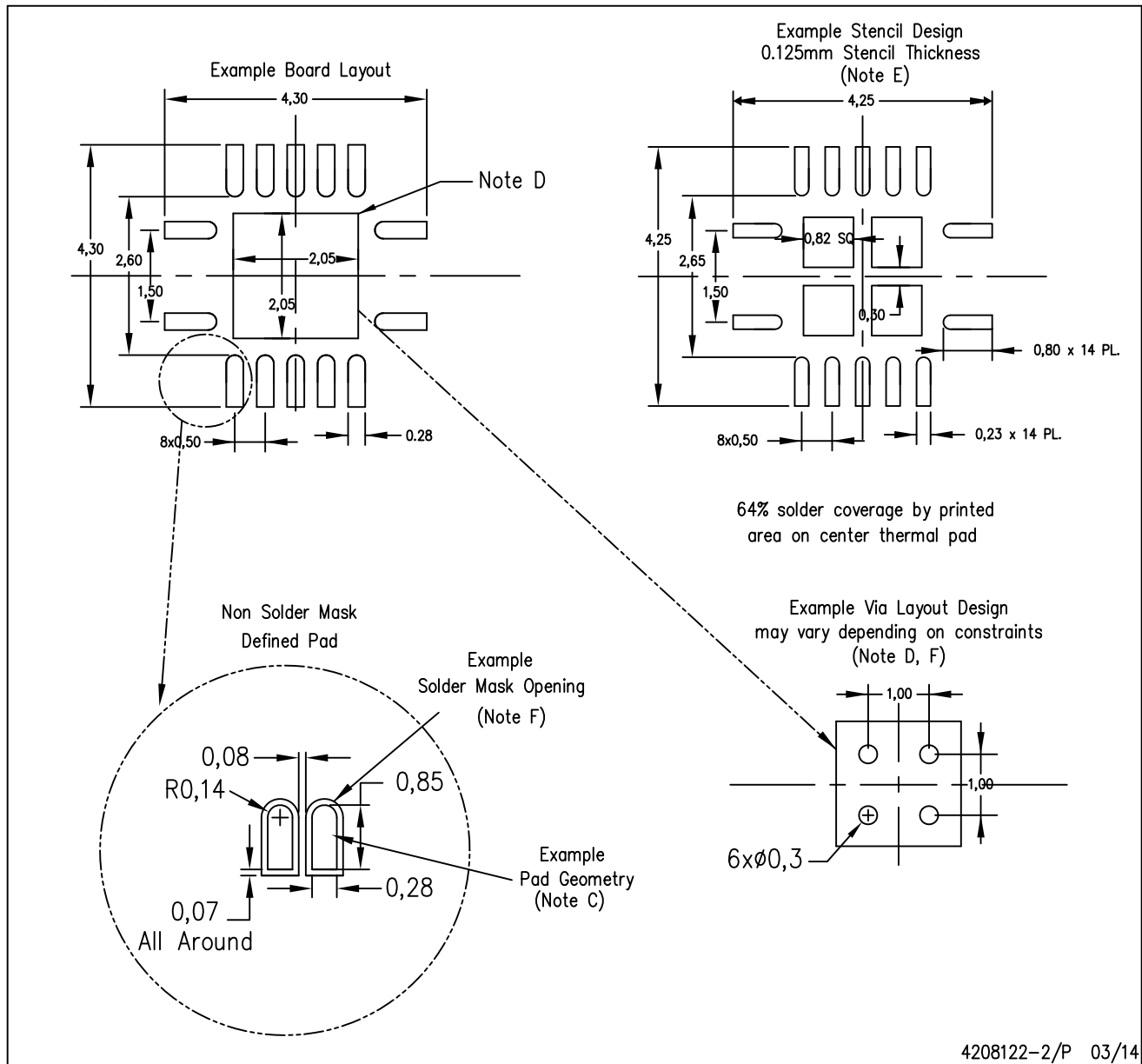
Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## GENERIC PACKAGE VIEW

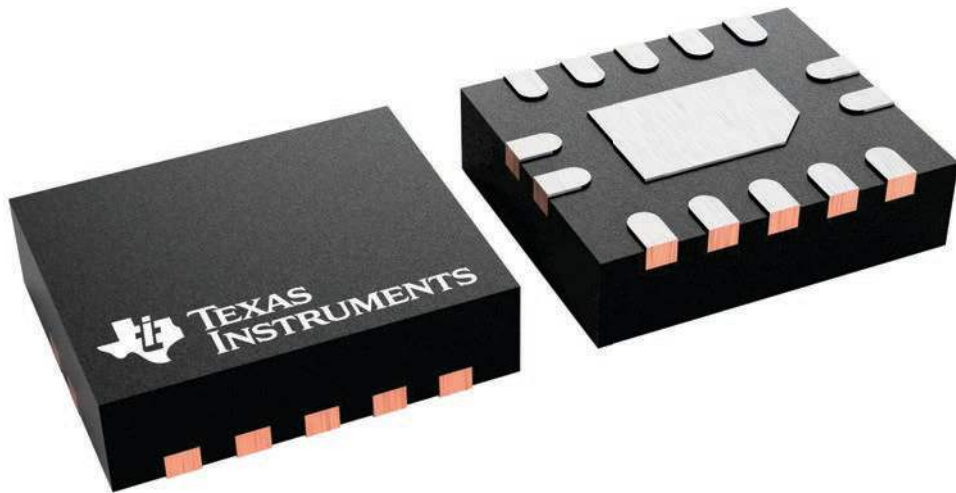
**BQA 14**

**WQFN - 0.8 mm max height**

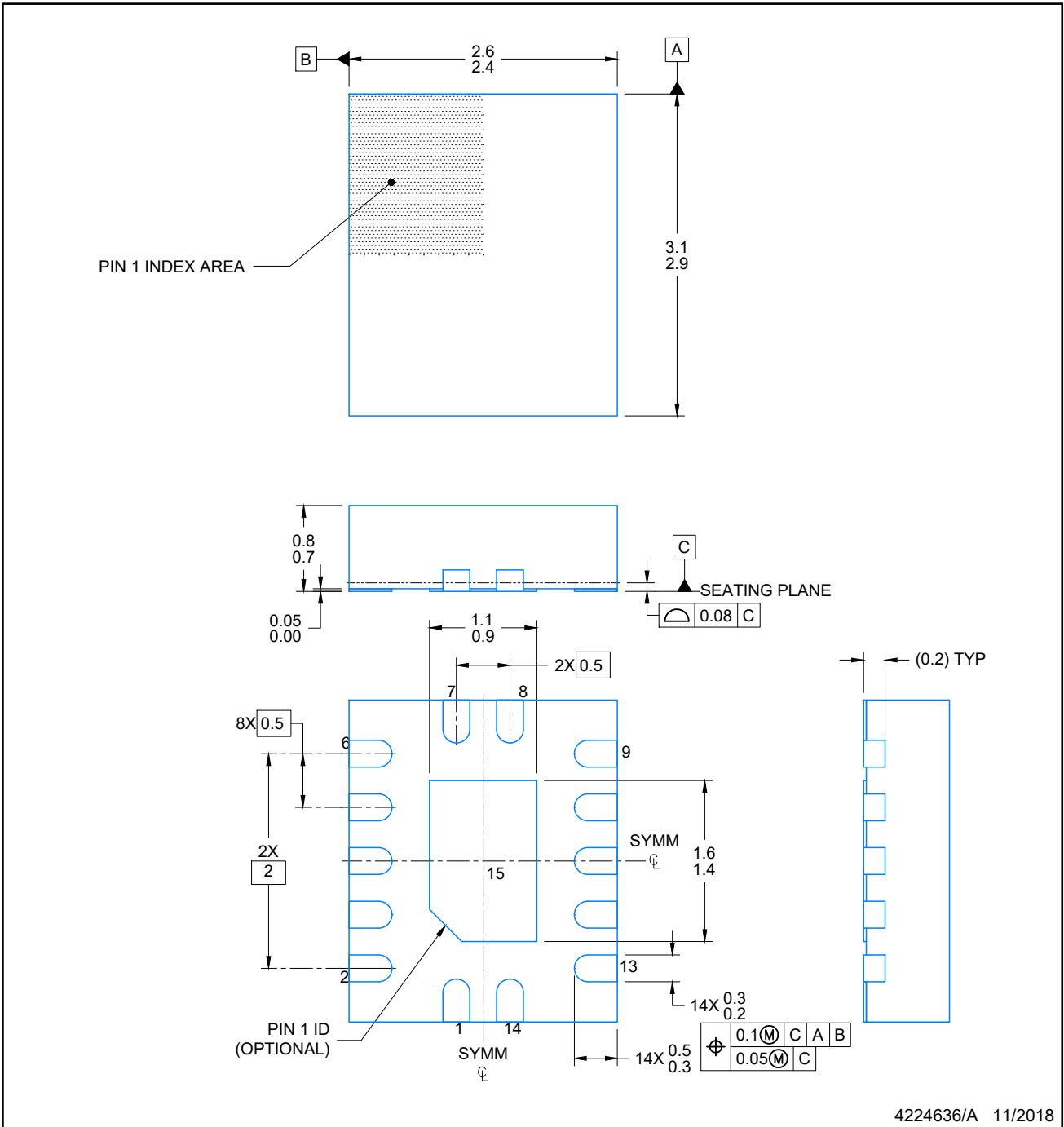
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4227145/A



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

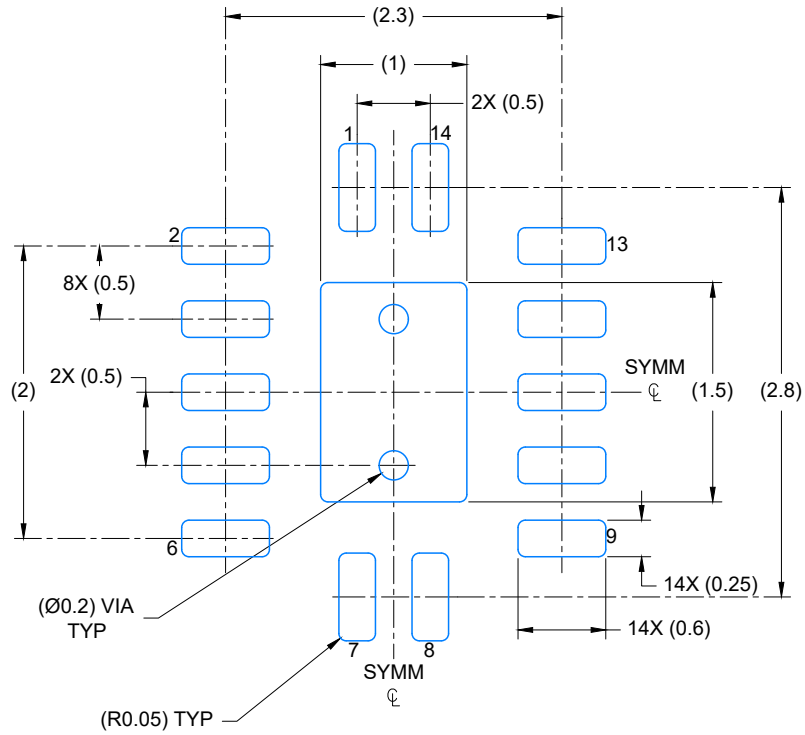


# EXAMPLE BOARD LAYOUT

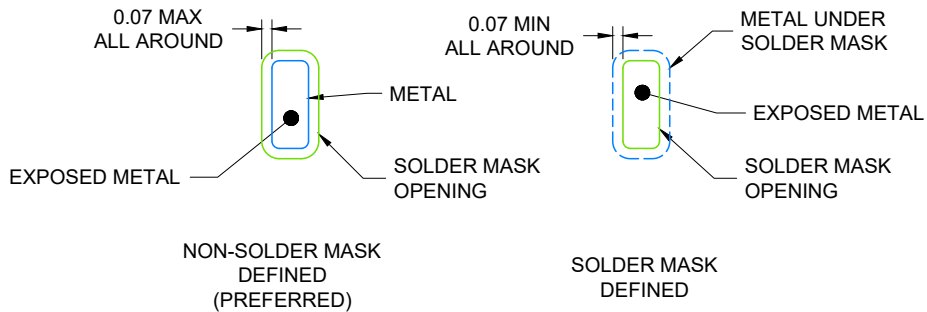
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

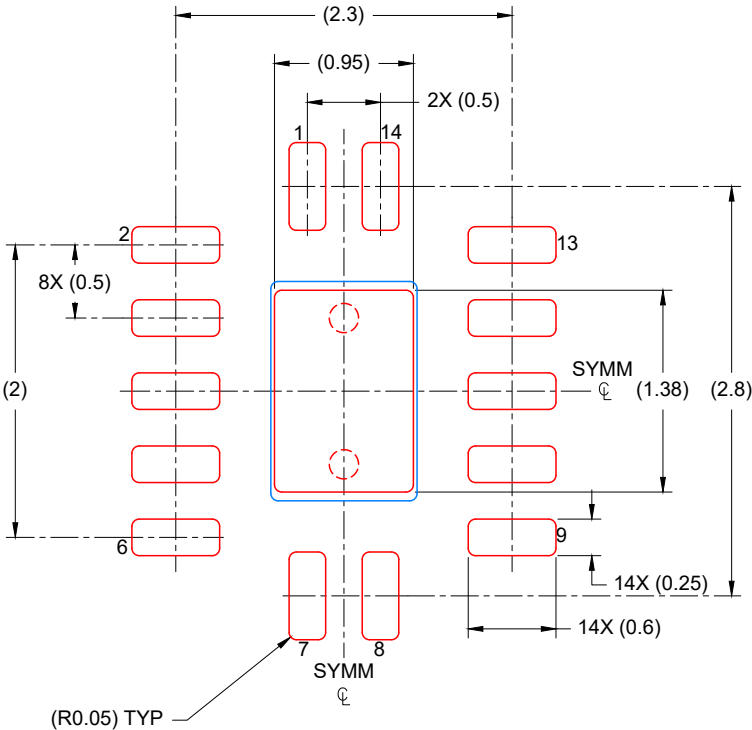
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
88% PRINTED COVERAGE BY AREA  
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

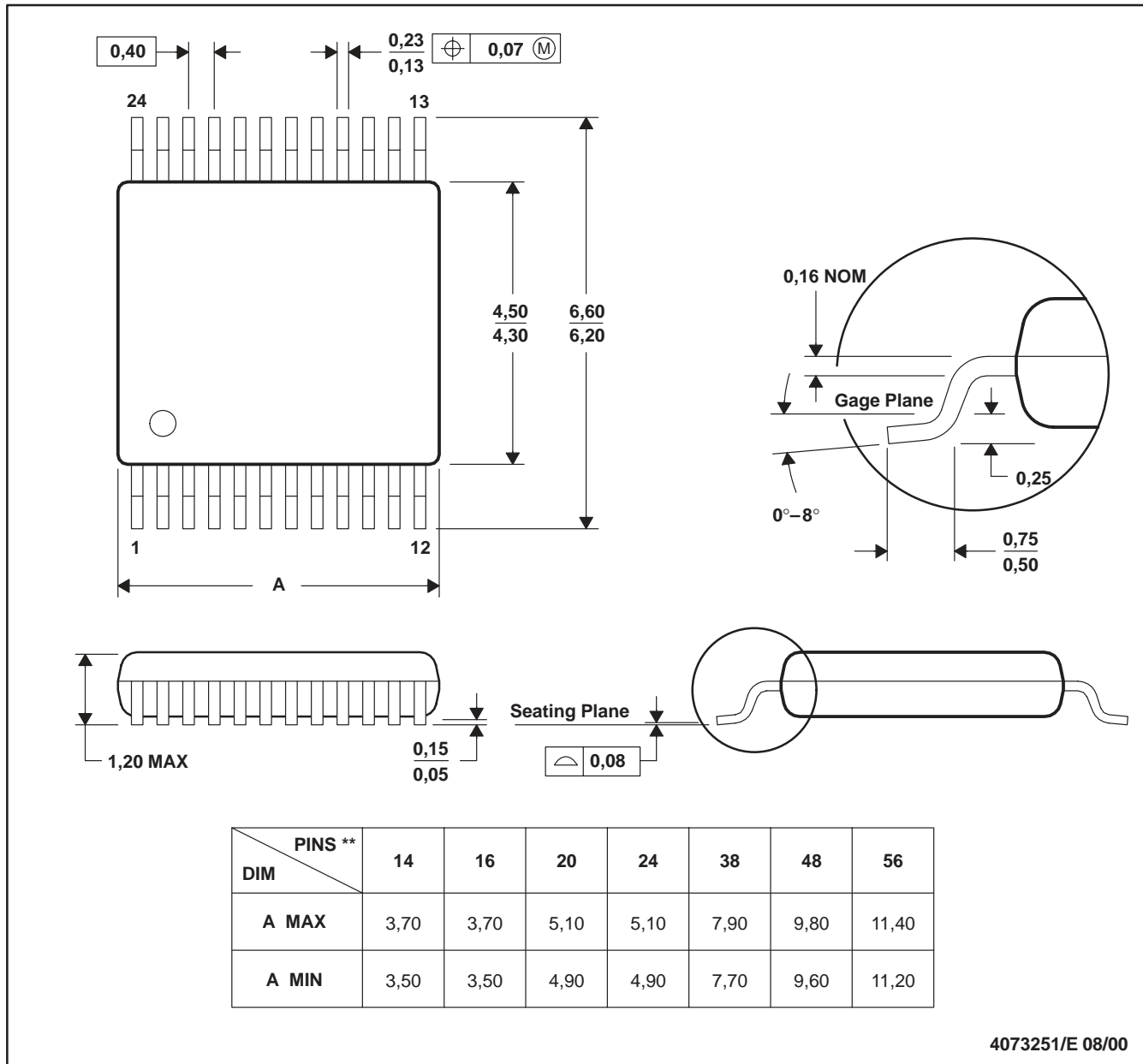


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F14

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## GENERIC PACKAGE VIEW

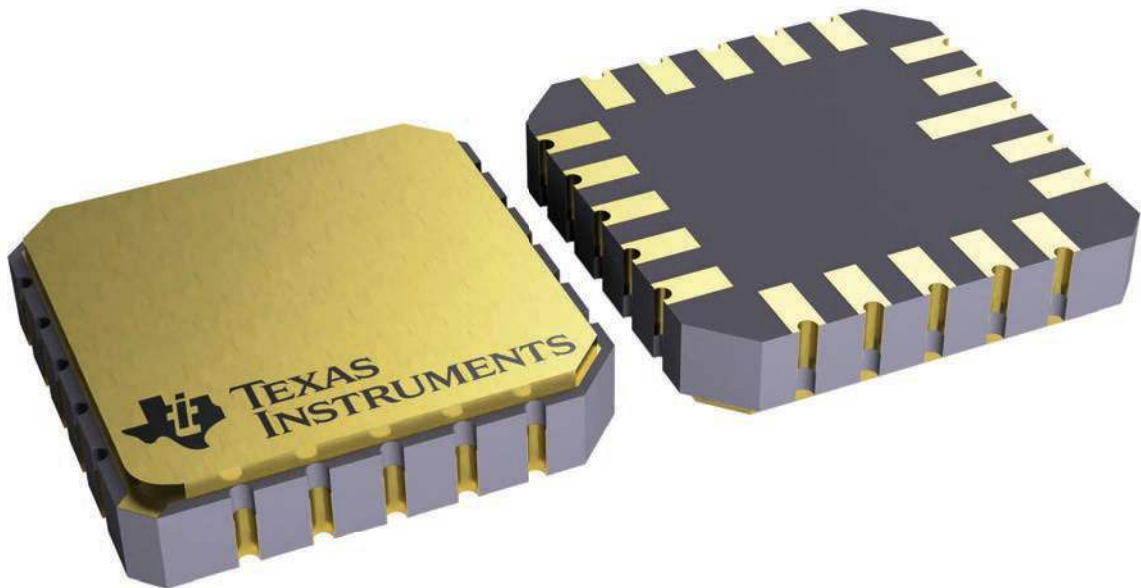
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

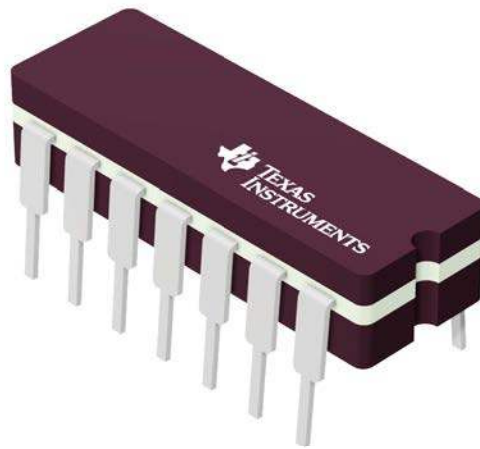
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

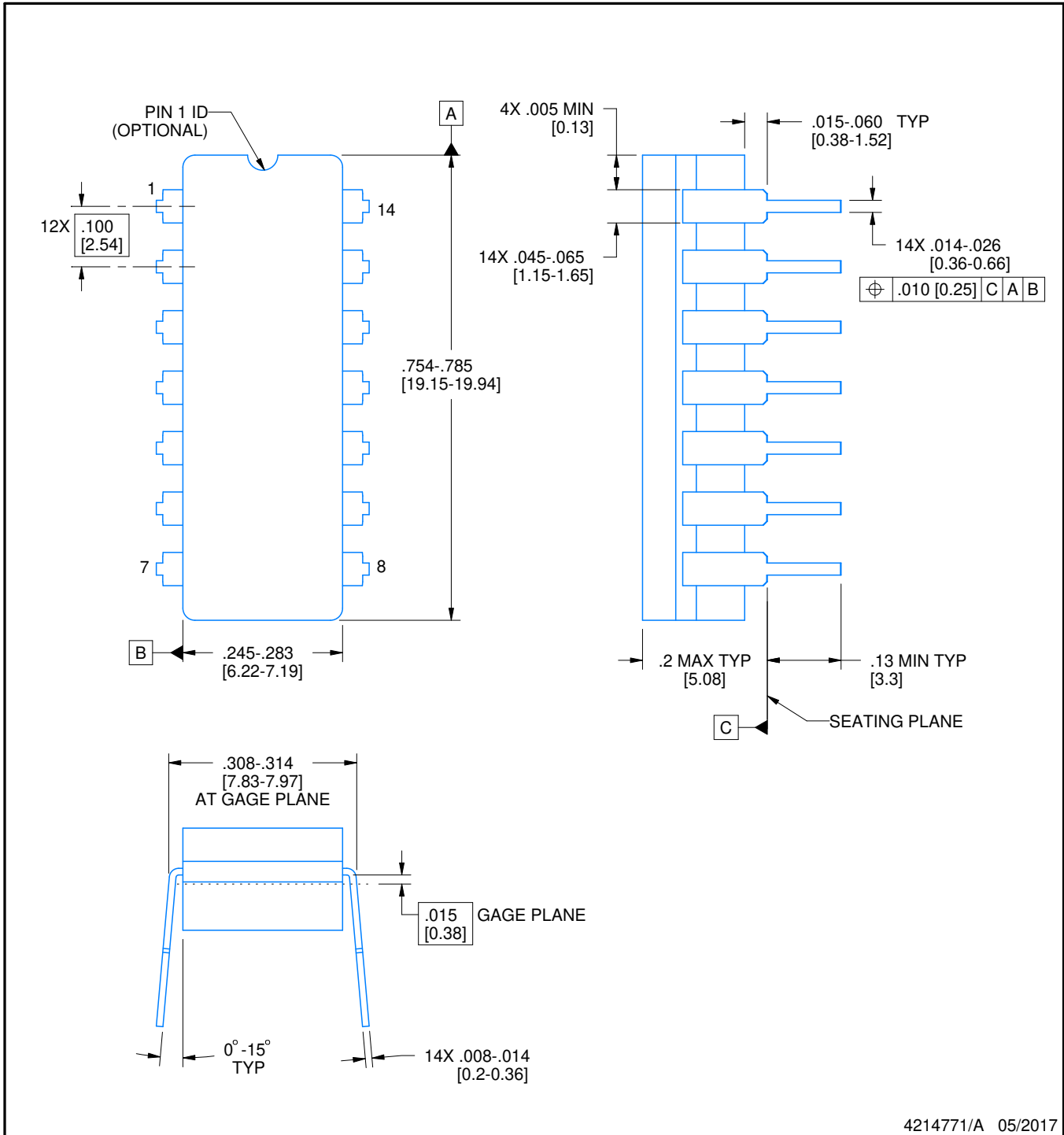
J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

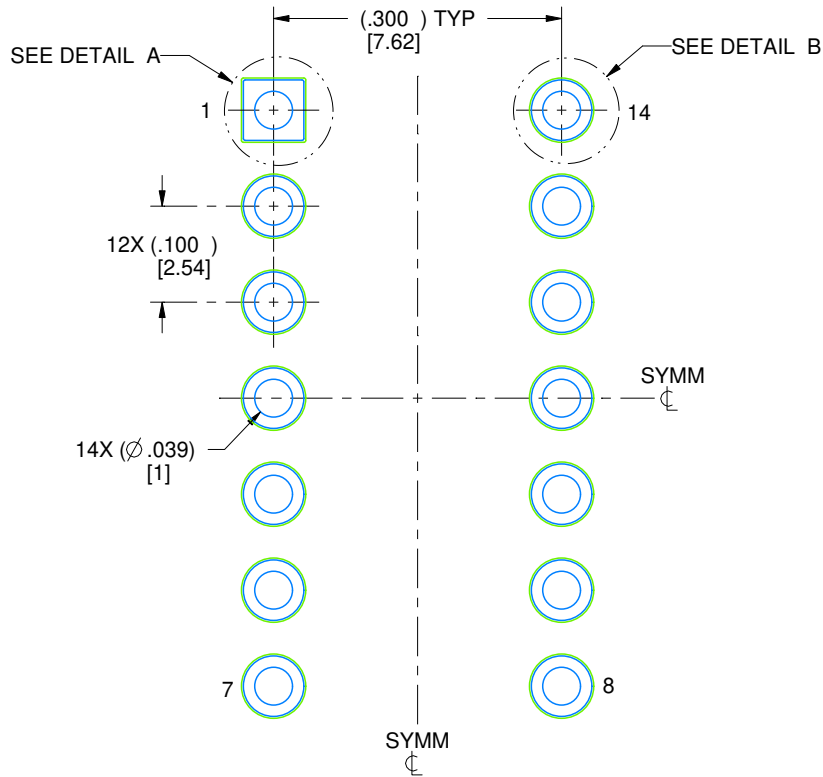


# EXAMPLE BOARD LAYOUT

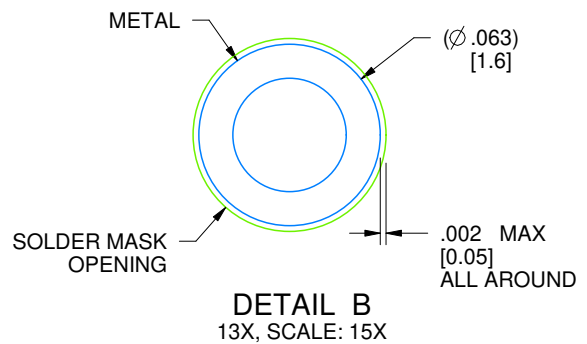
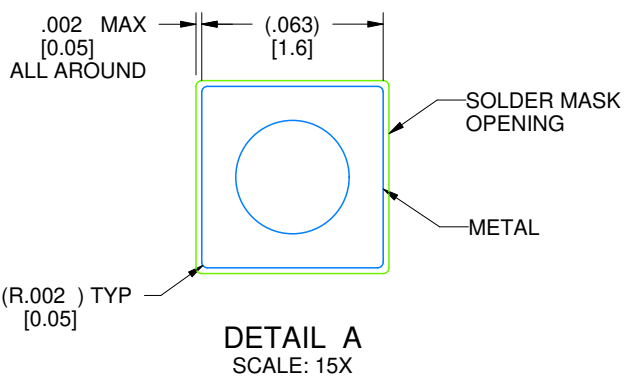
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



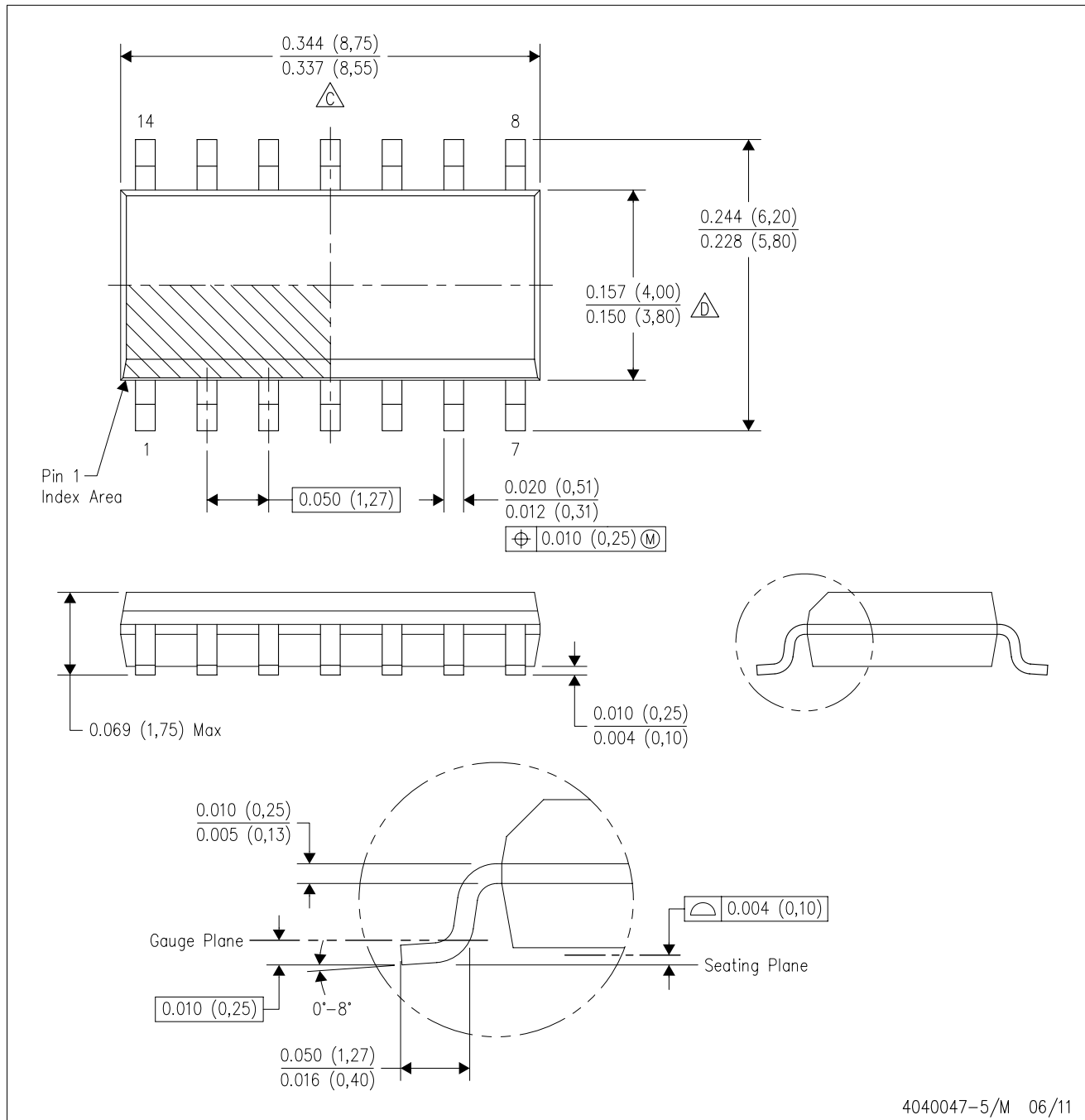
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

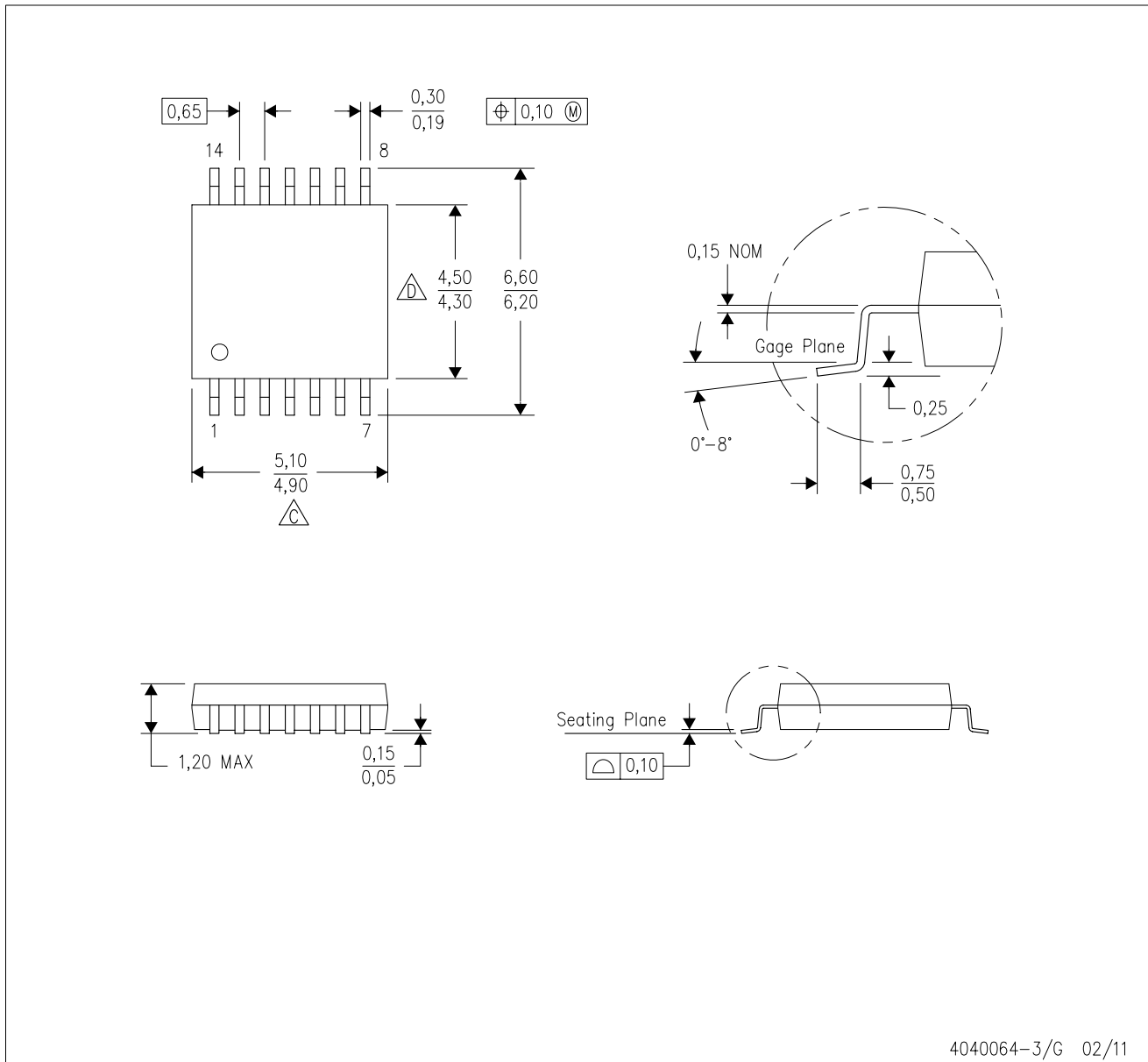
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

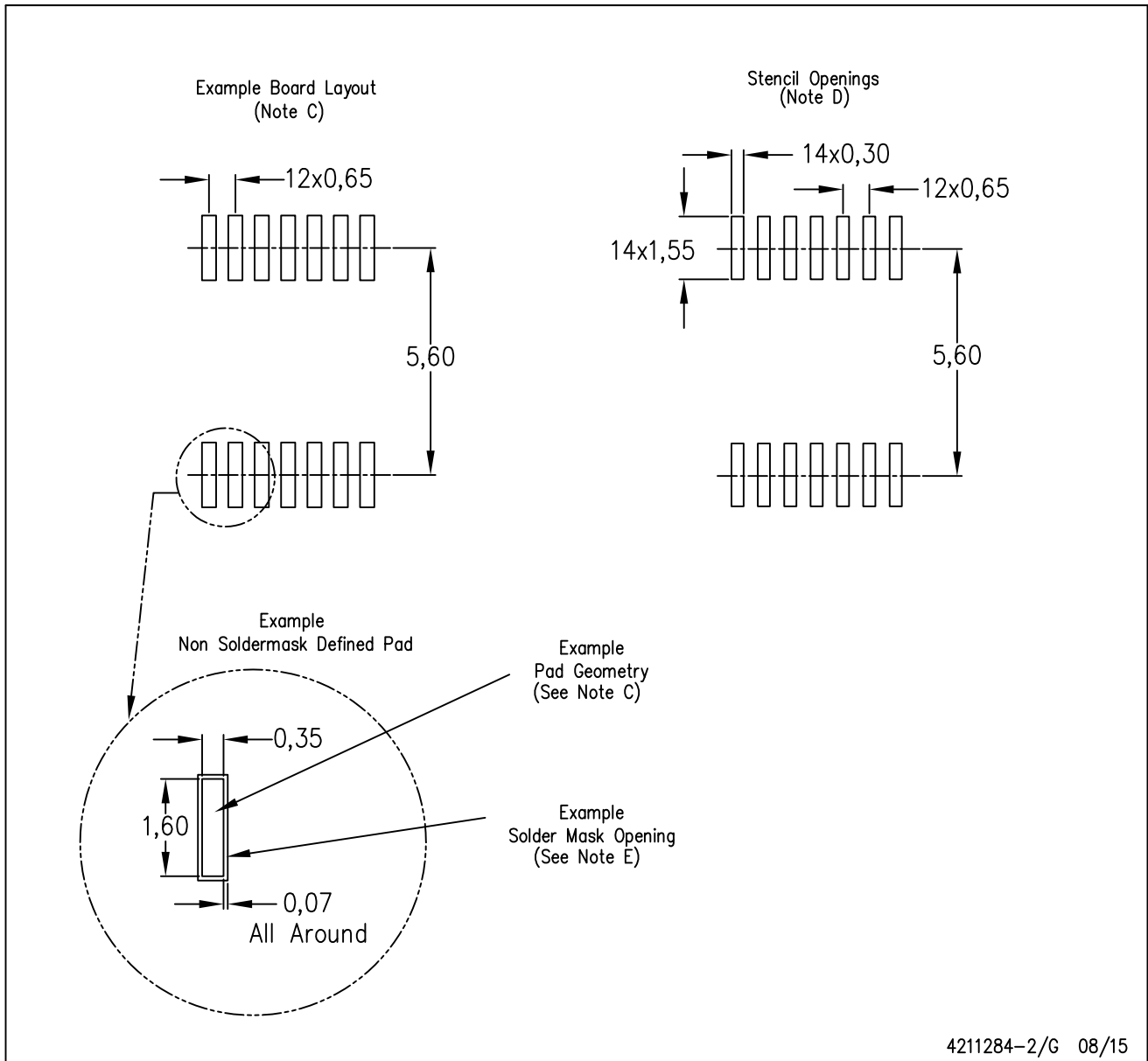
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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