

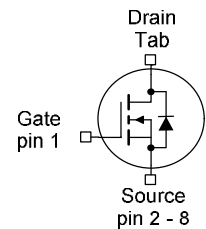
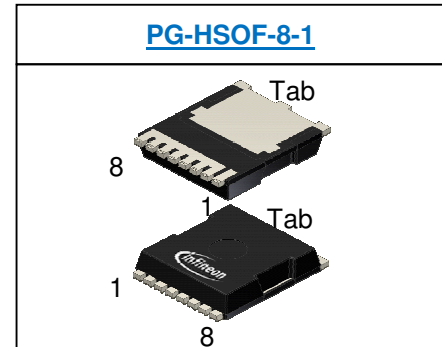
OptiMOS™-5 Power-Transistor

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	80	V
$R_{DS(on)}$	1.1	mΩ
I_D	300	A



Type	Package	Marking
IAUT300N08S5N011	PG-HSOF-8-1	5N08011

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$, Chip limitation ^{1,2)}	410	A
		$V_{GS}=10\text{ V}$, DC current ³⁾	300	
		$T_a=85\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,4)}	52	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$, $t_p=100\text{ }\mu\text{s}$	1505	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=150\text{ A}$	817	mJ
Avalanche current, single pulse	I_{AS}	-	300	A
Gate source voltage	V_{GS}	-	± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	375	W
Operating and storage temperature	T_j , T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}		-	-	0.4	K/W
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}		-	14.8	-	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=275\text{ }\mu\text{A}$	2.2	3	3.8	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=85\text{ °C}^{2)}$	-	1	20	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=6\text{ V}$, $I_D=75\text{ A}$	-	1.3	1.7	m Ω
		$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$	-	1.0	1.1	
Gate resistance ²⁾	R_G	-	-	1.5	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=40\text{ V},$ $f=1\text{ MHz}$	-	12500	16250	pF
Output capacitance	C_{oss}		-	2000	2600	
Reverse transfer capacitance	C_{rss}		-	86	130	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=100\text{ A}, R_G=3.5\ \Omega$	-	31	-	ns
Rise time	t_r		-	19	-	
Turn-off delay time	$t_{d(off)}$		-	69	-	
Fall time	t_f		-	55	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=40\text{ V}, I_D=100\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	56	73	nC
Gate to drain charge	Q_{gd}		-	37	56	
Gate charge total	Q_g		-	178	231	
Gate plateau voltage	$V_{plateau}$		-	4.5	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ °C}$	-	-	300	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25\text{ °C}$	-	-	1505	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=100\text{ A},$ $T_j=25\text{ °C}$	-	0.9	1.2	V
Reverse recovery time ²⁾	t_{rr}	$V_R=40\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	86	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	177	-	nC

¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

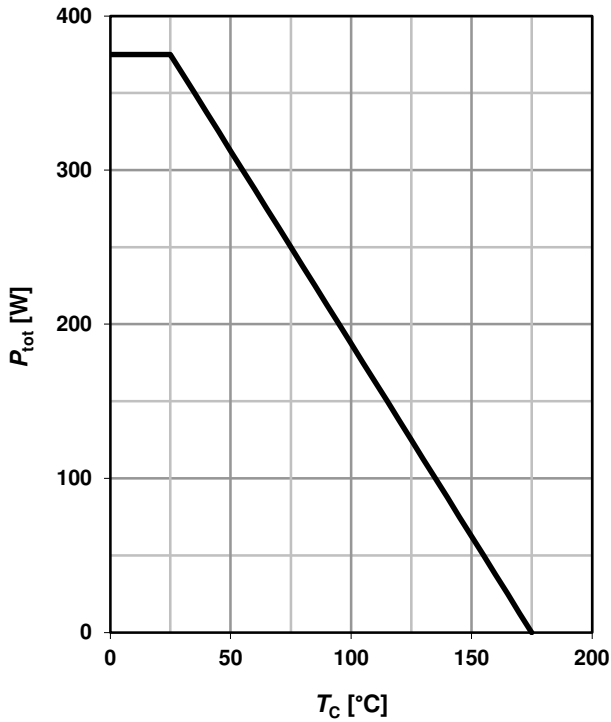
²⁾ The parameter is not subject to production testing – specified by design.

³⁾ Current is limited by the bondwires.

⁴⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

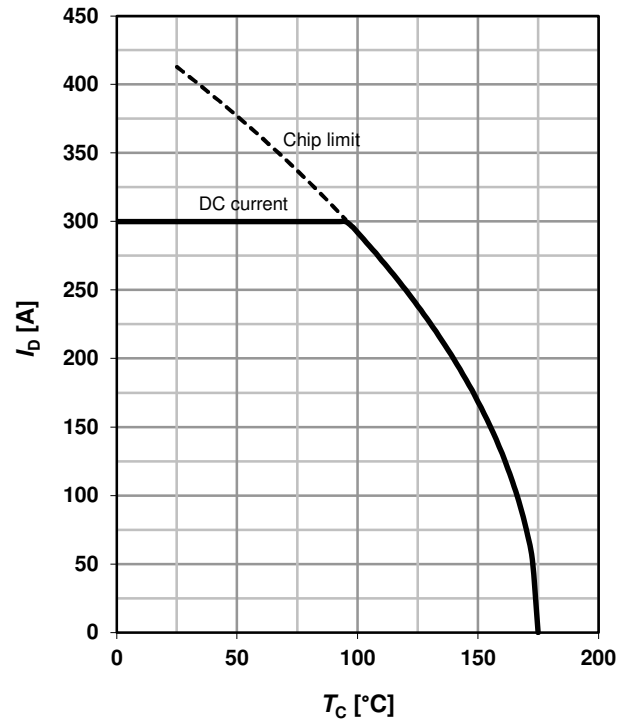
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

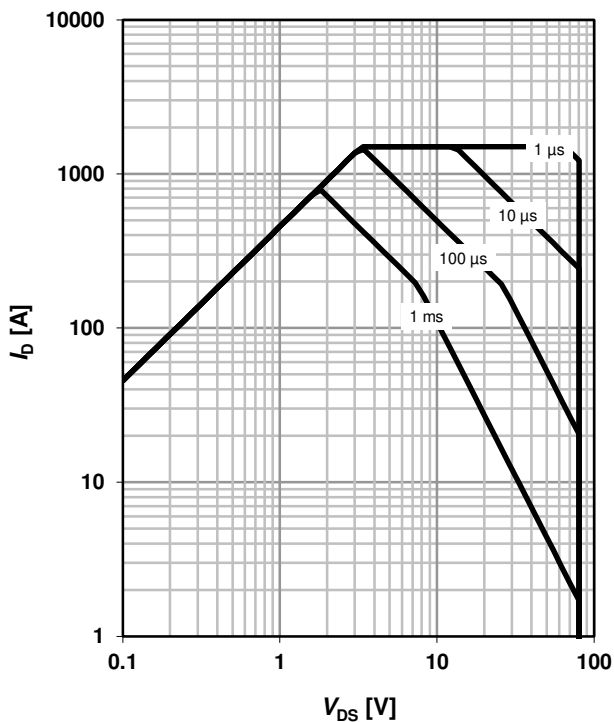
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

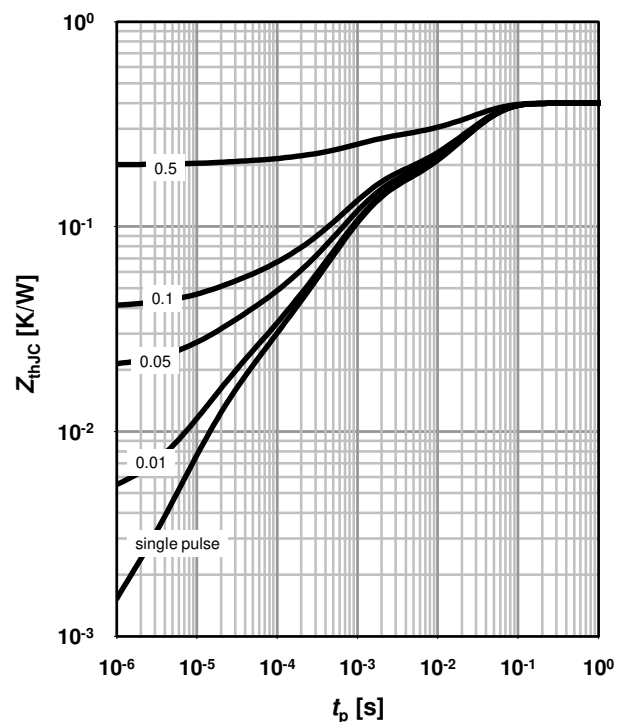
parameter: t_p



4 Max. transient thermal impedance

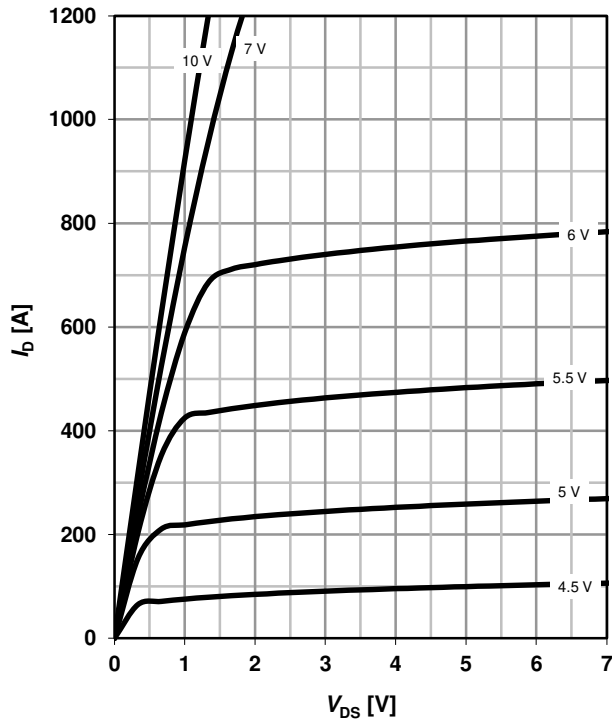
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$

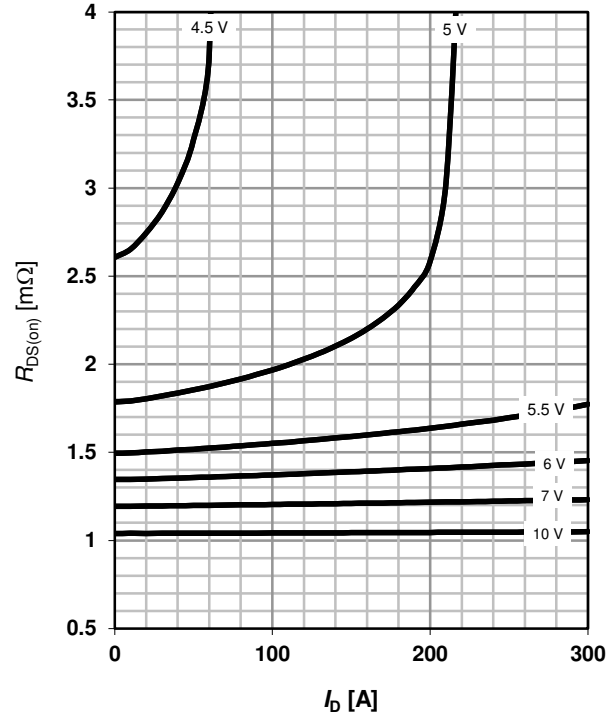


5 Typ. output characteristics

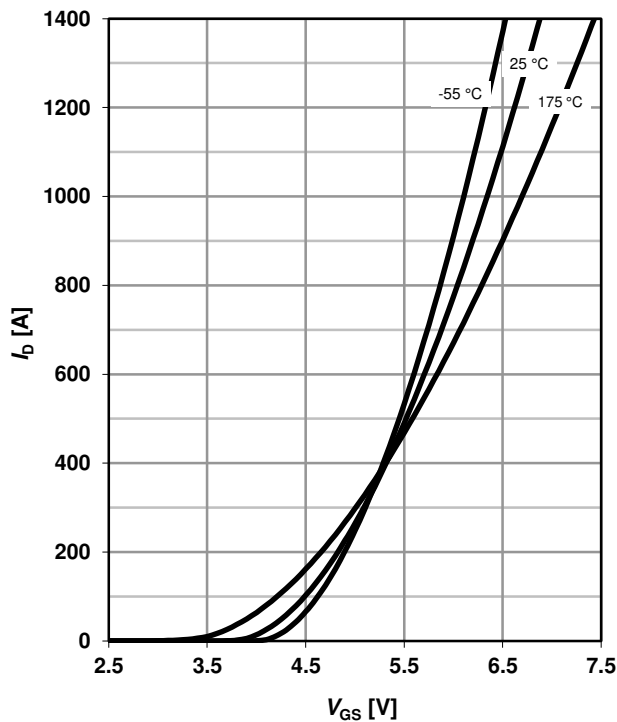
$$I_D = f(V_{DS}); T_j = 25\text{ °C}$$

 parameter: V_{GS}

6 Typ. drain-source on-state resistance

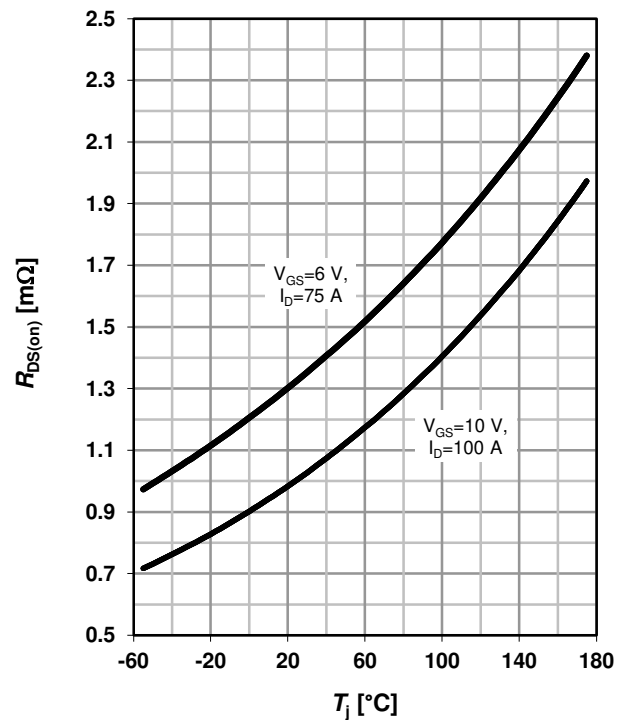
$$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$$

 parameter: V_{GS}

7 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$$

 parameter: T_j

8 Typ. drain-source on-state resistance

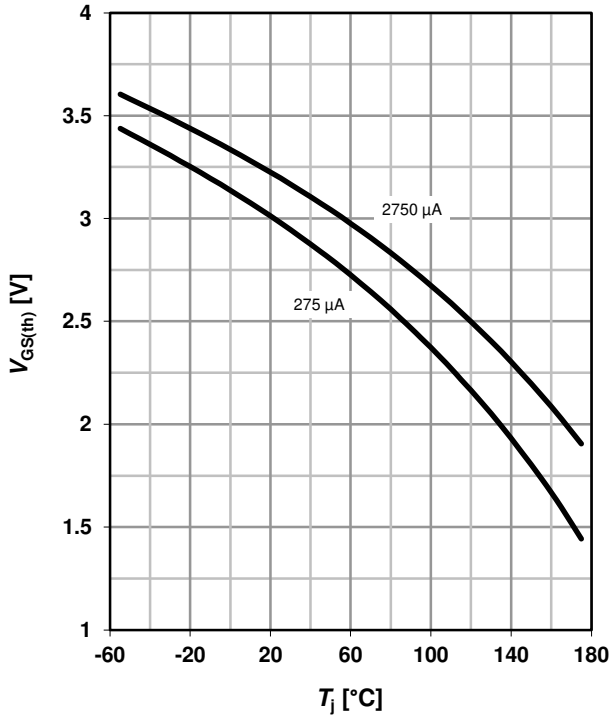
$$R_{DS(on)} = f(T_j)$$

 parameter: I_D, V_{GS}


9 Typ. gate threshold voltage

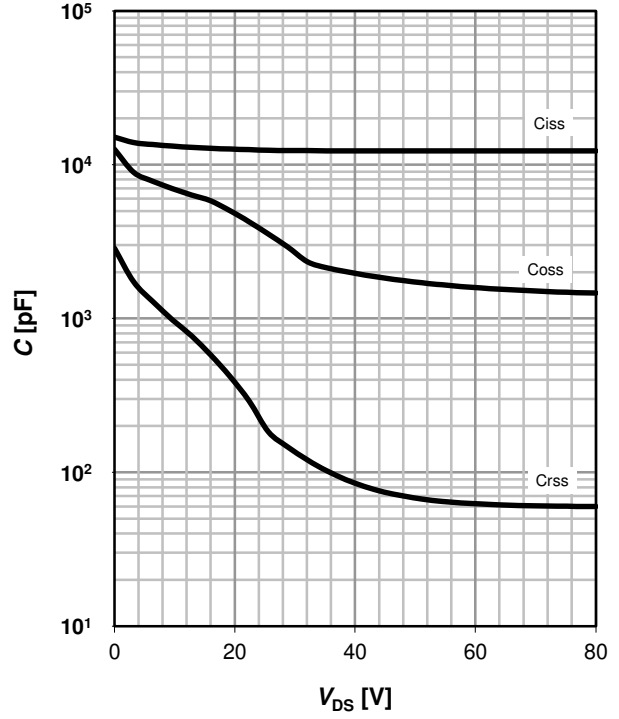
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

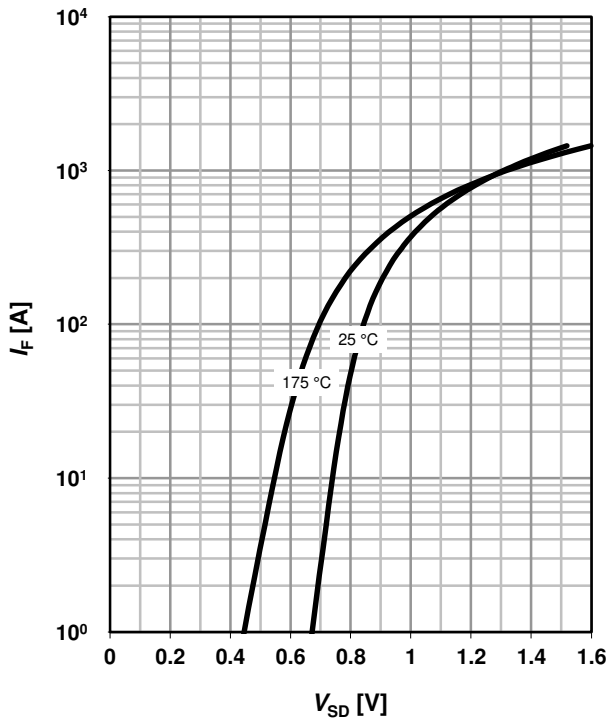
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

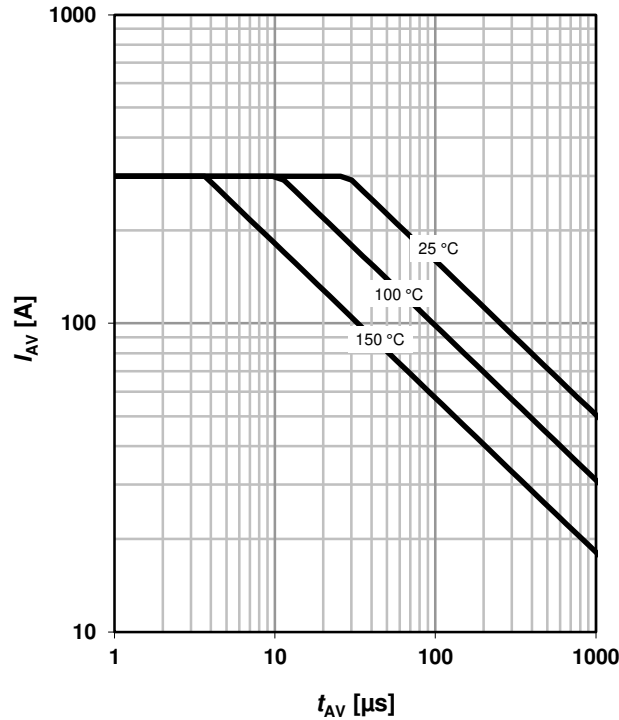
parameter: T_j



12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$

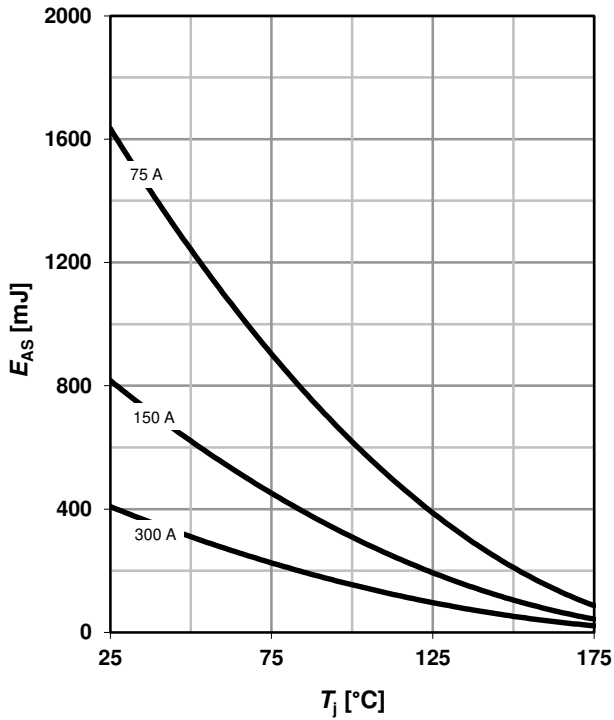
parameter: $T_{j(start)}$



13 Typical avalanche energy

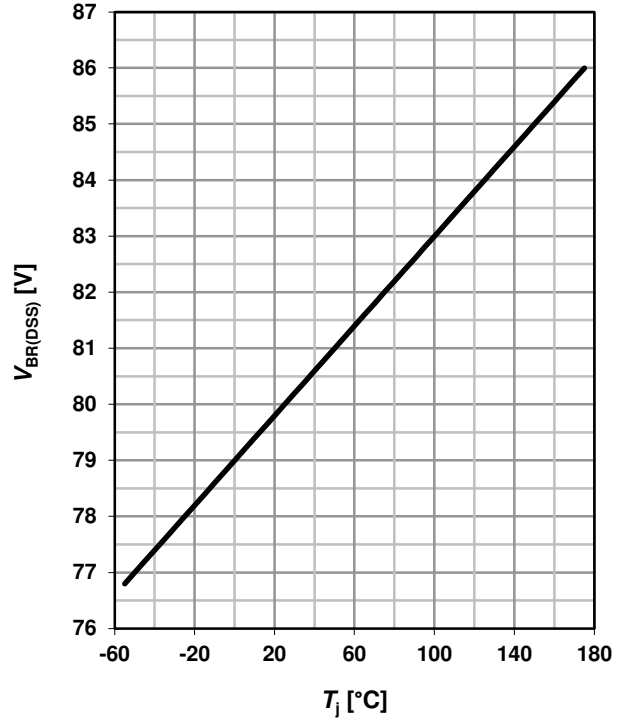
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

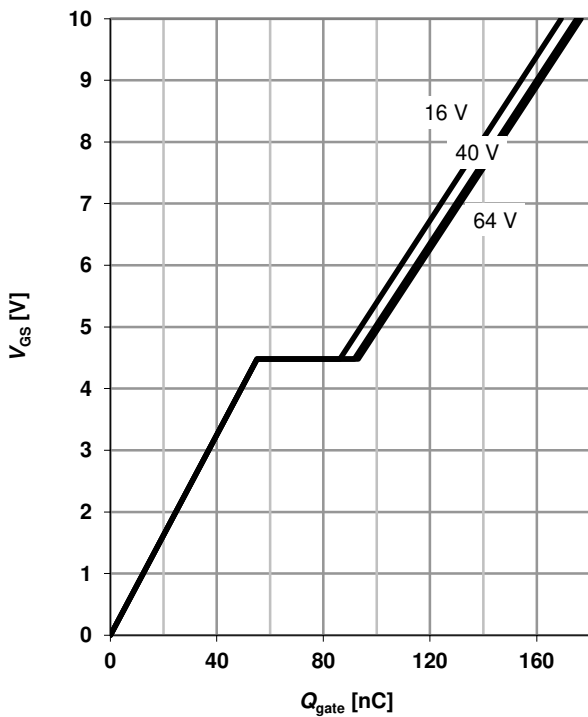
$$V_{BR(DSS)} = f(T_j); I_{D_typ} = 1 \text{ mA}$$



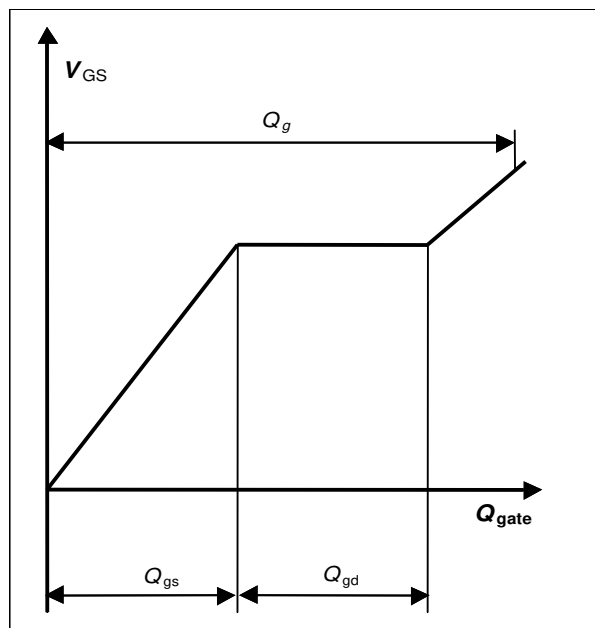
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 100 \text{ A pulsed}$$

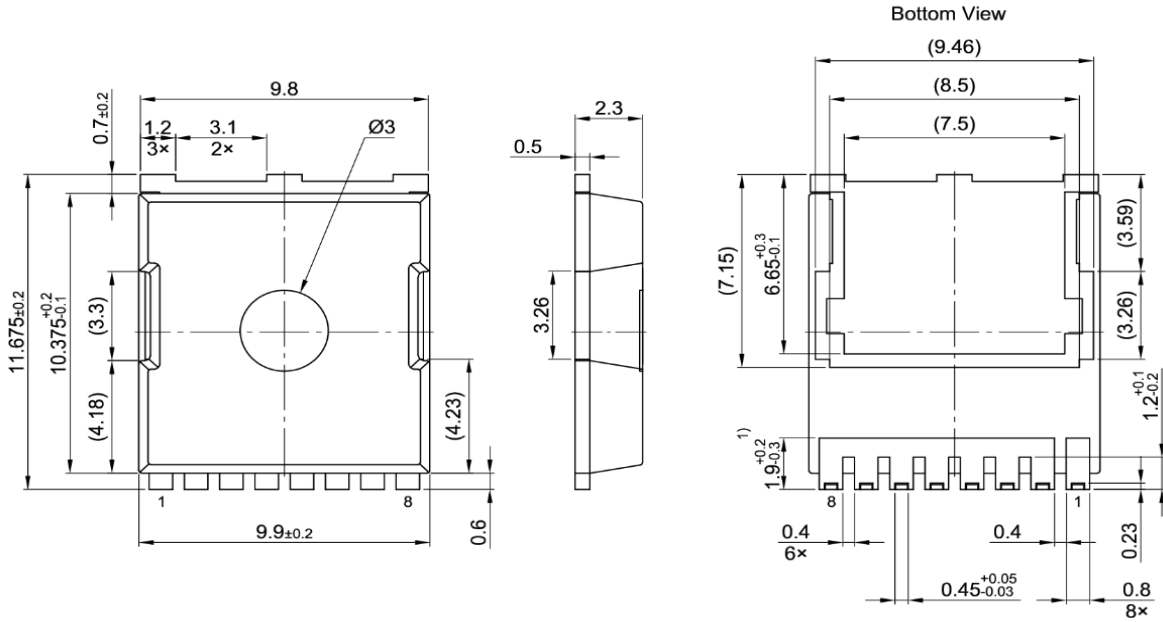
parameter: V_{DD}



16 Gate charge waveforms

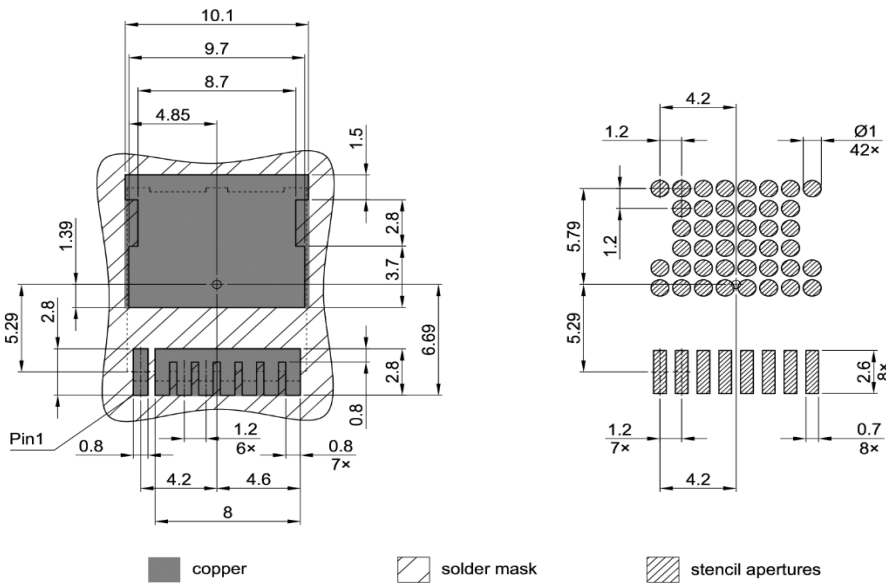


Package Outline



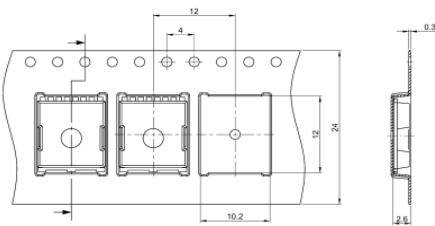
1) Lead length up to anti flash profile; mold flashes excluded
 All dimensions are in units mm
 The drawing is in compliance with ISO 128-30, Projection Method 1 []
 Drawing according to ISO 8015, general tolerances $\pm 0,1; \pm 1^\circ 30'$

Footprint



All pads are solder mask defined
 All dimensions are in units mm

Packaging



All dimensions are in units mm
 The drawing is in compliance with ISO 128-30, Projection Method 1 []

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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Version 1.0	2021-01-19	Final Datasheet
Version 1.1	2021-01-26	Part Marking Info corrected
Version 1.2	2023-02-07	package outline corrected, footprint updated