MODM7AE70

Ethernet Core Module

100 Version with RJ-45 | 200 Version with 10-pin header

NetBurner

DATASHEET

Key Points

- Use as a high-performance single board computer or add Ethernet connectivity to a new or existing design
- Customize with a development kit and begin writing application code immediately!
- Industrial temperature range (-40°C to 85°C)

Device Connectivity

- 10/100Mbps Ethernet with IEEE1588 PTP frames and 802.3az Energy-effecient support
- Up to 2 USARTs, 5 UARTs, 3 I^2C, and 4 SPI
- 11 Analog to Digital (ADC) Inputs
- 1 Digital to Analog (DAC) Output
- 53 digital I/Os
- 16-bit External Bus Interface

Performance and memory

- 32-bit 300 MHz Processor
- 8MB SDRAM and 2MB Flash

Companion development kit

The following is available with the development kit:

- Customize any aspect of operation including web pages, data filtering, or custom network applications
- Development software: NB Eclipse IDE, Graphical debugger, deployment tools, and examples
- Communication software: TCP/IP stack, HTTPS web server, FTP, E-mail, and flash file system
- System software: uC/OS RTOS, ANSI C/C++ compiler and linker
- Security software: Embedded SSL/TLS & SSH libraries

The following optional software modules are not included with kit and are sold separately:

- SNMP

Specifications

Processor and Memory

Microchip® SAM E70 32-bit ARM® Cortex®-M7 processor running at 300 MHz clock speed with 8MB SDRAM, 2MB embedded flash, 384Kb embedded multi-port SRAM, and 1KB embedded low-power backup RAM[1].
Single and double precision hardware Floating Point Unit (FPU), DSP Instructions, Thumb®-2 Instruction Set.

1. While the RAM is usable, it is unsuitable for low-power backup due to the power consumption of the module's components.

Network Interface

10/100 BaseT with RJ-45 connector (100 Version)
10-pin header (200 Version)

Data I/O Interface (P1 and P2)

- Up to 7 Asynchronous Serial Ports: 2 USARTs, 5 Two-wire UARTs
- Up to 53 digital I/O
- Up to 3 Two-Wire Interfaces (TWIHS)(I2C-compatible)
- Up to 4 SPI interface
- SD/MMC flash card ready
- 16-bit external bus interface
- Image Sensor Interface (ISI)
- Quad SPI Interface
- 11 Analog to Digital (ADC) Inputs
- 1 Digital to Analog (DAC) Output

SPI Configurations

The SPI interfaces are available from the following:

- 1 dedicated SPI
- 1 Quad SPI that can be configured to run as a native SPI or QSPI
- 2 from USART0 and USART1 that can be configured as SPI

Serial Configurations

The UARTs can be configured in the following ways:

- USART0/1
- ISO7816
- IrDA®
- RS-422/485
- Manchester

Note: USART0/1 supports SPI. USART1 supports Modem and LON mode.

Additional Peripherals

- Ethernet AVB support with IEEE802.1AS Time-stamping and IEEE802.1Qav credit-based traffic-shaping hardware support.
- Two master Controller Area Networks (MCAN) with Flexible Data Rate (CAN-FD) with SRAM-based mailboxes, time- and event-triggered transmission.
- Serial Synchronous Controller (SSC) with I2S and TDM support.
- High-speed Multimedia Card Interface (HSMCI) (SDIO/SD Card/e.MMC)
- Nine 16-bit Timer/Counters, can be chained to create 32 bit and 48 bit timer/counters. Functions include capture, compare, interrupt generation, frequency measurement, event counting, interval measurement, quadrature decoder, pulse generation, waveform generation, synchronization with PWM peripheral, delay timing pulse width modulation, 2-bit Gray Up/Down Counter for stepper motor control. Each channel has

three external clock inputs, five internal clock inputs and two multi-purpose input/output signals.[1]

- 12-bit 1Msps-per-channel Digital-to-Analog Controller (DAC) with differential and oversampling modes.
- One Analog Comparator (ACC) with flexible input selection, selectable input hysteresis.
- Watchdog Timer
- Three Two-Wire Interfaces (TWIHS) (I2C-compatible). Two-wire bus, made up of one clock line and one data line with speeds of up to 400 kbps in Fast mode, and up to 3.4 Mbps in High-speed slave mode. Easily interface to EEPROM and I^2C-compatible devices, such as a Real-Time Clock (RTC), Dot Matrix/Graphic LCD Controller
- Dedicated SPI. Note that USARTs 0 and 1 can also be used as SPI interfaces, as can the Quad SPI when in single bit mode.
- Seventeen 16-bit PWMs with complementary outputs, Dead Time Generator, fault inputs motor control and an external trigger.
- Two Analog Front-End Controllers (AFEC). The AFEC is based on an Analog Front-End cell (AFE) integrating a 12-bit Analog-to-Digital Converter (ADC), a Programmable Gain Amplifier (PGA), a Digital-to-Analog Converter (DAC) and two 6-to-1 analog multiplexers, making possible the conversions of 12 analog lines or two simultaneous conversions of 6 analog lines. The AFEC supports a 12-bit resolution mode which can be extended up to a 16-bit resolution by digital averaging. Up to 2Msps conversion rate. Automatic correction of gain and offset errors.
- Parallel Capture Interface consisting of clock, data and enable signals to continuously read data from peripherals such as a CMOS digital image sensor, a high-speed parallel ADC, a DSP synchronous port in synchronous mode, etc.
- Up to 53 GPIO lines. Each has several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Each GPIO line also has an on-die serial resistor for impedance matching, reducing overshoot, undershoot and EMI.
- Temperature sensor internal to processor.

LEDs

Link and Speed (100 Version only, on RJ-45)

Physical Characteristics

Dimensions (inches): 2.60" x 2.00"
Weight: 1 oz.
Mounting Holes: 2 x 0.125" dia.

Power

DC Input Voltage: 3.3V @ 100mA typical, 250mA max
Low power modes are able to reduce power draw, with consumption dependant on enabled peripherals.

Environmental Operating Temperature

-40° to 85° C

RoHS Compliance

The Restriction of Hazardous Substances guidelines ensure that electronics are manufactured with fewer environment harming materials.

1 Some timer I/O is unavailable due to SDRAM and Ethernet interfaces. Please consult the pinout for further details.

Part Numbers

MODM7AE70 Ethernet Core Module (100 Version, with RJ-45)
Part Number: MODM7AE70-100IR

MODM7AE70 Ethernet Core Module (200 Version, with 10-pin header)
Part Number: MODM7AE70-200IR

MOD7AE70 LC Development Kit
Part Number: NNDK-MODM7AE70LC-KIT
Kit includes all the hardware and software you need to customize the included platform hardware. See NetBurner Store product page for package contents. Note: Includes the MOD-DEV-70 development board.

SNMP V1 (Module License Version)
Part Number: NBLIC-SNMP
Available as an option if you are using a development kit.

Ordering Information

E-mail: sales@netburner.com
Online Store: www.NetBurner.com
Telephone: 1-800-695-6828

Pinout and Signal Description

The 200 version board has a 10-pin header instead of an RJ-45 jack. This header enables you to relocate the jack to another location or to add a different jack with power over ethernet (PoE) capabilities to your module. Table 1 provides descriptions of the pin functions of the 10-pin header.

Refer to the application note, "Adding an External Ethernet RJ-45 Connector and PCB Layout Guidlines for NetBurner -200 Version Modules", for details and examples.

Table 1: Pinout and Signal Descriptions for Ethernet Connector [1]

Pin	Signal	Description
1	TX-	Transmit -
2	TX+	Transmit +
3	TXCT[1]	Transmit Data Center Tap
4	RX+	Receive +
5	RX-	Receive -
6	RXCT[1]	Receive Data Center Tap
7	GND	Ground
8	N/C	Not Connected
9	LED	LED control sink, link/activity
10	LED	LED control sink, speed

Note:
1. Ethernet magnetics center tap voltage provided by NetBurner device.

The module has two dual in-line 50 pin headers which enable you to connect to one of our standard NetBurner Carrier Boards, or a board you create on your own. Table 2-3 provides descriptions of pin function of the module header. Most pins have a Primary and Alternate function. In the Primary function mode you can select one of up to four peripheral functions, A through D.

Table 2: Pinout and Signal Descriptions for P1 Connector [(1)]

P1 Connector					
Pin	Port	GPIO	Peripheral A Peripheral C	Peripheral B Peripheral D	Alternate
1	GND				
2	GND				
3	VCC_3V				
4	PC8	X	Lower Byte Write Access (NWR0) / Write Enable (NWE)	Timer 7 Line A (TIOA7)	
5[1]	PA22	X	SSC Receive Clock (100K pull-up at reset)(RK) Bus Chip Select 2 (NCS2)	PWM 0 External Trigger (PWMC0_PWMEXTRG1)	Parallel Capture Clock Input (PIODCCLK)[1]
6[1]	PC14	X	Bus Chip Select 0 (NCS0) CAN 1 Transmit (CANTX1)	Timer 8 Clock (TCLK8)	
7[1]	PD19	X	Bus Chip Select 3 (NCS3) Serial Port 6 TX (UTXD4)[5]		
8[1]	PC11	X	Read Signal (NRD)	Timer 8 Line A (TIOA8)	
9	PD15		NWR1/NBS1		
10	PA20		A16/BA0		
11					Transfer in Progress (TIP) footnote[2]
12	PC0		D0		
13	PC13	X	External Wait Signal (NWAIT)	PWM 0 Channel 3 Output High (PWMC0_PWMH3)	AFE 1 ADC Input 1 (AFE1_AD1)[3]
14	PC2		D2		
15	PC1		D1		
16	PC4		D4		

Note:

1. When the External Bus Interface (EBI) peripheral is enabled, this signal is locked to EBI functionality. Trying to use this signal while it is in use by the EBI peripheral can damage the module.

P1 Connector					
Pin	Port	GPIO	Peripheral A Peripheral C	Peripheral B Peripheral D	Alternate
17	PC3		D3		
18	PC6		D6		
19	PC5		D5		
20	PE0		D8		
21	PC7		D7		
22	PE2		D10		
23	PE1		D9		
24	PE4		D12		
25	PE3		D11		
26	PA15		D14		
27	PE5		D13		
28	NRST				
29	PA16		D15		
30	NRST				
31	PA6	X	Serial Port 3 TX (UTXD1)[5]	Programmable Clock Channel 0 Output (PCK0)	
32	PC18		A0/NBS0		
33	PC19	X	A1	PWM 0 Channel 2 Output High (PWMC0_PWMH2)	
34	PC20		A2		

P1 Connector					
Pin	Port	GPIO	Peripheral A Peripheral C	Peripheral B Peripheral D	Alternate
35	PC21		A3		
36	PC22		A4		
37	PC23		A5		
38	PC24		A6		
39	PC25		A7		
40	PC26		A8		
41	PC27		A9		
42	PC28		A10		
43	PC29		A11		
44	PC30	X	A12	Timer 5 Line B (TIOB5)	AFE 1 ADC Input 5 (AFE1_AD5)(5)[3]
45	PC31		A13		
46	PA18		A14		
47	PA19	X	A15	PWM 0 Channel 0 Output Low (PWMC0_PWML0) Sound Controller 1 Master Clock (I2SC1_MCK)	AFE 0 ADC Input 8 (AFE0_AD8) Wakeup Pin 9 (WKUP9)[4]
48	VCC_V3				
49	GND				
50	GND				

Note:

1. To select this extra function, refer to Section 32.5.14 “Parallel Capture Mode”.
2. Logical AND of PA.22, PC.14, PD.19. Typically used to control the enable of an external data bus buffer.
3. To select this extra function, refer to Section 50.5.1 “I/O Lines”.
4. Analog input has priority over WKUPx pin. To select the analog input, refer to Section 50.5.1 “I/O Lines”. WKUPx can be used if the PIO controller defines the I/O line as “input”.
5. See Table 5 for Serial Port to USART/UART mapping.

Table 3: Pinout and Signal Descriptions for P2 Connector [1]

P2 Connector					
Pin	Port	GPIO	Peripheral A	Peripheral B	Alternate
			Peripheral C	Peripheral D	
1	GND				
2	VCC_3V				
3	PB0	X	PWM 0 Channel 0 Output High (PWMC0_PWMH0)		AFE 0 ADC Input 10 (AFE0_AD10)
			Serial Port 0 RX (RXD0)[10]	SSC Transmit Frame Sync (TF)	RTCOUT0
4	PB1	X	PWM 0 Channel 1 Output High (PWMC0_PWMH1)	TSU Timer Comparison Valid 1588 (GTSUCOMP)	AFE 1 ADC Input 0 (AFE1_AD0)
			Serial Port 0 TX (TXD0)[10]	SSC Transmit Clock (TK)	RTCOUT1
5	VREFP		ADC Voltage Reference		
6	PC12	X		Timer 8 Line B (TIOB8)	AFE 1 ADC Input 3 (AFE1_AD3)[5]
			CAN 1 Receive (CANRX1)		
7	PD30	X	Serial Port 5 TX (UTXD3)[10]		AFE 0 ADC Input 0 (AFE0_AD0)[5]
				Image Sensor Data Input 10 (ISI_D10)	
8	PA17	X	QSPI Data 2 Quad Mode (QI2)	Programmable Clock Output 1 (PCK1)	AFE 0 ADC Input 6 (AFE0_AD6)[5]
			PWM 0 Chan 3 Output High (PWMC0_PWMH3)		
9	PA2	X	PWM 0 Channel 1 Output High (PWMC0_PWMH1)		Wakeup Pin 2 (WKUP2)[1]
			DAC Trigger Input (DATRG)		
10	PD18	X			
			Serial Port 6 RX (URXD4)[10]		
11	PB13	X	PWM 0 Channel 2 Output Low (PWMC0_PWML2)	Programmable Clock Output 0 (PCK0)	DAC Channel 0 Output (DAC0)[7]
			Serial Port 0 Serial Clock (SCK0)		
12	PA5	X	PWM 1 Channel 3 Output Low (PWMC1_PWML3)	Image Sensor Channel 4 Data Input (ISI_D4)	Wakeup Pin 4 (WKUP4)
			Serial Port 3 RX (URXD1)[10]		Parallel Capture Data 2 (PIODC2)
	PB5		Two-Wire (I2C) 1 Clock (TWCK1)	PWM 0 Channel 0 Output Low (PWMC0_PWML0)	Test Data Out (TDO/TRACESWO)(9)
				SSC Transmit Data (TD)	Wakeup Pin 13 (WKUP13)
13	PA8	X	PWM1 Channel 3 Output High (PWMC1_PWMH3)	AFE 0 ADC External Trigger (AFE0_ADTRG)	Slock Clock Osc Output (XOUT32)[4]
14	GND				
15	PD24	X	PWM 0 Channel 0 Output Low (PWMC0_PWML0)	SSC Receive Frame sync (RF)	
			Timer 11 Clock Input (TCLK11)	Image Sensor Horizontal Sync (ISI_HSYNC)	
16	PA28	X	Serial Port 1 DSR (100K pull-up at reset)(DSR1)[10]	Timer 1 Clock (TCLK1)	
			Multimedia Card Slot A Data Command (MCCDA)	PWM 1 Fault Input 2 (PWMC1_PWMFI2)	
17	PA26	X	Serial Port 1 DCD (100K pull-up at reset)(DCD1)[10]	Timer 2 Line A (TIOA2)	
			Multimedia Card Slot A Data 2 (MCDA2)	PWM 1 Fault Input 1 (PWMC1_PWMFI1)	

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P2 Connector					
Pin	Port	GPIO	Peripheral A Peripheral C	Peripheral B Peripheral D	Alternate
18	PA27	X	Serial Port 1 DTR (100K pull-up at reset)(DTR1)[10] Multimedia Card Slot A Data 3 (MCDA3)	Timer 2 Line B (TIOB2) Image Sensor Data Input 7 (ISI_D7)	
19	PA1	X	PWM 0 Channel 0 Output Low (PWMC0_PWML0) A18	Timer 0 Line B (TIOB0) Sound Controller 0 Serial Clock (I2SC0_CK)	Wakeup Pin 1 (WKUP1)[1]
20	PA29	X	Serial Port 1 RI (100K pull-up at reset)(RI1)[10]	Timer 2 Clock (TCLK2)	
21	PA21	X	Serial Port 1 RX (RXD1)[10] PWM 1 Chan 0 Fault Input (PWMC1_PWMFI0)	Programmable Clock Output 1 (PCK1)	AFE 0 ADC Input 1 (AFE0_AD1)(6) Parallel Capture Enable 2 (PIODCEN2)[8]
22	PB4	X	Two-Wire (I2C) 1 Data (TWD1)	PWM 0 Channel 2 Output High (PWMC0_PWMH2) Serial Port 1 TX (TXD1)[10]	Test Data In (TDI)[9]
23	PD28	X	Serial Port 5 RX (URXD3)[10] Two-Wire (I2C) 2 Clock (TWCK2)	CAN 1 Receive (CANRX1) Image Sensor Data Input 9 (ISI_D9)	Wakeup Pin 5 (WKUP5)[1]
24	PD31	X	QSPI Quad Mode Data 3 (QIO3) Programmable Clock 2 Output (PCK2)	Serial Port 5 TX (UTXD3)[10] Image Sensor Data Input 11 (ISI_D11)	
25	PD22	X	PWM 0 Channel 2 Output High (PWMC0_PWMH2) Timer 11 Line B (TIOB11)	SPI 0 Clock (SPI0_SPCK) Image Sensor Date Input 0 (ISI_D0)	
26	PD27	X	PWM 0 Channel 3 Output Low (PWMC0_PWML3) Two-Wire (I2C) 2 Serial Data (TWD2)	SPI 0 Chip Select 3 (SPI0_NPCS3) Image Sensor Date Input 8 (ISI_D8)	
27	PD20	X	PWM 0 Channel 0 Output High (PWMC0_PWMH0) TSU Timer Comparison Valid 1588 (GTSUCOMP)	SPI 0 Master In Slave Out (SPI0_MISO)	
28	PD21	X	PWM 0 Channel 1 Output High (PWMC0_PWMH1) Timer 11 Line A (TIOA11)	SPI 0 Master Out Slave In (SPI0_MOSI) Image Sensor Data Input 1 (ISI_D1)	
29	PB2	X	CAN 0 Transmit (CANTX0) Serial Port 0 CTS (CTS0)[10]	SPI 0 Chip Select 0 (SPI0_NPCS0)	AFE 0 ADC Input 5 (AFE0_AD5)
30	PD12	X	GMAC Receive Data 3 (GRX3) SPI 0 Chip Select 2 (SPI0_NPCS2)	CAN 1 Transmit (CANTX1) Image Sensor Data Input 6 (ISI_D6)	
31	PA23	X	Serial Port 1 Serial Clock (100K pull-up at reset) (SCK1) A19	PWM 0 Chan 0 Output High (PWMC0_PWMH0) PWM 1 Channel 2 Output Low (PWMC1_PWML2)	
32	PA24	X	Serial Port 1 RTS (RTS1)[10] A20	PWM 0 Chan 1 Output High (PWMC0_PWMH1) Image Sensor Data Clock (ISI_PCK)	
33	PA25	X	Serial Port 1 CTS (CTS1)[10] A23	PWM 0 Chan 2 Output High (PWMC0_PWMH2) Multimedia Card Clock (MCCK)	
34	PA9	X	Serial Port 2 RX (URXD0)[10] PWM 0 Fault Input 0 (100k pull-up reset) (PWMC0_PWMFI0)	Image Sensor Channel 3 Data Input (ISI_D3)	Wakeup Pin 6 (WKUP6) Parallel Capture Data 3 (PIODC3)[3]

P2 Connector					
Pin	Port	GPIO	Peripheral A Peripheral C	Peripheral B Peripheral D	Alternate
35	PA10	X	Serial Port 2 TX (UTXD0)[10] SSC Receive Data (100k pull-up at reset) (RD)	PWM 0 External Trigger 0 (PWMC0_PWMEXTRG0)	Parallel Capture Data 4 (PIODC4)[2]
36	PA30	X	PWMC0_PWML2 Multimedia Card Slot A Data 0 (MCDA0)	PWM 1 Chan 0 Trigger Input (PWMC1_PWMEXTRG0) Sounds Controller 0 Data Output (I2SC0_DO)	Wakeup Pin 11 (WKUP11)
37	PD11	X	GMAC Receive Data 2 (GRX2) TSU Timer Comparison Valid 1588 (GTSUCOMP)	PWM 0 Channel 0 Output High (PWMC0_PWMH0) Image Sensor Data Input 5 (ISI_D5)	
38	PB3	X	CAN 0 Receive (CANRX0) Serial Port 0 RTS (RTS0)[10]	Programmable Clock Output 2 (PCK2) Image Sensor Data Input 2 (ISI_D2)	AFE 0 ADC Input 2 (AFE0_AD2)/WKUP12[6]
39	PA3	X	Two-Wire (I2C) 0 Data (TWD0) Programmable Clock Output 2 (PCK2)	LON Chan 1 Collision Detect (LONCOL1)	Parallel Capture Data 0 (PIODC0)
40	PA31	X	SPI 0 Chip Select 1 (SPI0_NPCS1) Multimedia Card Slot A Data 1 (MCDA1)	Programmable Clock Output 2 (PCK2) PWM 1 Channel 2 Output High (PWMC1_PWMH2)	
41	PD25	X	PWM 0 Channel 1 Output Low (PWMC0_PWML1) Serial Port 4 RX (URXD2)[10]	SPI 0 Chip Select 1 (SPI0_NPCS1) Image Sensor Vertical Sync (ISI_VSYNC)	
42	PA4	X	Two-Wire (I2C) 0 Clock (TWCK0) Serial Port 3 TX (UTXD1)[10]	Timer 0 Clock (TCLK0)	Wakeup Pin 3 (WKUP3) Parallel Capture Data 1 (PIODC1)
43	PA13	X	QSPI MOSI Single Bit Mode, Data 0 Quad Mode (QIO0) PWM 1 Chan 1 Output Low (PWMC1_PWML1)	PWM 0 Channel 2 Output High (PWMC0_PWMH2)	Parallel Capture Data 7 (PIODC7)[2]
44	PD26	X	PWM 0 Channel 2 Output Low (PWMC0_PWML2) Serial Port 4 TX (UTXD2)[10]	SSC Transmt Data (TD) Serial Port 3 TX (UTXD1)[10]	
45	PA14	X	QSPI Serial Clock (QSCK) PWM 1 Chan 1 Output High (PWMC1_PWMH1)	PWM 0 Channel 3 Output High (PWMC0_PWMH3)	Wakeup Pin 8 (WKUP8) Parallel Capture Date En 1 (PIODCEN1)[3]
46	GND				
47	PA12	X	QSPI MISO Single Bit Mode, Data 1 Quad Mode (QIO1) PWM 1 Chan 0 Output High (PWMC1_PWMH0)	PWM 0 Channel 1 Output High (PWMC0_PWMH1)	Parallel Capture Data 6 (PIODC6)[2]
48	PA11	X	QPI Chip Select (QCS) PWM 1 Chan 0 Output Low (PWMC1_PWML0)	PWM 0 Channel 0 Output High (PWMC0_PWMH0)	Wakeup Pin 7 (WKUP7) Parallel Capture Data 5 (PIODC5)3
49	GND				
50	VCC_3V				

Note:

1. WKUPx can be used if the PIO Controller defines the I/O line as "input".
2. To select this extra function, refer to Section 32.5.14 "Parallel Capture Mode".
3. PIODCEN1/PIODCx has priority over WKUPx. Refer to Section 32.5.14 "Parallel Capture Mode".
4. Refer to Section 22.4.2 "Slow Clock Generator".
5. To select this extra function, refer to Section 50.5.1 "I/O Lines".
6. Analog input has priority over WKUPx pin. To select the analog input, refer to Section 50.5.1 "I/O Lines". WKUPx can be used if the PIO controller defines the I/O line as "input.

7. DAC0 is selected when DACC_CHER.CH0 is set. DAC1 is selected when DACC_CHER.CH1 is set. Refer to Section 51.7.4 "DACC Channel Enable Register".
8. Analog input has priority over WKUPx pin. To select the analog input, refer to Section 50.5.1 "I/O Lines". To select PIODCEN2, refer to Section 32.5.14 "Parallel Capture Mode".
9. Refer to the System I/O Configuration Register in Section 18. "Bus Matrix (MATRIX)".
10. See Table 5 for Serial Port to USART/UART mapping.

Table 4: Pinout and Signal Descriptions for P3, USB Connector

Pin	Signal	GPIO	Description
1	VCCUSB		USB VBUS Enable[1]
2	USB.D_N		USB Data Negative
3	USB.ID	X	USB ID Line
4	USB.D_P		USB Data Positive

Note:
1. Voltage divided for 5V signal tolerance.

Serial Port to USART/UART Mapping

This table details the mapping of the NetBurner software serial port number to the processor hardware signal name. The SAME70 processor provides both USART and UART serial ports. In addition to functioning as a UART, the USART ports can be configured for ISO7816, IrDA®, RS-485, SPI, Manchester and Modem modes; USART1 supports LON mode. Please refer to the SAME70 processor manual for details on the USARTs. USART 2 is available in custom and chip based designs, but is not fully pinned out on the MODM7AE70.

Table 5: Serial Port to USART/UART Mapping for P1 and P2 Connector

Serial Port Number	Hardware Module	
	USART	UART
0	0	
1	1	
2		0
3		1
4		2
5		3
6		4