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December 2014

# **FDZ191P**

# P-Channel 1.5V PowerTrench® WL-CSP MOSFET

-20V, -1A, 85mΩ

### **Features**

- Max  $r_{DS(on)}$  = 85m $\Omega$  at  $V_{GS}$  = -4.5V,  $I_D$  = -1A
- Max  $r_{DS(on)}$  = 123m $\Omega$  at  $V_{GS}$  = -2.5V,  $I_D$  = -1A
- Max  $r_{DS(on)}$  = 200m $\Omega$  at  $V_{GS}$  = -1.5V,  $I_D$  = -1A
- Occupies only 1.5 mm<sup>2</sup> of PCB area Less than 50% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.65 mm height when mounted to PCB
- RoHS Compliant

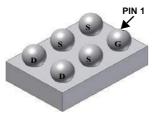


# **General Description**

Designed on Fairchild's advanced 1.5V PowerTrench process with state of the art "low pitch" WLCSP packaging process, the FDZ191P minimizes both PCB space and  $r_{DS(on)}$ . This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low  $r_{DS(on)}$ .

# **Application**

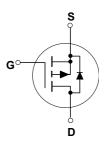
- Battery management
- Load switch
- Battery protection











# MOSFET Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
$V_{DS}$	Drain to Source Voltage		-20	V
$V_{GS}$	Gate to Source Voltage		±8	V
I <sub>D</sub>	Drain Current -Continuous	(Note 1a)	-3	۸
	-Pulsed		-15	Α
В	Power Dissipation	(Note 1a)	1.9	W
$P_{D}$	Power Dissipation	(Note 1b)	0.9	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

# **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	133	C/VV

## **Package Marking and Ordering Information**

Device Marking	evice Marking Device		e Package Reel Size		Quantity	
1	FDZ191P	WL-CSP	7"	8mm	5000 units	

# **Electrical Characteristics** T<sub>J</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0V$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = -250μA, referenced to 25°C		-12		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V			-1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 8V$ , $V_{DS} = 0V$			±100	nA

# **On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-0.4	-0.6	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, referenced to 25°C		2		mV/°C
		$V_{GS} = -4.5V, I_D = -1A$		67	85	
r	Drain to Source On Resistance	$V_{GS} = -2.5V, I_D = -1A$		85	123	mΩ
r <sub>DS(on)</sub>	Drain to Source On Nesistance	$V_{GS} = -1.5V, I_D = -1A$		140	200	11122
		$V_{GS} = -4.5V$ , $I_D = -1A T_J = 125$ °C		87	123	
$I_{D(on)}$	On to State Drain Current	$V_{GS} = -4.5V, V_{DS} = -5V$	-10			Α
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = -5V, I_{D} = -1A$		7		S

# **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V - 40V V - 0V	800	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = -10V, V <sub>GS</sub> = 0V, f = 1MHz	155	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1141112	90	pF
$R_g$	Gate Resistance	f = 1MHz	9	Ω

# **Switching Characteristics**

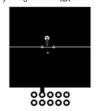
t <sub>d(on)</sub>	Turn-On Delay Time		11	20	ns
t <sub>r</sub>	Rise Time	$V_{DD}$ = -10V, $I_{D}$ = -1A $V_{GS}$ = -4.5V, $R_{GEN}$ = 6 $\Omega$	10	20	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = -4.5V, R <sub>GEN</sub> = 612	50	80	ns
t <sub>f</sub>	Fall Time		30	48	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0V \text{ to } 10V$ $V_{DD} = -10V$	9	13	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	I <sub>D</sub> = -1A	1		nC
Q <sub>ad</sub>	Gate to Drain "Miller" Charge		2		nC

## **Drain-Source Diode Characteristics**

$I_S$	Maximum continuous Drain-Source Diode Forward Current				-1.1	Α
$V_{SD}$	Source to Drain Diode Forward Voltage V <sub>GS</sub> = 0V, I <sub>S</sub> = -1.1A (Note 2)			-0.7	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = -1A, di/dt = 100A/μs		21		ns
Q <sub>rr</sub>	Reverse Recovery Charge	1F = -1A, αι/αι = 100A/μs		5		nC

Notes:

1: R<sub>0,IA</sub> is determined with the device mounted on a 1in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball, R<sub>0,IB</sub> is defined for reference. For R<sub>0,IC</sub> the thermal reference point for the case is defined as the top surface of the copper chip carrier. R<sub>0,IC</sub> and R<sub>0,IB</sub> are guaranteed by design while R<sub>0,IA</sub> is determined by the user's board design.



a. 65°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper,1.5" X 1.5" X 0.062" thick PCB



b. 133°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width <  $300\mu s$ , Duty cycle < 2.0%.

# **Typical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted

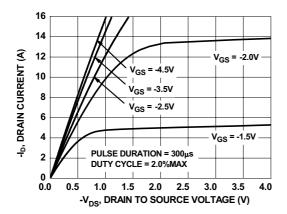


Figure 1. On Region Characteristics

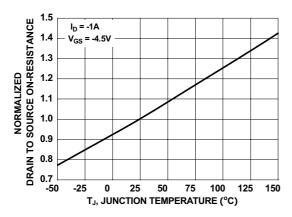


Figure 3. Normalized On Resistance vs Junction Temperature

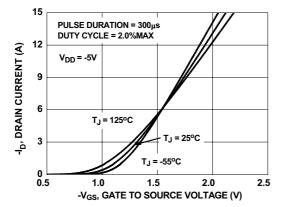


Figure 5. Transfer Characteristics

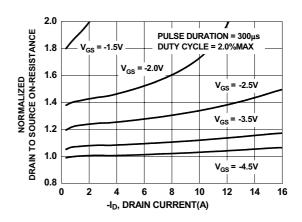


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

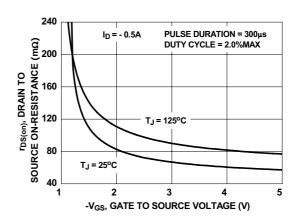


Figure 4. On-Resistance vs Gate to Source Voltage

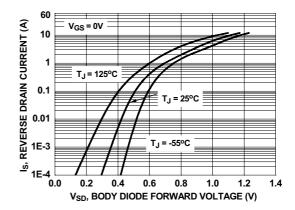


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# **Typical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted

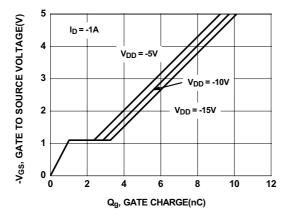


Figure 7. Gate Charge Characteristics

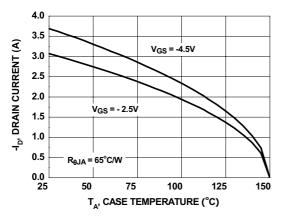


Figure 9. Maximum Continuous Drain Current vs Ambient Temperature

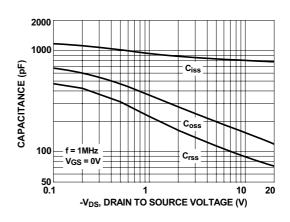


Figure 8. Capacitance vs Drain to Source Voltage

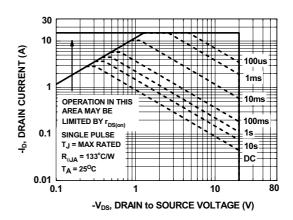


Figure 10. Forward Bias Safe Operating Area

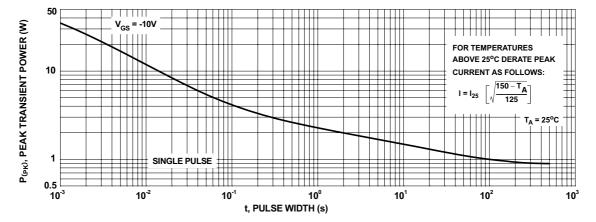


Figure 11. Single Pulse Maximum Power Dissipation

# Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

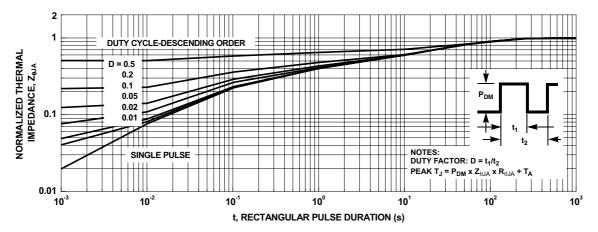
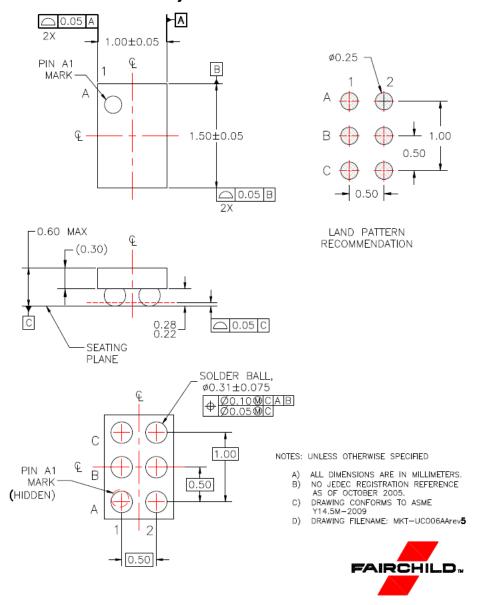


Figure 12. Transient Thermal Response Curve

# **Dimensional Outline and Pad Layout**



### **Pin Definations:**

Gate	Drain	Source
A1	C1, C2	A2, B1, B2

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