Photoflash Capacitor Charger with Programmable Current Limit and IGBT Driver

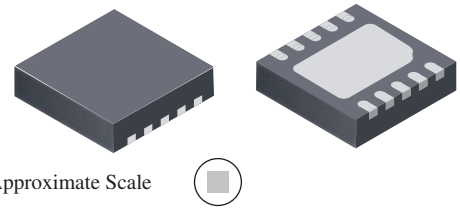
Features and Benefits

- Eight-level, digitally-programmable current limits from 550 mA to 1.75 A
- Voltage sensing feedback before output diode for low leakage
- No external pull-down resistors needed
- Power with 1 Li+ or 2 Alkaline/NiMH/NiCAD batteries
- Low quiescent current draw (1 µA max in shutdown mode)
- Zero-voltage switching for lower loss
- Adjustable output voltage
- Integrated IGBT driver with trigger
- Charge complete indication
- >75% efficiency
- Low-profile (0.75 mm high) 3 mm × 3 mm TDFN 10-contact package

Applications:

- Digital camera flash
- Film camera flash
- Cell phone flash
- Emergency strobe light

Package: 10-contact TDFN with exposed thermal pad (suffix EJ)



Approximate Scale

Description

The A8835 is a highly integrated IC that charges photoflash capacitors for digital and film cameras. An integrated MOSFET switch drives the transformer in a flyback topology. It also features an integrated IGBT driver that facilitates the flash discharge function and saves board space.

The CHARGE pin enables the A8835 and starts the charging of the output capacitor. When the designated output voltage is reached, the A8835 stops the charging until the CHARGE pin is toggled again. The $\overline{\text{DONE}}$ pin is an open-drain indicator of when the designated output voltage is reached.

The peak current limit can be adjusted to eight different levels between 550 mA and 1.75 A, by clocking the CHARGE pin. This allows the user to operate the flash even at low battery voltages.

The A8835 can be used with two Alkaline/NiMH/NiCAD or one single-cell Li+ battery connected to the transformer primary. Connect the VIN pin to a 3.0 to 5.5 V supply, which can be either the system rail or the Li+ battery, if used.

The A8835 is available in a very low profile (0.75 mm) 10-contact 3 mm × 3 mm TDFN package, making it ideal for space-constrained applications. It is lead (Pb) free, with 100% matte-tin leadframe plating and has an exposed pad for enhanced thermal dissipation.

Typical Applications

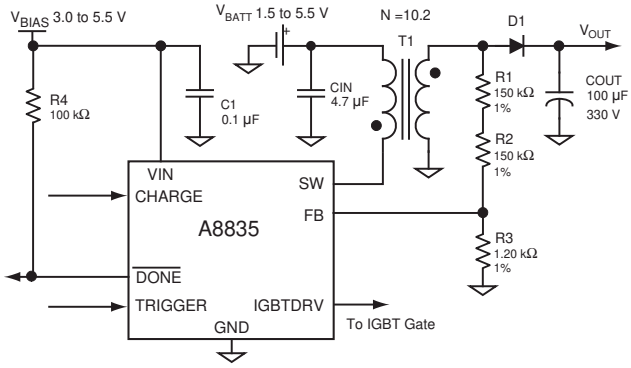


Figure 1. Typical circuit with separate power supply to transformer

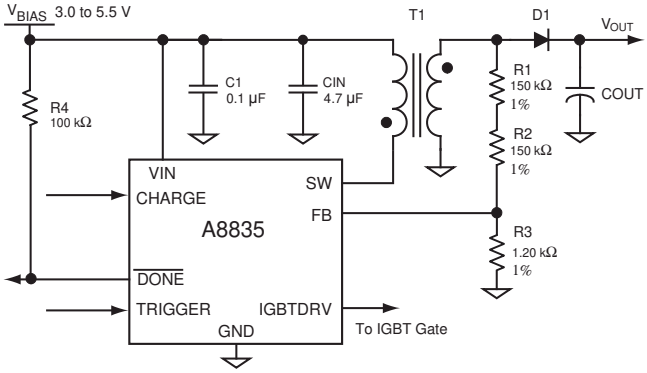


Figure 2. Typical circuit with single power supply

Selection Guide

Part Number	Package	Packing*
A8835EEJTR-T	10-pin TDFN	1500 pieces/ 7-in. reel

*Contact Allegro for additional packing options

Absolute Maximum Ratings

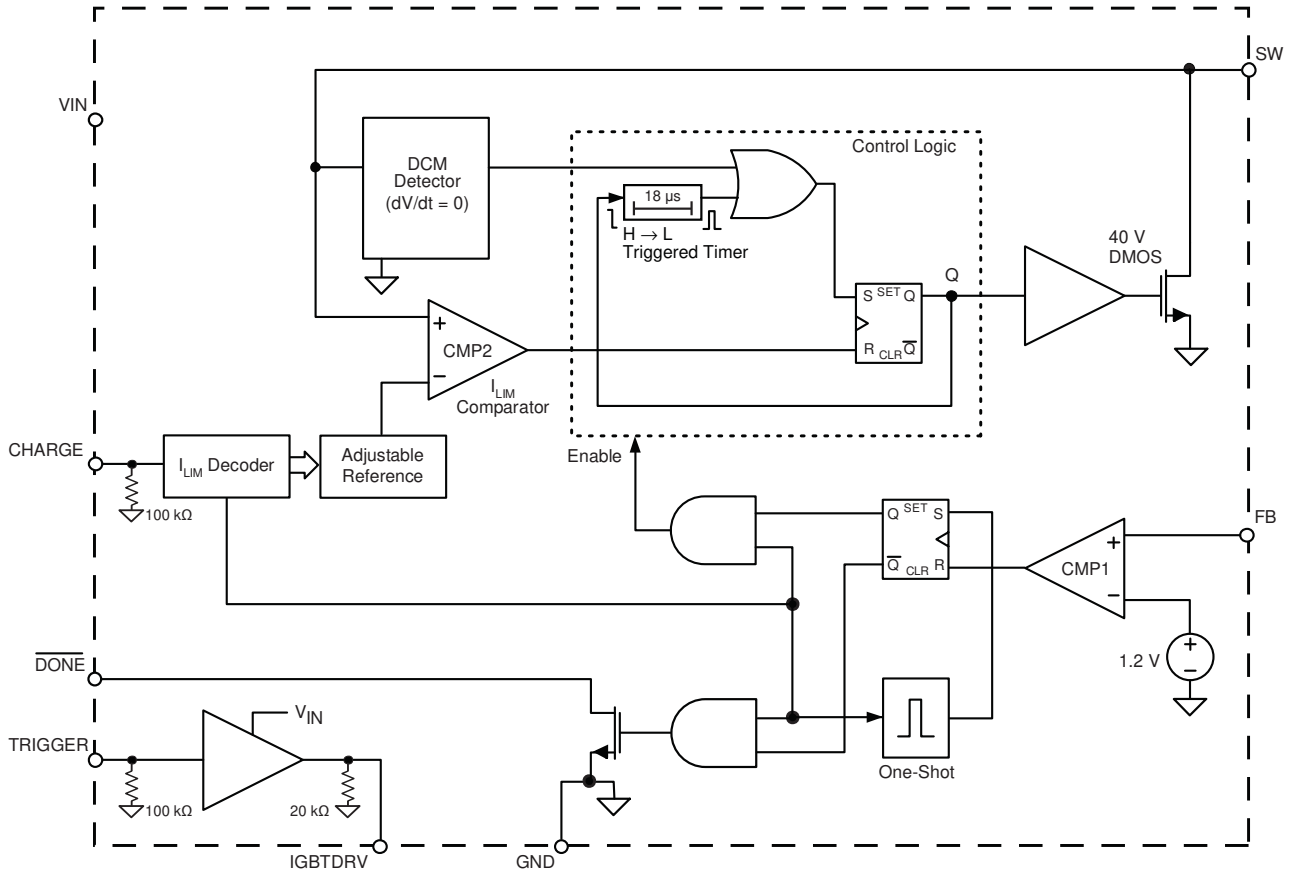
Characteristic	Symbol	Notes	Rating	Units
SW pin	V_{SW}	DC voltage. (V_{SW} is self-clamped by an internal active clamp and is allowed to exceed 40 V during flyback spike durations. Maximum repetitive energy during flyback spike: 0.5 µJ at frequency ≤ 400 kHz.)	–0.3 to 40	V
IGBTDRV pin	$V_{IGBTDRV}$		–0.3 to V_{IN} + 0.3	V
FB pin	V_{FB}		–0.3 to V_{IN}	V
All other pins	V_X		–0.3 to 7	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Package Thermal Characteristics

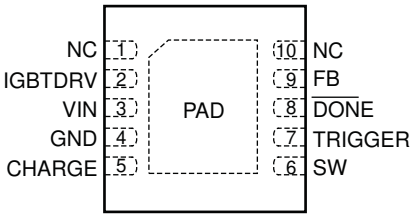
Characteristic	Symbol	Test Conditions*	Rating	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB, based on JEDEC standard	45	ºC/W

*Additional information is available on the Allegro website.

Functional Block Diagram



Device Pin-out Diagram



Terminal List Table

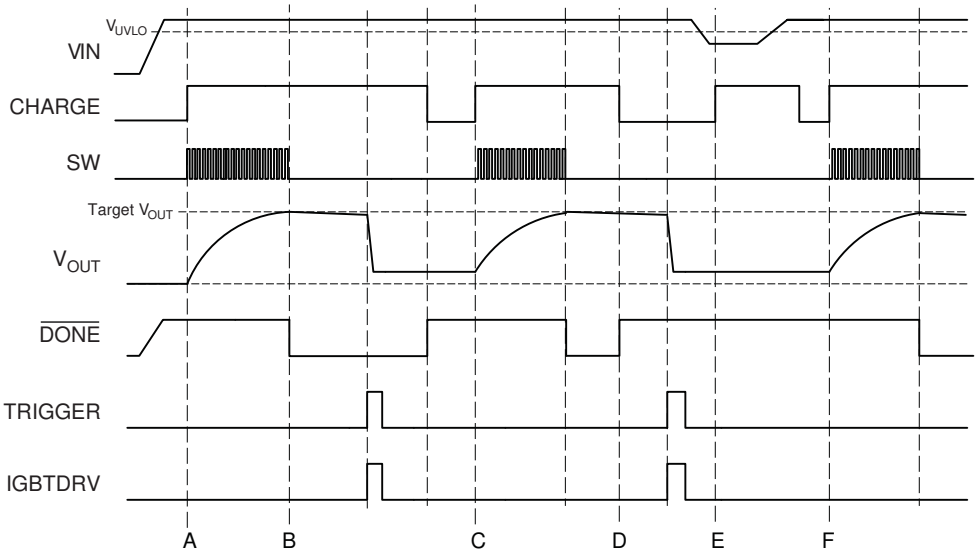
Number	Name	Function
1,10	NC	No connection.
2	IGBTDRV	IGBT driver gate drive output.
3	VIN	Input voltage. Connect to 3 to 5.5 V bias supply. Decouple V_{IN} voltage with 0.1 µF ceramic capacitor placed close to this pin.
4	GND	Device ground
5	CHARGE	Charge enable and current limit serial programming pin. Set this pin low to shut down the chip.
6	SW	Drain connection of internal DMOS switch. Connect to transformer primary winding.
7	TRIGGER	Strobe signal input
8	$\overline{\text{DONE}}$	Open collector output, pulls low when output reaches target value and CHARGE is high. Goes high during charging or whenever CHARGE is low.
9	FB	Output voltage feedback
–	PAD	Exposed pad for enhanced thermal dissipation. Connect to ground plane.

ELECTRICAL CHARACTERISTICS Valid at V_{IN} = 3.3 V, T_A = 25°C except ● indicates specifications guaranteed from −40°C to 85°C ambient, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Units
Supply Voltage*	V_{IN}		●	3	–	5.5	V
UVLO Enable Threshold	V_{UVLO}	V_{IN} rising		2.55	2.65	2.75	V
UVLO Hysteresis	$V_{UVLOHYS}$			–	150	–	mV
Supply Current	I_{IN}	Charging		–	1.5	–	mA
		Charging done		–	1	10	µA
		Shutdown (V_{CHARGE} = 0 V, $V_{TRIGGER}$ = 0 V)		–	0.01	1	µA
Primary Side Current Limit (ILIM clock input at CHARGE pin)	I_{SWLIM1}			1.58	1.75	1.93	A
	I_{SWLIM2}			–	1.58	–	A
	I_{SWLIM3}			–	1.4	–	A
	I_{SWLIM4}			–	1.22	–	A
	I_{SWLIM5}			–	1.05	–	A
	I_{SWLIM6}			–	0.86	–	A
	I_{SWLIM7}			–	0.7	–	A
	I_{SWLIM8}			–	0.55	–	A
SW On Resistance	$R_{DS(On)SW}$	V_{IN} = 3.3 V, I_D = 800 mA		–	0.27	–	Ω
SW Leakage Current*	I_{SWLKG}	V_{SW} = 35 V	●	–	–	1	µA
Switch Off Timeout	$t_{OFF(Max)}$			–	18	–	µs
Switch On Timeout	$t_{ON(Max)}$			–	18	–	µs
CHARGE Input Current	I_{CHARGE}	V_{CHARGE} = V_{IN}		–	33	–	µA
CHARGE Input Voltage*	$V_{CHARGE(H)}$		●	2	–	–	V
	$V_{CHARGE(L)}$		●	–	–	0.8	V
ILIM Clock High Time at CHARGE Pin	$t_{ILIM1(H)}$	Initial pulse		20	–	–	µs
	$t_{ILIM(H)}$	Subsequent pulses		0.2	–	–	µs
ILIM Clock Low Time at CHARGE Pin	$t_{ILIM(L)}$			0.2	–	–	µs
Total ILIM Setup Time	$t_{ILIM(SU)}$			–	54	–	µs
$\overline{\text{DONE}}$ Output Leakage Current*	$I_{DONELKG}$		●	–	–	1	µA
$\overline{\text{DONE}}$ Output Low Voltage*	$V_{DONE(L)}$	32 µA into $\overline{\text{DONE}}$ pin	●	–	–	100	mV
FB Voltage Threshold*	V_{FB}		●	1.187	1.205	1.223	V
FB Input Current	I_{FB}	V_{FB} = 1.205 V		–	–120	–	nA
IGBT Driver							
IGBTDRV On Resistance to VIN	$R_{DS(On)I-V}$	V_{IN} = 3.3 V, $V_{IGBTDRV}$ = 1.5 V, $V_{TRIGGER}$ = V_{IN}		–	5	–	Ω
IGBTDRV On Resistance to GND	$R_{DS(On)I-G}$	V_{IN} = 3.3 V, $V_{IGBTDRV}$ = 1.5 V, $V_{TRIGGER}$ = 0 V		–	6	–	Ω
TRIGGER Input Current	$I_{TRIGGER}$	$V_{TRIGGER}$ = V_{IN}		–	33	–	µA
TRIGGER Input Voltage*	$V_{TRIGGER(H)}$		●	2	–	–	V
	$V_{TRIGGER(L)}$		●	–	–	0.8	V
Propagation Delay, Rising	t_{Dr}	R_{gate}=12 Ω, C_{LOAD} = 6500 pF, V_{IN} = 3.3 V		–	30	–	ns
Propagation Delay, Falling	t_{Df}	R_{gate}=12 Ω, C_{LOAD} = 6500 pF, V_{IN} = 3.3 V		–	30	–	ns
Output Rise Time	t_r	R_{gate}=12 Ω, C_{LOAD} = 6500 pF, V_{IN} = 3.3 V		–	70	–	ns
Output Fall Time	t_f	R_{gate}=12 Ω, C_{LOAD} = 6500 pF, V_{IN} = 3.3 V		–	70	–	ns
dV/dt Threshold for ZVS Comparator	dV/dt	Measured at SW pin		–	20	–	V/µs

*Specification over the range T_A = –40°C to 85°C guaranteed by design and characterization.

Operation Timing Diagram



Explanation of Events:

A. Start charging by pulling CHARGE to high, provided that V_{IN} is above the V_{UVLO} level.

B. Charging stops when V_{OUT} reaches the target voltage. $\overline{DONE}$ goes low, to signal the completion of the charging process.

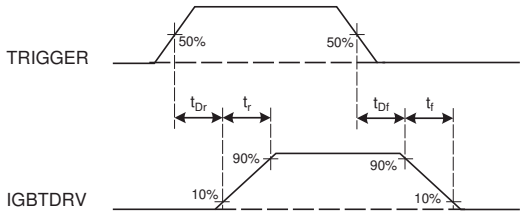
C. Start a new charging process with a low-to-high transition at the CHARGE pin.

D. Pull CHARGE to low, to put the controller in low-power standby mode.

E. Charging does not start, because V_{IN} is below V_{UVLO} level when CHARGE goes high.

F. After V_{IN} goes above V_{UVLO}, another low-to-high transition at the CHARGE pin is required to start charging.

IGBT Drive Timing Definition



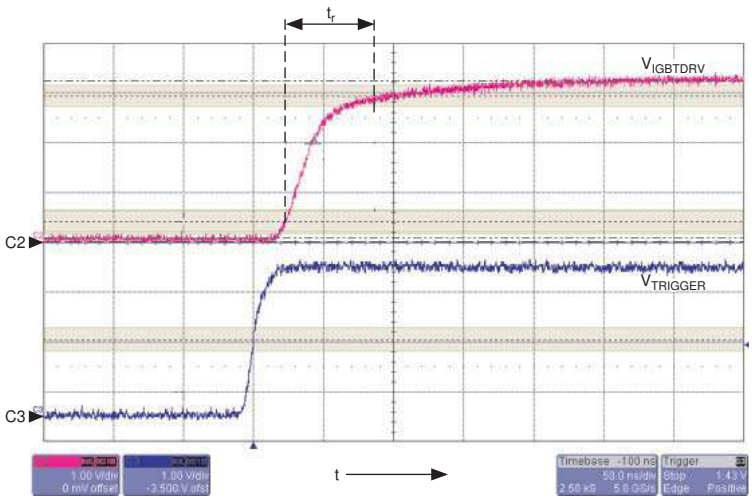
Performance Characteristics

IGBT Drive waveforms are measured with R-C load (12 Ω, 6800 pF)

IGBT Drive Performance

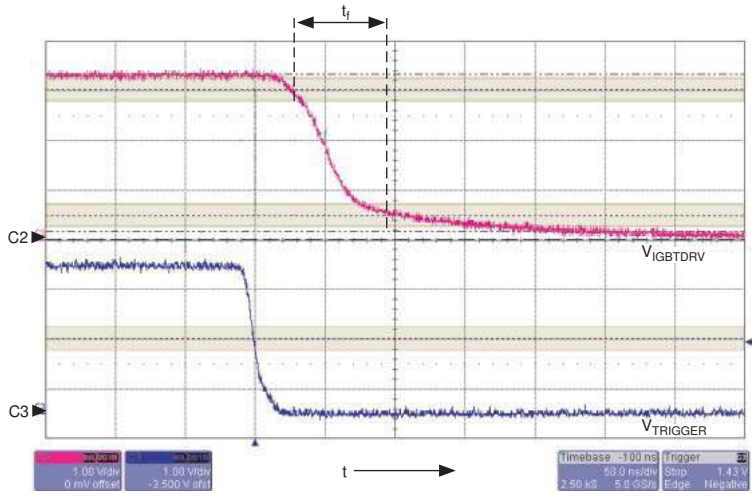
Rising Signal

Symbol	Parameter	Units/Division
C2	$V_{IGBTDRV}$	1 V
C3	$V_{TRIGGER}$	1 V
t	time	50 ns
Conditions	**Parameter**	**Value**
	t_{Dr}	22.881 ns
	t_r	63.125 ns
	C_{LOAD}	6800 pF
	R_{gate}	12 Ω



Falling Signal

Symbol	Parameter	Units/Division
C2	$V_{IGBTDRV}$	1 V
C3	$V_{TRIGGER}$	1 V
t	time	50 ns
Conditions	**Parameter**	**Value**
	t_{Df}	27.427 ns
	t_f	65.529 ns
	C_{LOAD}	6800 pF
	R_{gate}	12 Ω



Functional Description

Overview

The A8835 is a photoflash capacitor charger control IC with adjustable input current limiting. It also integrates an IGBT driver for strobe operation of the flash tube, dramatically saving board space in comparison to discrete solutions for strobe flash operation. The control logic is shown in the functional block diagram.

The charging operation of the A8835 is started by a low-to-high signal on the CHARGE pin, provided that V_{IN} is above V_{UVLO} level. It is strongly recommended to keep the CHARGE pin at logic low during power-up. When V_{IN} exceeds the UVLO level, a low-to-high transition on the CHARGE pin is required to start the charging. The primary peak current is set by input programming signals from the CHARGE pin. When a charging cycle is initiated, the transformer primary side current, $I_{Primary}$, ramps up linearly at a rate determined by the combined effect of the battery voltage, V_{BATT}, and the primary side inductance, $L_{Primary}$. When $I_{Primary}$ reaches the current limit, I_{SWLIM}, the internal MOSFET is turned off immediately, allowing the energy to be pushed into the photoflash capacitor, C_{OUT}, from the secondary winding. The secondary side current drops linearly as C_{OUT} charges. The switching cycle starts again, either after the transformer flux is reset, or after a predetermined time period, $t_{OFF(Max)}$ (18 µs), whichever occurs first.

The output voltage, V_{OUT}, is sensed by a resistor string, R_1, R_2, and R_3 (see application circuit diagrams), connected across the transformer secondary winding. This resistor string forms a voltage divider that feeds back to the FB pin. The resistors must be sized to achieve a desired output voltage level based on a typical value of 1.205 V at the FB pin. As soon as V_{OUT} reaches the desired value, the charging process is terminated. Toggling the CHARGE pin can start a refresh operation.

Input Current Limiting

The peak current limit can be programmed to eight different levels, from 1.75 A down to 550 mA, by clocking the CHARGE pin. An internal digital circuit decodes the input clock signals, which sets the switch current limit. This flexible scheme allows the user to operate the flash circuit according to different battery input voltages. The battery life can be effectively extended by setting a lower current limit at low battery voltages.

Figure 4 shows the ILIM clock timing scheme protocol. The total ILIM setup time, $t_{ILIM(SU)}$, denotes the time needed for the decoder circuit to receive ILIM inputs and set I_{SWLIM}. Apply current limit pulses during $t_{ILIM(SU)}$ (54 µs) period.

Figure 5 shows the timing definition of the primary current limiting circuit. At the end of the setup period, $t_{ILIM(SU)}$, primary current starts to ramp up to the set I_{SWLIM}. The I_{SWLIM} setting remains in effect as long as the CHARGE pin is high. To reset the ILIM counter, pull the CHARGE pin low before clocking in the new setting.

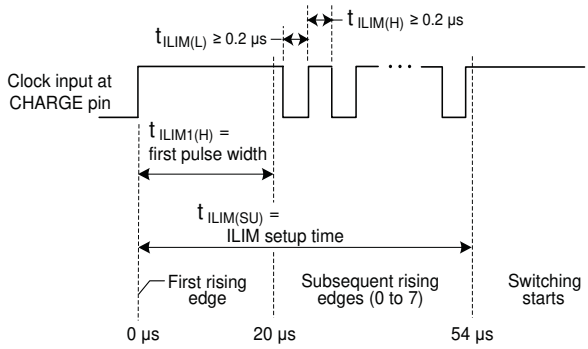


Figure 4. ILIM Clock Timing Definition

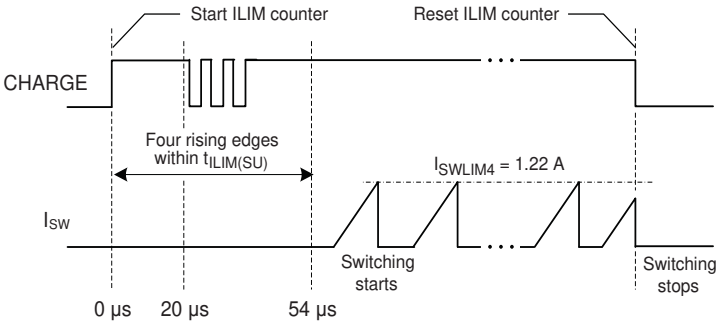


Figure 5. Current Limit Programming Example (I_{SWLIM4} selected).

After the first start-up or an ILIM decoder reset, each new current limit can be set by sending a burst of pulses to the CHARGE pin. The first rising edge starts the ILIM decoder, and up to 8 rising edges will be counted to set the I_{SWLIM} level. The first pulse width, $t_{ILIM1(H)}$, must be at least 20 µs long. Subsequent pulses (up to 7 more) can be as short as 0.2 µs. The last low-to-high edge must arrive within 54 µs from the first edge. The CHARGE pin will stay high afterwards.

Switch On-Time and Off-Time Control

The A8835 implements an adaptive on-time/off-time control. On-time duration, t_{on}, is equal to $t_{on} = I_{SWlim} \times L_P / V_{BAT}$. Off-time duration, t_{off}, depends on the operating conditions during switch off-time. The A8835 applies its two charging modes, Fast Charging mode and Timer mode, according to those conditions.

Timer Mode and Fast Charging Mode

The A8835 achieves fast charging times and high efficiency by operating in discontinuous conduction mode (DCM) through most of the charging process The relationship of Timer mode and Fast Charging mode is shown in figure 4.

The IC operates in Timer mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage, V_{OUT}, is less than approximately 15 to 20 V. Timer mode is a fixed period, 18 µs, off-time control. One advantage of having Timer mode is that it limits the initial battery current surge and thus acts as a "soft-start." A time-expanded view of a Timer mode interval is shown in figure 5.

As soon as a sufficient voltage has built up at the output capacitor, the IC enters Fast-Charging mode. In this mode, the next switching cycle starts after the secondary side current has stopped flowing, and the switch voltage has dropped to a minimum value. A proprietary circuit is used to allow minimum-voltage switching, even if the SW pin voltage does not drop to 0 V. This enables Fast-Charging mode to start earlier, thereby reducing the overall charging time. Minimum-voltage switching is shown in figure 6.

During Fast-Charging mode, when V_{OUT} is high enough (over 50 V), true zero-voltage switching (ZVS) is achieved. This further improves efficiency as well as reduces switching noise. A ZVS interval is shown in figure 7.

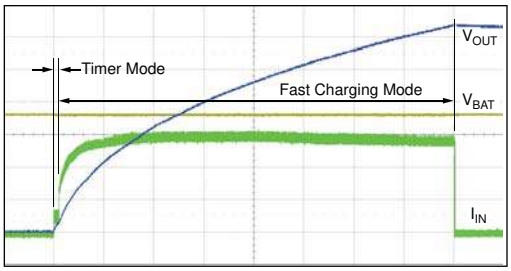


Figure 4. Timer mode and Fast Charging mode: t = 200 ms/div; V_{OUT} = 50 V/div; V_{BAT} = 1 V/div.; I_{IN} = 100 mA/div., V_{BAT} = 3.6 V; C_{OUT} = 20 µF / 330 V; and $I_{SWlim} \approx 0.7$ A.

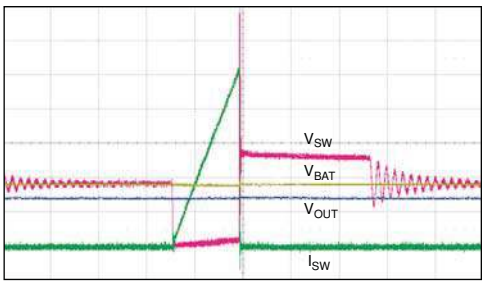


Figure 5. Expanded view of Timer mode: $V_{OUT} \leq 14$ V; t = 2 µs/div; V_{BAT} = 3.6 V; I_{SWlim} = 1.05 A.

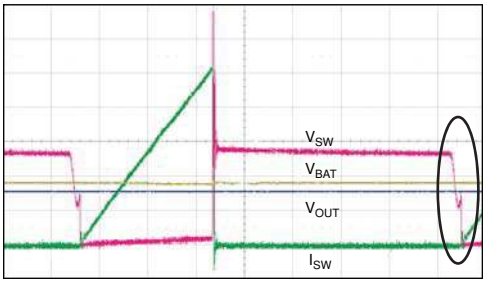


Figure 6. Minimum-voltage switching: $V_{OUT} \geq 15$ V; t =1 µs/div; V_{BAT} = 3.6 V; and I_{SWlim} = 1.05 A.

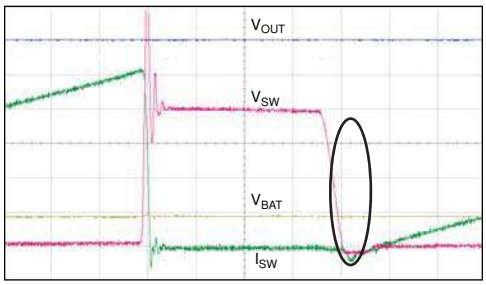


Figure 7. ZVS voltage switching: V_{OUT} = 120 V, t =0.2 µs/div, V_{BAT} = 3.6 V, I_{SWlim} = 1.05 A.

Applications Information

Transformer Design

Turns Ratio. The minimum transformer turns ratio, N, (Secondary : Primary) should be chosen based on the following formula:

$$N \geq \frac{V_{OUT} + V_{D\_Drop}}{40 - V_{BATT}} \quad (1)$$

where:

V_{OUT} (V) is the required output voltage level,
V_{D_Drop} (V) is the forward voltage drop of the output diode(s),
V_{BATT} (V) is the transformer battery supply, and
40 (V) is the rated voltage for the internal MOSFET switch, representing the maximum allowable reflected voltage from the output to the SW pin.

For example, if V_{BATT} is 3.5 V and V_{D_Drop} is 1.7 V (which could be the case when two high voltage diodes were in series), and the desired V_{OUT} is 320 V, then the turns ratio should be at least 8.9.

In a worst case, when V_{BATT} is highest and V_{D_Drop} and V_{OUT} are at their maximum tolerance limit, N will be higher. Taking V_{BATT} = 5.5 V, V_{D_Drop} = 2 V, and V_{OUT} = 320 V × 102 % = 326.4 V as the worst case condition, N can be determined to be 9.5.

In practice, always choose a turns ratio that is higher than the calculated value to give some safety margin. In the worst case example, a minimum turns ratio of N = 10 is recommended.

Primary Inductance. As a loose guideline when choosing the primary inductance, $L_{Primary}$ (µH), use the following formula:

$$L_{Primary} \geq \frac{300 \times 10^{-9} \times V_{OUT}}{N \times I_{SWLIM}} \quad . \quad (2)$$

Ideally, the charging time is not affected by transformer primary inductance. In practice, however, it is recommended that a primary inductance be chosen between 10 µH and 20 µH. When $L_{Primary}$ is lower than 10 µH, the converter operates at higher frequency, which increases switching loss proportionally. This leads to lower efficiency and longer charging time. When $L_{Primary}$ is greater than 20 µH, the rating of the transformer must be dramatically increased to handle the required power density, and the series resistances are usually higher. A design that is optimized to achieve a small footprint solution would have an $L_{Primary}$ of 12 to 14 µH, with minimized leakage inductance and secondary capacitance, and minimized primary and secondary series resistance. See the table Recommended Components for more information.

Leakage Inductance and Secondary Capacitance

The transformer design should minimize the leakage inductance to ensure the turn-off voltage spike at the SW node does not exceed the 40 V limit. An achievable minimum leakage inductance for this application, however, is usually compromised by an increase in parasitic capacitance. Furthermore, the transformer secondary capacitance should be minimized. Any secondary capacitance is multiplied by N^2 when reflected to the primary, leading to high initial current swings when the switch turns on, and to reduced efficiency.

Input Capacitor Selection

Ceramic capacitors with X5R or X7R dielectrics are recommended for the input capacitor, CIN. During initial timer mode the device operates with 18 µs off-time. A typical input section for a photoflash module with input filter inductor, or a test setup with long connecting wires is shown in figure 12. The resonant period caused by input filter inductor and capacitor should be at least 2 times greater or smaller than the 18 µs timer period, to reduce input ripple current during this period. See figure 13.

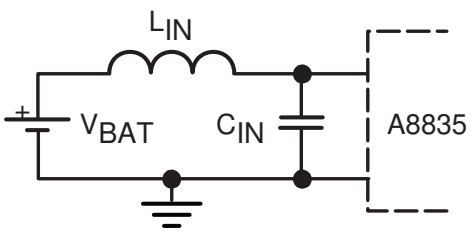
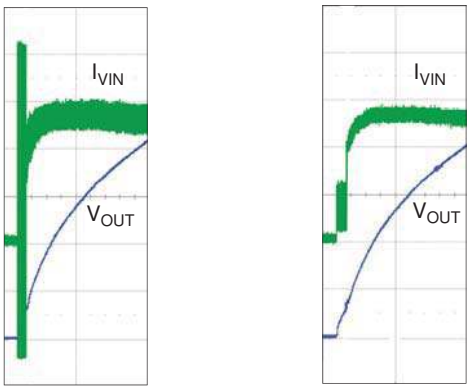


Figure 12. Typical input section with input inductance (inductance, L_{IN}, may be an input filter inductor or inductance due to long wires in test setup)



C_{IN} = 4.7 µF C_{IN} = 10 µF

Figure 13. Effects of changing the values of C_{IN}.

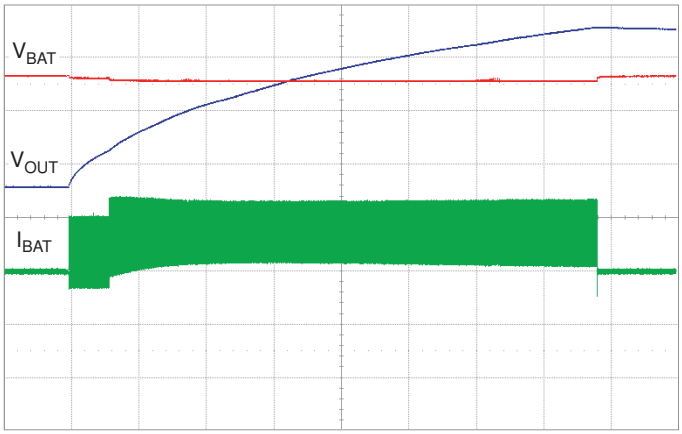


Figure 14. Input current waveforms with Li+ battery connected by 5-in. wire and decoupled by 4.7 µF capacitor. t = 500 ms/div; V_{BAT} = 2 V/div; V_{OUT} = 100 V/div.; I_{BAT} = 1 A/div.

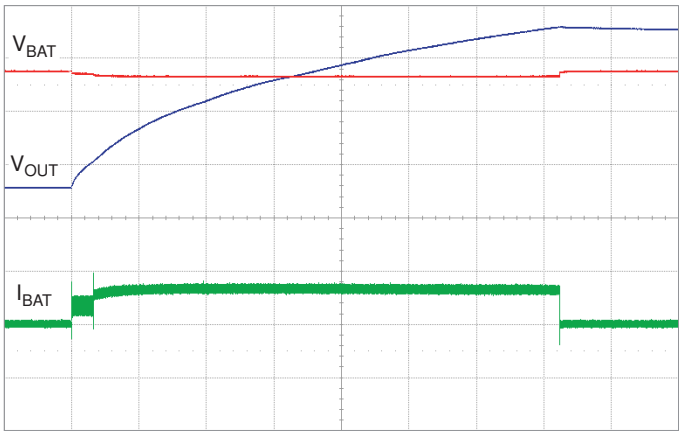


Figure 15. Input current waveforms with Li+ battery connected through 10 µH inductor and 4.7 µF capacitor. t = 500 ms/div; V_{BAT} = 2 V/div; V_{OUT} = 100 V/div.; I_{BAT} = 1 A/div.

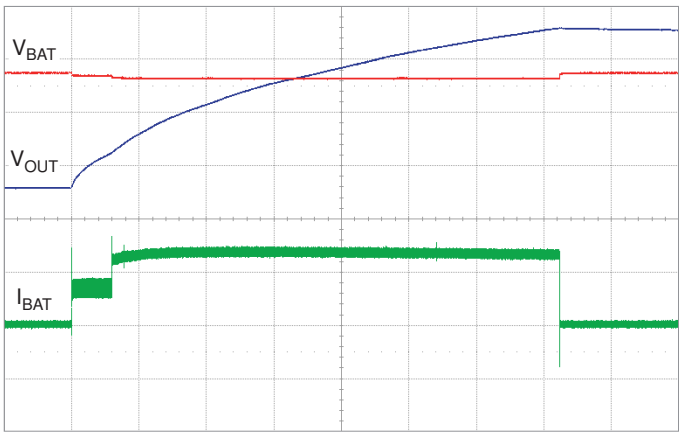


Figure 16. Input current waveforms with Li+ battery connected through 10 µH inductor and 10 µF capacitor. t = 500 ms/div; V_{BAT} = 2 V/div; V_{OUT} = 100 V/div.; I_{BAT} = 500 mA/div.

The resonant period is given by:

$$T_{res} = 2 \times \pi \times (L_{IN} \times C_{IN})^{½}$$

It is recommended to use at least 4.7 µF / 6.3 V to decouple the battery input, V_{BAT}, at the primary of the transformer. Decouple the V_{IN} pin using a 0.1 µF / 6.3 V bypass capacitor.

Output Diode Selection

Choose the rectifying diode(s), D1, to have small parasitic capacitance (short reverse recovery time) while satisfying the reverse voltage and forward current requirements. The peak reverse voltage of the diode, V_{DPeak}, occurs when the internal MOSFET switch is closed. It can be calculated as:

$$V_{DPeak} = V_{OUT} + N \times V_{BAT}$$

The peak current of the rectifying diode, I_{DPeak}, is calculated as:

$$I_{DPeak} = I_{PrimaryPeak} / N$$

Layout Guidelines

Key to a good layout for the photoflash capacitor charger circuit is to keep the parasitics minimized on the power switch loop (transformer primary side) and the rectifier loop (secondary side). Use short, thick traces for connections to the transformer primary and SW pin. It is important that the $\overline{\text{DONE}}$ signal trace and other signal traces be routed away from the transformer and other switching traces, in order to minimize noise pickup. In addition, high voltage isolation rules must be followed carefully to avoid breakdown failure of the circuit board.

Avoid locating the ground plane underneath transformer secondary and diode to minimize parasitic capacitance.

It is recommended to use a single high voltage resistor to sense output voltage. Two series resistors, R1 and R2, may be used on the high voltage V_{OUT} side. Referring to figure 17, a parasitic capacitor, CP1, across the R1-R2 junction and GND, can affect output voltage accuracy due to slow voltage sensing at the FB pin. A parasitic capacitor, CP2, between the R1-R2 junction and V_{OUT}, can affect output voltage accuracy due to overshoot in the sensed voltage at the FB pin. Very small capacitance (≈1 pF) can cause a significant error.

Minimize parasitic capacitors with careful layout. The center pad between R1 and R2 should be routed away from any GND and other traces. Avoid placing the GND plane directly underneath the center pad.

Place R1 and R2 as close as possible in a straight line as shown in figure 18.

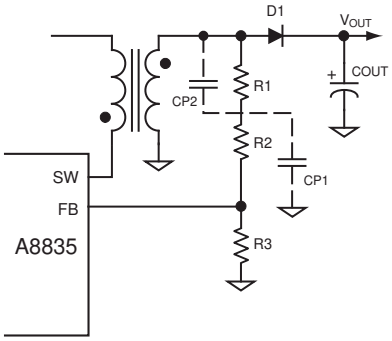


Figure 17. Equivalent circuit with parasitic capacitors across feedback divider.

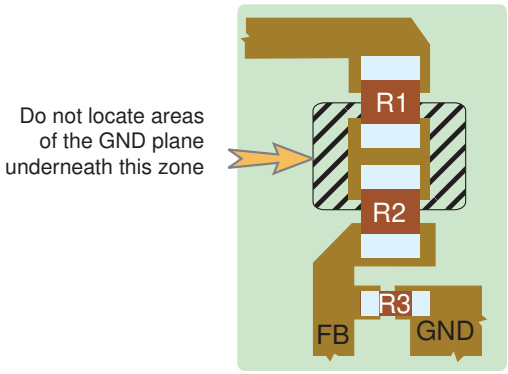
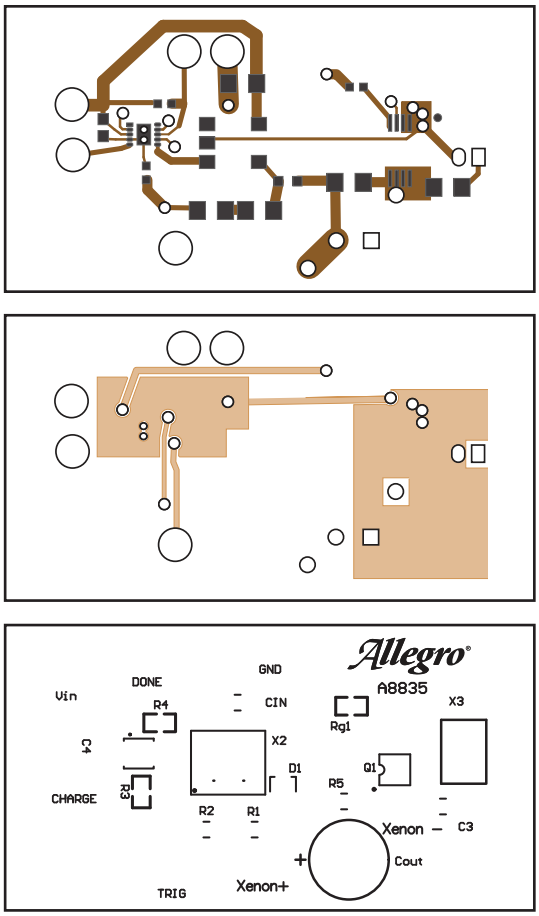
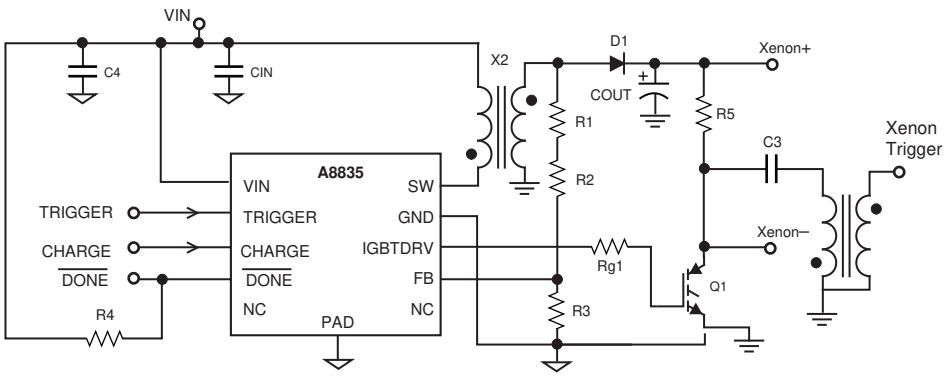


Figure 18. Recommended layout for feedback divider.

Recommended Layout

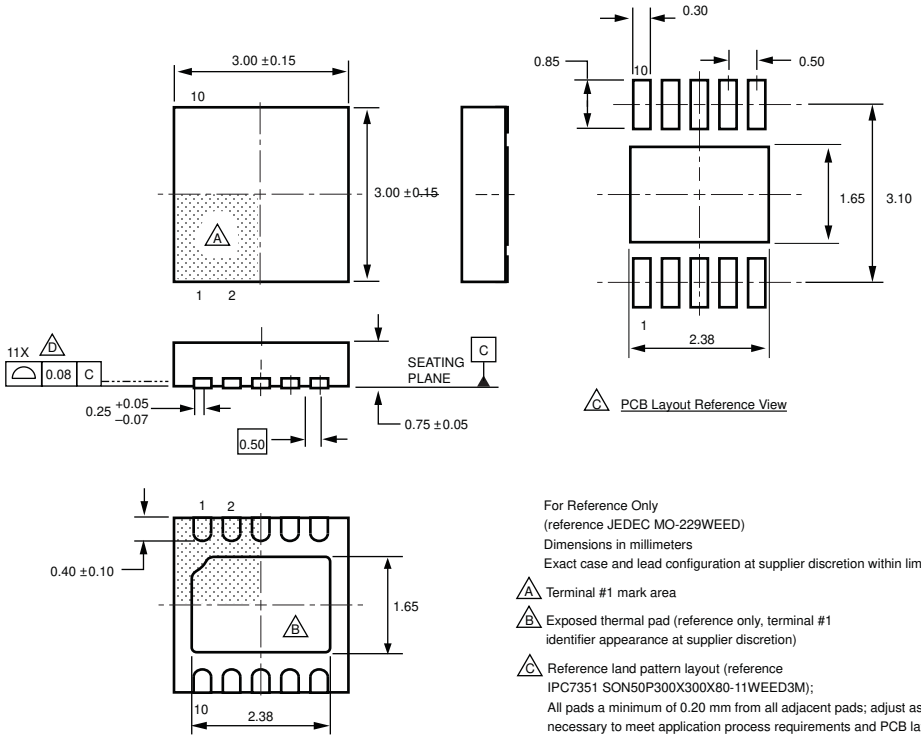




Recommended Components

Component	Rating	Part Number	Source	Remarks
C1, Input Capacitor	0.1 µF, ±10%, 16 V, X5R or X7R ceramic capacitor (0603)	GRM188R71C104KA01D	Murata	10 V minimum rating can be used
CIN, Input Capacitor	4.7 µF, ±10%, 10 V, X5R or X7R ceramic capacitor (0805)	LMK212BJ475KG	Taiyo Yuden	
COUT, Photoflash Capacitor	330 V 100 µF (or 19 to 180 µF)	EPH-331ELL101B131S	Chemi-Con	
D1, Output Diode	2 x 250 V, 225 mA, 5 pF	BAV23S	Philips Semiconductor, Fairchild Semiconductor	
R1, R2, FB Resistors	150 kΩ each $^1/_4$ W, ± 1%; 1206, 0805, or 0603 resistors rated for 150 V			Instead of two resistors, a single 300 kΩ resistor with 350 V rating can be used
R3, FB Resistor	1.2 kΩ $^1/_{10}$ W ±1% (0603 or 0402)			
T1, Transformer	L_P = 14.2 µH, I_P = 2 A, N = 10	T-15-154M	Tokyo Coil	Suitable for I_{LIM} from 0.55 to 1.75 A
	L_P = 7.4 µH, I_P = 2 A, N = 10	T-16-103A	Tokyo Coil	Suitable for I_{LIM} from 1.2 to 1.75 A only
	L_P = 12.8 µH, I_P = 1.5 A, N=10	T-16-024A	Tokyo Coil	Suitable for I_{LIM} from 0.55 to 1.4 A only

Package EJ, 10-Contact TDFN with Exposed Thermal Pad



For Reference Only
(reference JEDEC MO-229WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Revision History

Revision	Revision Date	Description of Revision
Rev. 1	April 19, 2012	Miscellaneous format changes

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