High-Speed CMOS Bus Exchange Switches with Active Termination (Bus Hold)

QS3388

FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Active termination drives bus pins to rails when off
- Zero propagation delay
- Undershoot Clamp diodes on all inputs
- Available in 24-pin DIP, SOIC (SO) and QSOP
- Low power CMOS proprietary technology
- Bus exchange allows nibble swap
- Zero ground bounce in flow-through mode
- TTL-compatible input and output levels

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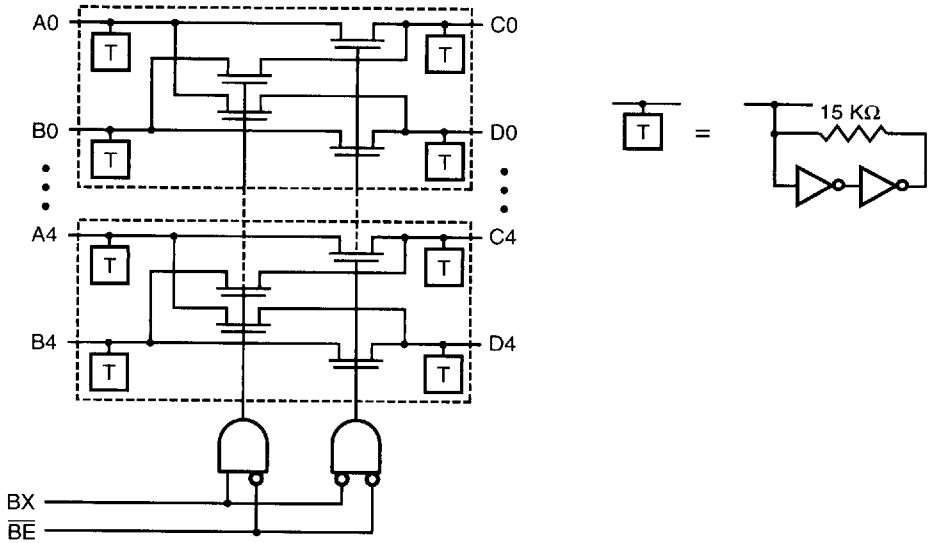
DESCRIPTION

The QS3388 provides two sets of five high-speed CMOS TTL compatible bus switches with active terminators on the bus switch I/O pins. The low ON resistance (5Ω) of the 3388 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. When the switches are turned off, a low drive active terminator circuit drives the disconnected pins to Vcc or ground, away from the TTL threshold. This moves undriven buses from the threshold region to a TTL HIGH or LOW, reducing system noise and power dissipation. The Bus Enable ($\overline{BE}$) signal turns the switches on. The Bus Exchange (BX) signal provides nibble swap of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a five 2-to-1 multiplexer and to create low delay barrel shifters, etc.

FUNCTIONAL BLOCK DIAGRAM

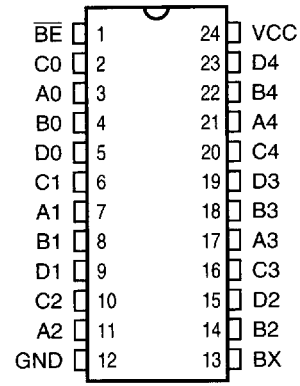


PIN DESCRIPTION

Name	I/O	Function
A4-A0, B4-B0	I/O	Buses A, B
C4-C0, D4-D0	I/O	Buses C, D
$\overline{BE}$	I	Bus Switch Enable
BX	I	Bus Exchange

PIN CONFIGURATION (All Pins Top View)

PDIP, SOIC (SO), QSOP



FUNCTION TABLE

$\overline{BE}$	BX	A4-A0	B4-B0	Function
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C4-C0	D4-D0	Connect
L	H	D4-D0	C4-C0	Exchange

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Switch Voltage V_S	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SOIC Typ	SOIC Max	QSOP Typ	QSOP Max	PDIP Typ	PDIP Max	Unit
Control Pins	3	4	3	4	4	5	pF
QuickSwitch Channels	7	8	7	8	8	9	pF

Note: Capacitance is characterized but not tested.

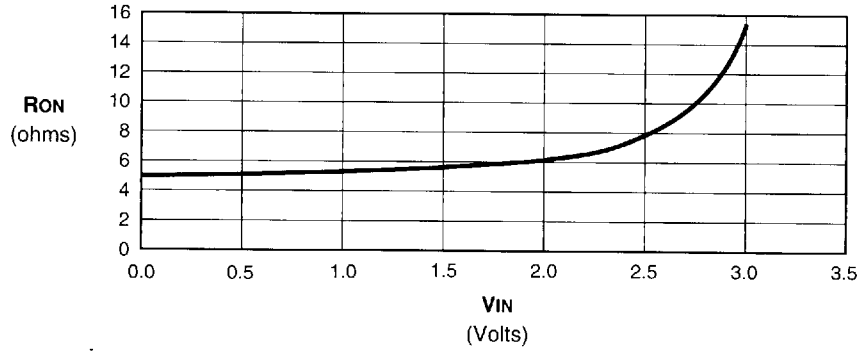
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
$\lvert I_{IN} \rvert$	Input Leakage Current(2)	$0 \le V_{IN} \le V_{CC}$	—	—	5	µA
I_T	Input Current, Disconnect	Vout = 0.5V, 4.5V; V_{CC} = 5V	15	33	70	µA
R_T	Terminator Resistance(6,7)		—	15	—	KΩ
I_{OS}	Short Circuit Current(3)	AB(CD) = 0V, CD(AB) = Vcc	—	300	—	mA
R_{ON}	Switch ON Resistance(4,5)	Vcc = Min., V_{IN} = 0.0V I_{ON} = 30 mA	—	5	7	Ω
R_{ON}	Switch ON Resistance(4,5)	Vcc = Min., V_{IN} = 2.4V I_{ON} = 15 mA	—	10	15	Ω

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. During input/output leakage, testing all pins are at a HIGH or LOW state, and the $\overline{BE}$ control is HIGH.
3. Not more than one output should be used to test this high power condition and the duration is ≤1 second.
4. Measured by voltage drop between AB and CD pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A or B, C or D) pins.
5. Max. value R_{ON} guaranteed but not tested.
6. Characterized but not tested.
7. Computed from parameter "I_T" and the test conditions.

Typical ON Resistance vs V_{IN} at 4.75 Vcc



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc = Max., V_{IN} = GND or Vcc, f = 0	1.5	µA
ΔI_{CC}	Power Supply Current per Input HIGH[2]	Vcc = Max., V_{IN} = 3.4V, f = 0 per Control Input	2.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz[3]	Vcc = Max., A, B, C, D Pins Open, Control Inputs Toggling @ 50% Duty Cycle	0.25	mA/ MHz
Ic	Total Power Supply Current[4,5]	Vcc = Max., A, B, C, D Pins at 0.0V, Control Inputs Toggling @ 50% Duty Cycle Vih = 3.4V, f Clock + MHz	9.0	mA

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V, control inputs only). A, B, C, D pins do not contribute to Icc.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A, B, C, D inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.
4. Ic = I Quiescent + I Inputs + I Dynamic.
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + Q_{CCD} (f_i N_i)$.
   I_{CC} = Power Supply Current for each TTL HIGH input (V_{IN} = 3.4V, control inputs only).
   D_H = Duty Cycle for each TTL input that is HIGH (control inputs only).
   N_T = Number of TTL inputs that are at D_H (control inputs only).
   f_i = frequency that the inputs are toggled (control inputs only).
5. Note that activity on A, B, C, D inputs do not contribute to Ic if A, B, C, D inputs are between GND and Vcc. The switches merely connect and pass through activity on these pins. For example: If the control inputs are at 0V and the switches are on, Ic will be equal to Icc only regardless of activity on the A, B, C, D pins.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	QS3388 Min	QS3388 Typ	QS3388 Max	Unit
t_{PLH} t_{PHL}	Data Propagation Delay[2,3] AiBi to CiDi, CiDi to AiBi	—	—	0.25[3]	ns
t_{PZL} t_{PZH}	Switch Turn-on Delay[1] $\overline{BE}$ to Ai, Bi, Ci, Di	1.5	—	6.5	ns
t_{PLZ} t_{PHZ}	Switch Turn-off Delay[1,2] $\overline{BE}$ to Ai, Bi, Ci, Di	1.5	—	5.5	ns
t_{BX}	Switch Multiplex Delay[1] BX to Ai, Bi, Ci, Di[1]	1.5	—	6.5	ns
$\lvert Q_{CI} \rvert$	Charge Injection[2,4]	—	1.5	—	pC
$\lvert Q_{DCI} \rvert$	Differential Charge Injection[2,5]	—	<0.5	—	pC

Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, V_{IN} at A = 0.0V.
5. Measured at switch turn off through bus multiplex, A to C ≥ A to D, B connected to C, load = 50 pF in parallel with 10 meg scope probe, V_{IN} at A = 0.0V. Charge injection is reduced because the injection from the turn off of the A to C switch is compensated by the turn on of the B to C switch.

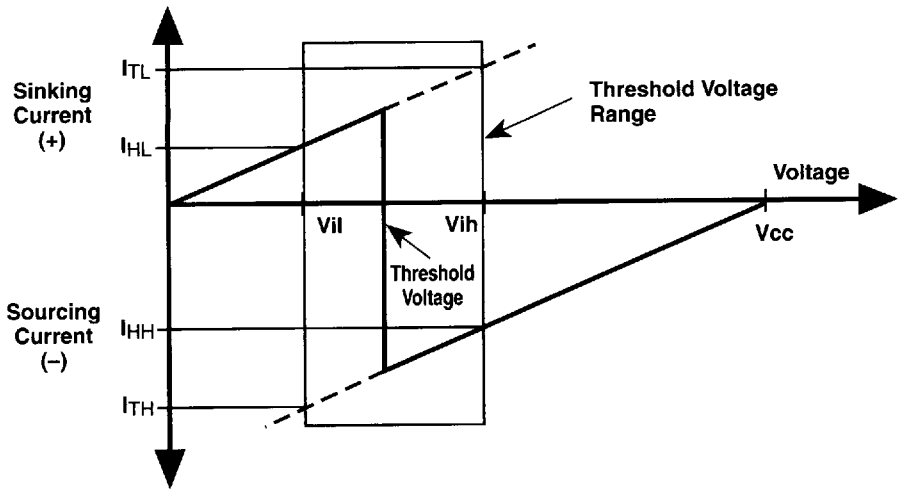


Figure 1: Trip and Hold Current Characteristics of the Last Value Latch

TTL Logic device datasheets specify V_{IL} and V_{IH} values which guarantee that HIGH and LOW logic level inputs will be interpreted correctly. V_{IL} and V_{IH} specifications accommodate variations over temperature and voltage of the inherent switching point of the device, commonly referred to as the threshold voltage. Threshold voltage could theoretically exist anywhere between V_{IL} and V_{IH}.

Figure 1 shows V-I characteristics of the terminator circuit. It demonstrates that as a forced input voltage increases from 0V (logic LOW), the sink current increases linearly. Conversely, if a current is forced into the device, then terminator voltage will gradually increase until V_{IL} is violated. This current value is the hold current for logic LOW (I_{HL}). Higher values of sink current will violate system V_{IL} levels. At some point, if sink current increases further, the terminator voltage will reach the switching threshold and the device will switch to logic HIGH. Since the maximum possible value of the threshold (allowed by spec) is V_{IH}, maximum trip current (I_{TL}) is specified as the current required to force the device up to V_{IH}.

If a terminator input signal is at V_{CC}, the node current is 0 µA, but if V_{IN} is forced downward, the node current gradually increases. If enough current is pulled from the terminator, system V_{IH} will be violated (I_{HH}). Since the minimum possible switching threshold is V_{IL}, I_{TH} is defined as the current required for the high signal to be forced to V_{IL}. Note that I_{TL} and I_{TH} are theoretical numbers. They will never be reached in practical situations since threshold voltage always lies between the V_{IL} and V_{IH} specifications.