AT91CAP9A-DK Development Kit

User Guide

6321B–CAP–02-Jul-07

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Section 1

AT91CAP9A-DK Development Board and AT91CAP-DKM Motherboard Overview

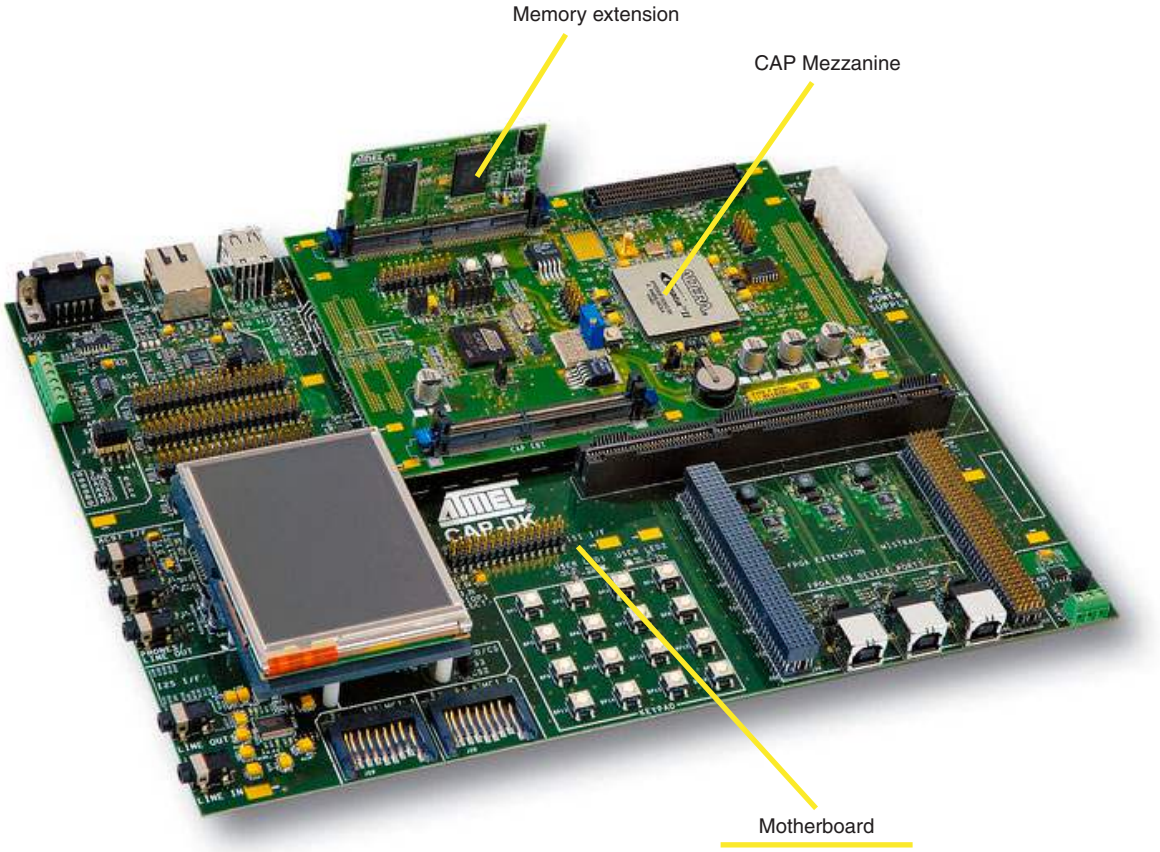
1.1 Scope

The AT91CAP9/Altera® development board (AT91CAP9A-DK) or “kit” is composed of three associated boards, namely **Motherboard, Mezzanine** and **Memory Extension** to be used jointly in order to develop AT91CAP9 processor applications.

The AT91CAP9A-DK development board implements the fixed portion of the AT91CAP9 device as a microcontroller standard product, tightly coupled to a high-density FPGA that emulates the MP Block. The boards also include a range of memories and physical interfaces/connectors representing external system components. This configuration enables parallel hardware/software testing of the application under development at close to operational speed, with no penalty for hardware modifications. This enables software development to proceed in parallel with hardware development, and significantly reduces the design cycle time, increasing confidence in a right-first-time system solution.

Section 1 through **Section 4** provide essential usage documentation for the AT91CAP-DKM **Motherboard**.

Figure 1-1. Overview of AT91CAP9A-DK Development Kit/AT91CAP-DKM Motherboard



1.2 Purpose

The AT91CAP-DKM Motherboard provides all the service items of an AT91CAP9A-DK development system. That is:

- Power supply input, conversion and distribution,
- Standard user interfaces,
- Prototyping interface and extension means.

Section 2

Setting Up the AT91CAP-DKM Motherboard

2.1 Electrostatic Warning

Upon delivery, the AT91CAP-DKM motherboard is wrapped in a protective anti-static bag. The board must not be exposed to electrostatic discharges. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other on-board metallic element.

2.2 Requirements

In order to set up an AT91CAP9A-DK development system, the following items are needed:

- AT91CAP-DKM motherboard
- PC/ATX standard power supply unit
- AT91CAP9A-DKZ mezzanine board (see Sections 5 through 8), with a memory extension (see sections 9 through 14)

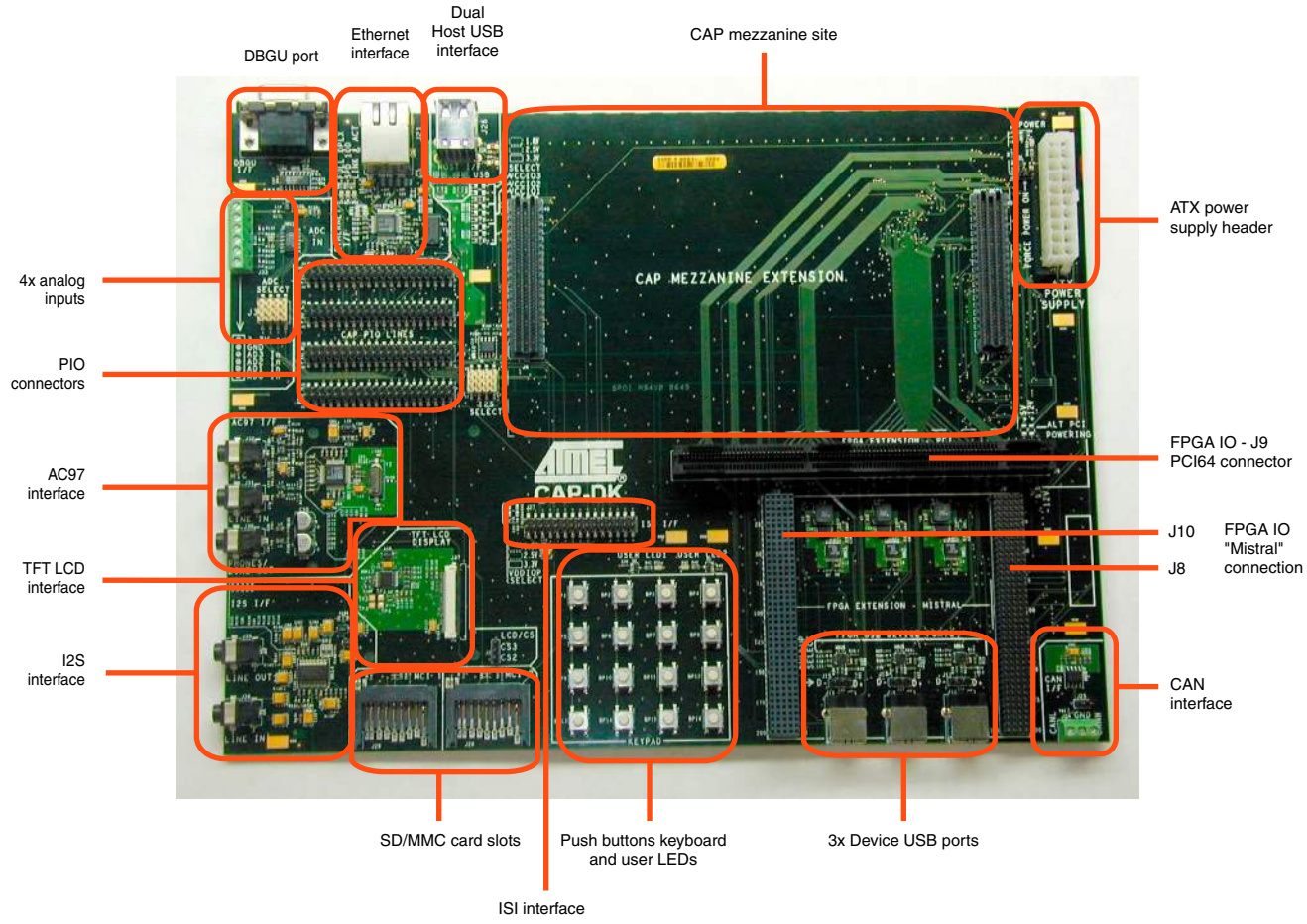
2.3 Layout

The AT91CAP-DKM motherboard features the following on-board interfaces:

- ATX power supply connector
- 2x Full-speed Host USB interfaces
- 100-base TX Ethernet PHY with three status LEDs
- DBGU serial communication port
- 4x analog inputs
- AC97 interface with three 3.5 mm audio jack connectors (MIC IN, LINE IN, LINE OUT)
- I2S audio codec with two 3.5 mm audio jack connectors (LINE IN, LINE OUT)
- 2x SD/MMC card slots
- Atmel TWI serial EEPROM
- 1/4 inch TFT LCD VGA interface
- Touch Screen Controller
- Image Sensor expansion connector
- 16 push buttons arranged in a keypad form
- CAN bus interface
- Software controlled Power LED
- 2x general-purpose LEDs

- PIO expansion connectors (PIOA, PIOB, PIOC, PIOD)
- CAP Mezzanine extension connectors (2x 320 pins)
- PCI64 form FPGA I/O extension connector
- Custom mezzanine-style FPGA I/O extension connector
- 3x USB device PHY interfaces with USB B connectors (FPGA controlled)

Figure 2-1. AT91CAP-DKM Motherboard Layout - Top View



2.4 Powering Up the Board

A complete AT91CAP9A-DK system is powered through the AT91CAP-DKM motherboard via a standard ATX PC power supply.

The power control signal is connected to the SHDN signal, generated by the AT91CAP9 chip from the AT91CAP9A-DKZ mezzanine board.

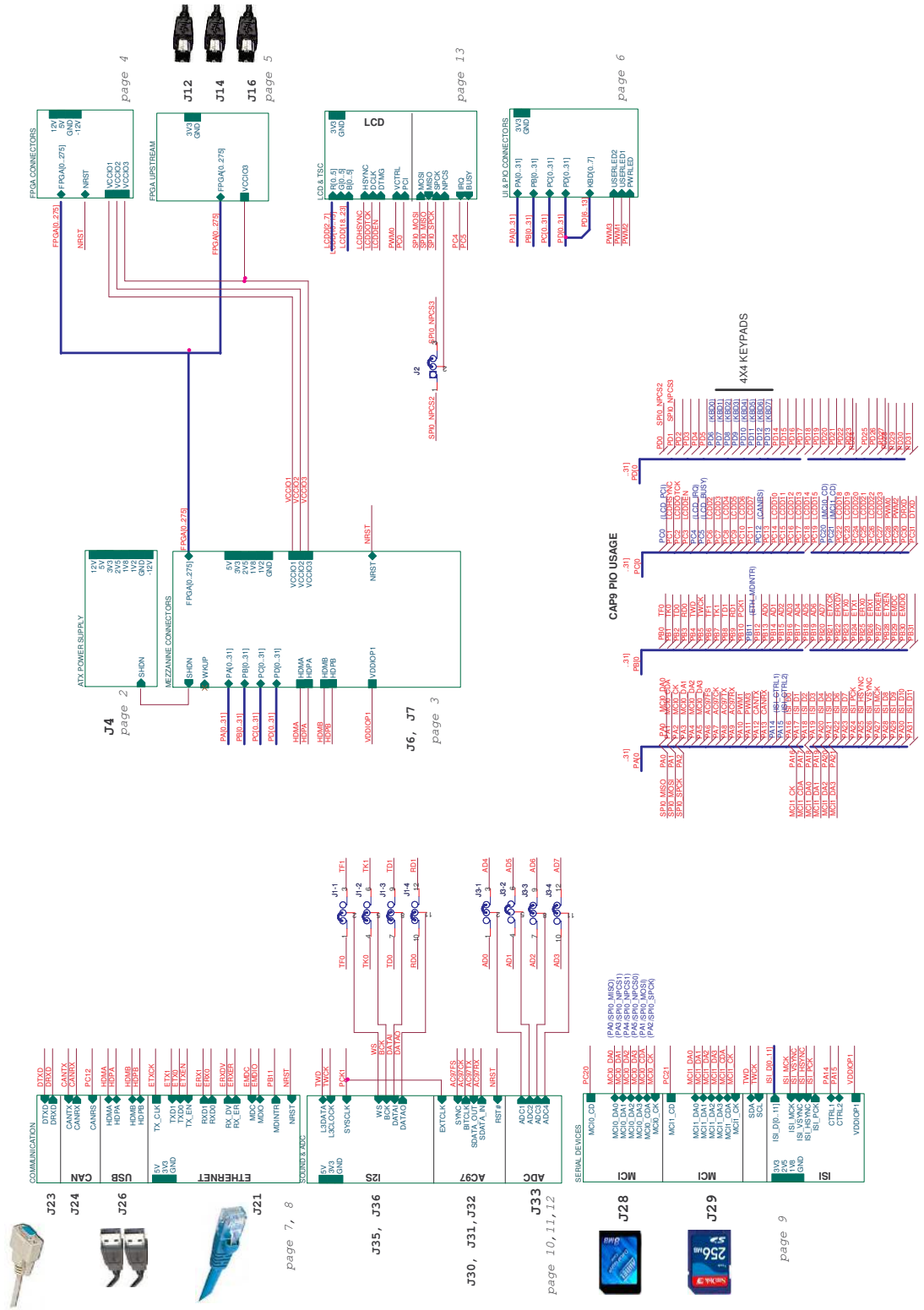
In case the AT91CAP-DKM motherboard has to be powered without a mezzanine or an AT91CAP9 chip in place, the “Force Power ON” jumper J5 must be installed.

Section 3

AT91CAP-DKM Motherboard

3.1 Block Diagram

Figure 3-1. AT91CAP-DKM Motherboard (see the complete schematic in Section 15, “AT91CAP-DKM Schematics”



3.2 Clock Circuity

There are two on-board clock sources:

- 24.576 MHz standard crystal for the AC97 audio interface
- 50.000 MHz oscillator for the RMII Ethernet interface

3.3 Reset Circuity

The AT91CAP9A-DKZ mezzanine board generates the NRST signal for the whole system.

3.4 Shutdown Controller

The SHDN signal issued by the Reset Controller of the AT91CAP9 chip is provided by the AT91CAP9A-DKZ mezzanine board and routed to the ATW connector, in order to control the power supply unit.

As explained in Section 2.4 “Powering Up the Board” on page 2-2, the remote controlling of the power supply can be bypassed with jumper J5.

3.5 Power Supply Circuity

The AT91CAP-DKM motherboard derives the necessary system voltages from the ATX supply.

On-board switching regulators provide the following voltage sources:

- 1.2V
- 1.8V
- 2.5V

3.6 Memory

The only memory resource available on the AT91CAP-DKM motherboard is an Atmel serial EEPROM (TWI bus connection).

System memory resources are to be connected directly to the AT91CAP9A-DKZ mezzanine via the AT91CAP9-MEMxx extension boards.

3.7 Remote Communication

3.7.1 CAN Interface

The AT91CAP-DKM board features one serial CAN 2.0B communication port which is physically connected to a J24 3-way screw-style connector.

An on-board standard 120-Ohm terminator is available. Simply install jumper J25 to enable termination.

3.7.2 Host USB Interface

A dual host connection (J26 = dual Type A socket) is available on the AT91CAP-DKM motherboard.

These two ports are routed directly from/to the AT91CAP9 chip installed on the mezzanine. In function of the AT91CAP9 chip connected in the system, these two ports can be non operating. For further information, please refer to the documentation specific to the mezzanine you intend to use.

3.7.3 Device USB Interface

Please refer to Section 3.14 “FPGA Extension” on page 3-5.

3.7.4 Ethernet Interface

On-board RMII 100-base TX PHY: DM9161 MN7 connected to a standard RJ45 socket J21. Three status LEDs (DS4, 5, 6) provide network activity feedback.

3.8 Audio Stereo Interface

3.8.1 AC97

One AC97 2.3 compliant Codec (MN11 = AD1981B, 20-bit PCM DAC) with the following connectors:

- 32-ohm stereo headset line-out
- stereo line input
- stereo electret microphone input

This interface has some configuration elements. Please refer to Section 4 “AT91CAP-DKM Configuration” and/or “AT91CAP-DKM Schematics” for in-depth details.

3.8.2 I2S

One I2S audio codec MN14 = UDA1342TS with the following connectors:

- line-out
- line-in

3.9 Analog Interface

Four analog inputs (range up to 3.3V). These are available through the J33 connector and are buffered by a quadruple gain-1 amplifier, MN12 = AD8040ARZ.

These four buffered signals can be connected to the eight AT91CAP9 analog input channels via the four configuration jumpers J3-1 to J3-4. Refer to Table 4-1 for more details.

3.10 User Interface

The various items interfaced with the AT91CAP-DKM motherboard are all driven by the PIO busses of the AT91CAP9 chip. (Refer to “AT91CAP-DKM Schematics” for detailed assignation)

- 4x4 keypad: uses 8 PIO lines in a matrix scheme, each button shunts two of them
- Two green LEDs
- One yellow power LED (note that it is software controlled)
- One 3.5 inch VGA display LCD with Touch Panel and white LED backlight

- One ISI connector (camera interface)

3.11 Debug Interface

The AT91CAP standard serial debug interface (DBGU) is carried through the DB9 male socket, J23. It is routed to the DBGU port of the AT91CAP9 chip installed on the mezzanine.

3.12 Memory Expansion Slots

Two memory card dedicated connectors:

- J28 for DataFlash, SD/SDIO/MMC card slot
- J29 for SD/SDIO/MMC card slot

Note that both adopt the same connector but that J28 is also DataFlash® compatible due to its signal muxing (refer to "PIO Usage" on page 3-24, (PIO A muxing table) and "AT91CAP-DKM Schematics").

3.13 PIO Connectors

All PIOs of the AT91CAP9 are routed to peripheral extension connectors (J17 to J20). This allows the developer to add external hardware components or boards.

Note: Most of the PIO lines already have an assignment on board. Therefore be aware of the schematic routing prior to customizing these lines in any way. Do not cause electrical contention as this may potentially damage the boards and the AT91CAP9 chip.

3.14 FPGA Extension

3.14.1 Overview

The AT91CAP-DKM motherboard routes most of the FPGA IOs coming from the mezzanine to on-board prototyping ports (free for custom user board implementation). These are grouped on sheet 4/13 of Section 15 "AT91CAP-DKM Schematics":

- J9 = PCI64 female connector for FPGA I/O expansion
- J8/J10 = two 200-pin connectors for "Mistral" extension board

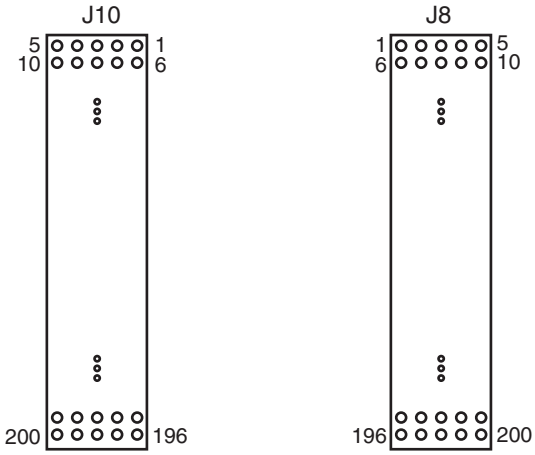
Warning: FPGA IOs are distributed among J8, J9 and J10 connectors and also the three USB device ports, some having dual connections as follows:

Table 3-1. FPGA IO Overlapping Table

Net Name Range	J8	J10	J9	USB
FPGA000 FPGA001 FPGA004..FPGA 093 FPGA098..FPGA117	X			
FPGA250..FPGA 252 FPGA260..FPGA 262	X		X	
FPGA118..FPGA174		X		
FPGA175..FPGA 189 FPGA191..FPGA 228 FPGA270		X	X	
FPGA229..FPGA245			X	
FPGA190 FPGA246..FPGA 249 FPGA253..FPGA 259 FPGA263..FPGA 269 FPGA271..FPGA 275			X	X
FPGA002 FPGA003 FPGA094..FPGA 097				X

3.14.2 AT91CAP-DKM Extension Connectors

Figure 3-2. J8 and J10 (Top View)



J8 and J10 as seen on AT91CAP9-DKM from above

3.14.3 “Mistral” Extension Connectors

Pins not listed in Table 3-2 below are not connected.

Table 3-2. J-8 (male) Pin Assignment Table

J8 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
1	B1	IO	CLK2p/DIFFIO_RX_C1p	U32	FPGA0
2					GND
3	B1	IO	CLK2n/DIFFIO_RX_C1n	U31	FPGA1
4					GND
5	B3	IO	DQ15T	E26	FPGA250
6	B3	IO		F21	FPGA251
7					GND
8	B1	IO	DIFFIO_RX28p	V31	FPGA4
9					GND
10	B1	IO	DIFFIO_RX28n	V30	FPGA5
11	B1	IO	DIFFIO_TX28p	U23	FPGA6
12					GND
13	B1	IO	DIFFIO_TX28n	U22	FPGA7
14					GND
15	B1	IO	DIFFIO_RX27p	W32	FPGA8
16	B1	IO	DIFFIO_RX27n	W31	FPGA9
17					GND
18	B1	IO	DIFFIO_TX27p	U28	FPGA10
19					GND
20	B1	IO	DIFFIO_TX27n	U27	FPGA11
21	B1	IO	DIFFIO_RX26p	AA32	FPGA12
22					GND
23	B1	IO	DIFFIO_RX26n	AA31	FPGA13
24					GND
25	B1	IO	DIFFIO_TX26p	V29	FPGA14
26	B1	IO	DIFFIO_TX26n	V28	FPGA15
27					GND
28	B1	IO	DIFFIO_RX25p	Y31	FPGA16
29					GND
30	B1	IO	DIFFIO_RX25n	Y30	FPGA17
31	B1	IO	DIFFIO_TX25p	V24	FPGA18
32					GND
33	B1	IO	DIFFIO_TX25n	V23	FPGA19
34					GND
35	B1	IO	DIFFIO_RX24p	AB32	FPGA20
36	B1	IO	DIFFIO_RX24n	AB31	FPGA21

Table 3-2. J-8 (male) Pin Assignment Table (Continued)

J8 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
37					GND
38	B1	IO	DIFFIO_TX24p	W29	FPGA22
39					GND
40	B1	IO	DIFFIO_TX24n	W28	FPGA23
41	B1	IO	DIFFIO_RX23p	AA30	FPGA24
42					GND
43	B1	IO	DIFFIO_RX23n	AA29	FPGA25
44					GND
45	B1	IO	DIFFIO_TX23p	W27	FPGA26
46	B1	IO	DIFFIO_TX23n	W26	FPGA27
47					GND
48	B1	IO	DIFFIO_RX22p	Y29	FPGA28
49					GND
50	B1	IO	DIFFIO_RX22n	Y28	FPGA29
51	B1	IO	DIFFIO_TX22p	W25	FPGA30
52					GND
53	B1	IO	DIFFIO_TX22n	W24	FPGA31
54					GND
55	B1	IO	DIFFIO_RX21p	AB30	FPGA32
56	B1	IO	DIFFIO_RX21n	AB29	FPGA33
57					GND
58	B1	IO	DIFFIO_TX21p	Y27	FPGA34
59					GND
60	B1	IO	DIFFIO_TX21n	Y26	FPGA35
61	B1	IO	DIFFIO_RX20p	AC32	FPGA36
62					GND
63	B1	IO	DIFFIO_RX20n	AC31	FPGA37
64					GND
65	B1	IO	DIFFIO_TX20p	AA27	FPGA38
66	B1	IO	DIFFIO_TX20n	AA26	FPGA39
67					GND
68	B1	IO	DIFFIO_RX19p	AB28	FPGA40
69					GND
70	B1	IO	DIFFIO_RX19n	AB27	FPGA41
71	B1	IO	DIFFIO_TX19p	Y25	FPGA42
72					GND

Table 3-2. J-8 (male) Pin Assignment Table (Continued)

J8 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
73	B1	IO	DIFFIO_TX19n	Y24	FPGA43
74					GND
75	B1	IO	DIFFIO_RX18p	AD32	FPGA44
76	B1	IO	DIFFIO_RX18n	AD31	FPGA45
77					GND
78	B1	IO	DIFFIO_TX18p	W23	FPGA46
79					GND
80	B1	IO	DIFFIO_TX18n	W22	FPGA47
81	B1	IO	DIFFIO_RX17p	AE32	FPGA48
82					GND
83	B1	IO	DIFFIO_RX17n	AE31	FPGA49
84					GND
85	B1	IO	DIFFIO_TX17p	AD27	FPGA50
86	B1	IO	DIFFIO_TX17n	AD26	FPGA51
87					GND
88	B1	IO	DIFFIO_RX16p	AF32	FPGA52
89					GND
90	B1	IO	DIFFIO_RX16n	AF31	FPGA53
91	B1	IO	DIFFIO_TX16p	AC27	FPGA54
92					GND
93	B1	IO	DIFFIO_TX16n	AC26	FPGA55
94					GND
95	B1	IO	DIFFIO_RX15p	AG32	FPGA56
96					NRST
97					GND
98	B1	IO	DIFFIO_RX15n	AG31	FPGA57
99					GND
100	B1	IO	DIFFIO_TX15p	Y23	FPGA58
101	B1	IO	DIFFIO_TX15n	Y22	FPGA59
102					GND
103	B1	IO	DIFFIO_RX14p	AC30	FPGA60
104					GND
105	B1	IO	DIFFIO_RX14n	AC29	FPGA61
106	B1	IO	DIFFIO_TX14p	AA25	FPGA62
107					GND
108	B1	IO	DIFFIO_TX14n	AA24	FPGA63

Table 3-2. J-8 (male) Pin Assignment Table (Continued)

J8 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
109					GND
110	B1	IO	DIFFIO_RX13p	AD30	FPGA64
111	B1	IO	DIFFIO_RX13n	AD29	FPGA65
112					GND
113	B1	IO	DIFFIO_TX13p	AB26	FPGA66
114					GND
115	B1	IO	DIFFIO_TX13n	AB25	FPGA67
116	B1	IO	DIFFIO_RX12p	AH32	FPGA68
117					GND
118	B1	IO	DIFFIO_RX12n	AH31	FPGA69
119					GND
120	B1	IO	DIFFIO_TX12p	AA23	FPGA70
121	B1	IO	DIFFIO_TX12n	AA22	FPGA71
122					GND
123	B1	IO	DIFFIO_RX11p	AE30	FPGA72
124					GND
125	B1	IO	DIFFIO_RX11n	AE29	FPGA73
126	B1	IO	DIFFIO_TX11p	AB24	FPGA74
127					GND
128	B1	IO	DIFFIO_TX11n	AB23	FPGA75
129					GND
130	B1	IO	DIFFIO_RX10p	AJ32	FPGA76
131	B1	IO	DIFFIO_RX10n	AJ31	FPGA77
132					GND
133	B1	IO	DIFFIO_TX10p	AC25	FPGA78
134					GND
135	B1	IO	DIFFIO_TX10n	AC24	FPGA79
136	B1	IO	DIFFIO_RX9p	AF30	FPGA80
137					GND
138	B1	IO	DIFFIO_RX9n	AF29	FPGA81
139					GND
140	B1	IO	DIFFIO_TX9p	AD25	FPGA82
141	B1	IO	DIFFIO_TX9n	AD24	FPGA83
142					GND
143	B1	IO	DIFFIO_RX8p	AG30	FPGA84
144					GND

Table 3-2. J-8 (male) Pin Assignment Table (Continued)

J8 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
145	B1	IO	DIFFIO_RX8n	AG29	FPGA85
146	B1	IO	DIFFIO_TX8p	AE26	FPGA86
147					GND
148	B1	IO	DIFFIO_TX8n	AE25	FPGA87
149					GND
150	B1	IO	DIFFIO_RX7p	AH30	FPGA88
151	B1	IO	DIFFIO_RX7n	AH29	FPGA89
152					GND
153	B1	IO	DIFFIO_TX7p	AE28	FPGA90
154					GND
155	B1	IO	DIFFIO_TX7n	AE27	FPGA91
156	B1	IO	DIFFIO_RX6p	AF28	FPGA92
157					GND
158	B1	IO	DIFFIO_RX6n	AF27	FPGA93
159					GND
160	B3	IO	DQS16T	B27	FPGA252
161	B3	IO	DQS17T	C28	FPGA260
162					GND
163	B3	IO	DQ17T	B29	FPGA261
164					GND
165	B3	IO	DQ17T	A29	FPGA262
166	B2	IO	DIFFIO_TX51p	K25	FPGA98
167					GND
168	B2	IO	DIFFIO_TX51n	K24	FPGA99
169					GND
170	B2	IO	DIFFIO_RX50p	G28	FPGA100
171	B2	IO	DIFFIO_RX50n	G27	FPGA101
172					GND
173	B2	IO	DIFFIO_TX50p	H28	FPGA102
174					GND
175	B2	IO	DIFFIO_TX50n	H27	FPGA103
176	B2	IO	DIFFIO_RX49p	E30	FPGA104
177					GND
178	B2	IO	DIFFIO_RX49n	E29	FPGA105
179					GND
180	B2	IO	DIFFIO_TX49p	K27	FPGA106

Table 3-2. J-8 (male) Pin Assignment Table (Continued)

J8 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
181	B2	IO	DIFFIO_TX49n	K26	FPGA107
182					GND
183	B2	IO	DIFFIO_RX48p	D32	FPGA108
184					GND
185	B2	IO	DIFFIO_RX48n	D31	FPGA109
186	B2	IO	DIFFIO_TX48p	J27	FPGA110
187					GND
188	B2	IO	DIFFIO_TX48n	J26	FPGA111
189					GND
190	B2	IO	DIFFIO_RX47p	F30	FPGA112
191	B2	IO	DIFFIO_RX47n	F29	FPGA113
192					GND
193	B2	IO	DIFFIO_TX47p	L28	FPGA114
194					GND
195	B2	IO	DIFFIO_TX47n	L27	FPGA115
196	B2	IO	DIFFIO_RX46p	G30	FPGA116
197					GND
198	B2	IO	DIFFIO_RX46n	G29	FPGA117
199					GND

Pins not listed in Table 3-3 below are not connected.

Table 3-3. J10 (female) Pin Assignment Table

J10 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
1	B2	IO	DIFFIO_TX46p	L26	FPGA118
2					GND
3	B2	IO	DIFFIO_TX46n	L25	FPGA119
4					GND
5	B2	IO	DIFFIO_RX45p	H30	FPGA120
6	B2	IO	DIFFIO_RX45n	H29	FPGA121
7					GND
8	B2	IO	DIFFIO_TX45p	L24	FPGA122
9					GND
10	B2	IO	DIFFIO_TX45n	L23	FPGA123
11	B2	IO	DIFFIO_RX44p	J30	FPGA124
12					GND

Table 3-3. J10 (female) Pin Assignment Table (Continued)

J10 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
13	B2	IO	DIFFIO_RX44n	J29	FPGA125
14					GND
15	B2	IO	DIFFIO_TX44p	M25	FPGA126
16	B2	IO	DIFFIO_TX44n	M24	FPGA127
17					GND
18	B2	IO	DIFFIO_RX43p	E32	FPGA128
19					GND
20	B2	IO	DIFFIO_RX43n	E31	FPGA129
21	B2	IO	DIFFIO_TX43p	M23	FPGA130
22					GND
23	B2	IO	DIFFIO_TX43n	M22	FPGA131
24					GND
25	B2	IO	DIFFIO_RX42p	F32	FPGA132
26	B2	IO	DIFFIO_RX42n	F31	FPGA133
27					GND
28	B2	IO	DIFFIO_TX42p	M27	FPGA134
29					GND
30	B2	IO	DIFFIO_TX42n	M26	FPGA135
31	B2	IO	DIFFIO_RX41p	G32	FPGA136
32					GND
33	B2	IO	DIFFIO_RX41n	G31	FPGA137
34					GND
35	B2	IO	DIFFIO_TX41p	N25	FPGA138
36	B2	IO	DIFFIO_TX41n	N24	FPGA139
37					GND
38	B2	IO	DIFFIO_RX40p	H32	FPGA140
39					GND
40	B2	IO	DIFFIO_RX40n	H31	FPGA141
41	B2	IO	DIFFIO_TX40p	N23	FPGA142
42					GND
43	B2	IO	DIFFIO_TX40n	N22	FPGA143
44					GND
45	B2	IO	DIFFIO_RX39p	J32	FPGA144
46	B2	IO	DIFFIO_RX39n	J31	FPGA145
47					GND
48	B2	IO	DIFFIO_TX39p	P23	FPGA146

Table 3-3. J10 (female) Pin Assignment Table (Continued)

J10 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
49					GND
50	B2	IO	DIFFIO_TX39n	P22	FPGA147
51	B2	IO	DIFFIO_RX38p	K30	FPGA148
52					GND
53	B2	IO	DIFFIO_RX38n	K29	FPGA149
54					GND
55	B2	IO	DIFFIO_TX38p	N27	FPGA150
56	B2	IO	DIFFIO_TX38n	N26	FPGA151
57					GND
58	B2	IO	DIFFIO_RX37p	K32	FPGA152
59					GND
60	B2	IO	DIFFIO_RX37n	K31	FPGA153
61	B2	IO	DIFFIO_TX37p	P29	FPGA154
62					GND
63	B2	IO	DIFFIO_TX37n	P28	FPGA155
64					GND
65	B2	IO	DIFFIO_RX36p	L30	FPGA156
66	B2	IO	DIFFIO_RX36n	L29	FPGA157
67					GND
68	B2	IO	DIFFIO_TX36p	P27	FPGA158
69					GND
70	B2	IO	DIFFIO_TX36n	P26	FPGA159
71	B2	IO	DIFFIO_RX35p	N29	FPGA160
72					GND
73	B2	IO	DIFFIO_RX35n	N28	FPGA161
74					GND
75	B2	IO	DIFFIO_TX35p	P25	FPGA162
76	B2	IO	DIFFIO_TX35n	P24	FPGA163
77					GND
78	B2	IO	DIFFIO_RX34p	M30	FPGA164
79					GND
80	B2	IO	DIFFIO_RX34n	M29	FPGA165
81	B2	IO	DIFFIO_TX34p	R27	FPGA166
82					GND
83	B2	IO	DIFFIO_TX34n	R26	FPGA167
84					GND

Table 3-3. J10 (female) Pin Assignment Table (Continued)

J10 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
85	B2	IO	DIFFIO_RX33p	L32	FPGA168
86	B2	IO	DIFFIO_RX33n	L31	FPGA169
87					GND
88	B2	IO	DIFFIO_TX33p	R23	FPGA170
89					GND
90	B2	IO	DIFFIO_TX33n	R22	FPGA171
91	B2	IO	DIFFIO_RX32p	N31	FPGA172
92					GND
93	B2	IO	DIFFIO_RX32n	N30	FPGA173
94					GND
95	B2	IO	DIFFIO_TX32p	R25	FPGA174
96	B2	CLK1p	INPUT	T30	FPGA175
97					GND
98	B2	IO	DIFFIO_RX31p	M32	FPGA176
99					GND
100	B2	IO	DIFFIO_RX31n	M31	FPGA177
101	B2	IO	DIFFIO_TX31p	R29	FPGA178
102					GND
103	B2	IO	DIFFIO_TX31n	R28	FPGA179
104					GND
105	B2	IO	DIFFIO_RX30p	P32	FPGA180
106	B2	IO	DIFFIO_RX30n	P31	FPGA181
107					GND
108	B2	IO	DIFFIO_TX30p	T28	FPGA182
109					GND
110	B2	IO	DIFFIO_TX30n	T27	FPGA183
111	B2	IO	DIFFIO_RX29p	R31	FPGA184
112					GND
113	B2	IO	DIFFIO_RX29n	R30	FPGA185
114					GND
115	B2	IO	DIFFIO_TX29p	T23	FPGA186
116	B2	IO	DIFFIO_TX29n	T22	FPGA187
117					GND
118	B2	IO	CLK0n/DIFFIO_RX_C0n	T31	FPGA188
119					GND
120	B2	IO	CLK0p/DIFFIO_RX_C0p	T32	FPGA189

Table 3-3. J10 (female) Pin Assignment Table (Continued)

J10 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
121	B3	IO		H23	FPGA270
122					GND
123	B2	IO	DIFFIO_TX32n	R24	FPGA191
124					GND
125	B3	IO	CLK14p	A17	FPGA192
126	B3	IO	CLK14n	B17	FPGA193
127					GND
128	B3	IO	CLK15p	C17	FPGA194
129					GND
130	B3	IO	CLK15n	D17	FPGA195
131	B3	IO		K18	FPGA196
132					GND
133	B3	IO		F18	FPGA197
134					GND
135	B3	IO		F19	FPGA198
136	B3	IO		E17	FPGA199
137					GND
138	B3	IO		G20	FPGA200
139					GND
140	B3	IO		F20	FPGA201
141	B3	IO	DQS10T	D19	FPGA202
142					GND
143	B3	IO	DQ10T	B20	FPGA203
144					GND
145	B3	IO	DQ10T	E19	FPGA204
146	B3	IO	DQ10T	C20	FPGA205
147					GND
148	B3	IO	DQSn10T	D20	FPGA206
149					GND
150	B3	IO	DQ10T	E20	FPGA207
151	B3	IO		L19	FPGA208
152					GND
153	B3	IO		L18	FPGA209
154					GND
155	B3	IO		J19	FPGA210
156	B3	IO		K19	FPGA211

Table 3-3. J10 (female) Pin Assignment Table (Continued)

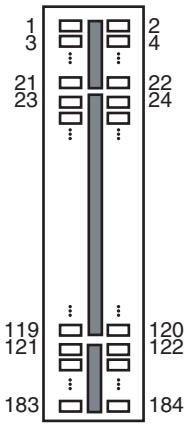
J10 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
157					GND
158	B3	IO	DQS11T	B21	FPGA212
159					GND
160	B3	IO	DQ11T	A21	FPGA213
161	B3	IO	DQ11T	C21	FPGA214
162					GND
163	B3	IO	DQ11T	A22	FPGA215
164					GND
165	B3	IO	DQSn11T	B22	FPGA216
166	B3	IO	DQ11T	C22	FPGA217
167					GND
168	B3	IO		L20	FPGA218
169					GND
170	B3	IO		H20	FPGA219
171	B3	IO		K20	FPGA220
172					GND
173	B3	IO	DQS12T	D22	FPGA221
174					GND
175	B3	IO	DQ12T	D23	FPGA222
176	B3	IO	DQ12T	D21	FPGA223
177					GND
178	B3	IO	DQ12T	F22	FPGA224
179					GND
180	B3	IO	DQSn12T	E22	FPGA225
181	B3	IO	DQ12T	F23	FPGA226
182					GND
183	B3	IO		L21	FPGA227
184					GND
185	B3	IO		J20	FPGA228
187					GND
189					GND
191					VCCIO1
192					GND
193					VCCIO2
194					GND
195					VCCIO3

Table 3-3. J10 (female) Pin Assignment Table (Continued)

J10 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
196					VCCIO1
197					GND
198					VCCIO2
199					GND
200					VCCIO3

3.14.3.1 PCI64 Extension Connector

Figure 3-3. J9 Pinout (Top view)



J9 as seen on AT91CAP9-DKM from above

Pins not listed in Table 3-4 below are not connected.

Table 3-4. PCI64 Extension Connector Table

J9 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
1	B2	IO	DIFFIO_TX31n	R28	FPGA179
2					-12VPCI
3					12VPCI
4	B2	IO	DIFFIO_RX31p	M32	FPGA176
5	B2	IO	DIFFIO_RX31n	M31	FPGA177
6					GND
7	B2	IO	DIFFIO_TX31p	R29	FPGA178
8	B2	CLK1p	INPUT	T30	FPGA175
9					5VPCI
10					5VPCI
11	B2	IO	DIFFIO_RX30p	P32	FPGA180
12					5VPCI

Table 3-4. PCI64 Extension Connector Table (Continued)

J9 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
13	B2	IO	DIFFIO_TX30p	T28	FPGA182
14	B2	IO	DIFFIO_RX30n	P31	FPGA181
15					5VPCI
16	B2	IO	DIFFIO_TX30n	T27	FPGA183
18	B2	IO	DIFFIO_RX29p	R31	FPGA184
19					VCCIO2
22	B2	IO	DIFFIO_RX29n	R30	FPGA185
26					GND
27					VCCIO2
28	B2	IO	DIFFIO_TX29p	T23	FPGA186
29	B2	IO	DIFFIO_TX29n	T22	FPGA187
30					GND
31					GND
32	B2	CLK1n	INPUT	T29	FPGA190
34					VCCIO2
35	B2	IO	CLK0p/DIFFIO_RX_C0p	T32	FPGA189
36	B2	IO	CLK0n/DIFFIO_RX_C0n	T31	FPGA188
37					VCCIO2
38	B2	IO	DIFFIO_TX32n	R24	FPGA191
39	B3	IO	CLK14p	A17	FPGA192
40					GND
41	B3	IO	CLK14n	B17	FPGA193
42	B3	IO	CLK15p	C17	FPGA194
43					GND
44	B3	IO	CLK15n	D17	FPGA195
45	B3	IO		K18	FPGA196
46					VCCIO3
47	B3	IO		F18	FPGA197
48	B3	IO		F19	FPGA198
49					VCCIO3
50	B3	IO		E17	FPGA199
51	B3	IO		G20	FPGA200
52					GND
53	B3	IO		F20	FPGA201
54	B3	IO	DQS10T	D19	FPGA202
55					GND

Table 3-4. PCI64 Extension Connector Table (Continued)

J9 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
56	B3	IO	DQ10T	B20	FPGA203
57	B3	IO	DQ10T	E19	FPGA204
58					VCCIO3
59	B3	IO	DQ10T	C20	FPGA205
60	B3	IO	DQSn10T	D20	FPGA206
61					VCCIO3
62	B3	IO	DQ10T	E20	FPGA207
63	B3	IO		L19	FPGA208
64					GND
65					GND
66	B3	IO		L18	FPGA209
67	B3	IO		J19	FPGA210
68					VCCIO3
69					GND
70	B3	IO		K19	FPGA211
71	B3	IO	DQS11T	B21	FPGA212
72					GND
73					VCCIO3
74	B3	IO	DQ11T	A21	FPGA213
75	B3	IO	DQ11T	C21	FPGA214
76	B3	IO	DQ11T	A22	FPGA215
77	B3	IO	DQSn11T	B22	FPGA216
78					VCCIO3
79					GND
80	B3	IO	DQ11T	C22	FPGA217
81	B3	IO		L20	FPGA218
82					VCCIO3
83	B3	IO		H20	FPGA219
84	B3	IO		K20	FPGA220
85					VCCIO3
86	B3	IO	DQS12T	D22	FPGA221
87	B3	IO	DQ12T	D23	FPGA222
88					GND
89	B3	IO	DQ12T	D21	FPGA223
90	B3	IO	DQ12T	F22	FPGA224
91					GND

Table 3-4. PCI64 Extension Connector Table (Continued)

J9 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
92	B3	IO	DQSn12T	E22	FPGA225
93	B3	IO	DQ12T	F23	FPGA226
94					GND
95					GND
96					GND
97					GND
98					GND
99	B3	IO		L21	FPGA227
100	B3	IO		J20	FPGA228
101					VCCIO3
102	B3	IO	DQS13T	B23	FPGA229
103	B3	IO	DQ13T	A23	FPGA230
104					VCCIO3
105	B3	IO	DQ13T	C23	FPGA231
106	B3	IO	DQ13T	C24	FPGA232
107					GND
108	B3	IO	DQSn13T	B24	FPGA233
109	B3	IO	DQ13T	A24	FPGA234
110					GND
111	B3	IO		K21	FPGA235
112	B3	IO		H21	FPGA236
113					VCCIO3
114					VCCIO3
115	B3	IO		J21	FPGA237
116	B3	IO	DQS14T	B25	FPGA238
117					5VPCI
118					5VPCI
119					5VPCI
120					5VPCI
121					GND
123	B3	IO	DQ14T	A25	FPGA239
124					GND
125	B3	IO	DQ14T	A26	FPGA240
126	B3	IO	DQ14T	D26	FPGA241
127					VCCIO3
128	B3	IO	DQSn14T	B26	FPGA242

Table 3-4. PCI64 Extension Connector Table (Continued)

J9 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
129	B3	IO	DQ14T	C26	FPGA243
130					GND
131	B3	IO		G21	FPGA244
132	B3	IO	DQS15T	D25	FPGA245
133					GND
134	B3	IO	DQ15T	E24	FPGA246
135	B3	IO	DQ15T	C25	FPGA247
136					VCCIO3
137	B3	IO	DQ15T	E27	FPGA248
138	B3	IO	DQSn15T	E25	FPGA249
139					GND
140	B3	IO	DQ15T	E26	FPGA250
141	B3	IO		F21	FPGA251
142					GND
143	B3	IO	DQS16T	B27	FPGA252
144	B3	IO	DQ16T	A27	FPGA253
145					VCCIO3
146	B3	IO	DQ16T	A28	FPGA254
147	B3	IO	DQ16T	D27	FPGA255
148					GND
149	B3	IO	DQSn16T	B28	FPGA256
150	B3	IO	DQ16T	C27	FPGA257
151					GND
152	B3	IO		H22	FPGA258
153	B3	IO		J22	FPGA259
154					VCCIO3
155	B3	IO	DQS17T	C28	FPGA260
156	B3	IO	DQ17T	B29	FPGA261
157					GND
158	B3	IO	DQ17T	A29	FPGA262
159	B3	IO	DQ17T	D28	FPGA263
160					GND
161	B3	IO	DQSn17T	C29	FPGA264
162	B3	IO	DQ17T	E28	FPGA265
163					VCCIO3
164	B3	IO		K22	FPGA266

Table 3-4. PCI64 Extension Connector Table (Continued)

J9 Pin	FPGA Bank	FPGA Pin Function	Other FPGA Pin Information	FPGA Ball	Board Net
165	B3	IO		F25	FPGA267
166					GND
167	B3	IO		G22	FPGA268
168	B3	IO		G23	FPGA269
169					GND
170	B3	IO		H23	FPGA270
171	B3	IO		J23	FPGA271
172					VCCIO3
173	B3	IO		L22	FPGA272
174	B3	IO		F24	FPGA273
175					GND
176	B3	IO		G24	FPGA274
177	B3	IO		H24	FPGA275
178					GND
181					GND
184					GND

3.14.4 USB Device interfaces

The three USB device interfaces are connected to the FPGA of the AT91CAP9A-DKZ mezzanine. Each of them includes an ISP1501 PHY (MN4, 5, 6). These are attached to USB Type-B connectors with on-board manual jumper selection (J11, 13, 15). This selection makes a pull-up connection to be applied either to D+ or D- and thereby selects the communication speed standard (low speed or full speed).

Warning: Some of these FPGA IOs are shared with extension connectors. Refer to Table 3-1, “FPGA IO Overlapping Table.

Table 3-5. USB Interface and FPGA Connection

FPGA Bank	FPGA Ball	Board Signal	Board Component	Pin	Function
B3	E24	FPGA246	R12	2	VBUS detection
B3	C25	FPGA247	MN4	1	/OE
B3	E27	FPGA248	MN4	5	SUSPEND
B1	U30	FPGA2	MN4	2	RCV
B1	U29	FPGA3	MN4	4	VM
B1	AJ29	FPGA94	MN4	3	VP
B3	A27	FPGA253	MN4	12	VMO/FSEO
B3	A28	FPGA254	MN4	11	VPO/VO
B3	D27	FPGA255	MN4	16	SOFTCON
B3	B28	FPGA256	R21	2	VBUS detection

Table 3-5. USB Interface and FPGA Connection (Continued)

FPGA Bank	FPGA Ball	Board Signal	Board Component	Pin	Function
B3	C27	FPGA257	MN5	1	/OE
B3	H22	FPGA258	MN5	5	SUSPEND
B3	J22	FPGA259	MN5	8	SPEED
B1	AJ30	FPGA95	MN5	2	RCV
B2	D30	FPGA96	MN5	4	VM
B3	D29	FPGA97	MN5	3	VP
B3	D28	FPGA263	MN5	12	VMO/FSEO
B3	C29	FPGA264	MN5	11	VPO/VO
B3	E28	FPGA265	MN5	16	SOFTCON
B3	K22	FPGA266	R30	2	VBUS detection
B3	F25	FPGA267	MN6	1	/OE
B3	G22	FPGA268	MN6	5	SUSPEND
B3	G23	FPGA269	MN6	8	SPEED
B2	T29	FPGA190	MN6	2	RCV
B3	J23	FPGA271	MN6	4	VM
B3	L22	FPGA272	MN6	3	VP
B3	F24	FPGA273	MN6	12	VMO/FSEO
B3	G24	FPGA274	MN6	11	VPO/VO
B3	H24	FPGA275	MN6	16	SOFTCON

3.15 AT91CAP9 Mezzanine Extension

J6/J7 are the two 320-pin connectors for hosting the AT91CAP9A-DKZ Mezzanine Board. Refer to "AT91CAP-DKM Schematics".

3.16 PIO Usage

Table 3-6. PIO Controller A

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PA0	MCI0_DA0	SPI0_MISO	SD/MMC/DATAFLASH SOCKET (J28)	MCI0_DA0/SPI0_MISO	VDDIOP0
PA1	MCI0_CDA	SPI0_MOSI	SD/MMC/DATAFLASH SOCKET (J28)	MCI0_CDA/SPI0_MOSI	VDDIOP0
PA2	MCI0_CK	SPI0_SPCK	SD/MMC/DATAFLASH SOCKET (J28)	MCI0_CK/SPI0_SPCK	VDDIOP0
PA3	MCI0_DA1	SPI0_NPCS1	SD/MMC/DATAFLASH SOCKET (J28)	MCI0_DA1	VDDIOP0
PA4	MCI0_DA2	SPI0_NPCS2	SD/MMC/DATAFLASH SOCKET (J28)	MCI0_DA2	VDDIOP0
PA5	MCI0_DA3	SPI0_NPCS0	SD/MMC/DATAFLASH SOCKET (J28)	MCI0_DA3/SPI0_NPCS0	VDDIOP0

Table 3-6. PIO Controller A (Continued)

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PA6	AC97FS		AC97 CODEC (MN11)	AC97FS	VDDIOP0
PA7	AC97CK		AC97 CODEC (MN11)	AC97CK	VDDIOP0
PA8	AC97TX		AC97 CODEC (MN11)	AC97TX	VDDIOP0
PA9	AC97RX		AC97 CODEC (MN11)	AC97RX	VDDIOP0
PA10	IRQ0	PWM1	USER'S LED1 CONTROL (DS1)	PA10 or PWM1	VDDIOP0
PA11	DMARQ0	PWM3	USER'S LED2 CONTROL (DS2)	PA11 or PWM3	VDDIOP0
PA12	CANTX	PCK0	CAN BUS INTERFACE (J24)	CANTX	VDDIOP0
PA13	CANRX		CAN BUS INTERFACE (J24)	CANRX	VDDIOP0
PA14	TCLK2	IRQ1	GENERAL PURPOSE ISI (J27)	PA14 as CTRL1	VDDIOP0
PA15	DMARQ3	PCK2	GENERAL PURPOSE ISI (J27)	PA15 as CTRL2	VDDIOP0
PA16	MCI1_CK	ISI_D0	SD/MMC SOCKET (J29), ISI (J27)	MCI1_CK/ISI_D0	VDDIOP1
PA17	MCI1_CDA	ISI_D1	SD/MMC SOCKET (J29), ISI (J27)	MCI1_CDA/ISI_D1	VDDIOP1
PA18	MCI1_DA0	ISI_D2	SD/MMC SOCKET (J29), ISI (J27)	MCI1_DA0/ISI_D2	VDDIOP1
PA19	MCI1_DA1	ISI_D3	SD/MMC SOCKET (J29), ISI (J27)	MCI1_DA1/ISI_D3	VDDIOP1
PA20	MCI1_DA2	ISI_D4	SD/MMC SOCKET (J29), ISI (J27)	MCI1_DA2/ISI_D4	VDDIOP1
PA21	MCI1_DA3	ISI_D5	SD/MMC SOCKET (J29), ISI (J27)	MCI1_DA3/ISI_D5	VDDIOP1
PA22	TXD0	ISI_D6	ISI (J27)	ISI_D6	VDDIOP1
PA23	RXD0	ISI_D7	ISI (J27)	ISI_D7	VDDIOP1
PA24	RTS0	ISI_PCK	ISI (J27)	ISI_PCK	VDDIOP1
PA25	CTS0	ISI_HSYNC	ISI (J27)	ISI_HSYNC	VDDIOP1
PA26	SCK0	ISI_VSYNC	ISI (J27)	ISI_VSYNC	VDDIOP1
PA27	PCK1	ISI_MCK	ISI (J27)	ISI_MCK	VDDIOP1
PA28	SPI0_NPCS3	ISI_D8	ISI (J27)	ISI_D8	VDDIOP1
PA29	TIOA0	ISI_D9	ISI (J27)	ISI_D9	VDDIOP1
PA30	TIOB0	ISI_D10	ISI (J27)	ISI_D10	VDDIOP1
PA31	DMARQ1	ISI_D11	ISI (J27)	ISI_D11	VDDIOP1

Table 3-7. PIO Controller B

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PB0	TF0		I2S CODEC (MN14) (1)	TF0	VDDIOP0
PB1	TK0		I2S CODEC (MN14) (1)	TK0	VDDIOP0
PB2	TD0		I2S CODEC (MN14) (1)	TD0	VDDIOP0
PB3	RD0		I2S CODEC (MN14) (1)	RD0	VDDIOP0
PB4	RK0	TWD	I2C MEMORY (MN10), ISI (J27)	TWD	VDDIOP0
PB5	RF0	TWCK	I2C MEMORY (MN10), ISI (J27)	TWCK	VDDIOP0

Table 3-7. PIO Controller B (Continued)

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PB6	TF1	TIOA1	I2S CODEC (MN14) (1)	TF1	VDDIOP0
PB7	TK1	TIOB1	I2S CODEC (MN14) (1)	TK1	VDDIOP0
PB8	TD1	PWM2	I2S CODEC (MN14) (1)	TD1	VDDIOP0
PB9	RD1	LCDCC	I2S CODEC (MN14) (1)	RD1	VDDIOP0
PB10	RK1	PCK1	I2S CODEC (MN14) SYSCLOCK or AC97 (MN11) optional EXTCLOCK	PCK1	VDDIOP0
PB11	RF1		ETHERNET RMII INTERFACE (MN7)	PB11 as INTERRUPT	VDDIOP0
PB12	SPI1_MISO				VDDIOP0
PB13	SPI1_MOSI	AD0	ANALOG INPUT INTERFACE (J33) (2)	AD0 (3)	VDDIOP0
PB14	SPI1_SPCK	AD1	ANALOG INPUT INTERFACE (J33) (2)	AD1(3)	VDDIOP0
PB15	SPI1_NPCS0	AD2	ANALOG INPUT INTERFACE (J33) (2)	AD2(3)	VDDIOP0
PB16	SPI1_NPCS1	AD3	ANALOG INPUT INTERFACE (J33) (2)	AD3(3)	VDDIOP0
PB17	SPI1_NPCS2	AD4		AD4(3)	VDDIOP0
PB18	SPI1_NPCS3	AD5		AD5(3)	VDDIOP0
PB19	PWM0	AD6		AD6(3)	VDDIOP0
PB20	PWM1	AD7		AD7(3)	VDDIOP0
PB21	ETXCK	TIOA2	ETHERNET RMII INTERFACE (MN7)	ETXCK	VDDIOP0
PB22	ERXDV	TIOB2	ETHERNET RMII INTERFACE (MN7)	ERXDV	VDDIOP0
PB23	ETX0	PCK3	ETHERNET RMII INTERFACE (MN7)	ETX0	VDDIOP0
PB24	ETX1		ETHERNET RMII INTERFACE (MN7)	ETX1	VDDIOP0
PB25	ERX0		ETHERNET RMII INTERFACE (MN7)	ERX0	VDDIOP0
PB26	ERX1		ETHERNET RMII INTERFACE (MN7)	ERX1	VDDIOP0
PB27	ERXER		ETHERNET RMII INTERFACE (MN7)	ERXER	VDDIOP0
PB28	ETXEN	TCLK0	ETHERNET RMII INTERFACE (MN7)	ETXEN	VDDIOP0
PB29	EMDC	PWM3	ETHERNET RMII INTERFACE (MN7)	EMDC	VDDIOP0
PB30	EMDIO		ETHERNET RMII INTERFACE (MN7)	EMDIO	VDDIOP0
PB31	ADTRIG	E_F100			VDDIOP0

Notes:
1. The user can configure the J1 jumper group to route either the SSC0 or the SSC1 signals to pilot the I2S codec. The factory setting is for SSC0.
2. Factory setting.
3. Please refer to the board's diagram, Figure 3-1. The AT91CAP9 chip has 8 ADC channels, only 4 of which can be buffered at a time.

Table 3-8. PIO Controller C

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PC0	LCDVSYNC				VDDIOP0
PC1	LCDHSYNC		LCD PANEL CONNECTOR (J37)	LCDHSYNC	VDDIOP0
PC2	LCDDOTCK		LCD PANEL CONNECTOR (J37)	LCDDOTCK	VDDIOP0
PC3	LCDDEN	PWM1	LCD PANEL CONNECTOR (J37)	LCDDEN	VDDIOP0
PC4	LCDD0	LCDD3	TOUCH SCREEN CONTROLLER (MN15)	PC4 as IRQ	VDDIOP0
PC5	LCDD1	LCDD4	TOUCH SCREEN CONTROLLER (MN15)	PC15 as BUSY	VDDIOP0
PC6	LCDD2	LCDD5	LCD PANEL CONNECTOR (J37)	LCDD2	VDDIOP0
PC7	LCDD3	LCDD6	LCD PANEL CONNECTOR (J37)	LCDD3	VDDIOP0
PC8	LCDD4	LCDD7	LCD PANEL CONNECTOR (J37)	LCDD4	VDDIOP0
PC9	LCDD5	LCDD10	LCD PANEL CONNECTOR (J37)	LCDD5	VDDIOP0
PC10	LCDD6	LCDD11	LCD PANEL CONNECTOR (J37)	LCDD6	VDDIOP0
PC11	LCDD7	LCDD12	LCD PANEL CONNECTOR (J37)	LCDD7	VDDIOP0
PC12	LCDD8	LCDD13	CAN BUS INTERFACE (J24)	PC12 as CANRS	VDDIOP0
PC13	LCDD9	LCDD14			VDDIOP0
PC14	LCDD10	LCDD15	LCD PANEL CONNECTOR (J37)	LCDD10	VDDIOP0
PC15	LCDD11	LCDD19	LCD PANEL CONNECTOR (J37)	LCDD11	VDDIOP0
PC16	LCDD12	LCDD20	LCD PANEL CONNECTOR (J37)	LCDD12	VDDIOP0
PC17	LCDD13	LCDD21	LCD PANEL CONNECTOR (J37)	LCDD13	VDDIOP0
PC18	LCDD14	LCDD22	LCD PANEL CONNECTOR (J37)	LCDD14	VDDIOP0
PC19	LCDD15	LCDD23	LCD PANEL CONNECTOR (J37)	LCDD15	VDDIOP0
PC20	LCDD16	ETX2	SD/MMC/DATAFLASH SOCKET (J28)	PC20 as CARD DETECT	VDDIOP0
PC21	LCDD17	ETX3	SD/MMC SOCKET (J29)	PC21 as CARD DETECT	VDDIOP0
PC22	LCDD18	ERX2	LCD PANEL CONNECTOR (J37)	LCDD18	VDDIOP0
PC23	LCDD19	ERX3	LCD PANEL CONNECTOR (J37)	LCDD19	VDDIOP0
PC24	LCDD20	ETXER	LCD PANEL CONNECTOR (J37)	LCDD20	VDDIOP0
PC25	LCDD21	ECRS	LCD PANEL CONNECTOR (J37)	LCDD21	VDDIOP0
PC26	LCDD22	ECOL	LCD PANEL CONNECTOR (J37)	LCDD22	VDDIOP0
PC27	LCDD23	ERXCK	LCD PANEL CONNECTOR (J37)	LCDD23	VDDIOP0
PC28	PWM0	TCLK1	LCD PANEL CONNECTOR (J37)	PWM0 as VCTRL	VDDIOP0
PC29	PCK0	PWM2	POWER LED CONTROL (DS3)	PC29 or PWM2	VDDIOP0
PC30	DRXD		DBGU RS232 INTERFACE (J23)	DRXD	VDDIOP0
PC31	DTXD		DBGU RS232 INTERFACE (J23)	DTXD	VDDIOP0

Table 3-9. PIO Controller D

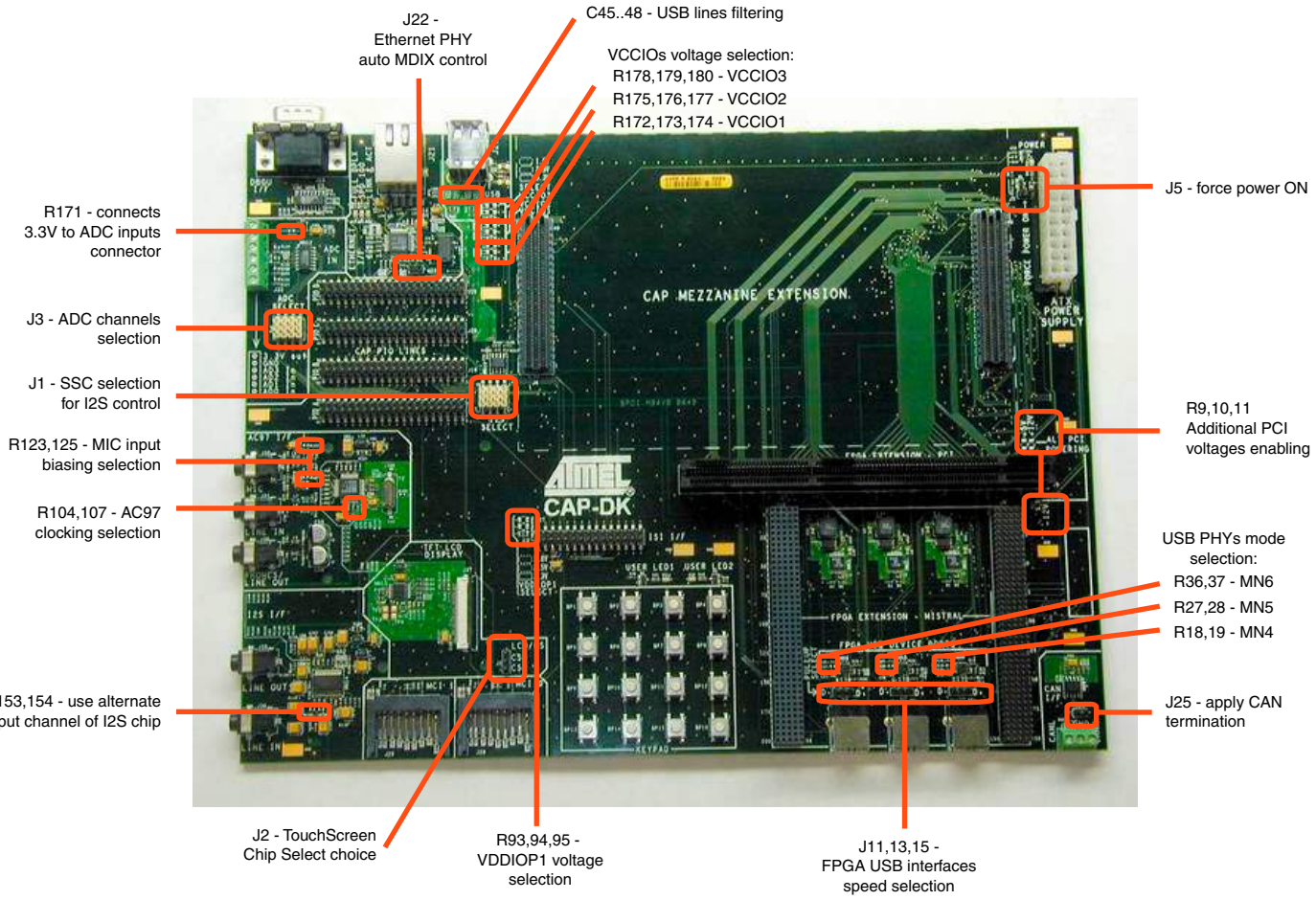
I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PD0	TXD1	SPI0_NPCS2	TOUCH SCREEN CONTROLLER (MN15)		VDDIOP0
PD1	RXD1	SPI0_NPCS3			VDDIOP0
PD2	TXD2	SPI1_NPCS2			VDDIOP0
PD3	RXD2	SPI1_NPCS3			VDDIOP0
PD4	FIQ				VDDIOP0
PD5	DMARQ2	RTS2			VDDIOP0
PD6	EBI_NWAIT	CTS2	4X4 KEYPADS	PD6 as KBD0 (row 0)	VDDIOM
PD7	EBI_NCS4/CFCS0	RTS1	4X4 KEYPADS	PD7 as KBD1 (row 1)	VDDIOM
PD8	EBI_NCS5/CFCS1	CTS1	4X4 KEYPADS	PD8 as KBD2 (row 2)	VDDIOM
PD9	EBI_CFCE1	SCK2	4X4 KEYPADS	PD9 as KBD3 (row 3)	VDDIOM
PD10	EBI_CFCE2	SCK1	4X4 KEYPADS	PD10 as KBD4 (column 0)	VDDIOM
PD11	EBI_NCS2		4X4 KEYPADS	PD11 as KBD5 (column 1)	VDDIOM
PD12	EBI_A23		4X4 KEYPADS	PD12 as KBD6 (column 2)	VDDIOM
PD13	EBI_A24		4X4 KEYPADS	PD13 as KBD7 (column 3)	VDDIOM
PD14	EBI_A25_CFRNW				VDDIOM
PD15	EBI_NCS3/NANDCS				VDDIOM
PD16	EBI_D16				VDDIOM
PD17	EBI_D17				VDDIOM
PD18	EBI_D18				VDDIOM
PD19	EBI_D19				VDDIOM
PD20	EBI_D20				VDDIOM
PD21	EBI_D21				VDDIOM
PD22	EBI_D22				VDDIOM
PD23	EBI_D23				VDDIOM
PD24	EBI_D24				VDDIOM
PD25	EBI_D25				VDDIOM
PD26	EBI_D26				VDDIOM
PD27	EBI_D27				VDDIOM
PD28	EBI_D28				VDDIOM
PD29	EBI_D29				VDDIOM
PD30	EBI_D30				VDDIOM
PD31	EBI_D31				VDDIOM

Section 4

AT91CAP-DKM Configuration

4.1 Configuration

Figure 4-1. AT91CAP-DKM Motherboard



4.2 Configuration Jumpers and Straps

Table 4-1. AT91CAP-DKM Configuration Jumpers and Straps

Designation	Default Setting	Feature
C45, 46, 47, 48	OFF	Optional 47 pF filtering capacitors for Host USB port lines (see "AT91CAP-DKM Schematics")
J1	no default	Selects which SSC drives the I2S interface. All jumpers in the upper position will select SSC0, all jumpers in the lower position will select SSC1.
J11	2-3	Selects FPGA USB interface MN4/J12 bus speed (1)
J13	2-3	Selects FPGA USB interface MN5/J14 bus speed (1)
J15	2-3	Selects FPGA USB interface MN6/J16 bus speed (1)
J2	1-2	Selects the TouchScreen controller selection signal. Default position = 2-3 (NPCS3). Position 1-2 chooses NPCS2.
J22	ON	Enables the Ethernet PHY MN7 auto MDIX control.
J25	ON	Applies 120 Ohm termination to the CAN port MN9/J24
J3	no default	These four jumpers select ADC channels (0123 or 4567) to be assigned to the four ADC inputs. Upper position selects channels 4567. Lower position selects channels 0123. Each jumper can be indifferently set to upper or lower position, no matter the position of the others. See "AT91CAP-DKM Schematics" for more details.
J5	OFF	Forces PC/ATX power supply power on. To be installed in case the SHDN signal (normally provided by the AT91CAP9 chip) is non operating or absent for some reason.
R104, 107	ON, ON (use 1K Ohm resistors)	Select the AC97 AD1981B clock frequency. Refer to "AT91CAP-DKM Schematics" and/or the AD1981B datasheet for in-depth explanations.
R123, 125	OFF, OFF	Optional MIC input biasing to VREFOUT for the AC97 AD1981B chip. Refer to "AT91CAP-DKM Schematics" and/or the AD1981B datasheet for in-depth explanations.
R153, 154	OFF, OFF	Optionally connects the I2S input lines to the secondary input channel of the UDA1342TS MN14 device. Use 0 Ohm resistors if needed.
R159	OFF	Reserved for future use. Do not mount.
R169	OFF	Optional divider bridge resistor (to be calculated jointly with R166) in order to adjust the touch screen controller VREF between 0 and 3.3V.
R171	OFF	Connects the analog 3.3V power line of the ADC input buffers to the dedicated connector J33. Use a 0 Ohm resistor if needed.
R172, 173, 174	ON, OFF, OFF (2)	Select FPGA IO BANK 1 VCCO voltage (3)
R175, 176, 177	ON, OFF, OFF (2)	Select FPGA IO BANK 2 VCCO voltage (3)
R178, 179, 180	ON, OFF, OFF (2)	Select FPGA IO BANK 3 VCCO voltage (3)
R18, 19	ON, OFF	Selects ISP1105BS PHY MN4 mode input. Please refer to the datasheet of this device for in-depth details.
R27, 28	ON, OFF	Selects ISP1105BS PHY MN5 mode input. Please refer to the datasheet of this device for in-depth details.

Table 4-1. AT91CAP-DKM Configuration Jumpers and Straps

Designation	Default Setting	Feature
R36, 37	ON, OFF	Selects ISP1105BS PHY MN6 mode input. Please refer to the datasheet of this device for in-depth details.
R9, 10, 11	OFF, OFF, OFF	Enable additional service voltages to be routed to the PCI64 connector J9. Solder 0 Ohm resistors to do so.
R93, 94, 95	ON, OFF, OFF	Select CAP VDDIOP1 voltage. On AT91CAP9 chip, VDDIOP1 is part of the PIOA port and is dedicated to the ISI interface (Connector J27). By default this voltage is fixed at 3.3V. Change this setting only if you are sure of what you are doing...!

Notes:
1. Position 1-2 = low speed (1.5 Mbps). Position 2-3 = full speed (12 Mbps).
2. Exactly **one** of these **must** be set. No less, no more.
3. Refer to "AT91CAP-DKM Schematics"to see the span of this IO bank (J8, 9, 10 connectors). By default this voltage is fixed at 3.3V. Change this setting only if you are sure of what you are doing...!

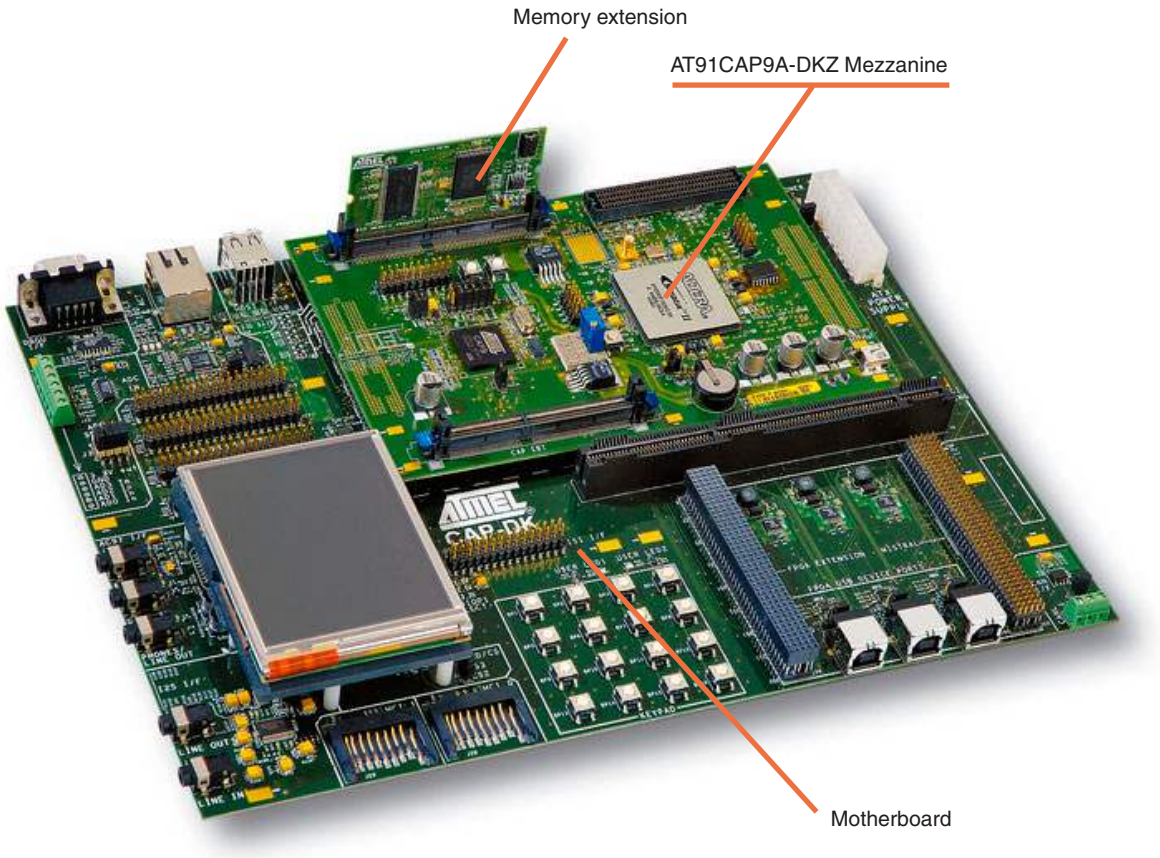
Section 5

Overview AT91CAP9A-DKZ Mezzanine

5.1 Scope

The **Mezzanine, Motherboard** and **Memory Extension** boards are used jointly to develop AT91CAP9 processor applications. **Section 5** through **Section 8** provide essential usage documentation for the AT91CAP9/Altera® mezzanine board (AT91CAP9A-DKZ).

Figure 5-1. AT91CAP9A-DKZ Overview



5.2 Purpose

The AT91CAP9A-DKZ mezzanine provides a configurable processor (AT91CAP9) and its associated FPGA, both being at the heart of an AT91CAP9A-DK development system layout.

Section 6

Setting Up the AT91CAP9A-DKZ Mezzanine

6.1 Electrostatic Warning

Upon delivery, the AT91CAP9A-DKZ Mezzanine is wrapped in a protective anti-static bag. The board must not be exposed to electrostatic discharges. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other on-board metallic element.

6.2 Requirements

In order to set up an AT91CAP9A-DK development system, the following items are needed:

- AT91CAP9A-DKZ mezzanine
- Memory extension board (see sections 9 through 14)
- AT91CAP-DKM motherboard (see sections 1 through 4)
- PC/ATX standard power supply unit

6.3 Layout

The board features essentially an AT91CAP9 chip connected to an FPGA to be used for prototyping the configurable part of the AT91CAP9 chip.

Around these two major components of the AT91CAP9A-DKZ board are some utility items as listed below:

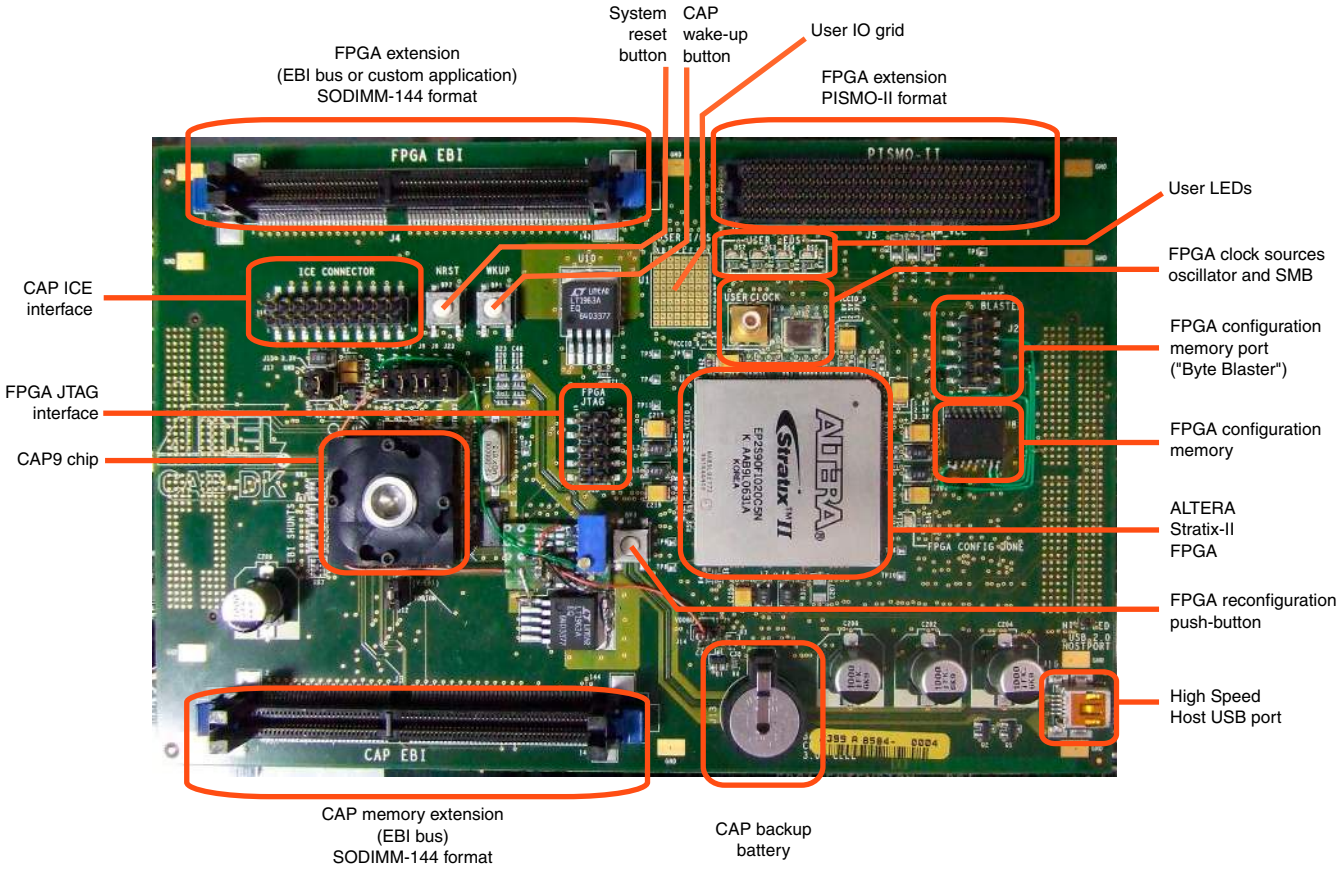
6.3.1 AT91CAP9 Specific

- High speed USB port mini-AB connector
- EBI memory extension port, SODIMM-144 format
- ICE interface
- Reset push-button (signal also connected to an FPGA IO)
- Wake-up push buttons
- Backup lithium battery
- 12 MHz crystal
- 32.768 kHz crystal

6.3.2 FPGA Specific (Altera Stratix-II EP2S90F1020C5)

- EPCS64SI16N configuration memory
- ByteBlaster configuration header
- JTAG header
- Reconfiguration push button
- 80-pad, 1.27 mm-spaced user IO grid
- Four user LEDs
- PISMO-II standard extension connector
- FPGA extension port (EBI memory module or custom application), SODIMM-144 format

Figure 6-1. AT91CAP9A-DKZ Mezzanine Board Layout - Top View



6.4 Powering Up the Board

A complete AT91CAP9A-DK system is powered through the AT91CAP-DKM motherboard via a standard ATX PC power supply.

The power control signal is connected to the SHDN signal, generated by the AT91CAP9 chip from the AT91CAP9A-DKZ mezzanine board.

Section 7

AT91CAP9A-DKZ Mezzanine Board

7.1 Block Diagram

Figure 7-1. AT91CAP9A-DKZ Mezzanine Block Diagram (see the complete schematic in Section 16)

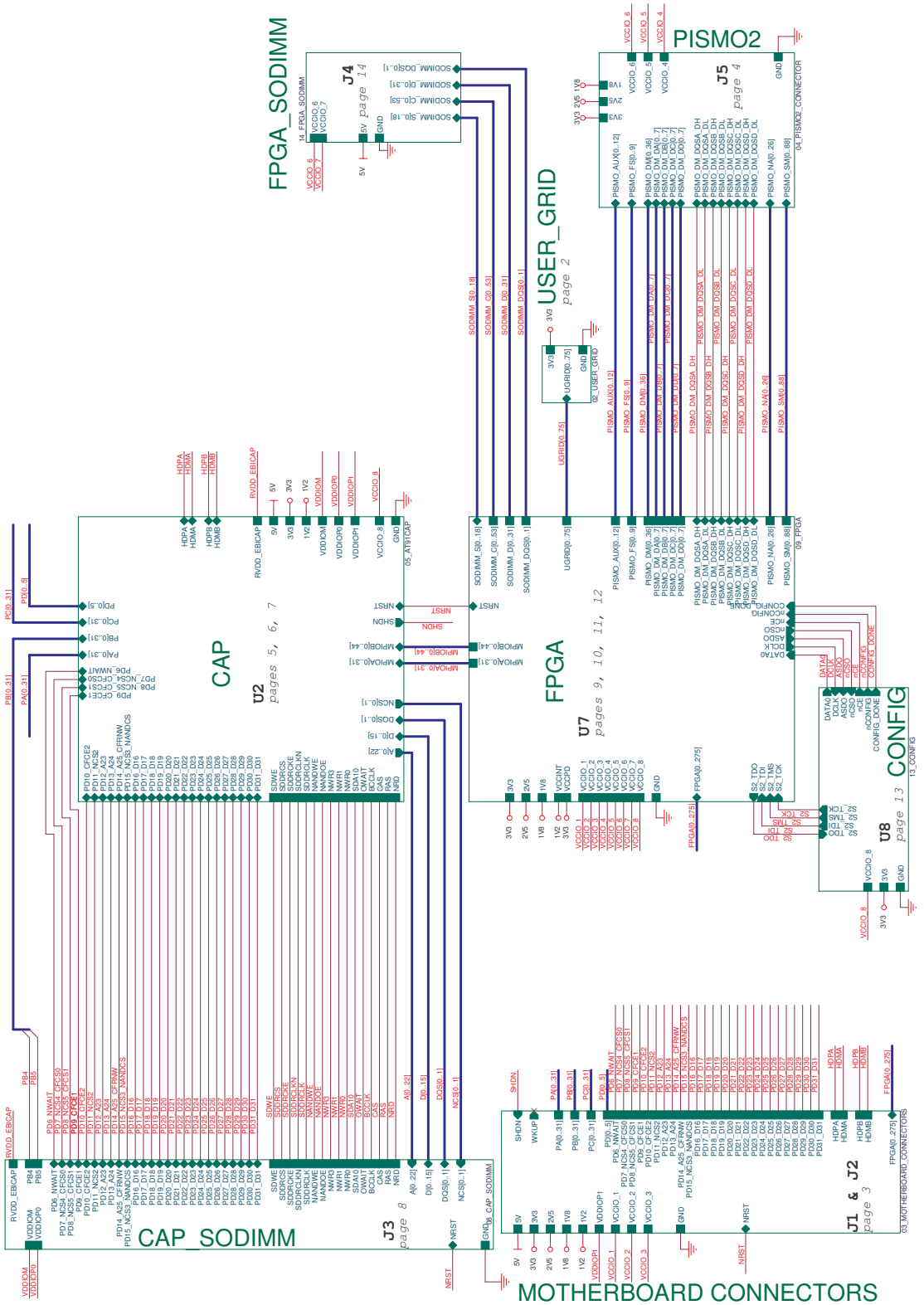
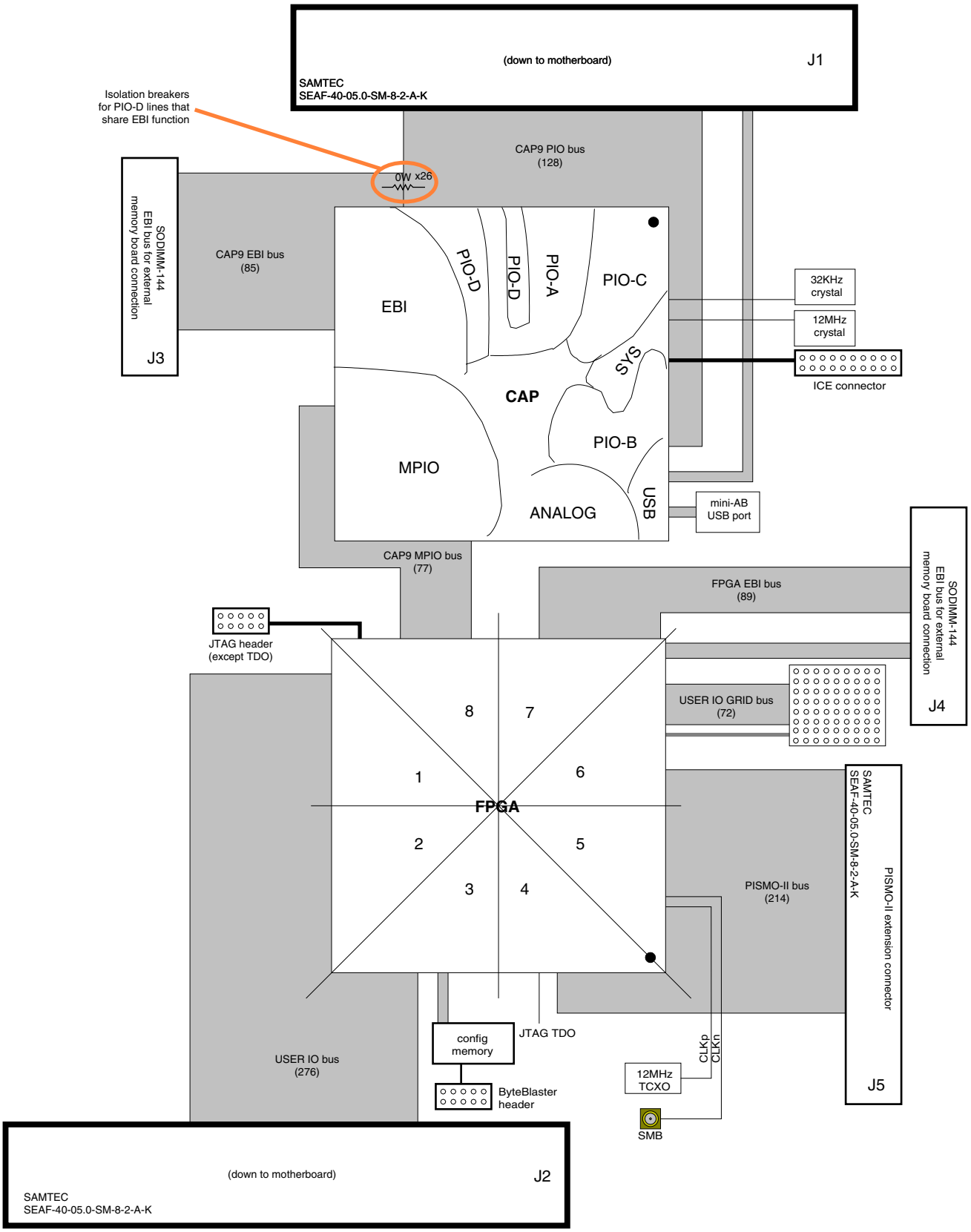


Figure 7-2. AT91CAP9/Altera Mezzanine Synoptic



7.2 Reset Path

The reset signal is named NRST. It is an open drain path that connects the following together:

- AT91CAP9 chip NRST pin (provides an integrated debouncing system)
- ICE connector
- Memory extension/EBI connector J3
- NRST push button BP2
- FPGA (standard IO pin AK17)
- Motherboard

7.3 Clocking Paths

The AT91CAP9 and the FPGA devices do not share common clocking sources. The only synchronization that exists between the two is integrated in the MPIO bus signaling.

7.3.1 AT91CAP9 Clock Sources

- On-board 12 MHz quartz
- On-board 32768 Hz quartz

Note that the AT91CAP9 chip has integrated PLLs, one being 480 MHz fixed, the two others being configurable and for internal AT91CAP9 chip use only.

7.3.2 FPGA Clock Sources

- On-board 12 MHz oscillator, connected to pin T3 (CLK11p)
- User clock connector, SMB format, connected to pin T4 (CLK11n)

7.4 Power Supply Circuitry

The AT91CAP9A-DKZ board derives most of the necessary voltages from the motherboard connectors. Some service voltage sources are regenerated on board.

Please look at the appended schematics: Section 16, sheets 1, 5, 9 and 10 for in-depth details on power paths.

7.5 Memory

System memory resources are provided via extension boards in SODIMM-144 format.

There is one each for the AT91CAP9 and the FPGA chips. These connections are labeled “EBI”, named after the Atmel standard “External Bus Interface”.

Note that the bus voltage of each of these extensions is automatically customizable:

- An adjustable regulator located on the mezzanine board, provides the bus voltage. This voltage powers both the VCCO of the memory boards and the VCCO of the AT91CAP9 (or the FPGA).
- A resistor, deported on the memory board, adjusts that VCCO voltage in function of the memory components that are mounted on the memory board, so that the AT91CAP9 (or FPGA) busses adapt automatically to it.

For technical details, please refer to the appended schematics: Section 16, sheet 5 (look for regulator U6) and sheet 14 (look for regulator U10)

7.6 Host USB Port

The mini-AB connector J16 is connected directly to the AT91CAP9 chip. Please refer to the appended schematics: Section 16, sheet 7 for in-depth details of its implementation.

7.7 FPGA Connections

7.7.1 FPGA Banking Allocations

As shown in the synoptic in Figure 7-1 “AT91CAP9A-DKZ Mezzanine Block Diagram (see the complete schematic in Section 16)”, the Altera component has eight different IO banks. Each of these can be powered separately, thereby allowing different signaling standards of a system to be implemented in parallel.

Banking Allocations:

- Banks 1, 2 and 3 = user IO going down to motherboard for user extension (PCI64, “Mistral” connection, USB device interfaces)
- Banks 4, 5 and 6 (partly) = PISMO-II extension connector
- Bank 6 (partly) = leftovers allocated between the user I/O grid and EBI/FPGA connector
- Bank 7 = EBI/FPGA connector
- Bank 8 = AT91CAP9 connection via MPIO bus.

7.7.2 CAP/MPIO Bus Connections

Table 7-1. MPIO-FPGA Signal Assignment

CAP/MPIO Signal	FPGA Pin	Alternate Pin Function	FPGA Bank
MPIOA00	AG25		8
MPIOA01	AB21		8
MPIOA02	AE22		8
MPIOA03	AF22		8
MPIOA04	AD22		8
MPIOA05	AH28	DQ17B	8
MPIOA06	AK29	DQSn17B	8
MPIOA07	AJ28	DQ17B	8
MPIOA08	AM29	DQ17B	8
MPIOA09	AL29	DQ17B	8
MPIOA10	AK28	DQS17B	8
MPIOA11	AC21		8
MPIOA12	AG21		8
MPIOA13	AK27	DQ16B	8

Table 7-1. MPIO-FPGA Signal Assignment (Continued)

CAP/MPIO Signal	FPGA Pin	Alternate Pin Function	FPGA Bank
MPIOA14	AL28	DQSn16B	8
MPIOA15	AJ27	DQ16B	8
MPIOA16	AM28	DQ16B	8
MPIOA17	AM27	DQ16B	8
MPIOA18	AL27	DQS16B	8
MPIOA19	AF21		8
MPIOA20	AK26	DQ15B	8
MPIOA21	AL26	DQSn15B	8
MPIOA22	AJ26	DQ15B	8
MPIOA23	AM25	DQ15B	8
MPIOA24	AM26	DQ15B	8
MPIOA25	AL25	DQS15B	8
MPIOA26	AD21		8
MPIOA27	AG24	DQ14B	8
MPIOA28	AH25	DQSn14B	8
MPIOA29	AH26	DQ14B	8
MPIOA30	AH24	DQ14B	8
MPIOA31	AK25	DQ14B	8
MPIOB00	AJ25	DQS14B	8
MPIOB01	AB20		8
MPIOB02	AE21		8
MPIOB03	AG20		8
MPIOB04	AF20		8
MPIOB05	AM24	DQ13B	8
MPIOB06	AL24	DQSn13B	8
MPIOB07	AK24	DQ13B	8
MPIOB08	AK23	DQ13B	8
MPIOB09	AM23	DQ13B	8
MPIOB10	AL23	DQS13B	8
MPIOB11	AD20		8
MPIOB12	AG23	DQ12B	8
MPIOB13	AH22	DQSn12B	8
MPIOB14	AG22	DQ12B	8
MPIOB15	AK22	DQ12B	8
MPIOB16	AJ23	DQ12B	8
MPIOB17	AJ22	DQS12B	8
MPIOB18	AC20		8

Table 7-1. MPIO-FPGA Signal Assignment (Continued)

CAP/MPIO Signal	FPGA Pin	Alternate Pin Function	FPGA Bank
MPIOB19	AB19		8
MPIOB20	AE20		8
MPIOB21	AC19		8
MPIOB22	AM22	DQ11B	8
MPIOB23	AL22	DQSn11B	8
MPIOB24 (1)	AM17	CLK4p	8
MPIOB25	AJ21	DQ11B	8
MPIOB26	AK21	DQ11B	8
MPIOB27	AM21	DQ11B	8
MPIOB28	AL21	DQS11B	8
MPIOB29	AD19		8
MPIOB30	AE19		8
MPIOB31	AF19		8
MPIOB32	AB18		8
MPIOB33	AH20	DQ10B	8
MPIOB34	AJ20	DQSn10B	8
MPIOB35	AJ19	DQ10B	8
MPIOB36	AH19	DQ10B	8
MPIOB37	AL20	DQ10B	8
MPIOB38	AK20	DQS10B	8
MPIOB39	AC18		8
MPIOB40	AD18		8
MPIOB41	AB17		8
MPIOB42	AC17		8
MPIOB43	AJ17	CLK5n	8
MPIOB44	AL17	CLK4n	8

Note: 1. MPIOB24 is the MPIO bus clock.

7.7.3 SODIMM Connection

Table 7-2. SODIMM-FPGA Signal Assignment

SODIMM PIN	Signal Name	FPGA Pin	FPGA Pin Alternate Function	FPGA Bank
1	GND			
2	GND			
3	SODIMM_D00	AL12	DQSn7B	7
4	SODIMM_D08	AG11	DQSn5B	7
5	SODIMM_D01	AM11	DQ7B	7
6	SODIMM_D09	AF10	DQ5B	7
7	SODIMM_D02	AJ12	DQ7B	7
8	SODIMM_D10	AG10	DQ5B	7
9	SODIMM_D03	AK12	DQ7B	7
10	SODIMM_D11	AF12	DQ5B	7
11	VCCIO_7			
12	VCCIO_7			
13	SODIMM_D04	AM10	DQ6B	7
14	SODIMM_D12	AM9	DQ4B	7
15	SODIMM_D05	AL10	DQ6B	7
16	SODIMM_D13	AJ8	DQ4B	7
17	SODIMM_D06	AH11	DQ6B	7
18	SODIMM_D14	AK8	DQ4B	7
19	SODIMM_D07	AJ11	DQ6B	7
20	SODIMM_D15	AJ10	DQ4B	7
21	GND			
22	GND			
23	SODIMM_D16	AL8	DQSn3B	7
24	SODIMM_D24	AH8	DQSn1B	7
25	SODIMM_D17	AJ7	DQ3B	7
26	SODIMM_D25	AH7	DQ1B	7
27	VCCIO_7			
28	VCCIO_7			
29	SODIMM_D18	AK7	DQ3B	7
30	SODIMM_D26	AH6	DQ1B	7
31	SODIMM_D19	AM7	DQ3B	7
32	SODIMM_D27	AG9	DQ1B	7
33	SODIMM_D20	AM6	DQ2B	7
34	SODIMM_D28	AM4	DQ0B	7

Table 7-2. SODIMM-FPGA Signal Assignment (Continued)

SODIMM PIN	Signal Name	FPGA Pin	FPGA Pin Alternate Function	FPGA Bank
35	GND			
36	GND			
37	SODIMM_D21	AJ6	DQ2B	7
38	SODIMM_D29	AH5	DQ0B	7
39	SODIMM_D22	AK6	DQ2B	7
40	SODIMM_D30	AJ5	DQ0B	7
41	SODIMM_D23	AM5	DQ2B	7
42	SODIMM_D31	AL4	DQ0B	7
43	SODIMM_DQS0	AK4	DQS0B	7
44	SODIMM_DQS1	AL5	DQS2B	7
45	VCCIO_7			
46	VCCIO_7			
47	SODIMM_C00	AB16		7
48	SODIMM_C27	AF11		7
49	SODIMM_C01	AC16		7
50	SODIMM_C28	AB14		7
51	SODIMM_C02	AC15		7
52	SODIMM_C29	AL9		7
53	SODIMM_C03	AM14	DQ9B	7
54	SODIMM_C30	AK9	DQS4B	7
55	GND			
56	GND			
57	SODIMM_C04	AL13	DQSn9B	7
58	SODIMM_C31	AC13		7
59	SODIMM_C05	AJ13	DQ9B	7
60	SODIMM_C32	AE12		7
61	SODIMM_C06	AJ14	DQ9B	7
62	SODIMM_C33	AM8	DQ3B	7
63	VCCIO_7			
64	VCCIO_7			
65	SODIMM_C07	AL14	DQ9B	7
66	SODIMM_C34	AL7	DQS3B	7
67	SODIMM_C08	AK13	DQS9B	7
68	SODIMM_C35	AB13		7
69	SODIMM_C09	AD14		7
70	SODIMM_C36	AD12		7

Table 7-2. SODIMM-FPGA Signal Assignment (Continued)

SODIMM PIN	Signal Name	FPGA Pin	FPGA Pin Alternate Function	FPGA Bank
71	SODIMM_C10	AE14		7
72	SODIMM_C37	AL6		7
73	SODIMM_C11	AG15	DQ8B	7
74	SODIMM_C38	AE11		7
75	GND			
76	GND			
77	SODIMM_C12	AH14	DQSn8B	7
78	SODIMM_C39	AH9	DQ1B	7
79	SODIMM_C13	AF13	DQ8B	7
80	SODIMM_C40	AG8	DQS1B	7
81	VCCIO_7			
82	VCCIO_7			
83	SODIMM_C14	AG13	DQ8B	7
84	SODIMM_C41	AD11		7
85	SODIMM_C15	AH13	DQ8B	7
86	SODIMM_C42	AC12		7
87	SODIMM_C16	AG14	DQS8B	7
88	SODIMM_C43	AK5	DQSn0B	7
89	SODIMM_C17	AB15		7
90	SODIMM_C44	AC11		7
91	GND			
92	GND			
93	SODIMM_C18	AF14		7
94	SODIMM_C45	AB12		7
95	SODIMM_C19	AM12	DQ7B	7
96	SODIMM_C46	AE10		7
97	SODIMM_C20	AL11	DQS7B	7
98	SODIMM_C47	AB11	RDN7	7
99	SODIMM_C21	AC14		7
100	SODIMM_C48	AD10		7
101	VCCIO_7			
102	VCCIO_7			
103	SODIMM_C22	AK11	DQSn6B	7
104	SODIMM_C49	AE9		7
105	SODIMM_C23	AK10	DQS6B	7
106	SODIMM_C50	AH16	CLK7p	7

Table 7-2. SODIMM-FPGA Signal Assignment (Continued)

SODIMM PIN	Signal Name	FPGA Pin	FPGA Pin Alternate Function	FPGA Bank
107	GND			
108	GND			
109	SODIMM_C24	AD13		7
110	SODIMM_C51	AG16		7
111	RVDD_EBIFPGA			
112	SODIMM_C52			
113	VCCIO_7			
114	VCCIO_7			
115	SODIMM_C25	AE13		7
116	SODIMM_C53	AL16		7
117	SODIMM_C26	AG12	DQ5B	7
118	SODIMM_S09	AA6	DIFFIO_TX100p	6
119	GND			
120	GND			
121	SODIMM_S00	AA11	DIFFIO_TX102n	6
122	SODIMM_S10	AE2	DIFFIO_RX100n	6
123	SODIMM_S01	AA10	DIFFIO_TX102p	6
124	SODIMM_S11	AE1	DIFFIO_RX100p	6
125	SODIMM_S02	AF2	DIFFIO_RX102n	6
126	SODIMM_S12	W11	DIFFIO_TX99n	6
127	SODIMM_S03	AF1	DIFFIO_RX102p	6
128	SODIMM_S13	W10	DIFFIO_TX99p	6
129	VCCIO_6			
130	VCCIO_6			
131	SODIMM_S04	Y11	DIFFIO_TX101n	6
132	SODIMM_S14	AD2	DIFFIO_RX99n	6
133	SODIMM_S05	Y10	DIFFIO_TX101p	6
134	SODIMM_S15	AD1	DIFFIO_RX99p	6
135	SODIMM_S06	AE4	DIFFIO_RX101n	6
136	SODIMM_S16	Y9	DIFFIO_TX98n	6
137	SODIMM_S07	AE3	DIFFIO_RX101p	6
138	SODIMM_S17	Y8	DIFFIO_TX98p	6
139	GND			
140	GND			
141	SODIMM_S08	AA7	DIFFIO_TX100n	6

Table 7-2. SODIMM-FPGA Signal Assignment (Continued)

SODIMM PIN	Signal Name	FPGA Pin	FPGA Pin Alternate Function	FPGA Bank
142	SODIMM_S18	AC4	DIFFIO_RX98n	6
143	VCCIO_6			
144	VCCIO_6			

7.7.4 PISMO-II Connector

The Pismo connector, J5 matches the PISMO-II standard definition, refer to this standard for further details.

Table 7-3. PISMO-FPGA Signal Assignment

PISMO Pin	Standard PISMO Name	Board Signal Name	FPGA Pin	Alternate FPGA Pin Function	FPGA Bank
A01	DM_DQS3_DH	PISMO_DM_DQSD_DH	F11	DQS6T	4
A02	DM_D26	PISMO_DM_DD2	G11	DQ6T	4
A03	DM_D27	PISMO_DM_DD3	G12	DQ6T	4
A04	DM_D29	PISMO_DM_DD5	D12	DQ7T	4
A05	DM_D30	PISMO_DM_DD6	A11	DQ7T	4
A06	DM_DQS1_DH	PISMO_DM_DQSB_DH	D7	DQS2T	4
A07	DM_D08	PISMO_DM_DB0	B7	DQ2T	4
A08	DM_D10	PISMO_DM_DB2	E6	DQ2T	4
A09	DM_D12	PISMO_DM_DB4	C9	DQ3T	4
A10	DM_D15	PISMO_DM_DB7	B9	DQSn3T	4
A11	DM_D01	PISMO_DM_DA1	D5	DQ0T	4
A12	DM_D03	PISMO_DM_DA3	A4	DQ0T	4
A13	DM_D05	PISMO_DM_DA5	D6	DQ1T	4
A14	DM_D06	PISMO_DM_DA6	C6	DQ1T	4
A15	DM_DQS0_DH	PISMO_DM_DQSA_DH	C4	DQS0T	4
A16	DM_D16	PISMO_DM_DC0	D8	DQ4T	4
A17	DM_D19	PISMO_DM_DC3	F10	DQ4T	4
A18	DM_D22	PISMO_DM_DC6	B10	DQ5T	4
A19	DM_D23	PISMO_DM_DC7	D10	DQ5T	4
A20	DM_DQS2_DH	PISMO_DM_DQSC_DH	F9	DQS4T	4
A21	VSS20	GND			
A22	SM_D23	PISMO_SM70	L8	DIFFIO_TX71n	5
A23	SM_D22	PISMO_SM69	F3	DIFFIO_RX72p	5
A24	SM_D21	PISMO_SM68	F4	DIFFIO_RX72n	5
A25	SM_D20	PISMO_SM67	L9	DIFFIO_TX72p	5
A26	SM_D19	PISMO_SM66	L10	DIFFIO_TX72n	5
A27	SM_D18	PISMO_SM65	F1	DIFFIO_RX73p	5

Table 7-3. PISMO-FPGA Signal Assignment (Continued)

PISMO Pin	Standard PISMO Name	Board Signal Name	FPGA Pin	Alternate FPGA Pin Function	FPGA Bank
A28	SM_D17	PISMO_SM64	F2	DIFFIO_RX73n	5
A29	SM_D16	PISMO_SM63	M8	DIFFIO_TX73p	5
A30	DNU16	n.c.			
A31	DNU17	n.c.			
A32	SM_D07	PISMO_SM54	M11	DIFFIO_TX75n	5
A33	SM_D06	PISMO_SM53	J3	DIFFIO_RX76p	5
A34	SM_D05	PISMO_SM52	J4	DIFFIO_RX76n	5
A35	SM_D04	PISMO_SM51	N10	DIFFIO_TX76p	5
A36	SM_D03	PISMO_SM50	N11	DIFFIO_TX76n	5
A37	SM_D02	PISMO_SM49	H1	DIFFIO_RX77p	5
A38	SM_D01	PISMO_SM48	H2	DIFFIO_RX77n	5
A39	SM_D00	PISMO_SM47	M6	DIFFIO_TX77p	5
A40	DNU14	n.c.			
B01	DM_DQS3_DL	PISMO_DM_DQSD_DL	F12	DQSn6T	4
B02	DM_D24	PISMO_DM_DD0	E11	DQ6T	4
B03	DM_D25	PISMO_DM_DD1	G10	DQ6T	4
B04	DM_D28	PISMO_DM_DD4	C12	DQS7T	4
B05	DM_D31	PISMO_DM_DD7	B11	DQ7T	4
B06	DM_DQS1_DL	PISMO_DM_DQSB_DL	C7	DQSn2T	4
B07	DM_D09	PISMO_DM_DB1	E7	DQ2T	4
B08	DM_D11	PISMO_DM_DB3	A7	DQ2T	4
B09	DM_D13	PISMO_DM_DB5	A8	DQ3T	4
B10	DM_D14	PISMO_DM_DB6	C8	DQ3T	4
B11	DM_D00	PISMO_DM_DA0	B4	DQ0T	4
B12	DM_D02	PISMO_DM_DA2	E5	DQ0T	4
B13	DM_D04	PISMO_DM_DA4	A5	DQ1T	4
B14	DM_D07	PISMO_DM_DA7	B6	DQSn1T	4
B15	DM_DQS0_DL	PISMO_DM_DQSA_DL	C5	DQSn0T	4
B16	DM_D17	PISMO_DM_DC1	E8	DQ4T	4
B17	DM_D18	PISMO_DM_DC2	F8	DQ4T	4
B18	DM_D20	PISMO_DM_DC4	C10	DQS5T	4
B19	DM_D21	PISMO_DM_DC5	A10	DQ5T	4
B20	DM_DQS2_DL	PISMO_DM_DQSC_DL	E9	DQSn4T	4
B21	VSS21	GND			
B22	SM_D31	PISMO_SM79	K6	DIFFIO_TX69p	5
B23	SM_D30	PISMO_SM78	K7	DIFFIO_TX69n	5

Table 7-3. PISMO-FPGA Signal Assignment (Continued)

PISMO Pin	Standard PISMO Name	Board Signal Name	FPGA Pin	Alternate FPGA Pin Function	FPGA Bank
B24	SM_D29	PISMO_SM77	E3	DIFFIO_RX70p	5
B25	SM_D28	PISMO_SM76	E4	DIFFIO_RX70n	5
B26	SM_D27	PISMO_SM75	K8	DIFFIO_TX70p	5
B27	SM_D26	PISMO_SM73	E1	DIFFIO_RX71p	5
B28	SM_D25	PISMO_SM72	E2	DIFFIO_RX71n	5
B29	SM_D24	PISMO_SM71	L7	DIFFIO_TX71p	5
B30	VSS12	GND			
B31	VSS9	GND			
B32	SM_D15	PISMO_SM62	M9	DIFFIO_TX73n	5
B33	SM_D14	PISMO_SM61	G3	DIFFIO_RX74p	5
B34	SM_D13	PISMO_SM60	G4	DIFFIO_RX74n	5
B35	SM_D12	PISMO_SM59	L5	DIFFIO_TX74p	5
B36	SM_D11	PISMO_SM58	L6	DIFFIO_TX74n	5
B37	SM_D10	PISMO_SM57	G1	DIFFIO_RX75p	5
B38	SM_D09	PISMO_SM56	G2	DIFFIO_RX75n	5
B39	SM_D08	PISMO_SM55	M10	DIFFIO_TX75p	5
B40	DNU15	n.c.			
C01	DNU11	n.c.			
C02	DM_BA2	PISMO_DM18	L16		4
C03	DM_RESET#	PISMO_DM35	C13	DQS9T	4
C04	DM_ODT1	PISMO_DM33	H14		4
C05	DM_ODT0	PISMO_DM32	F15	DQ8T	4
C06	DM_VREF	(see schematics, Section 16)			
C07	DM_VIO_9	VCCIO_4			
C08	DM_VIO_3	VCCIO_4			
C09	DM_VIO_6	VCCIO_4			
C10	DM_VIO_5	VCCIO_4			
C11	DM_VIO_8	VCCIO_4			
C12	DM_VIO_4	VCCIO_4			
C13	DM_VCC_3	(see schematics, Section 16)			
C14	DM_VIO_2	VCCIO_4			
C15	DM_VIO_7	VCCIO_4			
C16	DM_VCC_2	(see schematics, Section 16)			
C17	DM_VCC_1	(see schematics, Section 16)			
C18	DM_VIO_1	VCCIO_4			
C19	DM_VIO_0	VCCIO_4			

Table 7-3. PISMO-FPGA Signal Assignment (Continued)

PISMO Pin	Standard PISMO Name	Board Signal Name	FPGA Pin	Alternate FPGA Pin Function	FPGA Bank
C20	DM_VCC_0	(see schematics, Section 16)			
C21	VSS22	GND			
C22	SM_V33_2	3.3V			
C23	SM_V33_1	3.3V			
C24	SM_V33_0	3.3V			
C25	SM_VIO_8	VCCIO_5			
C26	SM_VIO_7	VCCIO_5			
C27	SM_VIO_6	VCCIO_5			
C28	SM_VIO_5	VCCIO_5			
C29	SM_CLK3	PISMO_SM41	K3	DIFFIO_RX79p	5
C30	SM_CLK2	PISMO_SM40	K4	DIFFIO_RX79n	5
C31	SM_CLK1	PISMO_SM39	N8	DIFFIO_TX79p	5
C32	SM_CLK0	PISMO_SM38	N9	DIFFIO_TX79n	5
C33	SM_VIO_4	VCCIO_5			
C34	SM_VIO_3	VCCIO_5			
C35	SM_VIO_2	VCCIO_5			
C36	SM_VIO_1	VCCIO_5			
C37	SM_VIO_0	VCCIO_5			
C38	SM_V18_2	1.8V			
C39	SM_V18_1	PISMO_SM88	D3	INPUT	5
C40	SM_V18_0	PISMO_SM87	D4	INPUT	5
D01	DM_CS1#	PISMO_DM27	F14	DQS8T	4
D02	DM_A15	PISMO_DM15	H12		4
D03	DM_A07	PISMO_DM07	L14		4
D04	DM_A11	PISMO_DM11	K13		4
D05	DM_CKE1	PISMO_DM21	K15		4
D06	DM_A14	PISMO_DM14	A9	DQ3T	4
D07	DM_A08	PISMO_DM08	B5	DQS1T	4
D08	DM_DQM1	PISMO_DM29	F13	DQ8T	4
D09	VSS37	GND			
D10	DM_CLK1_DH	PISMO_DM24	B12	DQSn7T	4
D11	VSS34	GND			
D12	DM_CLK0_DH	PISMO_DM22	H13		4
D13	VSS31	GND			
D14	DM_A10	PISMO_DM10	L15		4
D15	DM_WE#	PISMO_DM36	B14	DQ9T	4

Table 7-3. PISMO-FPGA Signal Assignment (Continued)

PISMO Pin	Standard PISMO Name	Board Signal Name	FPGA Pin	Alternate FPGA Pin Function	FPGA Bank
D16	DM_DQM0	PISMO_DM28	E13	DQ8T	4
D17	DM_RAS#	PISMO_DM34	L17		4
D18	DM_BA1	PISMO_DM17	J13		4
D19	DM_A01	PISMO_DM01	J11		4
D20	DM_DQM2	PISMO_DM30	G13	DQ8T	4
D21	VSS23	GND			
D22	SM_A30	PISMO_SM30	P7	DIFFIO_TX81n	5
D23	SM_A28	PISMO_SM28	N5	DIFFIO_RX82n	5
D24	SM_A26	PISMO_SM26	P5	DIFFIO_TX82n	5
D25	SM_A24	PISMO_SM24	M4	DIFFIO_RX83n	5
D26	SM_A22	PISMO_SM22	P11	DIFFIO_TX83n	5
D27	SM_A20	PISMO_SM20	L2	DIFFIO_RX84n	5
D28	SM_A18	PISMO_SM18	R7	DIFFIO_TX84n	5
D29	SM_A16	PISMO_SM16	N3	DIFFIO_RX85n	5
D30	VSS13	GND			
D31	VSS10	GND			
D32	SM_A14	PISMO_SM14	R5	DIFFIO_TX85n	5
D33	SM_A12	PISMO_SM12	M2	DIFFIO_RX86n	5
D34	SM_A10	PISMO_SM10	R11	DIFFIO_TX86n	5
D35	SM_A08	PISMO_SM08	R3	DIFFIO_RX87n	5
D36	SM_A06	PISMO_SM06	T6	DIFFIO_TX87n	5
D37	SM_A04	PISMO_SM04	P2	DIFFIO_RX88n	5
D38	SM_A02	PISMO_SM02	T11	DIFFIO_TX88n	5
D39	SM_A00	PISMO_SM00	T1	CLK10p/DIFFIO_RX_C3p	5
D40	SM_BE0#	PISMO_SM32	L4	DIFFIO_RX81n	5
E01	VSS46	GND			
E02	DM_A04	PISMO_DM04	H11		4
E03	DM_A06	PISMO_DM06	L13		4
E04	DM_A09	PISMO_DM09	A6	DQ1T	4
E05	DM_CKE0	PISMO_DM20	D11	DQ5T	4
E06	DM_DQM3	PISMO_DM31	E14	DQSn8T	4
E07	DM_A12	PISMO_DM12	J12		4
E08	DM_A05	PISMO_DM05	K12		4
E09	VSS38	GND			
E10	DM_CLK1_DL	PISMO_DM25	A12	DQ7T	4
E11	VSS35	GND			

Table 7-3. PISMO-FPGA Signal Assignment (Continued)

PISMO Pin	Standard PISMO Name	Board Signal Name	FPGA Pin	Alternate FPGA Pin Function	FPGA Bank
E12	DM_CLK0_DL	PISMO_DM23	J14		4
E13	VSS32	GND			
E14	DM_A02	PISMO_DM02	L12	RUP4	4
E15	DM_CS0#	PISMO_DM26	G14		4
E16	DM_A13	PISMO_DM13	B8	DQS3T	4
E17	DM_CAS#	PISMO_DM19	C11	DQSn5T	4
E18	DM_BA0	PISMO_DM16	K14		4
E19	DM_A00	PISMO_DM00	H9		4
E20	DM_A03	PISMO_DM03	K11	RDN4	4
E21	VSS24	GND			
E22	SM_A31	PISMO_SM31	P6	DIFFIO_TX81p	5
E23	SM_A29	PISMO_SM29	N4	DIFFIO_RX82p	5
E24	SM_A27	PISMO_SM27	P4	DIFFIO_TX82p	5
E25	SM_A25	PISMO_SM25	M3	DIFFIO_RX83p	5
E26	SM_A23	PISMO_SM23	P10	DIFFIO_TX83p	5
E27	SM_A21	PISMO_SM21	L1	DIFFIO_RX84p	5
E28	SM_A19	PISMO_SM19	R6	DIFFIO_TX84p	5
E29	SM_A17	PISMO_SM17	N2	DIFFIO_RX85p	5
E30	SM_BE2#	PISMO_SM34	P9	DIFFIO_TX80n	5
E31	SM_BE3#	PISMO_SM35	P8	DIFFIO_TX80p	5
E32	SM_A15	PISMO_SM15	R4	DIFFIO_TX85p	5
E33	SM_A13	PISMO_SM13	M1	DIFFIO_RX86p	5
E34	SM_A11	PISMO_SM11	R10	DIFFIO_TX86p	5
E35	SM_A09	PISMO_SM09	R2	DIFFIO_RX87p	5
E36	SM_A07	PISMO_SM07	T5	DIFFIO_TX87p	5
E37	SM_A05	PISMO_SM05	P1	DIFFIO_RX88p	5
E38	SM_A03	PISMO_SM03	T10	DIFFIO_TX88p	5
E39	SM_A01	PISMO_SM01	T2	CLK10n/DIFFIO_RX_C3n	5
E40	SM_BE1#	PISMO_SM33	L3	DIFFIO_RX81p	5
F01	FS_SCK	PISMO_FS06	K17		4
F02	VSS45	GND			
F03	FS_V33_0	3.3V			
F04	VSS44	GND			
F05	VSS43	GND			
F06	VSS42	GND			
F07	VSS41	GND			

Table 7-3. PISMO-FPGA Signal Assignment (Continued)

PISMO Pin	Standard PISMO Name	Board Signal Name	FPGA Pin	Alternate FPGA Pin Function	FPGA Bank
F08	VSS40	GND			
F09	VSS39	GND			
F10	VSS36	GND			
F11	AUX_V33_1	3.3V			
F12	VSS33	GND			
F13	AUX_V33_0	3.3V			
F14	VSS30	GND			
F15	VSS29	GND			
F16	NA_VIO_2	VCCIO_6			
F17	VSS28	GND			
F18	VSS27	GND			
F19	VSS26	GND			
F20	VSS25	GND			
F21	NA_VIO_1	VCCIO_6			
F22	VSS19	GND			
F23	VSS18	GND			
F24	VSS17	GND			
F25	VSS16	GND			
F26	NA_VIO_0	VCCIO_6			
F27	NA_V33_0	3.3V			
F28	NA_V18_0	1.8V			
F29	VSS15	GND			
F30	VSS14	GND			
F31	SM_OE#	PISMO_SM84	H4	DIFFIO_RX68n	5
F32	SM_WE#	PISMO_SM74	K9	DIFFIO_TX70n	5
F33	SM_LBA#	PISMO_SM83	J8	DIFFIO_TX68p	5
F34	SM_BUSY#	PISMO_SM36	K2	DIFFIO_RX80n	5
F35	SM_BWAIT#	PISMO_SM37	K1	DIFFIO_RX80p	5
F36	VSS4	GND			
F37	VSS3	GND			
F38	VSS2	GND			
F39	VSS1	GND			
F40	VSS0	GND			
G01	FS_SO	PISMO_FS08	A16	CLK12p	4
G02	FS_SI	PISMO_FS07	B16	CLK12n	4
G03	DNU9	n.c.			

Table 7-3. PISMO-FPGA Signal Assignment (Continued)

PISMO Pin	Standard PISMO Name	Board Signal Name	FPGA Pin	Alternate FPGA Pin Function	FPGA Bank
G04	FS_VIO_1	VCCIO_4			
G05	FS_VIO_0	VCCIO_4			
G06	FS_V18_0	1.8V			
G07	FS_WP#	PISMO_FS09	F16	CLK13n	4
G08	AUX_SCL	PISMO_AUX06	AD3	DIFFIO_RX103p	6
G09	AUX_SDA	PISMO_AUX07	J6	DIFFIO_TX67p	5
G10	AUX_TDI	PISMO_AUX10	H6	DIFFIO_TX66n	5
G11	AUX_TCK	PISMO_AUX09	G5	DIFFIO_RX67p	5
G12	DNU13	n.c.			
G13	AUX_POR#	PISMO_AUX01	AG2	DIFFIO_RX104n	6
G14	AUX_V33_2	3.3V			
G15	DNU7	n.c.			
G16	NA_IO15	PISMO_NA13	AJ1	DIFFIO_RX108p	6
G17	NA_IO14	PISMO_NA12	AJ2	DIFFIO_RX108n	6
G18	NA_IO13	PISMO_NA11	AC6	DIFFIO_TX108p	6
G19	NA_IO12	PISMO_NA10	AC7	DIFFIO_TX108n	6
G20	NA_IO11	PISMO_NA09	AG3	DIFFIO_RX109p	6
G21	NA_IO10	PISMO_NA08	AG4	DIFFIO_RX109n	6
G22	NA_IO9	PISMO_NA21	AH1	DIFFIO_RX106p	6
G23	NA_IO8	PISMO_NA20	AH2	DIFFIO_RX106n	6
G24	DNU12	n.c.			
G25	NA_RY	PISMO_NA24	AF4	DIFFIO_RX105n	6
G26	NA_CS2#	PISMO_NA04	AH4	DIFFIO_RX110n	6
G27	NA_CS1#	PISMO_NA03	AD6	DIFFIO_TX110p	6
G28	NA_CLE	PISMO_NA01	AF5	DIFFIO_RX111p	6
G29	NA_WE#	PISMO_NA25	AF3	DIFFIO_RX105p	6
G30	DNU5	n.c.			
G31	VSS11	GND			
G32	VSS8	GND			
G33	VSS7	GND			
G34	VSS6	GND			
G35	VSS5	GND			
G36	DNU1	n.c.			
G37	SM_IRQ#	PISMO_SM81	D1	DIFFIO_RX69p	5
G38	SM_CRE	PISMO_SM42	N7	DIFFIO_TX78n	5
G39	SM_DMARQ#	PISMO_SM80	D2	DIFFIO_RX69n	5

Table 7-3. PISMO-FPGA Signal Assignment (Continued)

PISMO Pin	Standard PISMO Name	Board Signal Name	FPGA Pin	Alternate FPGA Pin Function	FPGA Bank
G40	DNU0	n.c.			
H01	FS_RESET#	PISMO_FS05	K16		4
H02	FS_HOLD#	PISMO_FS04	J15		4
H03	FS_CS3#	PISMO_FS03	A14	DQ9T	4
H04	FS_CS2#	PISMO_FS02	B13	DQSn9T	4
H05	FS_CS1#	PISMO_FS01	D13	DQ9T	4
H06	FS_CS0#	PISMO_FS00	D14	DQ9T	4
H07	AUX_SA2	PISMO_AUX05	AD4	DIFFIO_RX103n	6
H08	AUX_SA1	PISMO_AUX04	AA8	DIFFIO_TX103p	6
H09	AUX_SA0	PISMO_AUX03	AA9	DIFFIO_TX103n	6
H10	AUX_TDO	PISMO_AUX11	H5	DIFFIO_TX66p	5
H11	AUX_TMS	PISMO_AUX12	E16	CLK13p	4
H12	AUX_PRESENT#	PISMO_AUX02	AG1	DIFFIO_RX104p	6
H13	AUX_HMR#	PISMO_AUX00	AB5	DIFFIO_TX104p	6
H14	AUX_STANDBY#	PISMO_AUX08	G6	DIFFIO_RX67n	5
H15	DNU8	n.c.			
H16	NA_IO7	PISMO_NA19	AB7	DIFFIO_TX106p	6
H17	NA_IO6	PISMO_NA18	AB8	DIFFIO_TX106n	6
H18	NA_IO5	PISMO_NA17	AE5	DIFFIO_RX107p	6
H19	NA_IO4	PISMO_NA16	AE6	DIFFIO_RX107n	6
H20	NA_IO3	PISMO_NA15	AC8	DIFFIO_TX107p	6
H21	NA_IO2	PISMO_NA14	AC9	DIFFIO_TX107n	6
H22	NA_IO1	PISMO_NA07	AD8	DIFFIO_TX109p	6
H23	NA_IO0	PISMO_NA06	AD9	DIFFIO_TX109n	6
H24	NA_PRE	PISMO_NA22	AB10	DIFFIO_TX105n	6
H25	NA_RE#	PISMO_NA23	AB9	DIFFIO_TX105p	6
H26	NA_CS3#	PISMO_NA05	AH3	DIFFIO_RX110p	6
H27	NA_CS0#	PISMO_NA02	AD7	DIFFIO_TX110n	6
H28	NA_ALE	PISMO_NA00	AF6	DIFFIO_RX111n	6
H29	NA_WP#	PISMO_NA26	AB6	DIFFIO_TX104n	6
H30	DNU6	n.c.			
H31	DNU4	n.c.			
H32	DNU3	n.c.			
H33	SM_WP#	PISMO_SM82	J9	DIFFIO_TX68n	5
H34	SM_RESET#	PISMO_SM86	J7	DIFFIO_TX67n	5
H35	SM_PD	PISMO_SM85	H3	DIFFIO_RX68p	5

Table 7-3. PISMO-FPGA Signal Assignment (Continued)

PISMO Pin	Standard PISMO Name	Board Signal Name	FPGA Pin	Alternate FPGA Pin Function	FPGA Bank
H36	DNU2	n.c.			
H37	SM_CS3#	PISMO_SM46	M7	DIFFIO_TX77n	5
H38	SM_CS2#	PISMO_SM45	J1	DIFFIO_RX78p	5
H39	SM_CS1#	PISMO_SM44	J2	DIFFIO_RX78n	5
H40	SM_CS0#	PISMO_SM43	N6	DIFFIO_TX78p	5

7.7.5 User LEDs and I/O Grid

The 1.27 mm spaced I/O grid gathers miscellaneous yet unused FPGA signals. The user must be aware that some of these signals share configuration functions and therefore may be active at boot time.

Note also the four signals that drive the user LEDs

- UGRID55 (LED DS2 - left)
- UGRID56 (LED DS3)
- UGRID57 (LED DS4)
- UGRID58 (LED DS5 - right)

The grid matrix assignment is as follows:

- Column A = UGRID00.. 09 (A0 = UGRID00.. A9 = UGRID09)
- Column B = UGRID10..19
- Column C = UGRID20..29
- Column D = UGRID30..39
- Column E = UGRID40..49
- Column F = UGRID50..59
- Column G = UGRID60..69
- Column H = UGRID70..75, 3.3V, 3.3V, GND, GND

Table 7-4. I/O Grid

FPGA Bank	Pin Name	Alternate Function	Configuration Function	Board Signal Name	FPGA Bank
B8	IO		CS	AC22	UGRID00
B8	IO		CLKUSR	AD23	UGRID01
B8	IO		nWS	AE23	UGRID02
B8	IO		nRS	AF23	UGRID03
B8	IO		RUnLU	AG17	UGRID04
B8	IO		DEV_OE	AH17	UGRID05
B8	IO		DEV_CLRn	AG19	UGRID06
B8	IO		nCS	AG18	UGRID07
B12	IO	PLL12_FBn/OUT2n		AL19	UGRID08
B12	IO	PLL12_FBp/OUT2p		AM19	UGRID09
B12	IO	PLL12_OUT1n		AH18	UGRID10

Table 7-4. I/O Grid (Continued)

FPGA Bank	Pin Name	Alternate Function	Configuration Function	Board Signal Name	FPGA Bank
B12	IO	PLL12_OUT1p		AJ18	UGRID11
B12	IO	PLL12_OUT0n		AK18	UGRID12
B12	IO	PLL12_OUT0p		AL18	UGRID13
B10	IO	PLL6_OUT1p		AJ15	UGRID14
B10	IO	PLL6_OUT1n		AH15	UGRID15
B10	IO	PLL6_OUT0p		AK16	UGRID16
B10	IO	PLL6_OUT0n		AJ16	UGRID17
B10	IO	PLL6_FBp/OUT2p		AL15	UGRID18
B10	IO	PLL6_FBn/OUT2n		AK15	UGRID19
B6	FPLL9CLKp	INPUT		AJ3	UGRID20(1)
B6	FPLL9CLKn	INPUT		AJ4	UGRID21(1)
B6	IO	DIFFIO_RX98p		AC3	UGRID22
B6	IO	DIFFIO_TX97n		Y7	UGRID23
B6	IO	DIFFIO_TX97p		Y6	UGRID24
B6	IO	DIFFIO_RX97n		AC2	UGRID25
B6	IO	DIFFIO_RX97p		AC1	UGRID26
B6	IO	DIFFIO_TX96n		W5	UGRID27
B6	IO	DIFFIO_TX96p		W4	UGRID28
B6	IO	DIFFIO_RX96n		AB4	UGRID29
B6	IO	DIFFIO_RX96p		AB3	UGRID30
B6	IO	DIFFIO_TX95n		W7	UGRID31
B6	IO	DIFFIO_TX95p		W6	UGRID32
B6	IO	DIFFIO_RX95n		AB2	UGRID33
B6	IO	DIFFIO_RX95p		AB1	UGRID34
B6	IO	DIFFIO_TX94n		W9	UGRID35
B6	IO	DIFFIO_TX94p		W8	UGRID36
B6	IO	DIFFIO_RX94n		Y5	UGRID37
B6	IO	DIFFIO_RX94p		Y4	UGRID38
B6	IO	DIFFIO_TX93n		V5	UGRID39
B6	IO	DIFFIO_TX93p		V4	UGRID40
B6	IO	DIFFIO_RX93n		AA4	UGRID41
B6	IO	DIFFIO_RX93p		AA3	UGRID42
B6	IO	DIFFIO_TX92n		V7	UGRID43
B6	IO	DIFFIO_TX92p		V6	UGRID44
B6	IO	DIFFIO_RX92n		AA2	UGRID45
B6	IO	DIFFIO_RX92p		AA1	UGRID46
B6	IO	DIFFIO_TX91n		V10	UGRID47

Table 7-4. I/O Grid (Continued)

FPGA Bank	Pin Name	Alternate Function	Configuration Function	Board Signal Name	FPGA Bank
B6	IO	DIFFIO_TX91p		V9	UGRID48
B6	IO	DIFFIO_RX91n		Y3	UGRID49
B6	IO	DIFFIO_RX91p		Y2	UGRID50
B6	IO	DIFFIO_TX90n		U11	UGRID51
B6	IO	DIFFIO_TX90p		U10	UGRID52
B6	IO	DIFFIO_RX90n		W2	UGRID53
B6	IO	DIFFIO_RX90p		W1	UGRID54
B6	IO	DIFFIO_TX89n		U6	UGRID55 (LED DS2 - left)
B6	IO	DIFFIO_TX89p		U5	UGRID56 (LED DS3)
B6	IO	DIFFIO_RX89n		V3	UGRID57 (LED DS4)
B6	IO	DIFFIO_RX89p		V2	UGRID58 (LED DS5 - right)
B6	CLK9n	INPUT		U4	UGRID59(1)
B6	CLK9p	INPUT		U3	UGRID60(1)
B6	IO	CLK8n/DIFFIO_RX_C2n		U2	UGRID61
B6	IO	CLK8p/DIFFIO_RX_C2p		U1	UGRID62
B9	IO	PLL5_FBn/OUT2n		E15	UGRID63
B9	IO	PLL5_FBp/OUT2p		D15	UGRID64
B9	IO	PLL5_OUT0n		C15	UGRID65
B9	IO	PLL5_OUT0p		B15	UGRID66
B9	IO	PLL5_OUT1n		D16	UGRID67
B9	IO	PLL5_OUT1p		C16	UGRID68
B11	IO	PLL11_OUT0p		B18	UGRID69
B11	IO	PLL11_OUT0n		C18	UGRID70
B11	IO	PLL11_OUT1p		D18	UGRID71
B11	IO	PLL11_OUT1n		E18	UGRID72
B11	IO	PLL11_FBp/OUT2p		A19	UGRID73
B11	IO	PLL11_FBn/OUT2n		B19	UGRID74
B3	IO		INIT_DONE	G25	UGRID75

Note: 1. FPGA-input-only pin.

7.7.6 FPGA Pinout Tables

Table 7-5. FPGA Pins Sorted by Bank/Signal Name

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	VCCINT			AA12	1V2
	VCCINT			AC10	1V2
	VCCINT			K10	1V2
	VCCINT			K23	1V2
	VCCINT			M21	1V2
	VCCINT			N13	1V2
	VCCINT			N15	1V2
	VCCINT			N17	1V2
	VCCINT			N19	1V2
	VCCINT			P14	1V2
	VCCINT			P16	1V2
	VCCINT			P18	1V2
	VCCINT			P20	1V2
	VCCINT			R13	1V2
	VCCINT			R15	1V2
	VCCINT			R17	1V2
	VCCINT			R19	1V2
	VCCINT			T14	1V2
	VCCINT			T16	1V2
	VCCINT			T18	1V2
	VCCINT			T20	1V2
	VCCINT			U13	1V2
	VCCINT			U15	1V2
	VCCINT			U17	1V2
	VCCINT			U19	1V2
	VCCINT			V14	1V2
	VCCINT			V16	1V2
	VCCINT			V18	1V2
	VCCINT			V20	1V2
	VCCINT			W13	1V2
	VCCINT			W15	1V2
	VCCINT			W17	1V2
	VCCINT			W19	1V2
	VCCINT			W21	1V2

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	VCCINT			Y14	1V2
	VCCINT			Y16	1V2
	VCCINT			Y18	1V2
	VCCINT			Y20	1V2
	VCCPD7			AA13	3V3
	VCCPD7			AA15	3V3
	VCCPD8			AA18	3V3
	VCCPD8			AA20	3V3
	VCCPD4			M13	3V3
	VCCPD4			M15	3V3
	VCCPD3			M18	3V3
	VCCPD3			M20	3V3
	VCCPD5			N12	3V3
	VCCPD2			N21	3V3
	VCCPD5			R12	3V3
	VCCPD2			R21	3V3
	VCCPD6			V12	3V3
	VCCPD1			V21	3V3
	VCCPD6			Y12	3V3
	VCCPD1			Y21	3V3
	GND			A13	GND
	GND			A2	GND
	GND			A20	GND
	GND			A31	GND
	GND			AA14	GND
	GND			AA19	GND
	GND			AA21	GND
	GND			AB22	GND
	GND			AC28	GND
	GND			AC5	GND
	GNDA_PLL6			AD16	GND
	GNDA_PLL12			AD17	GND
	GNDA_PLL6			AE16	GND
	GNDA_PLL12			AE17	GND
	GND			AF17	GND
	GNDA_PLL9			AF7	GND

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	GND			AF9	GND
	GNDA_PLL8			AG26	GND
	GNDA_PLL8			AG27	GND
	GND			AG6	GND
	GNDA_PLL9			AG7	GND
	GND			AH10	GND
	GND			AH23	GND
	GND			AH27	GND
	GND			AL1	GND
	GND			AL32	GND
	GND			AM13	GND
	GND			AM2	GND
	GND			AM20	GND
	GND			AM31	GND
	GND			B1	GND
	TEMPDIODEn			B3	GND
	GND			B32	GND
	GND			E10	GND
	GND			E23	GND
	GNDA_PLL7			F26	GND
	GND			F27	GND
	GND			F7	GND
	GNDA_PLL5			G16	GND
	GND			G17	GND
	GNDA_PLL11			G18	GND
	GNDA_PLL7			G26	GND
	GNDA_PLL10			G7	GND
	GNDA_PLL10			G8	GND
	TEMPDIODEp			G9	GND
	GNDA_PLL5			H16	GND
	GNDA_PLL11			H18	GND
	GND			J24	GND
	GND			K28	GND
	GND			K5	GND
	GND			L11	GND
	GND			M12	GND

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	GND			M14	GND
	GND			M19	GND
	GND			N1	GND
	GND			N14	GND
	GND			N16	GND
	GND			N18	GND
	GND			N20	GND
	GND			N32	GND
	GND			P12	GND
	GND			P13	GND
	GND			P15	GND
	GND			P17	GND
	GND			P19	GND
	GND			P21	GND
	GND			R14	GND
	GND			R16	GND
	GND			R18	GND
	GND			R20	GND
	GNDA_PLL4			R8	GND
	GND			T13	GND
	GND			T15	GND
	GND			T17	GND
	GND			T19	GND
	GNDA_PLL1			T25	GND
	GNDA_PLL1			T26	GND
	GND			T7	GND
	GNDA_PLL4			T8	GND
	GND			U14	GND
	GND			U16	GND
	GND			U18	GND
	GND			U20	GND
	GNDA_PLL2			U25	GND
	GNDA_PLL2			U26	GND
	GNDA_PLL3			U8	GND
	GND			V11	GND
	GND			V13	GND

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	GND			V15	GND
	GND			V17	GND
	GND			V19	GND
	GND			V22	GND
	GND			V27	GND
	GNDA_PLL3			V8	GND
	GND			W12	GND
	GND			W14	GND
	GND			W16	GND
	GND			W18	GND
	GND			W20	GND
	GND			Y1	GND
	GND			Y13	GND
	GND			Y15	GND
	GND			Y17	GND
	GND			Y19	GND
	GND			Y32	GND
	VCCA_PLL6			AE15	VCCA_PLL
	VCCA_PLL9			AE7	VCCA_PLL
	VCCA_PLL12			AF18	VCCA_PLL
	VCCA_PLL8			AF26	VCCA_PLL
	VCCA_PLL5			G15	VCCA_PLL
	VCCA_PLL11			H17	VCCA_PLL
	VCCA_PLL7			H26	VCCA_PLL
	VCCA_PLL10			H8	VCCA_PLL
	VCCA_PLL4			R9	VCCA_PLL
	VCCA_PLL1			T24	VCCA_PLL
	VCCA_PLL3			U9	VCCA_PLL
	VCCA_PLL2			V26	VCCA_PLL
	VCCD_PLL6			AD15	VCCD_PLL
	VCCD_PLL12			AE18	VCCD_PLL
	VCCD_PLL9			AE8	VCCD_PLL
	VCCD_PLL8			AF25	VCCD_PLL
	VCCD_PLL5			H15	VCCD_PLL
	VCCD_PLL7			H25	VCCD_PLL
	VCCD_PLL10			H7	VCCD_PLL

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	VCCD_PLL11			J18	VCCD_PLL
	VCCD_PLL4			T9	VCCD_PLL
	VCCD_PLL1			U24	VCCD_PLL
	VCCD_PLL3			U7	VCCD_PLL
	VCCD_PLL2			V25	VCCD_PLL
	VCCIO1			AA28	VCCIO_1
	VCCIO1			AK32	VCCIO_1
	VCCIO1			U21	VCCIO_1
	VCCIO1			V32	VCCIO_1
	VCCIO2			C32	VCCIO_2
	VCCIO2			M28	VCCIO_2
	VCCIO2			R32	VCCIO_2
	VCCIO2			T21	VCCIO_2
	VCCIO3			A18	VCCIO_3
	VCCIO3			A30	VCCIO_3
	VCCIO3			E21	VCCIO_3
	VCCIO3			M17	VCCIO_3
	VCCIO4			A15	VCCIO_4
	VCCIO4			A3	VCCIO_4
	VCCIO4			E12	VCCIO_4
	VCCIO4			M16	VCCIO_4
	VCCIO5			C1	VCCIO_5
	VCCIO5			M5	VCCIO_5
	VCCIO5			R1	VCCIO_5
	VCCIO5			T12	VCCIO_5
	VCCIO6			AA5	VCCIO_6
	VCCIO6			AK1	VCCIO_6
	VCCIO6			U12	VCCIO_6
	VCCIO6			V1	VCCIO_6
	VCCIO7			AA16	VCCIO_7
	VCCIO7			AH12	VCCIO_7
	VCCIO7			AM15	VCCIO_7
	VCCIO7			AM3	VCCIO_7
	VCCIO8			AA17	VCCIO_8
	VCCIO8			AH21	VCCIO_8
	VCCIO8			AM18	VCCIO_8

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	VCCIO8			AM30	VCCIO_8
B1	IO	CLK2p/DIFFIO_RX_C1p		U32	FPGA0
B1	IO	CLK2n/DIFFIO_RX_C1n		U31	FPGA1
B1	IO	DIFFIO_TX27p		U28	FPGA10
B1	IO	DIFFIO_TX27n		U27	FPGA11
B1	IO	DIFFIO_RX26p		AA32	FPGA12
B1	IO	DIFFIO_RX26n		AA31	FPGA13
B1	IO	DIFFIO_TX26p		V29	FPGA14
B1	IO	DIFFIO_TX26n		V28	FPGA15
B1	IO	DIFFIO_RX25p		Y31	FPGA16
B1	IO	DIFFIO_RX25n		Y30	FPGA17
B1	IO	DIFFIO_TX25p		V24	FPGA18
B1	IO	DIFFIO_TX25n		V23	FPGA19
B1	CLK3p	INPUT		U30	FPGA2
B1	IO	DIFFIO_RX24p		AB32	FPGA20
B1	IO	DIFFIO_RX24n		AB31	FPGA21
B1	IO	DIFFIO_TX24p		W29	FPGA22
B1	IO	DIFFIO_TX24n		W28	FPGA23
B1	IO	DIFFIO_RX23p		AA30	FPGA24
B1	IO	DIFFIO_RX23n		AA29	FPGA25
B1	IO	DIFFIO_TX23p		W27	FPGA26
B1	IO	DIFFIO_TX23n		W26	FPGA27
B1	IO	DIFFIO_RX22p		Y29	FPGA28
B1	IO	DIFFIO_RX22n		Y28	FPGA29
B1	CLK3n	INPUT		U29	FPGA3
B1	IO	DIFFIO_TX22p		W25	FPGA30
B1	IO	DIFFIO_TX22n		W24	FPGA31
B1	IO	DIFFIO_RX21p		AB30	FPGA32
B1	IO	DIFFIO_RX21n		AB29	FPGA33
B1	IO	DIFFIO_TX21p		Y27	FPGA34
B1	IO	DIFFIO_TX21n		Y26	FPGA35
B1	IO	DIFFIO_RX20p		AC32	FPGA36
B1	IO	DIFFIO_RX20n		AC31	FPGA37
B1	IO	DIFFIO_TX20p		AA27	FPGA38
B1	IO	DIFFIO_TX20n		AA26	FPGA39
B1	IO	DIFFIO_RX28p		V31	FPGA4

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B1	IO	DIFFIO_RX19p		AB28	FPGA40
B1	IO	DIFFIO_RX19n		AB27	FPGA41
B1	IO	DIFFIO_TX19p		Y25	FPGA42
B1	IO	DIFFIO_TX19n		Y24	FPGA43
B1	IO	DIFFIO_RX18p		AD32	FPGA44
B1	IO	DIFFIO_RX18n		AD31	FPGA45
B1	IO	DIFFIO_TX18p		W23	FPGA46
B1	IO	DIFFIO_TX18n		W22	FPGA47
B1	IO	DIFFIO_RX17p		AE32	FPGA48
B1	IO	DIFFIO_RX17n		AE31	FPGA49
B1	IO	DIFFIO_RX28n		V30	FPGA5
B1	IO	DIFFIO_TX17p		AD27	FPGA50
B1	IO	DIFFIO_TX17n		AD26	FPGA51
B1	IO	DIFFIO_RX16p		AF32	FPGA52
B1	IO	DIFFIO_RX16n		AF31	FPGA53
B1	IO	DIFFIO_TX16p		AC27	FPGA54
B1	IO	DIFFIO_TX16n		AC26	FPGA55
B1	IO	DIFFIO_RX15p		AG32	FPGA56
B1	IO	DIFFIO_RX15n		AG31	FPGA57
B1	IO	DIFFIO_TX15p		Y23	FPGA58
B1	IO	DIFFIO_TX15n		Y22	FPGA59
B1	IO	DIFFIO_TX28p		U23	FPGA6
B1	IO	DIFFIO_RX14p		AC30	FPGA60
B1	IO	DIFFIO_RX14n		AC29	FPGA61
B1	IO	DIFFIO_TX14p		AA25	FPGA62
B1	IO	DIFFIO_TX14n		AA24	FPGA63
B1	IO	DIFFIO_RX13p		AD30	FPGA64
B1	IO	DIFFIO_RX13n		AD29	FPGA65
B1	IO	DIFFIO_TX13p		AB26	FPGA66
B1	IO	DIFFIO_TX13n		AB25	FPGA67
B1	IO	DIFFIO_RX12p		AH32	FPGA68
B1	IO	DIFFIO_RX12n		AH31	FPGA69
B1	IO	DIFFIO_TX28n		U22	FPGA7
B1	IO	DIFFIO_TX12p		AA23	FPGA70
B1	IO	DIFFIO_TX12n		AA22	FPGA71
B1	IO	DIFFIO_RX11p		AE30	FPGA72

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B1	IO	DIFFIO_RX11n		AE29	FPGA73
B1	IO	DIFFIO_TX11p		AB24	FPGA74
B1	IO	DIFFIO_TX11n		AB23	FPGA75
B1	IO	DIFFIO_RX10p		AJ32	FPGA76
B1	IO	DIFFIO_RX10n		AJ31	FPGA77
B1	IO	DIFFIO_TX10p		AC25	FPGA78
B1	IO	DIFFIO_TX10n		AC24	FPGA79
B1	IO	DIFFIO_RX27p		W32	FPGA8
B1	IO	DIFFIO_RX9p		AF30	FPGA80
B1	IO	DIFFIO_RX9n		AF29	FPGA81
B1	IO	DIFFIO_TX9p		AD25	FPGA82
B1	IO	DIFFIO_TX9n		AD24	FPGA83
B1	IO	DIFFIO_RX8p		AG30	FPGA84
B1	IO	DIFFIO_RX8n		AG29	FPGA85
B1	IO	DIFFIO_TX8p		AE26	FPGA86
B1	IO	DIFFIO_TX8n		AE25	FPGA87
B1	IO	DIFFIO_RX7p		AH30	FPGA88
B1	IO	DIFFIO_RX7n		AH29	FPGA89
B1	IO	DIFFIO_RX27n		W31	FPGA9
B1	IO	DIFFIO_TX7p		AE28	FPGA90
B1	IO	DIFFIO_TX7n		AE27	FPGA91
B1	IO	DIFFIO_RX6p		AF28	FPGA92
B1	IO	DIFFIO_RX6n		AF27	FPGA93
B1	FPLL8CLKn	INPUT		AJ29	FPGA94
B1	FPLL8CLKp	INPUT		AJ30	FPGA95
B1	VREFB1N1	VREFB1N1		AD28	VREFB1
B1	VREFB1N2	VREFB1N2		AG28	VREFB1
B1	VREFB1N0	VREFB1N0		W30	VREFB1
B10	IO	PLL6_OUT1p		AJ15	UGRID14
B10	IO	PLL6_OUT1n		AH15	UGRID15
B10	IO	PLL6_OUT0p		AK16	UGRID16
B10	IO	PLL6_OUT0n		AJ16	UGRID17
B10	IO	PLL6_FBp/OUT2p		AL15	UGRID18
B10	IO	PLL6_FBn/OUT2n		AK15	UGRID19
B10	VCC_PLL6_OUT			AF15	VCC_PLL6
B11	IO	PLL11_OUT0p		B18	UGRID69

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B11	IO	PLL11_OUT0n		C18	UGRID70
B11	IO	PLL11_OUT1p		D18	UGRID71
B11	IO	PLL11_OUT1n		E18	UGRID72
B11	IO	PLL11_FBp/OUT2p		A19	UGRID73
B11	IO	PLL11_FBn/OUT2n		B19	UGRID74
B11	VCC_PLL11_OUT			J17	VCC_PLL11
B12	IO	PLL12_OUT1n		AH18	UGRID10
B12	IO	PLL12_OUT1p		AJ18	UGRID11
B12	IO	PLL12_OUT0n		AK18	UGRID12
B12	IO	PLL12_OUT0p		AL18	UGRID13
B12	IO	PLL12_FBn/OUT2n		AL19	UGRID8
B12	IO	PLL12_FBp/OUT2p		AM19	UGRID9
B12	VCC_PLL12_OUT			AF16	VCC_PLL12
B2	IO	DIFFIO_RX50p		G28	FPGA100
B2	IO	DIFFIO_RX50n		G27	FPGA101
B2	IO	DIFFIO_TX50p		H28	FPGA102
B2	IO	DIFFIO_TX50n		H27	FPGA103
B2	IO	DIFFIO_RX49p		E30	FPGA104
B2	IO	DIFFIO_RX49n		E29	FPGA105
B2	IO	DIFFIO_TX49p		K27	FPGA106
B2	IO	DIFFIO_TX49n		K26	FPGA107
B2	IO	DIFFIO_RX48p		D32	FPGA108
B2	IO	DIFFIO_RX48n		D31	FPGA109
B2	IO	DIFFIO_TX48p		J27	FPGA110
B2	IO	DIFFIO_TX48n		J26	FPGA111
B2	IO	DIFFIO_RX47p		F30	FPGA112
B2	IO	DIFFIO_RX47n		F29	FPGA113
B2	IO	DIFFIO_TX47p		L28	FPGA114
B2	IO	DIFFIO_TX47n		L27	FPGA115
B2	IO	DIFFIO_RX46p		G30	FPGA116
B2	IO	DIFFIO_RX46n		G29	FPGA117
B2	IO	DIFFIO_TX46p		L26	FPGA118
B2	IO	DIFFIO_TX46n		L25	FPGA119
B2	IO	DIFFIO_RX45p		H30	FPGA120
B2	IO	DIFFIO_RX45n		H29	FPGA121
B2	IO	DIFFIO_TX45p		L24	FPGA122

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B2	IO	DIFFIO_TX45n		L23	FPGA123
B2	IO	DIFFIO_RX44p		J30	FPGA124
B2	IO	DIFFIO_RX44n		J29	FPGA125
B2	IO	DIFFIO_TX44p		M25	FPGA126
B2	IO	DIFFIO_TX44n		M24	FPGA127
B2	IO	DIFFIO_RX43p		E32	FPGA128
B2	IO	DIFFIO_RX43n		E31	FPGA129
B2	IO	DIFFIO_TX43p		M23	FPGA130
B2	IO	DIFFIO_TX43n		M22	FPGA131
B2	IO	DIFFIO_RX42p		F32	FPGA132
B2	IO	DIFFIO_RX42n		F31	FPGA133
B2	IO	DIFFIO_TX42p		M27	FPGA134
B2	IO	DIFFIO_TX42n		M26	FPGA135
B2	IO	DIFFIO_RX41p		G32	FPGA136
B2	IO	DIFFIO_RX41n		G31	FPGA137
B2	IO	DIFFIO_TX41p		N25	FPGA138
B2	IO	DIFFIO_TX41n		N24	FPGA139
B2	IO	DIFFIO_RX40p		H32	FPGA140
B2	IO	DIFFIO_RX40n		H31	FPGA141
B2	IO	DIFFIO_TX40p		N23	FPGA142
B2	IO	DIFFIO_TX40n		N22	FPGA143
B2	IO	DIFFIO_RX39p		J32	FPGA144
B2	IO	DIFFIO_RX39n		J31	FPGA145
B2	IO	DIFFIO_TX39p		P23	FPGA146
B2	IO	DIFFIO_TX39n		P22	FPGA147
B2	IO	DIFFIO_RX38p		K30	FPGA148
B2	IO	DIFFIO_RX38n		K29	FPGA149
B2	IO	DIFFIO_TX38p		N27	FPGA150
B2	IO	DIFFIO_TX38n		N26	FPGA151
B2	IO	DIFFIO_RX37p		K32	FPGA152
B2	IO	DIFFIO_RX37n		K31	FPGA153
B2	IO	DIFFIO_TX37p		P29	FPGA154
B2	IO	DIFFIO_TX37n		P28	FPGA155
B2	IO	DIFFIO_RX36p		L30	FPGA156
B2	IO	DIFFIO_RX36n		L29	FPGA157
B2	IO	DIFFIO_TX36p		P27	FPGA158

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B2	IO	DIFFIO_TX36n		P26	FPGA159
B2	IO	DIFFIO_RX35p		N29	FPGA160
B2	IO	DIFFIO_RX35n		N28	FPGA161
B2	IO	DIFFIO_TX35p		P25	FPGA162
B2	IO	DIFFIO_TX35n		P24	FPGA163
B2	IO	DIFFIO_RX34p		M30	FPGA164
B2	IO	DIFFIO_RX34n		M29	FPGA165
B2	IO	DIFFIO_TX34p		R27	FPGA166
B2	IO	DIFFIO_TX34n		R26	FPGA167
B2	IO	DIFFIO_RX33p		L32	FPGA168
B2	IO	DIFFIO_RX33n		L31	FPGA169
B2	IO	DIFFIO_TX33p		R23	FPGA170
B2	IO	DIFFIO_TX33n		R22	FPGA171
B2	IO	DIFFIO_RX32p		N31	FPGA172
B2	IO	DIFFIO_RX32n		N30	FPGA173
B2	IO	DIFFIO_TX32p		R25	FPGA174
B2	CLK1p	INPUT		T30	FPGA175
B2	IO	DIFFIO_RX31p		M32	FPGA176
B2	IO	DIFFIO_RX31n		M31	FPGA177
B2	IO	DIFFIO_TX31p		R29	FPGA178
B2	IO	DIFFIO_TX31n		R28	FPGA179
B2	IO	DIFFIO_RX30p		P32	FPGA180
B2	IO	DIFFIO_RX30n		P31	FPGA181
B2	IO	DIFFIO_TX30p		T28	FPGA182
B2	IO	DIFFIO_TX30n		T27	FPGA183
B2	IO	DIFFIO_RX29p		R31	FPGA184
B2	IO	DIFFIO_RX29n		R30	FPGA185
B2	IO	DIFFIO_TX29p		T23	FPGA186
B2	IO	DIFFIO_TX29n		T22	FPGA187
B2	IO	CLK0n/DIFFIO_RX_C0n		T31	FPGA188
B2	IO	CLK0p/DIFFIO_RX_C0p		T32	FPGA189
B2	CLK1n	INPUT		T29	FPGA190
B2	IO	DIFFIO_TX32n		R24	FPGA191
B2	FPLL7CLKp	INPUT		D30	FPGA96
B2	FPLL7CLKn	INPUT		D29	FPGA97
B2	IO	DIFFIO_TX51p		K25	FPGA98

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B2	IO	DIFFIO_TX51n		K24	FPGA99
B2	VREFB2N0	VREFB2N0		F28	VREFB2
B2	VREFB2N1	VREFB2N1		J28	VREFB2
B2	VREFB2N2	VREFB2N2		P30	VREFB2
B3	IO		ASDO	F17	ASDO
B3	CONF_DONE		CONF_DONE	J25	CONFIG_DONE
B3	IO		DATA0	H19	DATA0
B3	DCLK		DCLK	B31	DCLK
B3	IO	CLK14p		A17	FPGA192
B3	IO	CLK14n		B17	FPGA193
B3	IO	CLK15p		C17	FPGA194
B3	IO	CLK15n		D17	FPGA195
B3	IO			K18	FPGA196
B3	IO		PGM2	F18	FPGA197
B3	IO		PGM1	F19	FPGA198
B3	IO		PGM0	E17	FPGA199
B3	IO		CRC_ERROR	G20	FPGA200
B3	IO		DATA1	F20	FPGA201
B3	IO	DQS10T		D19	FPGA202
B3	IO	DQ10T		B20	FPGA203
B3	IO	DQ10T		E19	FPGA204
B3	IO	DQ10T		C20	FPGA205
B3	IO	DQSn10T		D20	FPGA206
B3	IO	DQ10T		E20	FPGA207
B3	IO			L19	FPGA208
B3	IO			L18	FPGA209
B3	IO			J19	FPGA210
B3	IO			K19	FPGA211
B3	IO	DQS11T		B21	FPGA212
B3	IO	DQ11T		A21	FPGA213
B3	IO	DQ11T		C21	FPGA214
B3	IO	DQ11T		A22	FPGA215
B3	IO	DQSn11T		B22	FPGA216
B3	IO	DQ11T		C22	FPGA217
B3	IO			L20	FPGA218
B3	IO			H20	FPGA219

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B3	IO			K20	FPGA220
B3	IO	DQS12T		D22	FPGA221
B3	IO	DQ12T		D23	FPGA222
B3	IO	DQ12T		D21	FPGA223
B3	IO	DQ12T		F22	FPGA224
B3	IO	DQSn12T		E22	FPGA225
B3	IO	DQ12T		F23	FPGA226
B3	IO			L21	FPGA227
B3	IO			J20	FPGA228
B3	IO	DQS13T		B23	FPGA229
B3	IO	DQ13T		A23	FPGA230
B3	IO	DQ13T		C23	FPGA231
B3	IO	DQ13T		C24	FPGA232
B3	IO	DQSn13T		B24	FPGA233
B3	IO	DQ13T		A24	FPGA234
B3	IO			K21	FPGA235
B3	IO			H21	FPGA236
B3	IO			J21	FPGA237
B3	IO	DQS14T		B25	FPGA238
B3	IO	DQ14T		A25	FPGA239
B3	IO	DQ14T		A26	FPGA240
B3	IO	DQ14T		D26	FPGA241
B3	IO	DQSn14T		B26	FPGA242
B3	IO	DQ14T		C26	FPGA243
B3	IO			G21	FPGA244
B3	IO	DQS15T		D25	FPGA245
B3	IO	DQ15T		E24	FPGA246
B3	IO	DQ15T		C25	FPGA247
B3	IO	DQ15T		E27	FPGA248
B3	IO	DQSn15T		E25	FPGA249
B3	IO	DQ15T		E26	FPGA250
B3	IO			F21	FPGA251
B3	IO	DQS16T		B27	FPGA252
B3	IO	DQ16T		A27	FPGA253
B3	IO	DQ16T		A28	FPGA254
B3	IO	DQ16T		D27	FPGA255

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B3	IO	DQSn16T		B28	FPGA256
B3	IO	DQ16T		C27	FPGA257
B3	IO			H22	FPGA258
B3	IO			J22	FPGA259
B3	IO	DQS17T		C28	FPGA260
B3	IO	DQ17T		B29	FPGA261
B3	IO	DQ17T		A29	FPGA262
B3	IO	DQ17T		D28	FPGA263
B3	IO	DQSn17T		C29	FPGA264
B3	IO	DQ17T		E28	FPGA265
B3	IO			K22	FPGA266
B3	IO			F25	FPGA267
B3	IO			G22	FPGA268
B3	IO		DATA2	G23	FPGA269
B3	IO		DATA3	H23	FPGA270
B3	IO		DATA4	J23	FPGA271
B3	IO		DATA5	L22	FPGA272
B3	IO		DATA6	F24	FPGA273
B3	IO		DATA7	G24	FPGA274
B3	IO		RDYnBSY	H24	FPGA275
B3	nCE		nCE	C30	NCE
B3	IO		nCSO	G19	NCSO
B3	nSTATUS		nSTATUS	B30	NSTATUS
B3	IO		INIT_DONE	G25	UGRID75
B3	VREFB3N0	VREFB3N0		C19	VREFB3
B3	VREFB3N2	VREFB3N2		C31	VREFB3
B3	VREFB3N1	VREFB3N1		D24	VREFB3
B4	MSEL0		MSEL0	B2	MSEL0
B4	MSEL1		MSEL1	F6	MSEL1
B4	MSEL2		MSEL2	J10	MSEL2
B4	MSEL3		MSEL3	H10	MSEL3
B4	IO	CLK13p		E16	PISMO_AUX12
B4	IO	DQ0T		B4	PISMO_DM_DA0
B4	IO	DQ0T		D5	PISMO_DM_DA1
B4	IO	DQ0T		E5	PISMO_DM_DA2
B4	IO	DQ0T		A4	PISMO_DM_DA3

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B4	IO	DQ1T		A5	PISMO_DM_DA4
B4	IO	DQ1T		D6	PISMO_DM_DA5
B4	IO	DQ1T		C6	PISMO_DM_DA6
B4	IO	DQSn1T		B6	PISMO_DM_DA7
B4	IO	DQ2T		B7	PISMO_DM_DB0
B4	IO	DQ2T		E7	PISMO_DM_DB1
B4	IO	DQ2T		E6	PISMO_DM_DB2
B4	IO	DQ2T		A7	PISMO_DM_DB3
B4	IO	DQ3T		C9	PISMO_DM_DB4
B4	IO	DQ3T		A8	PISMO_DM_DB5
B4	IO	DQ3T		C8	PISMO_DM_DB6
B4	IO	DQSn3T		B9	PISMO_DM_DB7
B4	IO	DQ4T		D8	PISMO_DM_DC0
B4	IO	DQ4T		E8	PISMO_DM_DC1
B4	IO	DQ4T		F8	PISMO_DM_DC2
B4	IO	DQ4T		F10	PISMO_DM_DC3
B4	IO	DQS5T		C10	PISMO_DM_DC4
B4	IO	DQ5T		A10	PISMO_DM_DC5
B4	IO	DQ5T		B10	PISMO_DM_DC6
B4	IO	DQ5T		D10	PISMO_DM_DC7
B4	IO	DQ6T		E11	PISMO_DM_DD0
B4	IO	DQ6T		G10	PISMO_DM_DD1
B4	IO	DQ6T		G11	PISMO_DM_DD2
B4	IO	DQ6T		G12	PISMO_DM_DD3
B4	IO	DQS7T		C12	PISMO_DM_DD4
B4	IO	DQ7T		D12	PISMO_DM_DD5
B4	IO	DQ7T		A11	PISMO_DM_DD6
B4	IO	DQ7T		B11	PISMO_DM_DD7
B4	IO	DQS0T		C4	PISMO_DM_DQSA_DH
B4	IO	DQSn0T		C5	PISMO_DM_DQSA_DL
B4	IO	DQS2T		D7	PISMO_DM_DQSB_DH
B4	IO	DQSn2T		C7	PISMO_DM_DQSB_DL
B4	IO	DQS4T		F9	PISMO_DM_DQSC_DH

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B4	IO	DQSn4T		E9	PISMO_DM_DQSC_DL
B4	IO	DQS6T		F11	PISMO_DM_DQSD_DH
B4	IO	DQSn6T		F12	PISMO_DM_DQSD_DL
B4	IO			H9	PISMO_DM0
B4	IO			J11	PISMO_DM1
B4	IO			L15	PISMO_DM10
B4	IO			K13	PISMO_DM11
B4	IO			J12	PISMO_DM12
B4	IO	DQS3T		B8	PISMO_DM13
B4	IO	DQ3T		A9	PISMO_DM14
B4	IO			H12	PISMO_DM15
B4	IO			K14	PISMO_DM16
B4	IO			J13	PISMO_DM17
B4	IO			L16	PISMO_DM18
B4	IO	DQSn5T		C11	PISMO_DM19
B4	IO	RUP4		L12	PISMO_DM2
B4	IO	DQ5T		D11	PISMO_DM20
B4	IO			K15	PISMO_DM21
B4	IO			H13	PISMO_DM22
B4	IO			J14	PISMO_DM23
B4	IO	DQSn7T		B12	PISMO_DM24
B4	IO	DQ7T		A12	PISMO_DM25
B4	IO			G14	PISMO_DM26
B4	IO	DQS8T		F14	PISMO_DM27
B4	IO	DQ8T		E13	PISMO_DM28
B4	IO	DQ8T		F13	PISMO_DM29
B4	IO	RDN4		K11	PISMO_DM3
B4	IO	DQ8T		G13	PISMO_DM30
B4	IO	DQSn8T		E14	PISMO_DM31
B4	IO	DQ8T		F15	PISMO_DM32
B4	IO			H14	PISMO_DM33
B4	IO			L17	PISMO_DM34
B4	IO	DQS9T		C13	PISMO_DM35
B4	IO	DQ9T		B14	PISMO_DM36

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B4	IO			H11	PISMO_DM4
B4	IO			K12	PISMO_DM5
B4	IO			L13	PISMO_DM6
B4	IO			L14	PISMO_DM7
B4	IO	DQS1T		B5	PISMO_DM8
B4	IO	DQ1T		A6	PISMO_DM9
B4	IO	DQ9T		D14	PISMO_FS0
B4	IO	DQ9T		D13	PISMO_FS1
B4	IO	DQSn9T		B13	PISMO_FS2
B4	IO	DQ9T		A14	PISMO_FS3
B4	IO			J15	PISMO_FS4
B4	IO			K16	PISMO_FS5
B4	IO			K17	PISMO_FS6
B4	IO	CLK12n		B16	PISMO_FS7
B4	IO	CLK12p		A16	PISMO_FS8
B4	IO	CLK13n		F16	PISMO_FS9
B4	TDO		TDO	C3	S2_TDO
B4	VREFB4N2	VREFB4N2		C14	VREFB4
B4	VREFB4N0	VREFB4N0		C2	VREFB4
B4	VREFB4N1	VREFB4N1		D9	VREFB4
B5	CLK11n	INPUT		T4	EXT_CLK
B5	IO	DIFFIO_TX66n		H6	PISMO_AUX10
B5	IO	DIFFIO_TX66p		H5	PISMO_AUX11
B5	IO	DIFFIO_TX67p		J6	PISMO_AUX7
B5	IO	DIFFIO_RX67n		G6	PISMO_AUX8
B5	IO	DIFFIO_RX67p		G5	PISMO_AUX9
B5	IO	CLK10p/DIFFIO_RX_C3p		T1	PISMO_SM0
B5	IO	CLK10n/DIFFIO_RX_C3n		T2	PISMO_SM1
B5	IO	DIFFIO_TX86n		R11	PISMO_SM10
B5	IO	DIFFIO_TX86p		R10	PISMO_SM11
B5	IO	DIFFIO_RX86n		M2	PISMO_SM12
B5	IO	DIFFIO_RX86p		M1	PISMO_SM13
B5	IO	DIFFIO_TX85n		R5	PISMO_SM14
B5	IO	DIFFIO_TX85p		R4	PISMO_SM15
B5	IO	DIFFIO_RX85n		N3	PISMO_SM16
B5	IO	DIFFIO_RX85p		N2	PISMO_SM17

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B5	IO	DIFFIO_TX84n		R7	PISMO_SM18
B5	IO	DIFFIO_TX84p		R6	PISMO_SM19
B5	IO	DIFFIO_TX88n		T11	PISMO_SM2
B5	IO	DIFFIO_RX84n		L2	PISMO_SM20
B5	IO	DIFFIO_RX84p		L1	PISMO_SM21
B5	IO	DIFFIO_TX83n		P11	PISMO_SM22
B5	IO	DIFFIO_TX83p		P10	PISMO_SM23
B5	IO	DIFFIO_RX83n		M4	PISMO_SM24
B5	IO	DIFFIO_RX83p		M3	PISMO_SM25
B5	IO	DIFFIO_TX82n		P5	PISMO_SM26
B5	IO	DIFFIO_TX82p		P4	PISMO_SM27
B5	IO	DIFFIO_RX82n		N5	PISMO_SM28
B5	IO	DIFFIO_RX82p		N4	PISMO_SM29
B5	IO	DIFFIO_TX88p		T10	PISMO_SM3
B5	IO	DIFFIO_TX81n		P7	PISMO_SM30
B5	IO	DIFFIO_TX81p		P6	PISMO_SM31
B5	IO	DIFFIO_RX81n		L4	PISMO_SM32
B5	IO	DIFFIO_RX81p		L3	PISMO_SM33
B5	IO	DIFFIO_TX80n		P9	PISMO_SM34
B5	IO	DIFFIO_TX80p		P8	PISMO_SM35
B5	IO	DIFFIO_RX80n		K2	PISMO_SM36
B5	IO	DIFFIO_RX80p		K1	PISMO_SM37
B5	IO	DIFFIO_TX79n		N9	PISMO_SM38
B5	IO	DIFFIO_TX79p		N8	PISMO_SM39
B5	IO	DIFFIO_RX88n		P2	PISMO_SM4
B5	IO	DIFFIO_RX79n		K4	PISMO_SM40
B5	IO	DIFFIO_RX79p		K3	PISMO_SM41
B5	IO	DIFFIO_TX78n		N7	PISMO_SM42
B5	IO	DIFFIO_TX78p		N6	PISMO_SM43
B5	IO	DIFFIO_RX78n		J2	PISMO_SM44
B5	IO	DIFFIO_RX78p		J1	PISMO_SM45
B5	IO	DIFFIO_TX77n		M7	PISMO_SM46
B5	IO	DIFFIO_TX77p		M6	PISMO_SM47
B5	IO	DIFFIO_RX77n		H2	PISMO_SM48
B5	IO	DIFFIO_RX77p		H1	PISMO_SM49
B5	IO	DIFFIO_RX88p		P1	PISMO_SM5

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B5	IO	DIFFIO_TX76n		N11	PISMO_SM50
B5	IO	DIFFIO_TX76p		N10	PISMO_SM51
B5	IO	DIFFIO_RX76n		J4	PISMO_SM52
B5	IO	DIFFIO_RX76p		J3	PISMO_SM53
B5	IO	DIFFIO_TX75n		M11	PISMO_SM54
B5	IO	DIFFIO_TX75p		M10	PISMO_SM55
B5	IO	DIFFIO_RX75n		G2	PISMO_SM56
B5	IO	DIFFIO_RX75p		G1	PISMO_SM57
B5	IO	DIFFIO_TX74n		L6	PISMO_SM58
B5	IO	DIFFIO_TX74p		L5	PISMO_SM59
B5	IO	DIFFIO_TX87n		T6	PISMO_SM6
B5	IO	DIFFIO_RX74n		G4	PISMO_SM60
B5	IO	DIFFIO_RX74p		G3	PISMO_SM61
B5	IO	DIFFIO_TX73n		M9	PISMO_SM62
B5	IO	DIFFIO_TX73p		M8	PISMO_SM63
B5	IO	DIFFIO_RX73n		F2	PISMO_SM64
B5	IO	DIFFIO_RX73p		F1	PISMO_SM65
B5	IO	DIFFIO_TX72n		L10	PISMO_SM66
B5	IO	DIFFIO_TX72p		L9	PISMO_SM67
B5	IO	DIFFIO_RX72n		F4	PISMO_SM68
B5	IO	DIFFIO_RX72p		F3	PISMO_SM69
B5	IO	DIFFIO_TX87p		T5	PISMO_SM7
B5	IO	DIFFIO_TX71n		L8	PISMO_SM70
B5	IO	DIFFIO_TX71p		L7	PISMO_SM71
B5	IO	DIFFIO_RX71n		E2	PISMO_SM72
B5	IO	DIFFIO_RX71p		E1	PISMO_SM73
B5	IO	DIFFIO_TX70n		K9	PISMO_SM74
B5	IO	DIFFIO_TX70p		K8	PISMO_SM75
B5	IO	DIFFIO_RX70n		E4	PISMO_SM76
B5	IO	DIFFIO_RX70p		E3	PISMO_SM77
B5	IO	DIFFIO_TX69n		K7	PISMO_SM78
B5	IO	DIFFIO_TX69p		K6	PISMO_SM79
B5	IO	DIFFIO_RX87n		R3	PISMO_SM8
B5	IO	DIFFIO_RX69n		D2	PISMO_SM80
B5	IO	DIFFIO_RX69p		D1	PISMO_SM81
B5	IO	DIFFIO_TX68n		J9	PISMO_SM82

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B5	IO	DIFFIO_TX68p		J8	PISMO_SM83
B5	IO	DIFFIO_RX68n		H4	PISMO_SM84
B5	IO	DIFFIO_RX68p		H3	PISMO_SM85
B5	IO	DIFFIO_TX67n		J7	PISMO_SM86
B5	FPLL10CLKn	INPUT		D4	PISMO_SM87
B5	FPLL10CLKp	INPUT		D3	PISMO_SM88
B5	IO	DIFFIO_RX87p		R2	PISMO_SM9
B5	VREFB5N2	VREFB5N2		F5	VREFB5
B5	VREFB5N1	VREFB5N1		J5	VREFB5
B5	VREFB5N0	VREFB5N0		P3	VREFB5
B5	CLK11p	INPUT		T3	XTAL_CLK
B6	IO	DIFFIO_TX104p		AB5	PISMO_AUX0
B6	IO	DIFFIO_RX104n		AG2	PISMO_AUX1
B6	IO	DIFFIO_RX104p		AG1	PISMO_AUX2
B6	IO	DIFFIO_TX103n		AA9	PISMO_AUX3
B6	IO	DIFFIO_TX103p		AA8	PISMO_AUX4
B6	IO	DIFFIO_RX103n		AD4	PISMO_AUX5
B6	IO	DIFFIO_RX103p		AD3	PISMO_AUX6
B6	IO	DIFFIO_RX111n		AF6	PISMO_NA0
B6	IO	DIFFIO_RX111p		AF5	PISMO_NA1
B6	IO	DIFFIO_TX108n		AC7	PISMO_NA10
B6	IO	DIFFIO_TX108p		AC6	PISMO_NA11
B6	IO	DIFFIO_RX108n		AJ2	PISMO_NA12
B6	IO	DIFFIO_RX108p		AJ1	PISMO_NA13
B6	IO	DIFFIO_TX107n		AC9	PISMO_NA14
B6	IO	DIFFIO_TX107p		AC8	PISMO_NA15
B6	IO	DIFFIO_RX107n		AE6	PISMO_NA16
B6	IO	DIFFIO_RX107p		AE5	PISMO_NA17
B6	IO	DIFFIO_TX106n		AB8	PISMO_NA18
B6	IO	DIFFIO_TX106p		AB7	PISMO_NA19
B6	IO	DIFFIO_TX110n		AD7	PISMO_NA2
B6	IO	DIFFIO_RX106n		AH2	PISMO_NA20
B6	IO	DIFFIO_RX106p		AH1	PISMO_NA21
B6	IO	DIFFIO_TX105n		AB10	PISMO_NA22
B6	IO	DIFFIO_TX105p		AB9	PISMO_NA23
B6	IO	DIFFIO_RX105n		AF4	PISMO_NA24

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B6	IO	DIFFIO_RX105p		AF3	PISMO_NA25
B6	IO	DIFFIO_TX104n		AB6	PISMO_NA26
B6	IO	DIFFIO_TX110p		AD6	PISMO_NA3
B6	IO	DIFFIO_RX110n		AH4	PISMO_NA4
B6	IO	DIFFIO_RX110p		AH3	PISMO_NA5
B6	IO	DIFFIO_TX109n		AD9	PISMO_NA6
B6	IO	DIFFIO_TX109p		AD8	PISMO_NA7
B6	IO	DIFFIO_RX109n		AG4	PISMO_NA8
B6	IO	DIFFIO_RX109p		AG3	PISMO_NA9
B6	IO	DIFFIO_TX102n		AA11	SODIMM_S0
B6	IO	DIFFIO_TX102p		AA10	SODIMM_S1
B6	IO	DIFFIO_RX100n		AE2	SODIMM_S10
B6	IO	DIFFIO_RX100p		AE1	SODIMM_S11
B6	IO	DIFFIO_TX99n		W11	SODIMM_S12
B6	IO	DIFFIO_TX99p		W10	SODIMM_S13
B6	IO	DIFFIO_RX99n		AD2	SODIMM_S14
B6	IO	DIFFIO_RX99p		AD1	SODIMM_S15
B6	IO	DIFFIO_TX98n		Y9	SODIMM_S16
B6	IO	DIFFIO_TX98p		Y8	SODIMM_S17
B6	IO	DIFFIO_RX98n		AC4	SODIMM_S18
B6	IO	DIFFIO_RX102n		AF2	SODIMM_S2
B6	IO	DIFFIO_RX102p		AF1	SODIMM_S3
B6	IO	DIFFIO_TX101n		Y11	SODIMM_S4
B6	IO	DIFFIO_TX101p		Y10	SODIMM_S5
B6	IO	DIFFIO_RX101n		AE4	SODIMM_S6
B6	IO	DIFFIO_RX101p		AE3	SODIMM_S7
B6	IO	DIFFIO_TX100n		AA7	SODIMM_S8
B6	IO	DIFFIO_TX100p		AA6	SODIMM_S9
B6	FPLL9CLKp	INPUT		AJ3	UGRID20
B6	FPLL9CLKn	INPUT		AJ4	UGRID21
B6	IO	DIFFIO_RX98p		AC3	UGRID22
B6	IO	DIFFIO_TX97n		Y7	UGRID23
B6	IO	DIFFIO_TX97p		Y6	UGRID24
B6	IO	DIFFIO_RX97n		AC2	UGRID25
B6	IO	DIFFIO_RX97p		AC1	UGRID26
B6	IO	DIFFIO_TX96n		W5	UGRID27

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B6	IO	DIFFIO_TX96p		W4	UGRID28
B6	IO	DIFFIO_RX96n		AB4	UGRID29
B6	IO	DIFFIO_RX96p		AB3	UGRID30
B6	IO	DIFFIO_TX95n		W7	UGRID31
B6	IO	DIFFIO_TX95p		W6	UGRID32
B6	IO	DIFFIO_RX95n		AB2	UGRID33
B6	IO	DIFFIO_RX95p		AB1	UGRID34
B6	IO	DIFFIO_TX94n		W9	UGRID35
B6	IO	DIFFIO_TX94p		W8	UGRID36
B6	IO	DIFFIO_RX94n		Y5	UGRID37
B6	IO	DIFFIO_RX94p		Y4	UGRID38
B6	IO	DIFFIO_TX93n		V5	UGRID39
B6	IO	DIFFIO_TX93p		V4	UGRID40
B6	IO	DIFFIO_RX93n		AA4	UGRID41
B6	IO	DIFFIO_RX93p		AA3	UGRID42
B6	IO	DIFFIO_TX92n		V7	UGRID43
B6	IO	DIFFIO_TX92p		V6	UGRID44
B6	IO	DIFFIO_RX92n		AA2	UGRID45
B6	IO	DIFFIO_RX92p		AA1	UGRID46
B6	IO	DIFFIO_TX91n		V10	UGRID47
B6	IO	DIFFIO_TX91p		V9	UGRID48
B6	IO	DIFFIO_RX91n		Y3	UGRID49
B6	IO	DIFFIO_RX91p		Y2	UGRID50
B6	IO	DIFFIO_TX90n		U11	UGRID51
B6	IO	DIFFIO_TX90p		U10	UGRID52
B6	IO	DIFFIO_RX90n		W2	UGRID53
B6	IO	DIFFIO_RX90p		W1	UGRID54
B6	IO	DIFFIO_TX89n		U6	UGRID55
B6	IO	DIFFIO_TX89p		U5	UGRID56
B6	IO	DIFFIO_RX89n		V3	UGRID57
B6	IO	DIFFIO_RX89p		V2	UGRID58
B6	CLK9n	INPUT		U4	UGRID59
B6	CLK9p	INPUT		U3	UGRID60
B6	IO	CLK8n/DIFFIO_RX_C2n		U2	UGRID61
B6	IO	CLK8p/DIFFIO_RX_C2p		U1	UGRID62
B6	VREFB6N1	VREFB6N1		AD5	VREFB6

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B6	VREFB6N0	VREFB6N0		AG5	VREFB6
B6	VREFB6N2	VREFB6N2		W3	VREFB6
B7	nCEO		nCEO	AL3	NCEO
B7	nIO_PULLUP		nIO_PULLUP	AK3	NIO_PULLUP
B7	PLL_ENA		PLL_ENA	AF8	PLL_ENA
B7	PORSEL		PORSEL	AL2	PORSEL
B7	IO			AB16	SODIMM_C0
B7	IO			AC16	SODIMM_C1
B7	IO			AE14	SODIMM_C10
B7	IO	DQ8B		AG15	SODIMM_C11
B7	IO	DQSn8B		AH14	SODIMM_C12
B7	IO	DQ8B		AF13	SODIMM_C13
B7	IO	DQ8B		AG13	SODIMM_C14
B7	IO	DQ8B		AH13	SODIMM_C15
B7	IO	DQS8B		AG14	SODIMM_C16
B7	IO			AB15	SODIMM_C17
B7	IO			AF14	SODIMM_C18
B7	IO	DQ7B		AM12	SODIMM_C19
B7	IO			AC15	SODIMM_C2
B7	IO	DQS7B		AL11	SODIMM_C20
B7	IO			AC14	SODIMM_C21
B7	IO	DQSn6B		AK11	SODIMM_C22
B7	IO	DQS6B		AK10	SODIMM_C23
B7	IO			AD13	SODIMM_C24
B7	IO			AE13	SODIMM_C25
B7	IO	DQ5B		AG12	SODIMM_C26
B7	IO	DQS5B		AF11	SODIMM_C27
B7	IO			AB14	SODIMM_C28
B7	IO	DQSn4B		AL9	SODIMM_C29
B7	IO	DQ9B		AM14	SODIMM_C3
B7	IO	DQS4B		AK9	SODIMM_C30
B7	IO			AC13	SODIMM_C31
B7	IO			AE12	SODIMM_C32
B7	IO	DQ3B		AM8	SODIMM_C33
B7	IO	DQS3B		AL7	SODIMM_C34
B7	IO			AB13	SODIMM_C35

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B7	IO			AD12	SODIMM_C36
B7	IO	DQSn2B		AL6	SODIMM_C37
B7	IO			AE11	SODIMM_C38
B7	IO	DQ1B		AH9	SODIMM_C39
B7	IO	DQSn9B		AL13	SODIMM_C4
B7	IO	DQS1B		AG8	SODIMM_C40
B7	IO			AD11	SODIMM_C41
B7	IO			AC12	SODIMM_C42
B7	IO	DQSn0B		AK5	SODIMM_C43
B7	IO			AC11	SODIMM_C44
B7	IO			AB12	SODIMM_C45
B7	IO			AE10	SODIMM_C46
B7	IO	RDN7		AB11	SODIMM_C47
B7	IO	RUP7		AD10	SODIMM_C48
B7	IO			AE9	SODIMM_C49
B7	IO	DQ9B		AJ13	SODIMM_C5
B7	IO	CLK7p		AH16	SODIMM_C50
B7	IO	CLK7n		AG16	SODIMM_C51
B7	IO	CLK6p		AM16	SODIMM_C52
B7	IO	CLK6n		AL16	SODIMM_C53
B7	IO	DQ9B		AJ14	SODIMM_C6
B7	IO	DQ9B		AL14	SODIMM_C7
B7	IO	DQS9B		AK13	SODIMM_C8
B7	IO			AD14	SODIMM_C9
B7	IO	DQSn7B		AL12	SODIMM_D0
B7	IO	DQ7B		AM11	SODIMM_D1
B7	IO	DQ5B		AG10	SODIMM_D10
B7	IO	DQ5B		AF12	SODIMM_D11
B7	IO	DQ4B		AM9	SODIMM_D12
B7	IO	DQ4B		AJ8	SODIMM_D13
B7	IO	DQ4B		AK8	SODIMM_D14
B7	IO	DQ4B		AJ10	SODIMM_D15
B7	IO	DQSn3B		AL8	SODIMM_D16
B7	IO	DQ3B		AJ7	SODIMM_D17
B7	IO	DQ3B		AK7	SODIMM_D18
B7	IO	DQ3B		AM7	SODIMM_D19

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B7	IO	DQ7B		AJ12	SODIMM_D2
B7	IO	DQ2B		AM6	SODIMM_D20
B7	IO	DQ2B		AJ6	SODIMM_D21
B7	IO	DQ2B		AK6	SODIMM_D22
B7	IO	DQ2B		AM5	SODIMM_D23
B7	IO	DQSn1B		AH8	SODIMM_D24
B7	IO	DQ1B		AH7	SODIMM_D25
B7	IO	DQ1B		AH6	SODIMM_D26
B7	IO	DQ1B		AG9	SODIMM_D27
B7	IO	DQ0B		AM4	SODIMM_D28
B7	IO	DQ0B		AH5	SODIMM_D29
B7	IO	DQ7B		AK12	SODIMM_D3
B7	IO	DQ0B		AJ5	SODIMM_D30
B7	IO	DQ0B		AL4	SODIMM_D31
B7	IO	DQ6B		AM10	SODIMM_D4
B7	IO	DQ6B		AL10	SODIMM_D5
B7	IO	DQ6B		AH11	SODIMM_D6
B7	IO	DQ6B		AJ11	SODIMM_D7
B7	IO	DQSn5B		AG11	SODIMM_D8
B7	IO	DQ5B		AF10	SODIMM_D9
B7	IO	DQS0B		AK4	SODIMM_DQS0
B7	IO	DQS2B		AL5	SODIMM_DQS1
B7	VREFB7N1	VREFB7N1		AJ9	VREFB7
B7	VREFB7N0	VREFB7N0		AK14	VREFB7
B7	VREFB7N2	VREFB7N2		AK2	VREFB7
B8	IO			AG25	MPIOA0
B8	IO			AB21	MPIOA1
B8	IO	DQS17B		AK28	MPIOA10
B8	IO			AC21	MPIOA11
B8	IO			AG21	MPIOA12
B8	IO	DQ16B		AK27	MPIOA13
B8	IO	DQSn16B		AL28	MPIOA14
B8	IO	DQ16B		AJ27	MPIOA15
B8	IO	DQ16B		AM28	MPIOA16
B8	IO	DQ16B		AM27	MPIOA17
B8	IO	DQS16B		AL27	MPIOA18

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B8	IO			AF21	MPIOA19
B8	IO			AE22	MPIOA2
B8	IO	DQ15B		AK26	MPIOA20
B8	IO	DQSn15B		AL26	MPIOA21
B8	IO	DQ15B		AJ26	MPIOA22
B8	IO	DQ15B		AM25	MPIOA23
B8	IO	DQ15B		AM26	MPIOA24
B8	IO	DQS15B		AL25	MPIOA25
B8	IO			AD21	MPIOA26
B8	IO	DQ14B		AG24	MPIOA27
B8	IO	DQSn14B		AH25	MPIOA28
B8	IO	DQ14B		AH26	MPIOA29
B8	IO			AF22	MPIOA3
B8	IO	DQ14B		AH24	MPIOA30
B8	IO	DQ14B		AK25	MPIOA31
B8	IO			AD22	MPIOA4
B8	IO	DQ17B		AH28	MPIOA5
B8	IO	DQSn17B		AK29	MPIOA6
B8	IO	DQ17B		AJ28	MPIOA7
B8	IO	DQ17B		AM29	MPIOA8
B8	IO	DQ17B		AL29	MPIOA9
B8	IO	DQS14B		AJ25	MPIOB0
B8	IO			AB20	MPIOB1
B8	IO	DQS13B		AL23	MPIOB10
B8	IO			AD20	MPIOB11
B8	IO	DQ12B		AG23	MPIOB12
B8	IO	DQSn12B		AH22	MPIOB13
B8	IO	DQ12B		AG22	MPIOB14
B8	IO	DQ12B		AK22	MPIOB15
B8	IO	DQ12B		AJ23	MPIOB16
B8	IO	DQS12B		AJ22	MPIOB17
B8	IO			AC20	MPIOB18
B8	IO			AB19	MPIOB19
B8	IO			AE21	MPIOB2
B8	IO			AE20	MPIOB20
B8	IO			AC19	MPIOB21

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B8	IO	DQ11B		AM22	MPIOB22
B8	IO	DQSn11B		AL22	MPIOB23
B8	IO	CLK4p		AM17	MPIOB24
B8	IO	DQ11B		AJ21	MPIOB25
B8	IO	DQ11B		AK21	MPIOB26
B8	IO	DQ11B		AM21	MPIOB27
B8	IO	DQS11B		AL21	MPIOB28
B8	IO			AD19	MPIOB29
B8	IO			AG20	MPIOB3
B8	IO			AE19	MPIOB30
B8	IO			AF19	MPIOB31
B8	IO			AB18	MPIOB32
B8	IO	DQ10B		AH20	MPIOB33
B8	IO	DQSn10B		AJ20	MPIOB34
B8	IO	DQ10B		AJ19	MPIOB35
B8	IO	DQ10B		AH19	MPIOB36
B8	IO	DQ10B		AL20	MPIOB37
B8	IO	DQS10B		AK20	MPIOB38
B8	IO			AC18	MPIOB39
B8	IO			AF20	MPIOB4
B8	IO			AD18	MPIOB40
B8	IO			AB17	MPIOB41
B8	IO			AC17	MPIOB42
B8	IO	CLK5n		AJ17	MPIOB43
B8	IO	CLK4n		AL17	MPIOB44
B8	IO	DQ13B		AM24	MPIOB5
B8	IO	DQSn13B		AL24	MPIOB6
B8	IO	DQ13B		AK24	MPIOB7
B8	IO	DQ13B		AK23	MPIOB8
B8	IO	DQ13B		AM23	MPIOB9
B8	nCONFIG		nCONFIG	AL30	NCONFIG
B8	IO	CLK5p		AK17	NRST
B8	TCK		TCK	AF24	S2_TCK
B8	TDI		TDI	AL31	S2_TDI
B8	TMS		TMS	AE24	S2_TMS
B8	TRST		TRST	AK30	TRST

Table 7-5. FPGA Pins Sorted by Bank/Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B8	IO		CS	AC22	UGRID0
B8	IO		CLKUSR	AD23	UGRID1
B8	IO		nWS	AE23	UGRID2
B8	IO		nRS	AF23	UGRID3
B8	IO		RUnLU	AG17	UGRID4
B8	IO		DEV_OE	AH17	UGRID5
B8	IO		DEV_CLRn	AG19	UGRID6
B8	IO		nCS	AG18	UGRID7
B8	VCCSEL		VCCSEL	AC23	VCCSEL
B8	VREFB8N1	VREFB8N1		AJ24	VREFB8
B8	VREFB8N2	VREFB8N2		AK19	VREFB8
B8	VREFB8N0	VREFB8N0		AK31	VREFB8
B9	IO	PLL5_FBn/OUT2n		E15	UGRID63
B9	IO	PLL5_FBp/OUT2p		D15	UGRID64
B9	IO	PLL5_OUT0n		C15	UGRID65
B9	IO	PLL5_OUT0p		B15	UGRID66
B9	IO	PLL5_OUT1n		D16	UGRID67
B9	IO	PLL5_OUT1p		C16	UGRID68
B9	VCC_PLL5_OUT			J16	VCC_PLL5

Table 7-6. FPGA Pins Sorted by Signal Name

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	VCCINT			AA12	1V2
	VCCINT			AC10	1V2
	VCCINT			K10	1V2
	VCCINT			K23	1V2
	VCCINT			M21	1V2
	VCCINT			N13	1V2
	VCCINT			N15	1V2
	VCCINT			N17	1V2
	VCCINT			N19	1V2
	VCCINT			P14	1V2
	VCCINT			P16	1V2
	VCCINT			P18	1V2

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	VCCINT			P20	1V2
	VCCINT			R13	1V2
	VCCINT			R15	1V2
	VCCINT			R17	1V2
	VCCINT			R19	1V2
	VCCINT			T14	1V2
	VCCINT			T16	1V2
	VCCINT			T18	1V2
	VCCINT			T20	1V2
	VCCINT			U13	1V2
	VCCINT			U15	1V2
	VCCINT			U17	1V2
	VCCINT			U19	1V2
	VCCINT			V14	1V2
	VCCINT			V16	1V2
	VCCINT			V18	1V2
	VCCINT			V20	1V2
	VCCINT			W13	1V2
	VCCINT			W15	1V2
	VCCINT			W17	1V2
	VCCINT			W19	1V2
	VCCINT			W21	1V2
	VCCINT			Y14	1V2
	VCCINT			Y16	1V2
	VCCINT			Y18	1V2
	VCCINT			Y20	1V2
	VCCPD7			AA13	3V3
	VCCPD7			AA15	3V3
	VCCPD8			AA18	3V3
	VCCPD8			AA20	3V3
	VCCPD4			M13	3V3
	VCCPD4			M15	3V3
	VCCPD3			M18	3V3
	VCCPD3			M20	3V3
	VCCPD5			N12	3V3
	VCCPD2			N21	3V3

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	VCCPD5			R12	3V3
	VCCPD2			R21	3V3
	VCCPD6			V12	3V3
	VCCPD1			V21	3V3
	VCCPD6			Y12	3V3
	VCCPD1			Y21	3V3
B3	IO		ASDO	F17	ASDO
B3	CONF_DONE		CONF_DONE	J25	CONFIG_DONE
B3	IO		DATA0	H19	DATA0
B3	DCLK		DCLK	B31	DCLK
B5	CLK11n	INPUT		T4	EXT_CLK
B1	IO	CLK2p/DIFFIO_RX_C1p		U32	FPGA0
B1	IO	CLK2n/DIFFIO_RX_C1n		U31	FPGA1
B1	IO	DIFFIO_TX27p		U28	FPGA10
B2	IO	DIFFIO_RX50p		G28	FPGA100
B2	IO	DIFFIO_RX50n		G27	FPGA101
B2	IO	DIFFIO_TX50p		H28	FPGA102
B2	IO	DIFFIO_TX50n		H27	FPGA103
B2	IO	DIFFIO_RX49p		E30	FPGA104
B2	IO	DIFFIO_RX49n		E29	FPGA105
B2	IO	DIFFIO_TX49p		K27	FPGA106
B2	IO	DIFFIO_TX49n		K26	FPGA107
B2	IO	DIFFIO_RX48p		D32	FPGA108
B2	IO	DIFFIO_RX48n		D31	FPGA109
B1	IO	DIFFIO_TX27n		U27	FPGA11
B2	IO	DIFFIO_TX48p		J27	FPGA110
B2	IO	DIFFIO_TX48n		J26	FPGA111
B2	IO	DIFFIO_RX47p		F30	FPGA112
B2	IO	DIFFIO_RX47n		F29	FPGA113
B2	IO	DIFFIO_TX47p		L28	FPGA114
B2	IO	DIFFIO_TX47n		L27	FPGA115
B2	IO	DIFFIO_RX46p		G30	FPGA116
B2	IO	DIFFIO_RX46n		G29	FPGA117
B2	IO	DIFFIO_TX46p		L26	FPGA118
B2	IO	DIFFIO_TX46n		L25	FPGA119
B1	IO	DIFFIO_RX26p		AA32	FPGA12

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B2	IO	DIFFIO_RX45p		H30	FPGA120
B2	IO	DIFFIO_RX45n		H29	FPGA121
B2	IO	DIFFIO_TX45p		L24	FPGA122
B2	IO	DIFFIO_TX45n		L23	FPGA123
B2	IO	DIFFIO_RX44p		J30	FPGA124
B2	IO	DIFFIO_RX44n		J29	FPGA125
B2	IO	DIFFIO_TX44p		M25	FPGA126
B2	IO	DIFFIO_TX44n		M24	FPGA127
B2	IO	DIFFIO_RX43p		E32	FPGA128
B2	IO	DIFFIO_RX43n		E31	FPGA129
B1	IO	DIFFIO_RX26n		AA31	FPGA13
B2	IO	DIFFIO_TX43p		M23	FPGA130
B2	IO	DIFFIO_TX43n		M22	FPGA131
B2	IO	DIFFIO_RX42p		F32	FPGA132
B2	IO	DIFFIO_RX42n		F31	FPGA133
B2	IO	DIFFIO_TX42p		M27	FPGA134
B2	IO	DIFFIO_TX42n		M26	FPGA135
B2	IO	DIFFIO_RX41p		G32	FPGA136
B2	IO	DIFFIO_RX41n		G31	FPGA137
B2	IO	DIFFIO_TX41p		N25	FPGA138
B2	IO	DIFFIO_TX41n		N24	FPGA139
B1	IO	DIFFIO_TX26p		V29	FPGA14
B2	IO	DIFFIO_RX40p		H32	FPGA140
B2	IO	DIFFIO_RX40n		H31	FPGA141
B2	IO	DIFFIO_TX40p		N23	FPGA142
B2	IO	DIFFIO_TX40n		N22	FPGA143
B2	IO	DIFFIO_RX39p		J32	FPGA144
B2	IO	DIFFIO_RX39n		J31	FPGA145
B2	IO	DIFFIO_TX39p		P23	FPGA146
B2	IO	DIFFIO_TX39n		P22	FPGA147
B2	IO	DIFFIO_RX38p		K30	FPGA148
B2	IO	DIFFIO_RX38n		K29	FPGA149
B1	IO	DIFFIO_TX26n		V28	FPGA15
B2	IO	DIFFIO_TX38p		N27	FPGA150
B2	IO	DIFFIO_TX38n		N26	FPGA151
B2	IO	DIFFIO_RX37p		K32	FPGA152

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B2	IO	DIFFIO_RX37n		K31	FPGA153
B2	IO	DIFFIO_TX37p		P29	FPGA154
B2	IO	DIFFIO_TX37n		P28	FPGA155
B2	IO	DIFFIO_RX36p		L30	FPGA156
B2	IO	DIFFIO_RX36n		L29	FPGA157
B2	IO	DIFFIO_TX36p		P27	FPGA158
B2	IO	DIFFIO_TX36n		P26	FPGA159
B1	IO	DIFFIO_RX25p		Y31	FPGA16
B2	IO	DIFFIO_RX35p		N29	FPGA160
B2	IO	DIFFIO_RX35n		N28	FPGA161
B2	IO	DIFFIO_TX35p		P25	FPGA162
B2	IO	DIFFIO_TX35n		P24	FPGA163
B2	IO	DIFFIO_RX34p		M30	FPGA164
B2	IO	DIFFIO_RX34n		M29	FPGA165
B2	IO	DIFFIO_TX34p		R27	FPGA166
B2	IO	DIFFIO_TX34n		R26	FPGA167
B2	IO	DIFFIO_RX33p		L32	FPGA168
B2	IO	DIFFIO_RX33n		L31	FPGA169
B1	IO	DIFFIO_RX25n		Y30	FPGA17
B2	IO	DIFFIO_TX33p		R23	FPGA170
B2	IO	DIFFIO_TX33n		R22	FPGA171
B2	IO	DIFFIO_RX32p		N31	FPGA172
B2	IO	DIFFIO_RX32n		N30	FPGA173
B2	IO	DIFFIO_TX32p		R25	FPGA174
B2	CLK1p	INPUT		T30	FPGA175
B2	IO	DIFFIO_RX31p		M32	FPGA176
B2	IO	DIFFIO_RX31n		M31	FPGA177
B2	IO	DIFFIO_TX31p		R29	FPGA178
B2	IO	DIFFIO_TX31n		R28	FPGA179
B1	IO	DIFFIO_TX25p		V24	FPGA18
B2	IO	DIFFIO_RX30p		P32	FPGA180
B2	IO	DIFFIO_RX30n		P31	FPGA181
B2	IO	DIFFIO_TX30p		T28	FPGA182
B2	IO	DIFFIO_TX30n		T27	FPGA183
B2	IO	DIFFIO_RX29p		R31	FPGA184
B2	IO	DIFFIO_RX29n		R30	FPGA185

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B2	IO	DIFFIO_TX29p		T23	FPGA186
B2	IO	DIFFIO_TX29n		T22	FPGA187
B2	IO	CLK0n/DIFFIO_RX_C0n		T31	FPGA188
B2	IO	CLK0p/DIFFIO_RX_C0p		T32	FPGA189
B1	IO	DIFFIO_TX25n		V23	FPGA19
B2	CLK1n	INPUT		T29	FPGA190
B2	IO	DIFFIO_TX32n		R24	FPGA191
B3	IO	CLK14p		A17	FPGA192
B3	IO	CLK14n		B17	FPGA193
B3	IO	CLK15p		C17	FPGA194
B3	IO	CLK15n		D17	FPGA195
B3	IO			K18	FPGA196
B3	IO		PGM2	F18	FPGA197
B3	IO		PGM1	F19	FPGA198
B3	IO		PGM0	E17	FPGA199
B1	CLK3p	INPUT		U30	FPGA2
B1	IO	DIFFIO_RX24p		AB32	FPGA20
B3	IO		CRC_ERROR	G20	FPGA200
B3	IO		DATA1	F20	FPGA201
B3	IO	DQS10T		D19	FPGA202
B3	IO	DQ10T		B20	FPGA203
B3	IO	DQ10T		E19	FPGA204
B3	IO	DQ10T		C20	FPGA205
B3	IO	DQSn10T		D20	FPGA206
B3	IO	DQ10T		E20	FPGA207
B3	IO			L19	FPGA208
B3	IO			L18	FPGA209
B1	IO	DIFFIO_RX24n		AB31	FPGA21
B3	IO			J19	FPGA210
B3	IO			K19	FPGA211
B3	IO	DQS11T		B21	FPGA212
B3	IO	DQ11T		A21	FPGA213
B3	IO	DQ11T		C21	FPGA214
B3	IO	DQ11T		A22	FPGA215
B3	IO	DQSn11T		B22	FPGA216
B3	IO	DQ11T		C22	FPGA217

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B3	IO			L20	FPGA218
B3	IO			H20	FPGA219
B1	IO	DIFFIO_TX24p		W29	FPGA22
B3	IO			K20	FPGA220
B3	IO	DQS12T		D22	FPGA221
B3	IO	DQ12T		D23	FPGA222
B3	IO	DQ12T		D21	FPGA223
B3	IO	DQ12T		F22	FPGA224
B3	IO	DQSn12T		E22	FPGA225
B3	IO	DQ12T		F23	FPGA226
B3	IO			L21	FPGA227
B3	IO			J20	FPGA228
B3	IO	DQS13T		B23	FPGA229
B1	IO	DIFFIO_TX24n		W28	FPGA23
B3	IO	DQ13T		A23	FPGA230
B3	IO	DQ13T		C23	FPGA231
B3	IO	DQ13T		C24	FPGA232
B3	IO	DQSn13T		B24	FPGA233
B3	IO	DQ13T		A24	FPGA234
B3	IO			K21	FPGA235
B3	IO			H21	FPGA236
B3	IO			J21	FPGA237
B3	IO	DQS14T		B25	FPGA238
B3	IO	DQ14T		A25	FPGA239
B1	IO	DIFFIO_RX23p		AA30	FPGA24
B3	IO	DQ14T		A26	FPGA240
B3	IO	DQ14T		D26	FPGA241
B3	IO	DQSn14T		B26	FPGA242
B3	IO	DQ14T		C26	FPGA243
B3	IO			G21	FPGA244
B3	IO	DQS15T		D25	FPGA245
B3	IO	DQ15T		E24	FPGA246
B3	IO	DQ15T		C25	FPGA247
B3	IO	DQ15T		E27	FPGA248
B3	IO	DQSn15T		E25	FPGA249
B1	IO	DIFFIO_RX23n		AA29	FPGA25

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B3	IO	DQ15T		E26	FPGA250
B3	IO			F21	FPGA251
B3	IO	DQS16T		B27	FPGA252
B3	IO	DQ16T		A27	FPGA253
B3	IO	DQ16T		A28	FPGA254
B3	IO	DQ16T		D27	FPGA255
B3	IO	DQSn16T		B28	FPGA256
B3	IO	DQ16T		C27	FPGA257
B3	IO			H22	FPGA258
B3	IO			J22	FPGA259
B1	IO	DIFFIO_TX23p		W27	FPGA26
B3	IO	DQS17T		C28	FPGA260
B3	IO	DQ17T		B29	FPGA261
B3	IO	DQ17T		A29	FPGA262
B3	IO	DQ17T		D28	FPGA263
B3	IO	DQSn17T		C29	FPGA264
B3	IO	DQ17T		E28	FPGA265
B3	IO			K22	FPGA266
B3	IO			F25	FPGA267
B3	IO			G22	FPGA268
B3	IO		DATA2	G23	FPGA269
B1	IO	DIFFIO_TX23n		W26	FPGA27
B3	IO		DATA3	H23	FPGA270
B3	IO		DATA4	J23	FPGA271
B3	IO		DATA5	L22	FPGA272
B3	IO		DATA6	F24	FPGA273
B3	IO		DATA7	G24	FPGA274
B3	IO		RDYnBSY	H24	FPGA275
B1	IO	DIFFIO_RX22p		Y29	FPGA28
B1	IO	DIFFIO_RX22n		Y28	FPGA29
B1	CLK3n	INPUT		U29	FPGA3
B1	IO	DIFFIO_TX22p		W25	FPGA30
B1	IO	DIFFIO_TX22n		W24	FPGA31
B1	IO	DIFFIO_RX21p		AB30	FPGA32
B1	IO	DIFFIO_RX21n		AB29	FPGA33
B1	IO	DIFFIO_TX21p		Y27	FPGA34

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B1	IO	DIFFIO_TX21n		Y26	FPGA35
B1	IO	DIFFIO_RX20p		AC32	FPGA36
B1	IO	DIFFIO_RX20n		AC31	FPGA37
B1	IO	DIFFIO_TX20p		AA27	FPGA38
B1	IO	DIFFIO_TX20n		AA26	FPGA39
B1	IO	DIFFIO_RX28p		V31	FPGA4
B1	IO	DIFFIO_RX19p		AB28	FPGA40
B1	IO	DIFFIO_RX19n		AB27	FPGA41
B1	IO	DIFFIO_TX19p		Y25	FPGA42
B1	IO	DIFFIO_TX19n		Y24	FPGA43
B1	IO	DIFFIO_RX18p		AD32	FPGA44
B1	IO	DIFFIO_RX18n		AD31	FPGA45
B1	IO	DIFFIO_TX18p		W23	FPGA46
B1	IO	DIFFIO_TX18n		W22	FPGA47
B1	IO	DIFFIO_RX17p		AE32	FPGA48
B1	IO	DIFFIO_RX17n		AE31	FPGA49
B1	IO	DIFFIO_RX28n		V30	FPGA5
B1	IO	DIFFIO_TX17p		AD27	FPGA50
B1	IO	DIFFIO_TX17n		AD26	FPGA51
B1	IO	DIFFIO_RX16p		AF32	FPGA52
B1	IO	DIFFIO_RX16n		AF31	FPGA53
B1	IO	DIFFIO_TX16p		AC27	FPGA54
B1	IO	DIFFIO_TX16n		AC26	FPGA55
B1	IO	DIFFIO_RX15p		AG32	FPGA56
B1	IO	DIFFIO_RX15n		AG31	FPGA57
B1	IO	DIFFIO_TX15p		Y23	FPGA58
B1	IO	DIFFIO_TX15n		Y22	FPGA59
B1	IO	DIFFIO_TX28p		U23	FPGA6
B1	IO	DIFFIO_RX14p		AC30	FPGA60
B1	IO	DIFFIO_RX14n		AC29	FPGA61
B1	IO	DIFFIO_TX14p		AA25	FPGA62
B1	IO	DIFFIO_TX14n		AA24	FPGA63
B1	IO	DIFFIO_RX13p		AD30	FPGA64
B1	IO	DIFFIO_RX13n		AD29	FPGA65
B1	IO	DIFFIO_TX13p		AB26	FPGA66
B1	IO	DIFFIO_TX13n		AB25	FPGA67

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B1	IO	DIFFIO_RX12p		AH32	FPGA68
B1	IO	DIFFIO_RX12n		AH31	FPGA69
B1	IO	DIFFIO_TX28n		U22	FPGA7
B1	IO	DIFFIO_TX12p		AA23	FPGA70
B1	IO	DIFFIO_TX12n		AA22	FPGA71
B1	IO	DIFFIO_RX11p		AE30	FPGA72
B1	IO	DIFFIO_RX11n		AE29	FPGA73
B1	IO	DIFFIO_TX11p		AB24	FPGA74
B1	IO	DIFFIO_TX11n		AB23	FPGA75
B1	IO	DIFFIO_RX10p		AJ32	FPGA76
B1	IO	DIFFIO_RX10n		AJ31	FPGA77
B1	IO	DIFFIO_TX10p		AC25	FPGA78
B1	IO	DIFFIO_TX10n		AC24	FPGA79
B1	IO	DIFFIO_RX27p		W32	FPGA8
B1	IO	DIFFIO_RX9p		AF30	FPGA80
B1	IO	DIFFIO_RX9n		AF29	FPGA81
B1	IO	DIFFIO_TX9p		AD25	FPGA82
B1	IO	DIFFIO_TX9n		AD24	FPGA83
B1	IO	DIFFIO_RX8p		AG30	FPGA84
B1	IO	DIFFIO_RX8n		AG29	FPGA85
B1	IO	DIFFIO_TX8p		AE26	FPGA86
B1	IO	DIFFIO_TX8n		AE25	FPGA87
B1	IO	DIFFIO_RX7p		AH30	FPGA88
B1	IO	DIFFIO_RX7n		AH29	FPGA89
B1	IO	DIFFIO_RX27n		W31	FPGA9
B1	IO	DIFFIO_TX7p		AE28	FPGA90
B1	IO	DIFFIO_TX7n		AE27	FPGA91
B1	IO	DIFFIO_RX6p		AF28	FPGA92
B1	IO	DIFFIO_RX6n		AF27	FPGA93
B1	FPLL8CLKn	INPUT		AJ29	FPGA94
B1	FPLL8CLKp	INPUT		AJ30	FPGA95
B2	FPLL7CLKp	INPUT		D30	FPGA96
B2	FPLL7CLKn	INPUT		D29	FPGA97
B2	IO	DIFFIO_TX51p		K25	FPGA98
B2	IO	DIFFIO_TX51n		K24	FPGA99
	GND			A13	GND

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	GND			A2	GND
	GND			A20	GND
	GND			A31	GND
	GND			AA14	GND
	GND			AA19	GND
	GND			AA21	GND
	GND			AB22	GND
	GND			AC28	GND
	GND			AC5	GND
	GNDA_PLL6			AD16	GND
	GNDA_PLL12			AD17	GND
	GNDA_PLL6			AE16	GND
	GNDA_PLL12			AE17	GND
	GND			AF17	GND
	GNDA_PLL9			AF7	GND
	GND			AF9	GND
	GNDA_PLL8			AG26	GND
	GNDA_PLL8			AG27	GND
	GND			AG6	GND
	GNDA_PLL9			AG7	GND
	GND			AH10	GND
	GND			AH23	GND
	GND			AH27	GND
	GND			AL1	GND
	GND			AL32	GND
	GND			AM13	GND
	GND			AM2	GND
	GND			AM20	GND
	GND			AM31	GND
	GND			B1	GND
	TEMPDIODEn			B3	GND
	GND			B32	GND
	GND			E10	GND
	GND			E23	GND
	GNDA_PLL7			F26	GND
	GND			F27	GND

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	GND			F7	GND
	GNDA_PLL5			G16	GND
	GND			G17	GND
	GNDA_PLL11			G18	GND
	GNDA_PLL7			G26	GND
	GNDA_PLL10			G7	GND
	GNDA_PLL10			G8	GND
	TEMPDIODEp			G9	GND
	GNDA_PLL5			H16	GND
	GNDA_PLL11			H18	GND
	GND			J24	GND
	GND			K28	GND
	GND			K5	GND
	GND			L11	GND
	GND			M12	GND
	GND			M14	GND
	GND			M19	GND
	GND			N1	GND
	GND			N14	GND
	GND			N16	GND
	GND			N18	GND
	GND			N20	GND
	GND			N32	GND
	GND			P12	GND
	GND			P13	GND
	GND			P15	GND
	GND			P17	GND
	GND			P19	GND
	GND			P21	GND
	GND			R14	GND
	GND			R16	GND
	GND			R18	GND
	GND			R20	GND
	GNDA_PLL4			R8	GND
	GND			T13	GND
	GND			T15	GND

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	GND			T17	GND
	GND			T19	GND
	GNDA_PLL1			T25	GND
	GNDA_PLL1			T26	GND
	GND			T7	GND
	GNDA_PLL4			T8	GND
	GND			U14	GND
	GND			U16	GND
	GND			U18	GND
	GND			U20	GND
	GNDA_PLL2			U25	GND
	GNDA_PLL2			U26	GND
	GNDA_PLL3			U8	GND
	GND			V11	GND
	GND			V13	GND
	GND			V15	GND
	GND			V17	GND
	GND			V19	GND
	GND			V22	GND
	GND			V27	GND
	GNDA_PLL3			V8	GND
	GND			W12	GND
	GND			W14	GND
	GND			W16	GND
	GND			W18	GND
	GND			W20	GND
	GND			Y1	GND
	GND			Y13	GND
	GND			Y15	GND
	GND			Y17	GND
	GND			Y19	GND
	GND			Y32	GND
B8	IO			AG25	MPIOA0
B8	IO			AB21	MPIOA1
B8	IO	DQS17B		AK28	MPIOA10
B8	IO			AC21	MPIOA11

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B8	IO			AG21	MPIOA12
B8	IO	DQ16B		AK27	MPIOA13
B8	IO	DQSn16B		AL28	MPIOA14
B8	IO	DQ16B		AJ27	MPIOA15
B8	IO	DQ16B		AM28	MPIOA16
B8	IO	DQ16B		AM27	MPIOA17
B8	IO	DQS16B		AL27	MPIOA18
B8	IO			AF21	MPIOA19
B8	IO			AE22	MPIOA2
B8	IO	DQ15B		AK26	MPIOA20
B8	IO	DQSn15B		AL26	MPIOA21
B8	IO	DQ15B		AJ26	MPIOA22
B8	IO	DQ15B		AM25	MPIOA23
B8	IO	DQ15B		AM26	MPIOA24
B8	IO	DQS15B		AL25	MPIOA25
B8	IO			AD21	MPIOA26
B8	IO	DQ14B		AG24	MPIOA27
B8	IO	DQSn14B		AH25	MPIOA28
B8	IO	DQ14B		AH26	MPIOA29
B8	IO			AF22	MPIOA3
B8	IO	DQ14B		AH24	MPIOA30
B8	IO	DQ14B		AK25	MPIOA31
B8	IO			AD22	MPIOA4
B8	IO	DQ17B		AH28	MPIOA5
B8	IO	DQSn17B		AK29	MPIOA6
B8	IO	DQ17B		AJ28	MPIOA7
B8	IO	DQ17B		AM29	MPIOA8
B8	IO	DQ17B		AL29	MPIOA9
B8	IO	DQS14B		AJ25	MPIOB0
B8	IO			AB20	MPIOB1
B8	IO	DQS13B		AL23	MPIOB10
B8	IO			AD20	MPIOB11
B8	IO	DQ12B		AG23	MPIOB12
B8	IO	DQSn12B		AH22	MPIOB13
B8	IO	DQ12B		AG22	MPIOB14
B8	IO	DQ12B		AK22	MPIOB15

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B8	IO	DQ12B		AJ23	MPIOB16
B8	IO	DQS12B		AJ22	MPIOB17
B8	IO			AC20	MPIOB18
B8	IO			AB19	MPIOB19
B8	IO			AE21	MPIOB2
B8	IO			AE20	MPIOB20
B8	IO			AC19	MPIOB21
B8	IO	DQ11B		AM22	MPIOB22
B8	IO	DQSn11B		AL22	MPIOB23
B8	IO	CLK4p		AM17	MPIOB24
B8	IO	DQ11B		AJ21	MPIOB25
B8	IO	DQ11B		AK21	MPIOB26
B8	IO	DQ11B		AM21	MPIOB27
B8	IO	DQS11B		AL21	MPIOB28
B8	IO			AD19	MPIOB29
B8	IO			AG20	MPIOB3
B8	IO			AE19	MPIOB30
B8	IO			AF19	MPIOB31
B8	IO			AB18	MPIOB32
B8	IO	DQ10B		AH20	MPIOB33
B8	IO	DQSn10B		AJ20	MPIOB34
B8	IO	DQ10B		AJ19	MPIOB35
B8	IO	DQ10B		AH19	MPIOB36
B8	IO	DQ10B		AL20	MPIOB37
B8	IO	DQS10B		AK20	MPIOB38
B8	IO			AC18	MPIOB39
B8	IO			AF20	MPIOB4
B8	IO			AD18	MPIOB40
B8	IO			AB17	MPIOB41
B8	IO			AC17	MPIOB42
B8	IO	CLK5n		AJ17	MPIOB43
B8	IO	CLK4n		AL17	MPIOB44
B8	IO	DQ13B		AM24	MPIOB5
B8	IO	DQSn13B		AL24	MPIOB6
B8	IO	DQ13B		AK24	MPIOB7
B8	IO	DQ13B		AK23	MPIOB8

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B8	IO	DQ13B		AM23	MPIOB9
B4	MSEL0		MSEL0	B2	MSEL0
B4	MSEL1		MSEL1	F6	MSEL1
B4	MSEL2		MSEL2	J10	MSEL2
B4	MSEL3		MSEL3	H10	MSEL3
B3	nCE		nCE	C30	NCE
B7	nCEO		nCEO	AL3	NCEO
B8	nCONFIG		nCONFIG	AL30	NCONFIG
B3	IO		nCSO	G19	NCSO
B7	nIO_PULLUP		nIO_PULLUP	AK3	NIO_PULLUP
B8	IO	CLK5p		AK17	NRST
B3	nSTATUS		nSTATUS	B30	NSTATUS
B6	IO	DIFFIO_TX104p		AB5	PISMO_AUX0
B6	IO	DIFFIO_RX104n		AG2	PISMO_AUX1
B5	IO	DIFFIO_TX66n		H6	PISMO_AUX10
B5	IO	DIFFIO_TX66p		H5	PISMO_AUX11
B4	IO	CLK13p		E16	PISMO_AUX12
B6	IO	DIFFIO_RX104p		AG1	PISMO_AUX2
B6	IO	DIFFIO_TX103n		AA9	PISMO_AUX3
B6	IO	DIFFIO_TX103p		AA8	PISMO_AUX4
B6	IO	DIFFIO_RX103n		AD4	PISMO_AUX5
B6	IO	DIFFIO_RX103p		AD3	PISMO_AUX6
B5	IO	DIFFIO_TX67p		J6	PISMO_AUX7
B5	IO	DIFFIO_RX67n		G6	PISMO_AUX8
B5	IO	DIFFIO_RX67p		G5	PISMO_AUX9
B4	IO	DQ0T		B4	PISMO_DM_DA0
B4	IO	DQ0T		D5	PISMO_DM_DA1
B4	IO	DQ0T		E5	PISMO_DM_DA2
B4	IO	DQ0T		A4	PISMO_DM_DA3
B4	IO	DQ1T		A5	PISMO_DM_DA4
B4	IO	DQ1T		D6	PISMO_DM_DA5
B4	IO	DQ1T		C6	PISMO_DM_DA6
B4	IO	DQSn1T		B6	PISMO_DM_DA7
B4	IO	DQ2T		B7	PISMO_DM_DB0
B4	IO	DQ2T		E7	PISMO_DM_DB1
B4	IO	DQ2T		E6	PISMO_DM_DB2

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B4	IO	DQ2T		A7	PISMO_DM_DB3
B4	IO	DQ3T		C9	PISMO_DM_DB4
B4	IO	DQ3T		A8	PISMO_DM_DB5
B4	IO	DQ3T		C8	PISMO_DM_DB6
B4	IO	DQSn3T		B9	PISMO_DM_DB7
B4	IO	DQ4T		D8	PISMO_DM_DC0
B4	IO	DQ4T		E8	PISMO_DM_DC1
B4	IO	DQ4T		F8	PISMO_DM_DC2
B4	IO	DQ4T		F10	PISMO_DM_DC3
B4	IO	DQS5T		C10	PISMO_DM_DC4
B4	IO	DQ5T		A10	PISMO_DM_DC5
B4	IO	DQ5T		B10	PISMO_DM_DC6
B4	IO	DQ5T		D10	PISMO_DM_DC7
B4	IO	DQ6T		E11	PISMO_DM_DD0
B4	IO	DQ6T		G10	PISMO_DM_DD1
B4	IO	DQ6T		G11	PISMO_DM_DD2
B4	IO	DQ6T		G12	PISMO_DM_DD3
B4	IO	DQS7T		C12	PISMO_DM_DD4
B4	IO	DQ7T		D12	PISMO_DM_DD5
B4	IO	DQ7T		A11	PISMO_DM_DD6
B4	IO	DQ7T		B11	PISMO_DM_DD7
B4	IO	DQS0T		C4	PISMO_DM_DQSA_DH
B4	IO	DQSn0T		C5	PISMO_DM_DQSA_DL
B4	IO	DQS2T		D7	PISMO_DM_DQSB_DH
B4	IO	DQSn2T		C7	PISMO_DM_DQSB_DL
B4	IO	DQS4T		F9	PISMO_DM_DQSC_DH
B4	IO	DQSn4T		E9	PISMO_DM_DQSC_DL
B4	IO	DQS6T		F11	PISMO_DM_DQSD_DH
B4	IO	DQSn6T		F12	PISMO_DM_DQSD_DL
B4	IO			H9	PISMO_DM0
B4	IO			J11	PISMO_DM1

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B4	IO			L15	PISMO_DM10
B4	IO			K13	PISMO_DM11
B4	IO			J12	PISMO_DM12
B4	IO	DQS3T		B8	PISMO_DM13
B4	IO	DQ3T		A9	PISMO_DM14
B4	IO			H12	PISMO_DM15
B4	IO			K14	PISMO_DM16
B4	IO			J13	PISMO_DM17
B4	IO			L16	PISMO_DM18
B4	IO	DQSn5T		C11	PISMO_DM19
B4	IO	RUP4		L12	PISMO_DM2
B4	IO	DQ5T		D11	PISMO_DM20
B4	IO			K15	PISMO_DM21
B4	IO			H13	PISMO_DM22
B4	IO			J14	PISMO_DM23
B4	IO	DQSn7T		B12	PISMO_DM24
B4	IO	DQ7T		A12	PISMO_DM25
B4	IO			G14	PISMO_DM26
B4	IO	DQS8T		F14	PISMO_DM27
B4	IO	DQ8T		E13	PISMO_DM28
B4	IO	DQ8T		F13	PISMO_DM29
B4	IO	RDN4		K11	PISMO_DM3
B4	IO	DQ8T		G13	PISMO_DM30
B4	IO	DQSn8T		E14	PISMO_DM31
B4	IO	DQ8T		F15	PISMO_DM32
B4	IO			H14	PISMO_DM33
B4	IO			L17	PISMO_DM34
B4	IO	DQS9T		C13	PISMO_DM35
B4	IO	DQ9T		B14	PISMO_DM36
B4	IO			H11	PISMO_DM4
B4	IO			K12	PISMO_DM5
B4	IO			L13	PISMO_DM6
B4	IO			L14	PISMO_DM7
B4	IO	DQS1T		B5	PISMO_DM8
B4	IO	DQ1T		A6	PISMO_DM9
B4	IO	DQ9T		D14	PISMO_FS0

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B4	IO	DQ9T		D13	PISMO_FS1
B4	IO	DQSn9T		B13	PISMO_FS2
B4	IO	DQ9T		A14	PISMO_FS3
B4	IO			J15	PISMO_FS4
B4	IO			K16	PISMO_FS5
B4	IO			K17	PISMO_FS6
B4	IO	CLK12n		B16	PISMO_FS7
B4	IO	CLK12p		A16	PISMO_FS8
B4	IO	CLK13n		F16	PISMO_FS9
B6	IO	DIFFIO_RX111n		AF6	PISMO_NA0
B6	IO	DIFFIO_RX111p		AF5	PISMO_NA1
B6	IO	DIFFIO_TX108n		AC7	PISMO_NA10
B6	IO	DIFFIO_TX108p		AC6	PISMO_NA11
B6	IO	DIFFIO_RX108n		AJ2	PISMO_NA12
B6	IO	DIFFIO_RX108p		AJ1	PISMO_NA13
B6	IO	DIFFIO_TX107n		AC9	PISMO_NA14
B6	IO	DIFFIO_TX107p		AC8	PISMO_NA15
B6	IO	DIFFIO_RX107n		AE6	PISMO_NA16
B6	IO	DIFFIO_RX107p		AE5	PISMO_NA17
B6	IO	DIFFIO_TX106n		AB8	PISMO_NA18
B6	IO	DIFFIO_TX106p		AB7	PISMO_NA19
B6	IO	DIFFIO_TX110n		AD7	PISMO_NA2
B6	IO	DIFFIO_RX106n		AH2	PISMO_NA20
B6	IO	DIFFIO_RX106p		AH1	PISMO_NA21
B6	IO	DIFFIO_TX105n		AB10	PISMO_NA22
B6	IO	DIFFIO_TX105p		AB9	PISMO_NA23
B6	IO	DIFFIO_RX105n		AF4	PISMO_NA24
B6	IO	DIFFIO_RX105p		AF3	PISMO_NA25
B6	IO	DIFFIO_TX104n		AB6	PISMO_NA26
B6	IO	DIFFIO_TX110p		AD6	PISMO_NA3
B6	IO	DIFFIO_RX110n		AH4	PISMO_NA4
B6	IO	DIFFIO_RX110p		AH3	PISMO_NA5
B6	IO	DIFFIO_TX109n		AD9	PISMO_NA6
B6	IO	DIFFIO_TX109p		AD8	PISMO_NA7
B6	IO	DIFFIO_RX109n		AG4	PISMO_NA8
B6	IO	DIFFIO_RX109p		AG3	PISMO_NA9

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B5	IO	CLK10p/DIFFIO_RX_C3p		T1	PISMO_SM0
B5	IO	CLK10n/DIFFIO_RX_C3n		T2	PISMO_SM1
B5	IO	DIFFIO_TX86n		R11	PISMO_SM10
B5	IO	DIFFIO_TX86p		R10	PISMO_SM11
B5	IO	DIFFIO_RX86n		M2	PISMO_SM12
B5	IO	DIFFIO_RX86p		M1	PISMO_SM13
B5	IO	DIFFIO_TX85n		R5	PISMO_SM14
B5	IO	DIFFIO_TX85p		R4	PISMO_SM15
B5	IO	DIFFIO_RX85n		N3	PISMO_SM16
B5	IO	DIFFIO_RX85p		N2	PISMO_SM17
B5	IO	DIFFIO_TX84n		R7	PISMO_SM18
B5	IO	DIFFIO_TX84p		R6	PISMO_SM19
B5	IO	DIFFIO_TX88n		T11	PISMO_SM2
B5	IO	DIFFIO_RX84n		L2	PISMO_SM20
B5	IO	DIFFIO_RX84p		L1	PISMO_SM21
B5	IO	DIFFIO_TX83n		P11	PISMO_SM22
B5	IO	DIFFIO_TX83p		P10	PISMO_SM23
B5	IO	DIFFIO_RX83n		M4	PISMO_SM24
B5	IO	DIFFIO_RX83p		M3	PISMO_SM25
B5	IO	DIFFIO_TX82n		P5	PISMO_SM26
B5	IO	DIFFIO_TX82p		P4	PISMO_SM27
B5	IO	DIFFIO_RX82n		N5	PISMO_SM28
B5	IO	DIFFIO_RX82p		N4	PISMO_SM29
B5	IO	DIFFIO_TX88p		T10	PISMO_SM3
B5	IO	DIFFIO_TX81n		P7	PISMO_SM30
B5	IO	DIFFIO_TX81p		P6	PISMO_SM31
B5	IO	DIFFIO_RX81n		L4	PISMO_SM32
B5	IO	DIFFIO_RX81p		L3	PISMO_SM33
B5	IO	DIFFIO_TX80n		P9	PISMO_SM34
B5	IO	DIFFIO_TX80p		P8	PISMO_SM35
B5	IO	DIFFIO_RX80n		K2	PISMO_SM36
B5	IO	DIFFIO_RX80p		K1	PISMO_SM37
B5	IO	DIFFIO_TX79n		N9	PISMO_SM38
B5	IO	DIFFIO_TX79p		N8	PISMO_SM39
B5	IO	DIFFIO_RX88n		P2	PISMO_SM4
B5	IO	DIFFIO_RX79n		K4	PISMO_SM40

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B5	IO	DIFFIO_RX79p		K3	PISMO_SM41
B5	IO	DIFFIO_TX78n		N7	PISMO_SM42
B5	IO	DIFFIO_TX78p		N6	PISMO_SM43
B5	IO	DIFFIO_RX78n		J2	PISMO_SM44
B5	IO	DIFFIO_RX78p		J1	PISMO_SM45
B5	IO	DIFFIO_TX77n		M7	PISMO_SM46
B5	IO	DIFFIO_TX77p		M6	PISMO_SM47
B5	IO	DIFFIO_RX77n		H2	PISMO_SM48
B5	IO	DIFFIO_RX77p		H1	PISMO_SM49
B5	IO	DIFFIO_RX88p		P1	PISMO_SM5
B5	IO	DIFFIO_TX76n		N11	PISMO_SM50
B5	IO	DIFFIO_TX76p		N10	PISMO_SM51
B5	IO	DIFFIO_RX76n		J4	PISMO_SM52
B5	IO	DIFFIO_RX76p		J3	PISMO_SM53
B5	IO	DIFFIO_TX75n		M11	PISMO_SM54
B5	IO	DIFFIO_TX75p		M10	PISMO_SM55
B5	IO	DIFFIO_RX75n		G2	PISMO_SM56
B5	IO	DIFFIO_RX75p		G1	PISMO_SM57
B5	IO	DIFFIO_TX74n		L6	PISMO_SM58
B5	IO	DIFFIO_TX74p		L5	PISMO_SM59
B5	IO	DIFFIO_TX87n		T6	PISMO_SM6
B5	IO	DIFFIO_RX74n		G4	PISMO_SM60
B5	IO	DIFFIO_RX74p		G3	PISMO_SM61
B5	IO	DIFFIO_TX73n		M9	PISMO_SM62
B5	IO	DIFFIO_TX73p		M8	PISMO_SM63
B5	IO	DIFFIO_RX73n		F2	PISMO_SM64
B5	IO	DIFFIO_RX73p		F1	PISMO_SM65
B5	IO	DIFFIO_TX72n		L10	PISMO_SM66
B5	IO	DIFFIO_TX72p		L9	PISMO_SM67
B5	IO	DIFFIO_RX72n		F4	PISMO_SM68
B5	IO	DIFFIO_RX72p		F3	PISMO_SM69
B5	IO	DIFFIO_TX87p		T5	PISMO_SM7
B5	IO	DIFFIO_TX71n		L8	PISMO_SM70
B5	IO	DIFFIO_TX71p		L7	PISMO_SM71
B5	IO	DIFFIO_RX71n		E2	PISMO_SM72
B5	IO	DIFFIO_RX71p		E1	PISMO_SM73

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B5	IO	DIFFIO_TX70n		K9	PISMO_SM74
B5	IO	DIFFIO_TX70p		K8	PISMO_SM75
B5	IO	DIFFIO_RX70n		E4	PISMO_SM76
B5	IO	DIFFIO_RX70p		E3	PISMO_SM77
B5	IO	DIFFIO_TX69n		K7	PISMO_SM78
B5	IO	DIFFIO_TX69p		K6	PISMO_SM79
B5	IO	DIFFIO_RX87n		R3	PISMO_SM8
B5	IO	DIFFIO_RX69n		D2	PISMO_SM80
B5	IO	DIFFIO_RX69p		D1	PISMO_SM81
B5	IO	DIFFIO_TX68n		J9	PISMO_SM82
B5	IO	DIFFIO_TX68p		J8	PISMO_SM83
B5	IO	DIFFIO_RX68n		H4	PISMO_SM84
B5	IO	DIFFIO_RX68p		H3	PISMO_SM85
B5	IO	DIFFIO_TX67n		J7	PISMO_SM86
B5	FPLL10CLKn	INPUT		D4	PISMO_SM87
B5	FPLL10CLKp	INPUT		D3	PISMO_SM88
B5	IO	DIFFIO_RX87p		R2	PISMO_SM9
B7	PLL_ENA		PLL_ENA	AF8	PLL_ENA
B7	PORSEL		PORSEL	AL2	PORSEL
B8	TCK		TCK	AF24	S2_TCK
B8	TDI		TDI	AL31	S2_TDI
B4	TDO		TDO	C3	S2_TDO
B8	TMS		TMS	AE24	S2_TMS
B7	IO			AB16	SODIMM_C0
B7	IO			AC16	SODIMM_C1
B7	IO			AE14	SODIMM_C10
B7	IO	DQ8B		AG15	SODIMM_C11
B7	IO	DQSn8B		AH14	SODIMM_C12
B7	IO	DQ8B		AF13	SODIMM_C13
B7	IO	DQ8B		AG13	SODIMM_C14
B7	IO	DQ8B		AH13	SODIMM_C15
B7	IO	DQS8B		AG14	SODIMM_C16
B7	IO			AB15	SODIMM_C17
B7	IO			AF14	SODIMM_C18
B7	IO	DQ7B		AM12	SODIMM_C19
B7	IO			AC15	SODIMM_C2

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B7	IO	DQS7B		AL11	SODIMM_C20
B7	IO			AC14	SODIMM_C21
B7	IO	DQSn6B		AK11	SODIMM_C22
B7	IO	DQS6B		AK10	SODIMM_C23
B7	IO			AD13	SODIMM_C24
B7	IO			AE13	SODIMM_C25
B7	IO	DQ5B		AG12	SODIMM_C26
B7	IO	DQS5B		AF11	SODIMM_C27
B7	IO			AB14	SODIMM_C28
B7	IO	DQSn4B		AL9	SODIMM_C29
B7	IO	DQ9B		AM14	SODIMM_C3
B7	IO	DQS4B		AK9	SODIMM_C30
B7	IO			AC13	SODIMM_C31
B7	IO			AE12	SODIMM_C32
B7	IO	DQ3B		AM8	SODIMM_C33
B7	IO	DQS3B		AL7	SODIMM_C34
B7	IO			AB13	SODIMM_C35
B7	IO			AD12	SODIMM_C36
B7	IO	DQSn2B		AL6	SODIMM_C37
B7	IO			AE11	SODIMM_C38
B7	IO	DQ1B		AH9	SODIMM_C39
B7	IO	DQSn9B		AL13	SODIMM_C4
B7	IO	DQS1B		AG8	SODIMM_C40
B7	IO			AD11	SODIMM_C41
B7	IO			AC12	SODIMM_C42
B7	IO	DQSn0B		AK5	SODIMM_C43
B7	IO			AC11	SODIMM_C44
B7	IO			AB12	SODIMM_C45
B7	IO			AE10	SODIMM_C46
B7	IO	RDN7		AB11	SODIMM_C47
B7	IO	RUP7		AD10	SODIMM_C48
B7	IO			AE9	SODIMM_C49
B7	IO	DQ9B		AJ13	SODIMM_C5
B7	IO	CLK7p		AH16	SODIMM_C50
B7	IO	CLK7n		AG16	SODIMM_C51
B7	IO	CLK6p		AM16	SODIMM_C52

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B7	IO	CLK6n		AL16	SODIMM_C53
B7	IO	DQ9B		AJ14	SODIMM_C6
B7	IO	DQ9B		AL14	SODIMM_C7
B7	IO	DQS9B		AK13	SODIMM_C8
B7	IO			AD14	SODIMM_C9
B7	IO	DQSn7B		AL12	SODIMM_D0
B7	IO	DQ7B		AM11	SODIMM_D1
B7	IO	DQ5B		AG10	SODIMM_D10
B7	IO	DQ5B		AF12	SODIMM_D11
B7	IO	DQ4B		AM9	SODIMM_D12
B7	IO	DQ4B		AJ8	SODIMM_D13
B7	IO	DQ4B		AK8	SODIMM_D14
B7	IO	DQ4B		AJ10	SODIMM_D15
B7	IO	DQSn3B		AL8	SODIMM_D16
B7	IO	DQ3B		AJ7	SODIMM_D17
B7	IO	DQ3B		AK7	SODIMM_D18
B7	IO	DQ3B		AM7	SODIMM_D19
B7	IO	DQ7B		AJ12	SODIMM_D2
B7	IO	DQ2B		AM6	SODIMM_D20
B7	IO	DQ2B		AJ6	SODIMM_D21
B7	IO	DQ2B		AK6	SODIMM_D22
B7	IO	DQ2B		AM5	SODIMM_D23
B7	IO	DQSn1B		AH8	SODIMM_D24
B7	IO	DQ1B		AH7	SODIMM_D25
B7	IO	DQ1B		AH6	SODIMM_D26
B7	IO	DQ1B		AG9	SODIMM_D27
B7	IO	DQ0B		AM4	SODIMM_D28
B7	IO	DQ0B		AH5	SODIMM_D29
B7	IO	DQ7B		AK12	SODIMM_D3
B7	IO	DQ0B		AJ5	SODIMM_D30
B7	IO	DQ0B		AL4	SODIMM_D31
B7	IO	DQ6B		AM10	SODIMM_D4
B7	IO	DQ6B		AL10	SODIMM_D5
B7	IO	DQ6B		AH11	SODIMM_D6
B7	IO	DQ6B		AJ11	SODIMM_D7
B7	IO	DQSn5B		AG11	SODIMM_D8

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B7	IO	DQ5B		AF10	SODIMM_D9
B7	IO	DQS0B		AK4	SODIMM_DQS0
B7	IO	DQS2B		AL5	SODIMM_DQS1
B6	IO	DIFFIO_TX102n		AA11	SODIMM_S0
B6	IO	DIFFIO_TX102p		AA10	SODIMM_S1
B6	IO	DIFFIO_RX100n		AE2	SODIMM_S10
B6	IO	DIFFIO_RX100p		AE1	SODIMM_S11
B6	IO	DIFFIO_TX99n		W11	SODIMM_S12
B6	IO	DIFFIO_TX99p		W10	SODIMM_S13
B6	IO	DIFFIO_RX99n		AD2	SODIMM_S14
B6	IO	DIFFIO_RX99p		AD1	SODIMM_S15
B6	IO	DIFFIO_TX98n		Y9	SODIMM_S16
B6	IO	DIFFIO_TX98p		Y8	SODIMM_S17
B6	IO	DIFFIO_RX98n		AC4	SODIMM_S18
B6	IO	DIFFIO_RX102n		AF2	SODIMM_S2
B6	IO	DIFFIO_RX102p		AF1	SODIMM_S3
B6	IO	DIFFIO_TX101n		Y11	SODIMM_S4
B6	IO	DIFFIO_TX101p		Y10	SODIMM_S5
B6	IO	DIFFIO_RX101n		AE4	SODIMM_S6
B6	IO	DIFFIO_RX101p		AE3	SODIMM_S7
B6	IO	DIFFIO_TX100n		AA7	SODIMM_S8
B6	IO	DIFFIO_TX100p		AA6	SODIMM_S9
B8	TRST		TRST	AK30	TRST
B8	IO		CS	AC22	UGRID0
B8	IO		CLKUSR	AD23	UGRID1
B12	IO	PLL12_OUT1n		AH18	UGRID10
B12	IO	PLL12_OUT1p		AJ18	UGRID11
B12	IO	PLL12_OUT0n		AK18	UGRID12
B12	IO	PLL12_OUT0p		AL18	UGRID13
B10	IO	PLL6_OUT1p		AJ15	UGRID14
B10	IO	PLL6_OUT1n		AH15	UGRID15
B10	IO	PLL6_OUT0p		AK16	UGRID16
B10	IO	PLL6_OUT0n		AJ16	UGRID17
B10	IO	PLL6_FBp/OUT2p		AL15	UGRID18
B10	IO	PLL6_FBn/OUT2n		AK15	UGRID19
B8	IO		nWS	AE23	UGRID2

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B6	FPLL9CLKp	INPUT		AJ3	UGRID20
B6	FPLL9CLKn	INPUT		AJ4	UGRID21
B6	IO	DIFFIO_RX98p		AC3	UGRID22
B6	IO	DIFFIO_TX97n		Y7	UGRID23
B6	IO	DIFFIO_TX97p		Y6	UGRID24
B6	IO	DIFFIO_RX97n		AC2	UGRID25
B6	IO	DIFFIO_RX97p		AC1	UGRID26
B6	IO	DIFFIO_TX96n		W5	UGRID27
B6	IO	DIFFIO_TX96p		W4	UGRID28
B6	IO	DIFFIO_RX96n		AB4	UGRID29
B8	IO		nRS	AF23	UGRID3
B6	IO	DIFFIO_RX96p		AB3	UGRID30
B6	IO	DIFFIO_TX95n		W7	UGRID31
B6	IO	DIFFIO_TX95p		W6	UGRID32
B6	IO	DIFFIO_RX95n		AB2	UGRID33
B6	IO	DIFFIO_RX95p		AB1	UGRID34
B6	IO	DIFFIO_TX94n		W9	UGRID35
B6	IO	DIFFIO_TX94p		W8	UGRID36
B6	IO	DIFFIO_RX94n		Y5	UGRID37
B6	IO	DIFFIO_RX94p		Y4	UGRID38
B6	IO	DIFFIO_TX93n		V5	UGRID39
B8	IO		RUnLU	AG17	UGRID4
B6	IO	DIFFIO_TX93p		V4	UGRID40
B6	IO	DIFFIO_RX93n		AA4	UGRID41
B6	IO	DIFFIO_RX93p		AA3	UGRID42
B6	IO	DIFFIO_TX92n		V7	UGRID43
B6	IO	DIFFIO_TX92p		V6	UGRID44
B6	IO	DIFFIO_RX92n		AA2	UGRID45
B6	IO	DIFFIO_RX92p		AA1	UGRID46
B6	IO	DIFFIO_TX91n		V10	UGRID47
B6	IO	DIFFIO_TX91p		V9	UGRID48
B6	IO	DIFFIO_RX91n		Y3	UGRID49
B8	IO		DEV_OE	AH17	UGRID5
B6	IO	DIFFIO_RX91p		Y2	UGRID50
B6	IO	DIFFIO_TX90n		U11	UGRID51
B6	IO	DIFFIO_TX90p		U10	UGRID52

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B6	IO	DIFFIO_RX90n		W2	UGRID53
B6	IO	DIFFIO_RX90p		W1	UGRID54
B6	IO	DIFFIO_TX89n		U6	UGRID55
B6	IO	DIFFIO_TX89p		U5	UGRID56
B6	IO	DIFFIO_RX89n		V3	UGRID57
B6	IO	DIFFIO_RX89p		V2	UGRID58
B6	CLK9n	INPUT		U4	UGRID59
B8	IO		DEV_CLRn	AG19	UGRID6
B6	CLK9p	INPUT		U3	UGRID60
B6	IO	CLK8n/DIFFIO_RX_C2n		U2	UGRID61
B6	IO	CLK8p/DIFFIO_RX_C2p		U1	UGRID62
B9	IO	PLL5_FBn/OUT2n		E15	UGRID63
B9	IO	PLL5_FBp/OUT2p		D15	UGRID64
B9	IO	PLL5_OUT0n		C15	UGRID65
B9	IO	PLL5_OUT0p		B15	UGRID66
B9	IO	PLL5_OUT1n		D16	UGRID67
B9	IO	PLL5_OUT1p		C16	UGRID68
B11	IO	PLL11_OUT0p		B18	UGRID69
B8	IO		nCS	AG18	UGRID7
B11	IO	PLL11_OUT0n		C18	UGRID70
B11	IO	PLL11_OUT1p		D18	UGRID71
B11	IO	PLL11_OUT1n		E18	UGRID72
B11	IO	PLL11_FBp/OUT2p		A19	UGRID73
B11	IO	PLL11_FBn/OUT2n		B19	UGRID74
B3	IO		INIT_DONE	G25	UGRID75
B12	IO	PLL12_FBn/OUT2n		AL19	UGRID8
B12	IO	PLL12_FBp/OUT2p		AM19	UGRID9
B11	VCC_PLL11_OUT			J17	VCC_PLL11
B12	VCC_PLL12_OUT			AF16	VCC_PLL12
B9	VCC_PLL5_OUT			J16	VCC_PLL5
B10	VCC_PLL6_OUT			AF15	VCC_PLL6
	VCCA_PLL6			AE15	VCCA_PLL
	VCCA_PLL9			AE7	VCCA_PLL
	VCCA_PLL12			AF18	VCCA_PLL
	VCCA_PLL8			AF26	VCCA_PLL
	VCCA_PLL5			G15	VCCA_PLL

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	VCCA_PLL11			H17	VCCA_PLL
	VCCA_PLL7			H26	VCCA_PLL
	VCCA_PLL10			H8	VCCA_PLL
	VCCA_PLL4			R9	VCCA_PLL
	VCCA_PLL1			T24	VCCA_PLL
	VCCA_PLL3			U9	VCCA_PLL
	VCCA_PLL2			V26	VCCA_PLL
	VCCD_PLL6			AD15	VCCD_PLL
	VCCD_PLL12			AE18	VCCD_PLL
	VCCD_PLL9			AE8	VCCD_PLL
	VCCD_PLL8			AF25	VCCD_PLL
	VCCD_PLL5			H15	VCCD_PLL
	VCCD_PLL7			H25	VCCD_PLL
	VCCD_PLL10			H7	VCCD_PLL
	VCCD_PLL11			J18	VCCD_PLL
	VCCD_PLL4			T9	VCCD_PLL
	VCCD_PLL1			U24	VCCD_PLL
	VCCD_PLL3			U7	VCCD_PLL
	VCCD_PLL2			V25	VCCD_PLL
	VCCIO1			AA28	VCCIO_1
	VCCIO1			AK32	VCCIO_1
	VCCIO1			U21	VCCIO_1
	VCCIO1			V32	VCCIO_1
	VCCIO2			C32	VCCIO_2
	VCCIO2			M28	VCCIO_2
	VCCIO2			R32	VCCIO_2
	VCCIO2			T21	VCCIO_2
	VCCIO3			A18	VCCIO_3
	VCCIO3			A30	VCCIO_3
	VCCIO3			E21	VCCIO_3
	VCCIO3			M17	VCCIO_3
	VCCIO4			A15	VCCIO_4
	VCCIO4			A3	VCCIO_4
	VCCIO4			E12	VCCIO_4
	VCCIO4			M16	VCCIO_4
	VCCIO5			C1	VCCIO_5

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
	VCCIO5			M5	VCCIO_5
	VCCIO5			R1	VCCIO_5
	VCCIO5			T12	VCCIO_5
	VCCIO6			AA5	VCCIO_6
	VCCIO6			AK1	VCCIO_6
	VCCIO6			U12	VCCIO_6
	VCCIO6			V1	VCCIO_6
	VCCIO7			AA16	VCCIO_7
	VCCIO7			AH12	VCCIO_7
	VCCIO7			AM15	VCCIO_7
	VCCIO7			AM3	VCCIO_7
	VCCIO8			AA17	VCCIO_8
	VCCIO8			AH21	VCCIO_8
	VCCIO8			AM18	VCCIO_8
	VCCIO8			AM30	VCCIO_8
B8	VCCSEL		VCCSEL	AC23	VCCSEL
B1	VREFB1N1	VREFB1N1		AD28	VREFB1
B1	VREFB1N2	VREFB1N2		AG28	VREFB1
B1	VREFB1N0	VREFB1N0		W30	VREFB1
B2	VREFB2N0	VREFB2N0		F28	VREFB2
B2	VREFB2N1	VREFB2N1		J28	VREFB2
B2	VREFB2N2	VREFB2N2		P30	VREFB2
B3	VREFB3N0	VREFB3N0		C19	VREFB3
B3	VREFB3N2	VREFB3N2		C31	VREFB3
B3	VREFB3N1	VREFB3N1		D24	VREFB3
B4	VREFB4N2	VREFB4N2		C14	VREFB4
B4	VREFB4N0	VREFB4N0		C2	VREFB4
B4	VREFB4N1	VREFB4N1		D9	VREFB4
B5	VREFB5N2	VREFB5N2		F5	VREFB5
B5	VREFB5N1	VREFB5N1		J5	VREFB5
B5	VREFB5N0	VREFB5N0		P3	VREFB5
B6	VREFB6N1	VREFB6N1		AD5	VREFB6
B6	VREFB6N0	VREFB6N0		AG5	VREFB6
B6	VREFB6N2	VREFB6N2		W3	VREFB6
B7	VREFB7N1	VREFB7N1		AJ9	VREFB7
B7	VREFB7N0	VREFB7N0		AK14	VREFB7

Table 7-6. FPGA Pins Sorted by Signal Name (Continued)

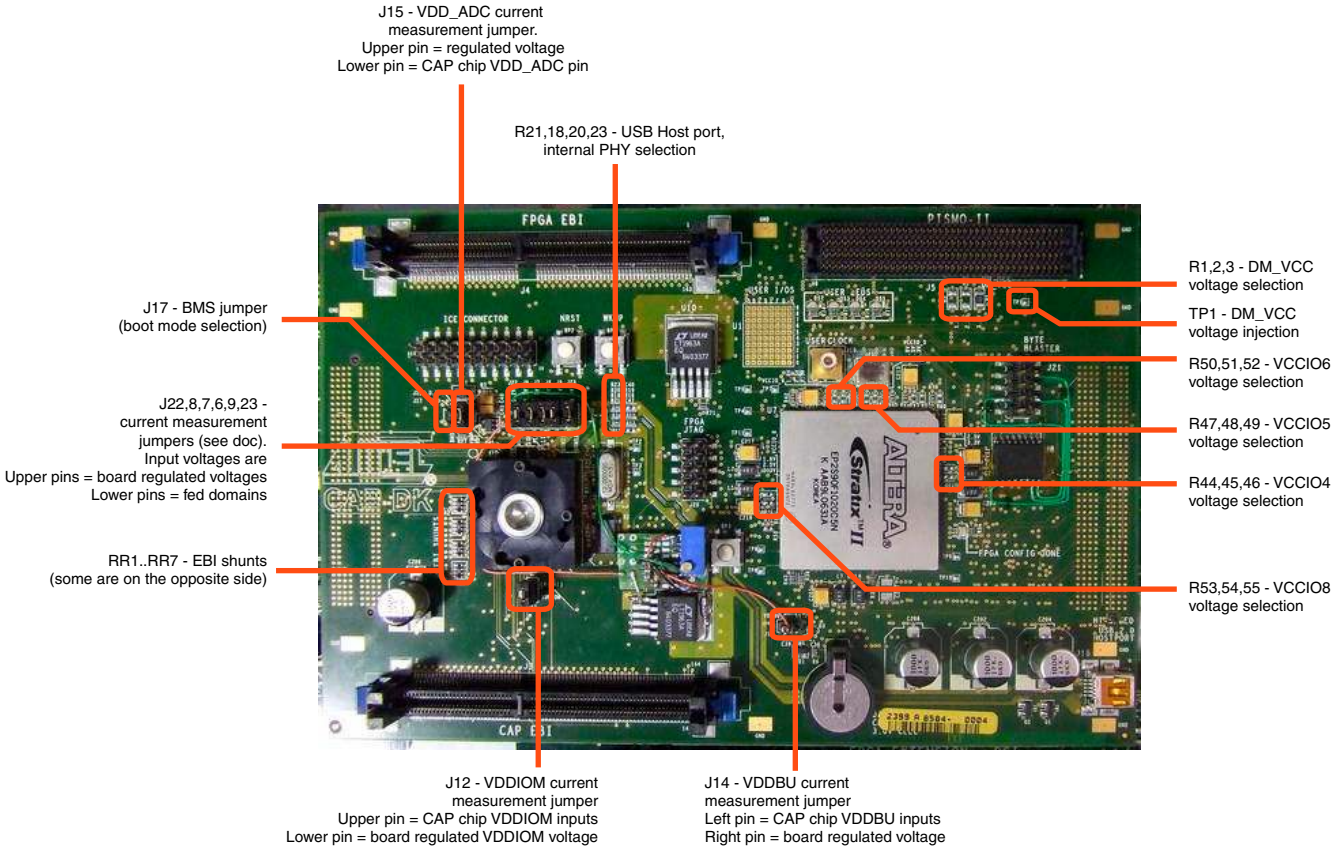
Bank	Pin Type Name	Other Pin Information	Configuration Function	Ball	Board Net
B7	VREFB7N2	VREFB7N2		AK2	VREFB7
B8	VREFB8N1	VREFB8N1		AJ24	VREFB8
B8	VREFB8N2	VREFB8N2		AK19	VREFB8
B8	VREFB8N0	VREFB8N0		AK31	VREFB8
B5	CLK11p	INPUT		T3	XTAL_CLK

Section 8

AT91CAP9A-DKZ Configuration

8.1 Configuration

Figure 8-1. AT91CAP9A-DKZ Mezzanine



8.2 Configuration Items

Table 8-1. AT91CAP9A-DKZ Configuration Items

Designation	Default Setting	Feature
RR1..RR7	all ON	PIO_D/EBI lines connect to the motherboard. Removing these 7 resistor networks will restrict the routing of this part of the EBI bus to be local to the mezzanine. This is implemented for signal integrity purposes, so that the tracks going down to the motherboard (unused when in EBI mode) do not act as stubs, which could corrupt the high-speed EBI signals integrity.
R1, 2, 3	ON, OFF, OFF	DM_VCC selection. See schematics Section 16. (1)
TP1	-	Testpoint for DM_VREF injection if needed.
J22	ON	CAP VDDCORE circuit opener (current measurement purpose)
J8	ON	CAP VDDIOP0 circuit opener (current measurement purpose)
J9	ON	CAP VDDUTMI12 circuit opener (current measurement purpose)
J12	ON	CAP VDDIOM circuit opener (current measurement purpose)
J14	ON	CAP VDDBU circuit opener (current measurement purpose)
J15	ON	CAP VDDADC circuit opener (current measurement purpose)
J23	ON	CAP VDDUTMI33 circuit opener (current measurement purpose)
J6	ON	CAP VDDPLL12 circuit opener (current measurement purpose)
J7	ON	CAP VDDPLL circuit opener (current measurement purpose)
R21, 18, 20, 23	ON, OFF, ON, OFF	USB host port internal PHY selection. Selects either high-speed PHY or full-speed PHY.
J17	ON	Boot Mode Selection (BMS). Selects boot memory to be internal or external. Refer to AT91CAP9 datasheet.
R44, 45, 46	ON, OFF, OFF (2)	Selects VCCIO_4 voltage. Default 3.3V (3)
R47, 48, 49	ON, OFF, OFF(2)	Selects VCCIO_5 voltage. Default 3.3V (3)
R50, 51, 52	ON, OFF, OFF(2)	Selects VCCIO_6 voltage. Default 3.3V (3)
R53,54, 55	ON, OFF, OFF (2)	Selects VCCIO_8 voltage. Default 3.3V (3)

Notes:
1. Only one of these shall be mounted, to do otherwise will cause a short out of the power supply.
2. Exactly **one** of these **must** be set. No less, no more.
3. Refer to "AT91CAP9A-DKZ Schematics" to see the span of this IO bank. By default this voltage is fixed at 3.3V. Change this setting only if you are sure of what you are doing...!

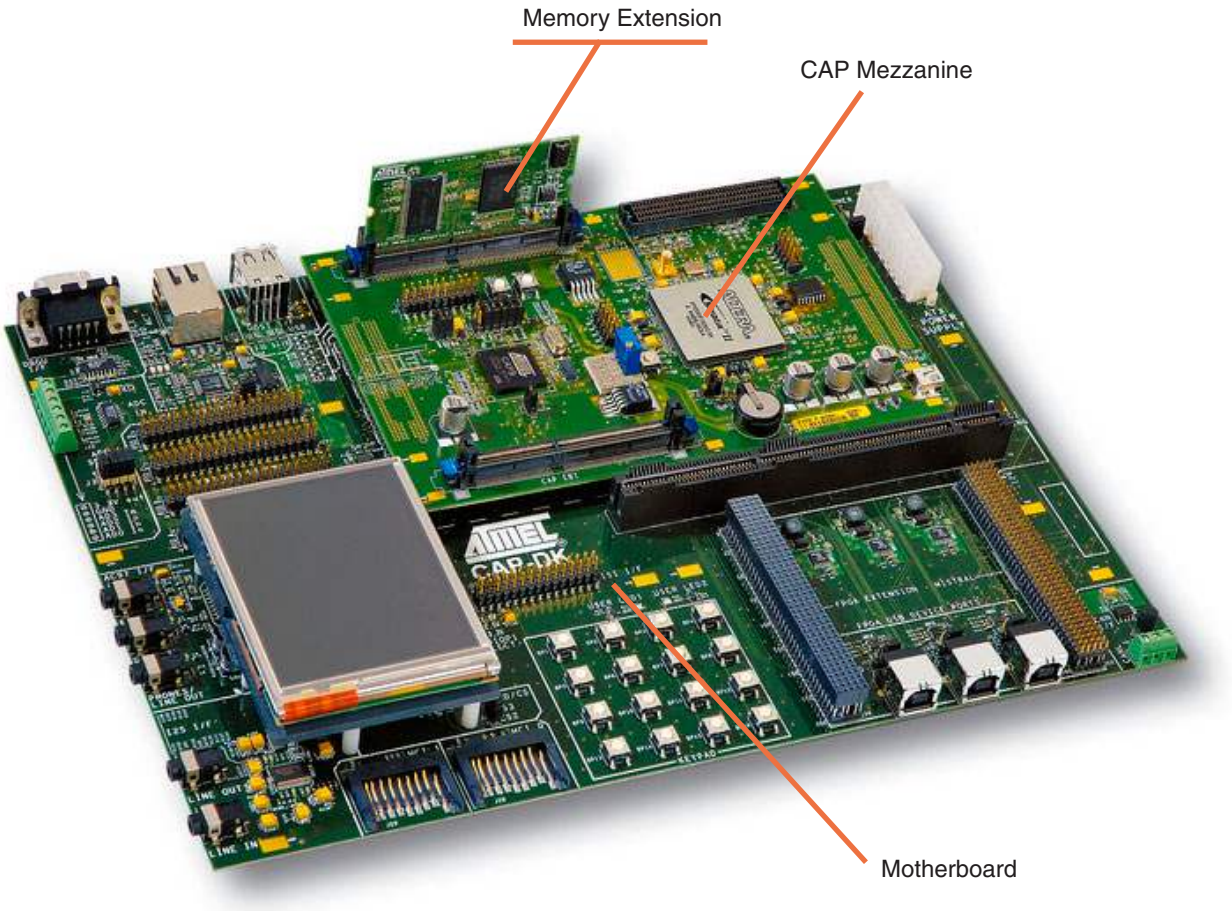
Section 9

Overview AT91CAP-MEM18 (CAP 1.8V Memory Board)

9.1 Scope

The **Memory Extension, Motherboard** and **Mezzanine** boards are used jointly to develop AT91CAP9 processor applications. **Section 9** through **Section 11** provide essential usage documentation for the AT91CAP 1.8V Memory Extension Board (AT91CAP-MEM18).

Figure 9-1. AT91CAP-MEM18 Overview



9.2 Purpose

The AT91CAP-MEM18 board provides a composite memory extension for any AT91CAP9-DK mezzanine. Its featured devices are 1.8V powered.

Section 10

Setting Up the AT91CAP-MEM18 Board

10.1 Electrostatic Warning

Upon delivery, the AT91CAP-MEM18 board is wrapped in a protective anti-static bag. The board must not be exposed to electrostatic discharges. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other on-board metallic element.

10.2 Requirements

In order to set up an AT91CAP9A-DK development system, the following items are needed:

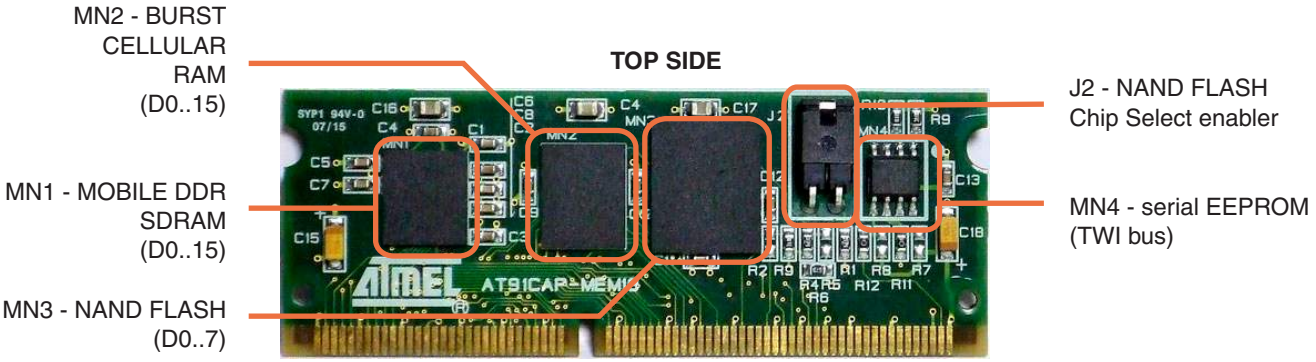
- AT91CAP9A-DKZ mezzanine board
- Memory extension board such as the AT91CAP-MEM18
- AT91CAP-DKM motherboard
- PC/ATX standard power supply unit

10.3 Layout

The board features a set of memory devices connected together on the same address/data bus:

- Burst cellular RAM
- NAND Flash
- Mobile DDR SDRAM
- A service TWI EEPROM

Figure 10-1. AT91CAP-MEM18 Board Layout - Top View



10.4 Powering Up the Board

The AT91CAP-MEM18 memory extension is powered by the AT91CAP9A-DKZ mezzanine it is connected to. This is automatically configured via resistor R6. This resistor sets the output level of an adjustable voltage regulator located on the mezzanine.

Section 11

AT91CAP-MEM18 Configuration

11.1 Configuration

Table 11-1. AT91CAP-MEM18 Configuration Items

Designation	Default Setting	Feature
J2	ON	NAND Flash chip select circuit opener. Removing the jumper disables the access to the NAND Flash device. This may be useful in case of corrupted contents, in order to force the system to boot on another default device (refer to AT91CAP9 chip and mezzanine documentation in this case).

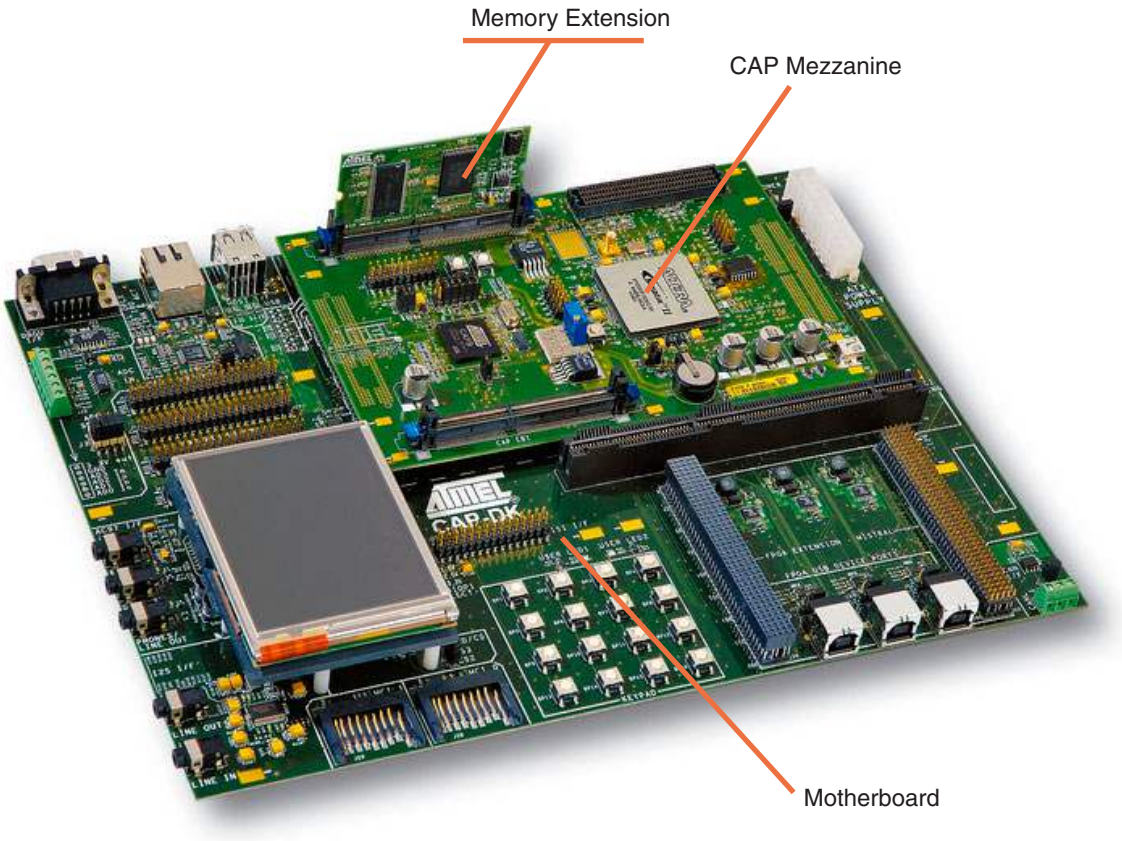
Section 12

Overview AT91CAP-MEM33 (CAP 3.3V Memory Board)

12.1 Scope

The **Memory Extension, Motherboard** and **Mezzanine** boards are used jointly to develop AT91CAP9 processor applications. **Section 12** through **Section 14** provide essential usage documentation for the AT91CAP 3.3V Memory Extension Board (AT91CAP-MEM33).

Figure 12-1. AT91CAP-MEM33 Overview



12.2 Purpose

The AT91CAP-MEM33 board provides a composite memory extension for any AT91CAP9-DK mezzanine. Its featured devices are 3.3V powered.

Section 13

Setting Up the AT91CAP-MEM33 Board

13.1 Electrostatic Warning

Upon delivery, the AT91CAP-MEM33 board is wrapped in a protective anti-static bag. The board must not be exposed to electrostatic discharges. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other on-board metallic element.

13.2 Requirements

In order to set up an AT91CAP9A-DK development system, the following items are needed:

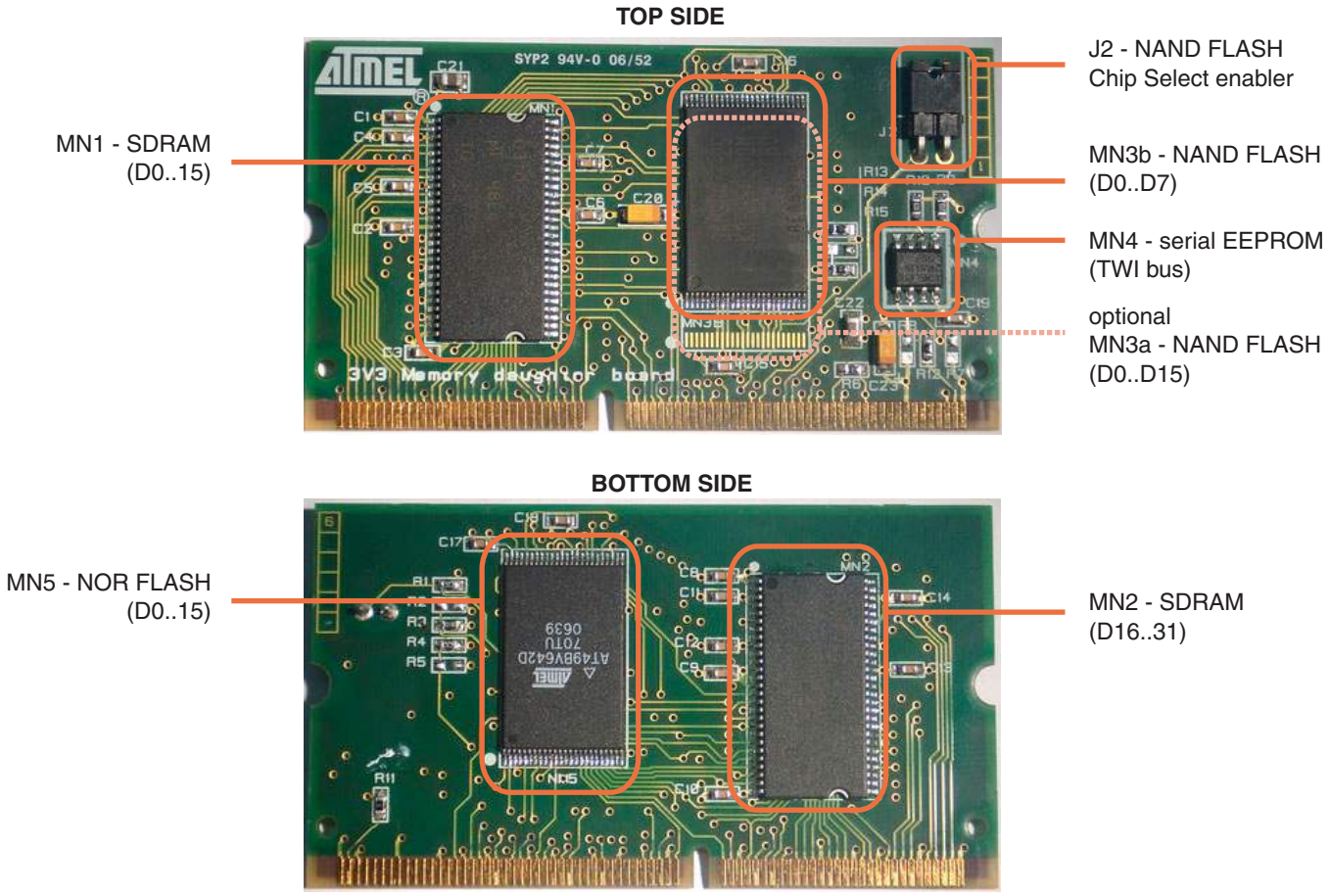
- AT91CAP9A-DKZ mezzanine board
- Memory extension board such as the AT91CAP-MEM33
- AT91CAP-DKM motherboard
- PC/ATX standard power supply unit

13.3 Layout

The board features a set of memory devices connected together on the same address/data bus:

- SDRAM
- NAND Flash
- NOR Flash
- A service TWI EEPROM

Figure 13-1. AT91CAP-MEM33 Board Layout - Top View



13.4 Powering Up the Board

The AT91CAP-MEM33 memory extension is powered by the AT91CAP9A-DKZ mezzanine it is connected to. This is automatically configured via resistor R6. This resistor sets the output level of an adjustable voltage regulator located on the mezzanine.

Section 14

AT91CAP-MEM33 Configuration

14.1 Configuration

Table 14-1. AT91CAP-MEM18 Configuration Items

Designation	Default Setting	Feature
J2	ON	NOR Flash chip select circuit opener. Removing the jumper disables the access to the NOR Flash device. This may be useful in case of corrupted contents, in order to force the system to boot on another default device (refer to AT91CAP9 chip and mezzanine documentation in this case).

Section 15

AT91CAP-DKM Schematics

15.1 Schematics

This section contains the following appended schematics:

- AT91CAP9-DKM Diagram
- Power Supply
- Mezzanine Connectors
- FPGA Connectors
- Upstream Interfaces
- User Interface and PIOs
- Ethernet (RJ45 Connector)
- Serial Interfaces
  - Serial Debug Port
  - CAN Bus
  - USB Host Interface
- Serial Devices
  - Image Sensor Connector
  - SD Card/MMC Card - DataFlash Card Interface
  - SD Card/MMC Card Interface
  - Serial EEPROM
- Audio AC97
- ADC Inputs
- Audio I2S
- LCD Panel

J23

J24

J26

J21

page 7, 8

J35, J36

J30, J31,J32

J33

page 10,11,12

J28

J29

page 9

TP5 5016 TP6 5016 TP7 5016 TP8 5016 TP9 5016 TP10 5016 TP11 5016 TP12 5016 TP13 5016 TP14 5016 TP15 5016

COMMUNICATION

CAN: DTXD, DRXD

CAN: CANTX, CANRX, CANRS

USB: HDMA, HDPA, HDMB, HDPB

ETHERNET: 5V, 3V3, GND, TX_CLK, TXD1, TXD0, TX_EN, RXD1, RXD0, RX_DV, RX_ER, MDC, MDIO, MDINTR, NRST

SOUND & ADC

I2S: 5V, 3V3, GND, L3DATA, L3CLOCK, SYSCLK, WS, BCK, DATAI, DATAO, EXTCLK

AC97: SYNC, BITCLK, SDATA_OUT, SDATA_IN, RST#

ADC: ADC1, ADC2, ADC3, ADC4

SERIAL DEVICES

MCI: MCI0_CD, MCI0_DA0, MCI0_DA1, MCI0_DA2, MCI0_DA3, MCI0_CDA, MCI0_CK

MCI: MCI1_CD, MCI1_DA0, MCI1_DA1, MCI1_DA2, MCI1_DA3, MCI1_CDA, MCI1_CK

SDA, SCL

ISI: 3V3, 2V5, 1V8, GND, ISI_D[0..11], ISI_MCK, ISI_VSYNC, ISI_HSYNC, ISI_PCK, CTRL1, CTRL2, VDDIOP1

J1-1 J1-2 J1-3 J1-4

J3-1 J3-2 J3-3 J3-4

ATX POWER SUPPLY

J4

page 2

12V, 5V, 3V3, 2V5, 1V8, 1V2, GND, -12V, SHDN

MEZZANINE CONNECTORS

SHDN, WKUP, PA[0..31], PB[0..31], PC[0..31], PD[0..31], HDMA, HDPA, HDMB, HDPB, VDDIOP1

FPGA[0..275], 5V, 3V3, 2V5, 1V8, 1V2, GND, VCCIO1, VCCIO2, VCCIO3, NRST

J6, J7

page 3

FPGA CONNECTORS

FPGA[0..275], NRST, 12V, 5V, GND, -12V, VCCIO1, VCCIO2, VCCIO3

page 4

FPGA UPSTREAM

3V3, GND, FPGA[0..275], VCCIO3

J12 J14 J16

page 5

LCD & TSC

LCD: 3V3, GND, R[0..5], G[0..5], B[0..5], LCDD[2..7], LCDD[10..15], LCDD[18..23], LCDHSYNC, LCDDOTCK, LCDDEN, HSYNC, DCLK, DTMG, PWM0, PC0, VCTRL, PCI

J2: SPI0_NPCS2, SPI0_NPCS3

SPI0_MOSI, SPI0_MISO, SPI0_SPCK, MOSI, MISO, SPCK, NPCS

PC4, PC5, IRQ, BUSY

page 13

UI & PIO CONNECTORS

PA[0..31], PB[0..31], PC[0..31], PD[0..31], PD[6..13], KBD[0..7], 3V3, GND, PWM3, PWM1, PWM2, USERLED2, USERLED1, PWRLED

page 6

CAP9 PIO USAGE

PA[0..31]

SPI0_MISO	PA0	PA0	MCI0_DA0
SPI0_MOSI	PA1	PA1	MCI0_CDA
SPI0_SPCK	PA2	PA2	MCI0_CK
		PA3	MCI0_DA1
		PA4	MCI0_DA2
		PA5	MCI0_DA3
		PA6	AC97FS
		PA7	AC97CK
		PA8	AC97TX
		PA9	AC97RX
		PA10	PWM1
		PA11	PWM3
		PA12	CANTX
		PA13	CANRX
		PA14	(ISI_CTRL1)
		PA15	(ISI_CTRL2)
MCI1_CK	PA16	PA16	ISI_D0
MCI1_CDA	PA17	PA17	ISI_D1
MCI1_DA0	PA18	PA18	ISI_D2
MCI1_DA1	PA19	PA19	ISI_D3
MCI1_DA2	PA20	PA20	ISI_D4
MCI1_DA3	PA21	PA21	ISI_D5
		PA22	ISI_D6
		PA23	ISI_D7
		PA24	ISI_PCK
		PA25	ISI_HSYNC
		PA26	ISI_VSYNC
		PA27	ISI_MCK
		PA28	ISI_D8
		PA29	ISI_D9
		PA30	ISI_D10
		PA31	ISI_D11

PB[0..31]

PB0	TF0	
PB1	TK0	
PB2	TD0	
PB3	RD0	
PB4	TWD	
PB5	TWCK	
PB6	TF1	
PB7	TK1	
PB8	TD1	
PB9	RD1	
PB10	PCK1	
PB11	(ETH_MDINTR)	
PB12		
PB13	AD0	
PB14	AD1	
PB15	AD2	
PB16	AD3	
PB17	AD4	
PB18	AD5	
PB19	AD6	
PB20	AD7	
PB21	ETXCK	
PB22	ERXDV	
PB23	ETX0	
PB24	ETX1	
PB25	ERX0	
PB26	ERX1	
PB27	ERXER	
PB28	ETXEN	
PB29	EMDC	
PB30	EMDIO	
PB31		

PC[0..31]

PC0	(LCD_PCI)
PC1	LCDHSYNC
PC2	LCDDOTCK
PC3	LCDDEN
PC4	(LCD_IRQ)
PC5	(LCD_BUSY)
PC6	LCDD2
PC7	LCDD3
PC8	LCDD4
PC9	LCDD5
PC10	LCDD6
PC11	LCDD7
PC12	(CANRS)
PC13	
PC14	LCDD10
PC15	LCDD11
PC16	LCDD12
PC17	LCDD13
PC18	LCDD14
PC19	LCDD15
PC20	(MCI0_CD)
PC21	(MCI1_CD)
PC22	LCDD18
PC23	LCDD19
PC24	LCDD20
PC25	LCDD21
PC26	LCDD22
PC27	LCDD23
PC28	PWM0
PC29	PWM2
PC30	DRXD
PC31	DTXD

PD[0..31]

PD0	SPI0_NPCS2
PD1	SPI0_NPCS3
PD2	
PD3	
PD4	
PD5	
PD6	(KBD0)
PD7	(KBD1)
PD8	(KBD2)
PD9	(KBD3)
PD10	(KBD4)
PD11	(KBD5)
PD12	(KBD6)
PD13	(KBD7)
PD14	
PD15	
PD16	
PD17	
PD18	
PD19	
PD20	
PD21	
PD22	
PD23	
PD24	
PD25	
PD26	
PD27	
PD28	
PD29	
PD30	
PD31	

4X4 KEYPADS

ATMEL ROUSSET

AT91CAP-DKM

DIAGRAM

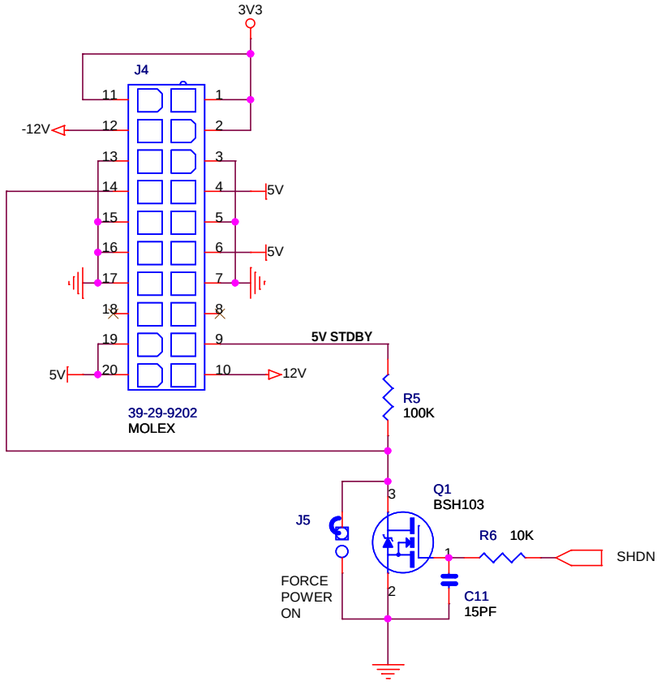
REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	24-APR-07		
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX

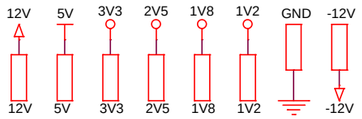
SCALE 1/1

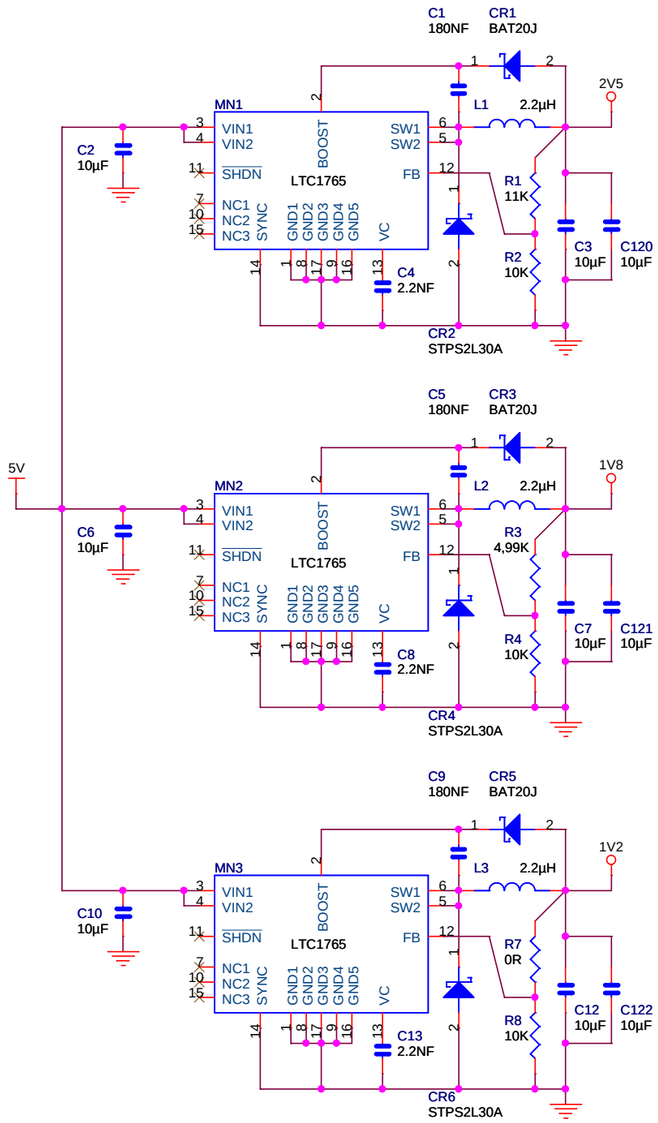
REV. B

SHEET 1/13

ATX POWER SUPPLY







B		JPG	24-APR-07		
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX
REV	MODIF.	DES.	DATE	VER.	DATE

ROUSSET

AT91CAP-DKM

POWER SUPPLY

SCALE 1/1

REV. B

SHEET 2/13

320 pins SAMTEC SEAM-40-02.0-SM-8-2-A-K

VDDIOP1
NRST
HDPA
HDMA
HDPB
HDMB
SHDN
WKUP
PA[0..31]
PB[0..31]
PC[0..31]
PD[0..31]

R172 0R
R173 NOT POPULATED
R174 NOT POPULATED
3V3, 2V5, 1V8 → VCCIO1 → VCCIO1
FPGA BANK1 POWER

R175 0R
R176 NOT POPULATED
R177 NOT POPULATED
3V3, 2V5, 1V8 → VCCIO2 → VCCIO2
FPGA BANK2 POWER

R178 0R
R179 NOT POPULATED
R180 NOT POPULATED
3V3, 2V5, 1V8 → VCCIO3 → VCCIO3
FPGA BANK3 POWER

5V 3V3 2V5 1V8 1V2 GND

FPGA[0..275]

J6-1

1	5V	2	5V	3		4	3V3
9		10		11		12	
17		18		19		20	
25	VDDIOP1	26	VDDIOP1	27		28	1V2
33		34		35		36	
41		42		43		44	
49	VCCIO1	50	VCCIO1	51		52	
57		58		59		60	
65		66		67		68	
73	VCCIO2	74	VCCIO2	75		76	
81		82		83		84	
89		90		91		92	
97	VCCIO3	98	VCCIO3	99		100	
105		106		107		108	
113		114		115		116	
121		122		123		124	
129	PA0	130	PA1	131	PA2	132	PA3
137	PA8	138	PA9	139	PA10	140	PA11
145	PA16	146	PA17	147	PA18	148	PA19
153	PA24	154	PA25	155	PA26	156	PA27
161		162		163		164	
169		170		171		172	
177	PB0	178	PB1	179	PB2	180	PB3
185	PB8	186	PB9	187	PB10	188	PB11
193	PB16	194	PB17	195	PB18	196	PB19
201	PB24	202	PB25	203	PB26	204	PB27
209		210		211		212	
217		218		219		220	
225	PC0	226	PC1	227	PC2	228	PC3
233	PC8	234	PC9	235	PC10	236	PC11
241	PC16	242	PC17	243	PC18	244	PC19
249	PC24	250	PC25	251	PC26	252	PC27
257		258		259		260	
265		266		267		268	
273	PD0	274	PD1	275	PD2	276	PD3
281	PD8	282	PD9	283	PD10	284	PD11
289	PD16	290	PD17	291	PD18	292	PD19
297	PD24	298	PD25	299	PD26	300	PD27
305		306		307		308	
313		314		315		316	

J6-5

5	3V3	6		7	2V5	8	2V5
13		14		15		16	
21		22		23		24	
29	1V2	30		31	1V8	32	1V8
37		38		39		40	
45		46		47		48	
53		54	NRST	55		56	HDPA
61		62		63		64	HDMA
69		70		71		72	
77		78		79		80	HDPB
85		86		87		88	HDMB
93		94		95		96	
101		102		103		104	SHDN
109		110		111		112	WKUP
117		118		119		120	
125		126		127		128	
133	PA4	134	PA5	135	PA6	136	PA7
141	PA12	142	PA13	143	PA14	144	PA15
149	PA20	150	PA21	151	PA22	152	PA23
157	PA28	158	PA29	159	PA30	160	PA31
165		166		167		168	
173		174		175		176	
181	PB4	182	PB5	183	PB6	184	PB7
189	PB12	190	PB13	191	PB14	192	PB15
197	PB20	198	PB21	199	PB22	200	PB23
205	PB28	206	PB29	207	PB30	208	PB31
213		214		215		216	
221		222		223		224	
229	PC4	230	PC5	231	PC6	232	PC7
237	PC12	238	PC13	239	PC14	240	PC15
245	PC20	246	PC21	247	PC22	248	PC23
253	PC28	254	PC29	255	PC30	256	PC31
261		262		263		264	
269		270		271		272	
277	PD4	278	PD5	279	PD6	280	PD7
285	PD12	286	PD13	287	PD14	288	PD15
293	PD20	294	PD21	295	PD22	296	PD23
301	PD28	302	PD29	303	PD30	304	PD31
309		310		311		312	
317		318		319		320	

320 pins SAMTEC SEAM-40-02.0-SM-8-2-A-K

J7-1

1	5V	2	5V	3		4	3V3
9		10		11		12	
17		18		19		20	
25	FPGA0	26	FPGA1	27		28	1V2
33	FPGA2	34	FPGA3	35		36	
41		42		43		44	
49	FPGA4	50	FPGA5	51	FPGA6	52	FPGA7
57	FPGA12	58	FPGA13	59	FPGA14	60	FPGA15
65	FPGA20	66	FPGA21	67	FPGA22	68	FPGA23
73	FPGA28	74	FPGA29	75	FPGA30	76	FPGA31
81	FPGA36	82	FPGA37	83	FPGA38	84	FPGA39
89	FPGA44	90	FPGA45	91	FPGA46	92	FPGA47
97	FPGA52	98	FPGA53	99	FPGA54	100	FPGA55
105	FPGA60	106	FPGA61	107	FPGA62	108	FPGA63
113	FPGA68	114	FPGA69	115	FPGA70	116	FPGA71
121	FPGA76	122	FPGA77	123	FPGA78	124	FPGA79
129	FPGA84	130	FPGA85	131	FPGA86	132	FPGA87
137	FPGA92	138	FPGA93	139	FPGA94	140	FPGA95
145	FPGA100	146	FPGA101	147	FPGA102	148	FPGA103
153	FPGA108	154	FPGA109	155	FPGA110	156	FPGA111
161	FPGA116	162	FPGA117	163	FPGA118	164	FPGA119
169	FPGA124	170	FPGA125	171	FPGA126	172	FPGA127
177	FPGA132	178	FPGA133	179	FPGA134	180	FPGA135
185	FPGA140	186	FPGA141	187	FPGA142	188	FPGA143
193	FPGA148	194	FPGA149	195	FPGA150	196	FPGA151
201	FPGA156	202	FPGA157	203	FPGA158	204	FPGA159
209	FPGA164	210	FPGA165	211	FPGA166	212	FPGA167
217	FPGA172	218	FPGA173	219	FPGA174	220	FPGA175
225	FPGA180	226	FPGA181	227	FPGA182	228	FPGA183
233	FPGA188	234	FPGA189	235	FPGA190	236	FPGA191
241	FPGA196	242	FPGA197	243	FPGA198	244	FPGA199
249	FPGA204	250	FPGA205	251	FPGA206	252	FPGA207
257	FPGA212	258	FPGA213	259	FPGA214	260	FPGA215
265	FPGA220	266	FPGA221	267	FPGA222	268	FPGA223
273	FPGA228	274	FPGA229	275	FPGA230	276	FPGA231
281	FPGA236	282	FPGA237	283	FPGA238	284	FPGA239
289	FPGA244	290	FPGA245	291	FPGA246	292	FPGA247
297	FPGA252	298	FPGA253	299	FPGA254	300	FPGA255
305	FPGA260	306	FPGA261	307	FPGA262	308	FPGA263
313	FPGA268	314	FPGA269	315	FPGA270	316	FPGA271

J7-5

5	3V3	6		7	2V5	8	2V5
13		14		15		16	
21		22		23		24	
29	1V2	30		31	1V8	32	1V8
37		38		39		40	
45		46		47		48	
53	FPGA8	54	FPGA9	55	FPGA10	56	FPGA11
61	FPGA16	62	FPGA17	63	FPGA18	64	FPGA19
69	FPGA24	70	FPGA25	71	FPGA26	72	FPGA27
77	FPGA32	78	FPGA33	79	FPGA34	80	FPGA35
85	FPGA40	86	FPGA41	87	FPGA42	88	FPGA43
93	FPGA48	94	FPGA49	95	FPGA50	96	FPGA51
101	FPGA56	102	FPGA57	103	FPGA58	104	FPGA59
109	FPGA64	110	FPGA65	111	FPGA66	112	FPGA67
117	FPGA72	118	FPGA73	119	FPGA74	120	FPGA75
125	FPGA80	126	FPGA81	127	FPGA82	128	FPGA83
133	FPGA88	134	FPGA89	135	FPGA90	136	FPGA91
141	FPGA96	142	FPGA97	143	FPGA98	144	FPGA99
149	FPGA104	150	FPGA105	151	FPGA106	152	FPGA107
157	FPGA112	158	FPGA113	159	FPGA114	160	FPGA115
165	FPGA120	166	FPGA121	167	FPGA122	168	FPGA123
173	FPGA128	174	FPGA129	175	FPGA130	176	FPGA131
181	FPGA136	182	FPGA137	183	FPGA138	184	FPGA139
189	FPGA144	190	FPGA145	191	FPGA146	192	FPGA147
197	FPGA152	198	FPGA153	199	FPGA154	200	FPGA155
205	FPGA160	206	FPGA161	207	FPGA162	208	FPGA163
213	FPGA168	214	FPGA169	215	FPGA170	216	FPGA171
221	FPGA176	222	FPGA177	223	FPGA178	224	FPGA179
229	FPGA184	230	FPGA185	231	FPGA186	232	FPGA187
237	FPGA192	238	FPGA193	239	FPGA194	240	FPGA195
245	FPGA200	246	FPGA201	247	FPGA202	248	FPGA203
253	FPGA208	254	FPGA209	255	FPGA210	256	FPGA211
261	FPGA216	262	FPGA217	263	FPGA218	264	FPGA219
269	FPGA224	270	FPGA225	271	FPGA226	272	FPGA227
277	FPGA232	278	FPGA233	279	FPGA234	280	FPGA235
285	FPGA240	286	FPGA241	287	FPGA242	288	FPGA243
293	FPGA248	294	FPGA249	295	FPGA250	296	FPGA251
301	FPGA256	302	FPGA257	303	FPGA258	304	FPGA259
309	FPGA264	310	FPGA265	311	FPGA266	312	FPGA267
317	FPGA272	318	FPGA273	319	FPGA274	320	FPGA275

ATMEL ROUSSET

AT91CAP-DKM

MEZZANINE CONNECTORS

REV		DES.	DATE	VER.	DATE
B		JPG	24-APR-07		
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX

SCALE 1/1

REV. B

SHEET 3/13

FPGA[0..275]

NRST

12V 5V GND -12V

12V 5V -12V

200 pins SAMTEC
MALE CONNECTORS
QTT-140-01-S-5

VCCIO1 — VCCIO1

VCCIO2 — VCCIO2

VCCIO3 — VCCIO3

200 pins SAMTEC
FEMALE CONNECTORS
QST-140-02-S-5

J8-1

1	FPGA0	6	FPGA251
11	FPGA6	16	FPGA9
21	FPGA12	26	FPGA15
31	FPGA18	36	FPGA21
41	FPGA24	46	FPGA27
51	FPGA30	56	FPGA33
61	FPGA36	66	FPGA39
71	FPGA42	76	FPGA45
81	FPGA48	86	FPGA51
91	FPGA54	96	NRST
101	FPGA59	106	FPGA62
111	FPGA65	116	FPGA68
121	FPGA71	126	FPGA74
131	FPGA77	136	FPGA80
141	FPGA83	146	FPGA86
151	FPGA89	156	FPGA92
161	FPGA260	166	FPGA98
171	FPGA101	176	FPGA104
181	FPGA107	186	FPGA110
191	FPGA113	196	FPGA116

J8-2

2		7	
12		17	
22		27	
32		37	
42		47	
52		57	
62		67	
72		77	
82		87	
92		97	
102		107	
112		117	
122		127	
132		137	
142		147	
152		157	
162		167	
172		177	
182		187	
192		197	

J8-3

3	FPGA1	8	FPGA4
13	FPGA7	18	FPGA10
23	FPGA13	28	FPGA16
33	FPGA19	38	FPGA22
43	FPGA25	48	FPGA28
53	FPGA31	58	FPGA34
63	FPGA37	68	FPGA40
73	FPGA43	78	FPGA46
83	FPGA49	88	FPGA52
93	FPGA55	98	FPGA57
103	FPGA60	108	FPGA63
113	FPGA66	118	FPGA69
123	FPGA72	128	FPGA75
133	FPGA78	138	FPGA81
143	FPGA84	148	FPGA87
153	FPGA90	158	FPGA93
163	FPGA261	168	FPGA99
173	FPGA102	178	FPGA105
183	FPGA108	188	FPGA111
193	FPGA114	198	FPGA117

J8-4

4		9	
14		19	
24		29	
34		39	
44		49	
54		59	
64		69	
74		79	
84		89	
94		99	
104		109	
114		119	
124		129	
134		139	
144		149	
154		159	
164		169	
174		179	
184		189	
194		199	

J8-5

5	FPGA250	10	FPGA5
15	FPGA8	20	FPGA11
25	FPGA14	30	FPGA17
35	FPGA20	40	FPGA23
45	FPGA26	50	FPGA29
55	FPGA32	60	FPGA35
65	FPGA38	70	FPGA41
75	FPGA44	80	FPGA47
85	FPGA50	90	FPGA53
95	FPGA56	100	FPGA58
105	FPGA61	110	FPGA64
115	FPGA67	120	FPGA70
125	FPGA73	130	FPGA76
135	FPGA79	140	FPGA82
145	FPGA85	150	FPGA88
155	FPGA91	160	FPGA252
165	FPGA262	170	FPGA100
175	FPGA103	180	FPGA106
185	FPGA109	190	FPGA112
195	FPGA115	200	

BANK1

BANK2

J10-1

1	FPGA118	6	FPGA121
11	FPGA124	16	FPGA127
21	FPGA130	26	FPGA133
31	FPGA136	36	FPGA139
41	FPGA142	46	FPGA145
51	FPGA148	56	FPGA151
61	FPGA154	66	FPGA157
71	FPGA160	76	FPGA163
81	FPGA166	86	FPGA169
91	FPGA172	96	FPGA175
101	FPGA178	106	FPGA181
111	FPGA184	116	FPGA187
121	FPGA270	126	FPGA193
131	FPGA196	136	FPGA199
141	FPGA202	146	FPGA205
151	FPGA208	156	FPGA211
161	FPGA214	166	FPGA217
171	FPGA220	176	FPGA223
181	FPGA226	186	
191	VCCIO1	196	

J10-2

2		7	
12		17	
22		27	
32		37	
42		47	
52		57	
62		67	
72		77	
82		87	
92		97	
102		107	
112		117	
122		127	
132		137	
142		147	
152		157	
162		167	
172		177	
182		187	
192		197	

J10-3

3	FPGA119	8	FPGA122
13	FPGA125	18	FPGA128
23	FPGA131	28	FPGA134
33	FPGA137	38	FPGA140
43	FPGA143	48	FPGA146
53	FPGA149	58	FPGA152
63	FPGA155	68	FPGA158
73	FPGA161	78	FPGA164
83	FPGA167	88	FPGA170
93	FPGA173	98	FPGA176
103	FPGA179	108	FPGA182
113	FPGA185	118	FPGA188
123	FPGA191	128	FPGA194
133	FPGA197	138	FPGA200
143	FPGA203	148	FPGA206
153	FPGA209	158	FPGA212
163	FPGA215	168	FPGA218
173	FPGA221	178	FPGA224
183	FPGA227	188	
193	VCCIO2	198	

J10-4

4		9	
14		19	
24		29	
34		39	
44		49	
54		59	
64		69	
74		79	
84		89	
94		99	
104		109	
114		119	
124		129	
134		139	
144		149	
154		159	
164		169	
174		179	
184		189	
194		199	

J10-5

5	FPGA120	10	FPGA123
15	FPGA126	20	FPGA129
25	FPGA132	30	FPGA135
35	FPGA138	40	FPGA141
45	FPGA144	50	FPGA147
55	FPGA150	60	FPGA153
65	FPGA156	70	FPGA159
75	FPGA162	80	FPGA165
85	FPGA168	90	FPGA171
95	FPGA174	100	FPGA177
105	FPGA180	110	FPGA183
115	FPGA186	120	FPGA189
125	FPGA192	130	FPGA195
135	FPGA198	140	FPGA201
145	FPGA204	150	FPGA207
155	FPGA210	160	FPGA213
165	FPGA216	170	FPGA219
175	FPGA222	180	FPGA225
185	FPGA228	190	
195	VCCIO3	200	

BANK3

OPTIONAL PCI POWER SUPPLY

R9
NOT POPULATED
5V — 5VPCI

R10
NOT POPULATED
12V — 12VPCI

R11
NOT POPULATED
-12V — -12VPCI

PCI64 CONNECTORS

FCI
CEE2X92PF-180PY4LF

J9

FPGA179	1	2	-12VPCI
12VPCI	3	4	FPGA176
FPGA177	5	6	
FPGA178	7	8	FPGA175
5VPCI	9	10	
FPGA180	11	12	5VPCI
FPGA182	13	14	FPGA181
5VPCI	15	16	FPGA183
VCCIO2	17	18	FPGA184
	19	20	
	21	22	FPGA185
	23	24	
	25	26	
VCCIO2	27	28	FPGA186
FPGA187	29	30	
	31	32	FPGA190
	33	34	VCCIO2
FPGA189	35	36	FPGA188
VCCIO2	37	38	FPGA191
FPGA192	39	40	
FPGA193	41	42	FPGA194
	43	44	FPGA195
FPGA196	45	46	VCCIO3
FPGA197	47	48	FPGA198
VCCIO3	49	50	FPGA199
FPGA200	51	52	
FPGA201	53	54	FPGA202
	55	56	FPGA203
FPGA204	57	58	VCCIO3
FPGA205	59	60	FPGA206
VCCIO3	61	62	FPGA207
FPGA208	63	64	
	65	66	FPGA209
FPGA210	67	68	VCCIO3
	69	70	FPGA211
FPGA212	71	72	
VCCIO3	73	74	FPGA213
FPGA214	75	76	FPGA215
FPGA216	77	78	VCCIO3
	79	80	FPGA217
FPGA218	81	82	VCCIO3
FPGA219	83	84	FPGA220
VCCIO3	85	86	FPGA221
FPGA222	87	88	
FPGA223	89	90	FPGA224
	91	92	FPGA225
FPGA226	93	94	
	95	96	
	97	98	
FPGA227	99	100	FPGA228
VCCIO3	101	102	FPGA229
FPGA230	103	104	VCCIO3
FPGA231	105	106	FPGA232
	107	108	FPGA233
FPGA234	109	110	
FPGA235	111	112	FPGA236
VCCIO3	113	114	VCCIO3
FPGA237	115	116	FPGA238
	117	118	
5VPCI	119	120	5VPCI
	121	122	
FPGA239	123	124	
FPGA240	125	126	FPGA241
VCCIO3	127	128	FPGA242
FPGA243	129	130	
FPGA244	131	132	FPGA245
	133	134	FPGA246
FPGA247	135	136	VCCIO3
FPGA248	137	138	FPGA249
	139	140	FPGA250
FPGA251	141	142	
FPGA252	143	144	FPGA253
VCCIO3	145	146	FPGA254
FPGA255	147	148	
FPGA256	149	150	FPGA257
	151	152	FPGA258
FPGA259	153	154	VCCIO3
FPGA260	155	156	FPGA261
	157	158	FPGA262
FPGA263	159	160	
FPGA264	161	162	FPGA265
VCCIO3	163	164	FPGA266
FPGA267	165	166	
FPGA268	167	168	FPGA269
	169	170	FPGA270
FPGA271	171	172	VCCIO3
FPGA272	173	174	FPGA273
	175	176	FPGA274
FPGA275	177	178	
	179	180	
	181	182	
	183	184	

BANK2

BANK3

ATMEL ROUSSET

AT91CAP-DKM

FPGA CONNECTORS

REV		DES.	DATE	VER.	DATE
B		JPG	24-APR-07		
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX

SCALE 1/1

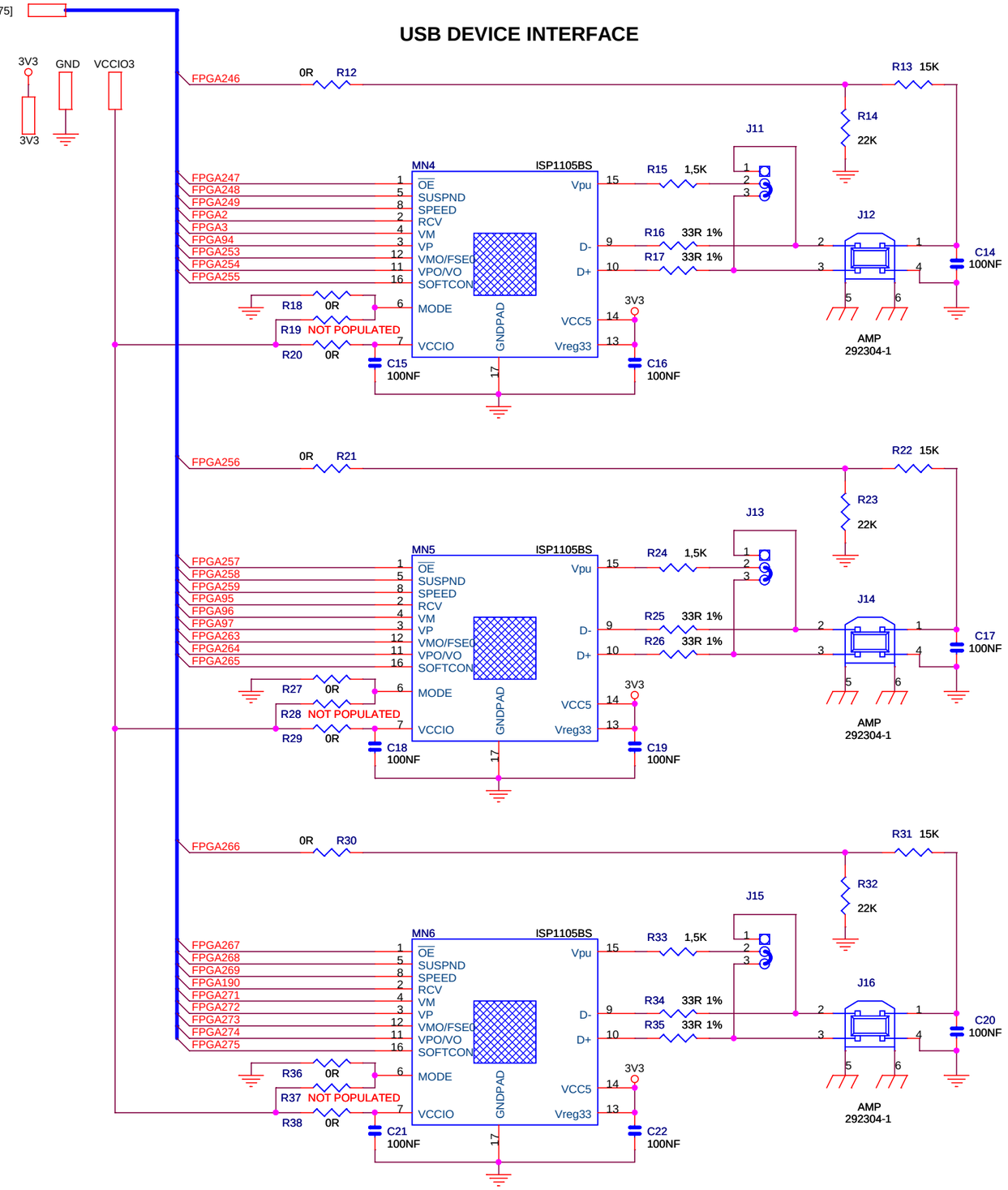
REV. B

SHEET 4/13

FPGA BANK3
Powered by VCCIO3

FPGA[0..275]

USB DEVICE INTERFACE



B		JPG	24-APR-07			
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX	
REV	MODIF.	DES.	DATE	VER.	DATE	

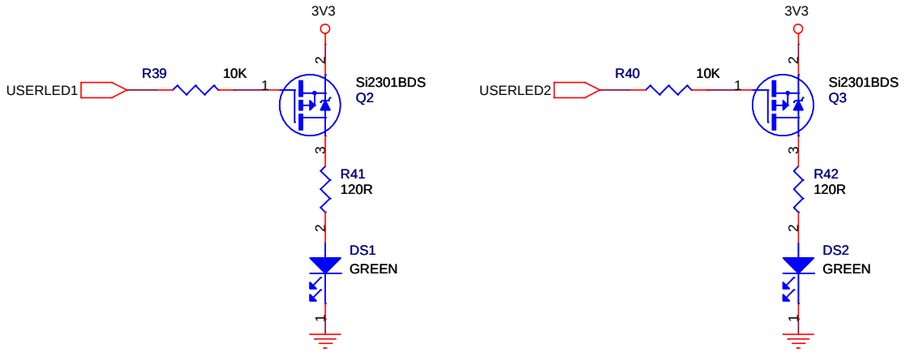
AT91CAP-DKM

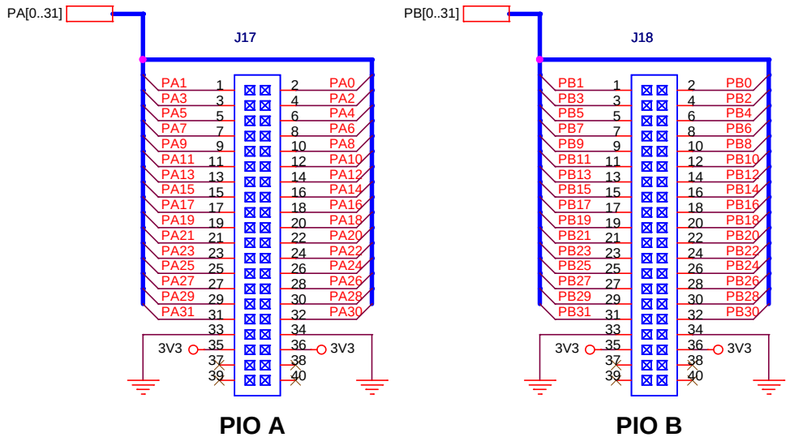
UPSTREAM INTERFACES

SCALE 1/1

REV. B

SHEET 5/13

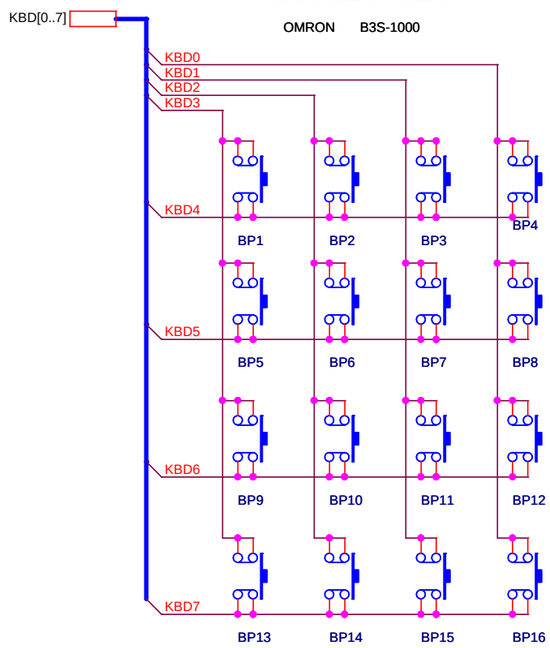


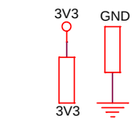


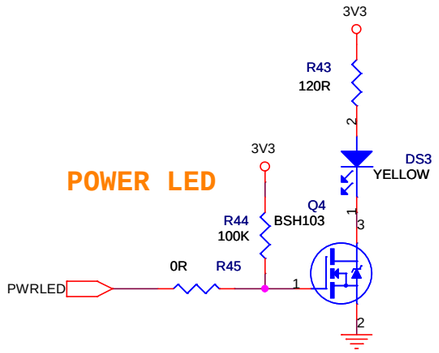
FOUR 40 pins MALE CONNECTORS
SAMTEC TSM-120-01-L-DV

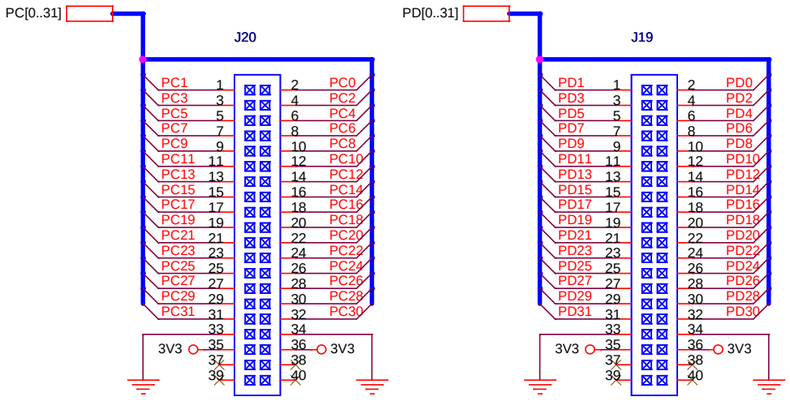
4X4 KEYPADS

OMRON B3S-1000









REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	24-APR-07		
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX

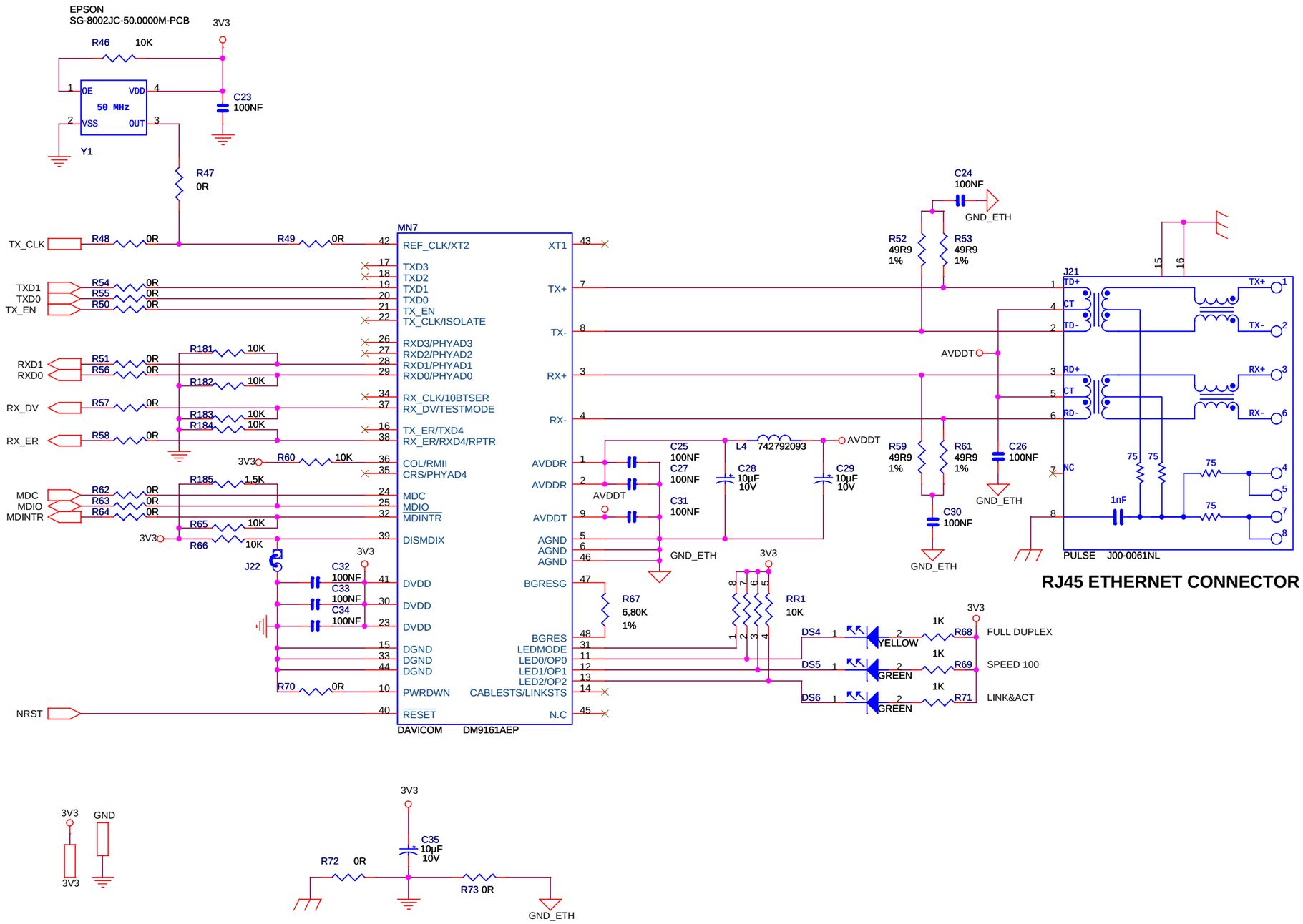
AT91CAP-DKM

USER INTERFACE & PIO

SCALE 1/1

REV. B

SHEET 6/13



RJ45 ETHERNET CONNECTOR

B		JPG	24-APR-07		
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX
REV	MODIF.	DES.	DATE	VER.	DATE

AT91CAP-DKM

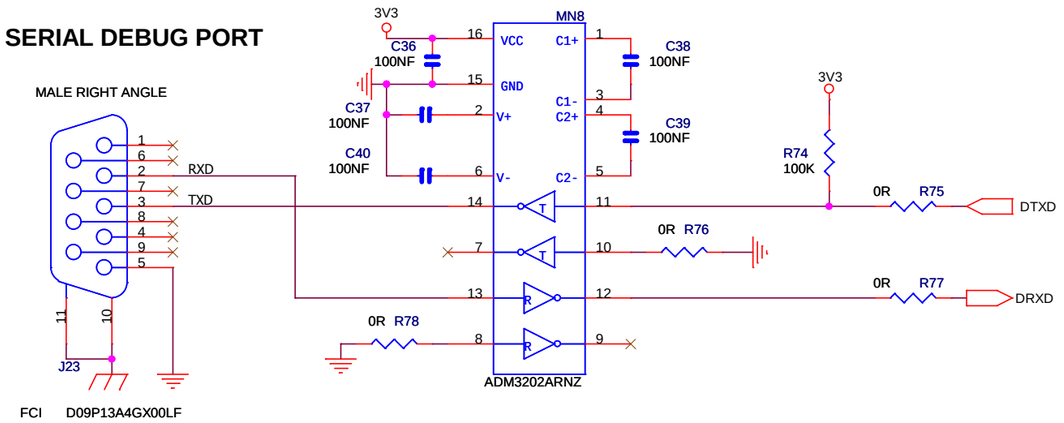
ETHERNET

SCALE 1/1

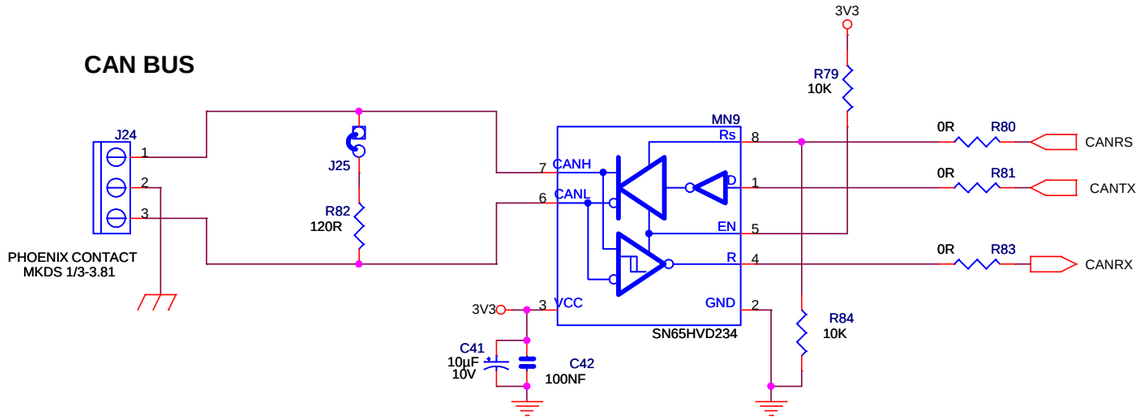
REV. B

SHEET 7/13

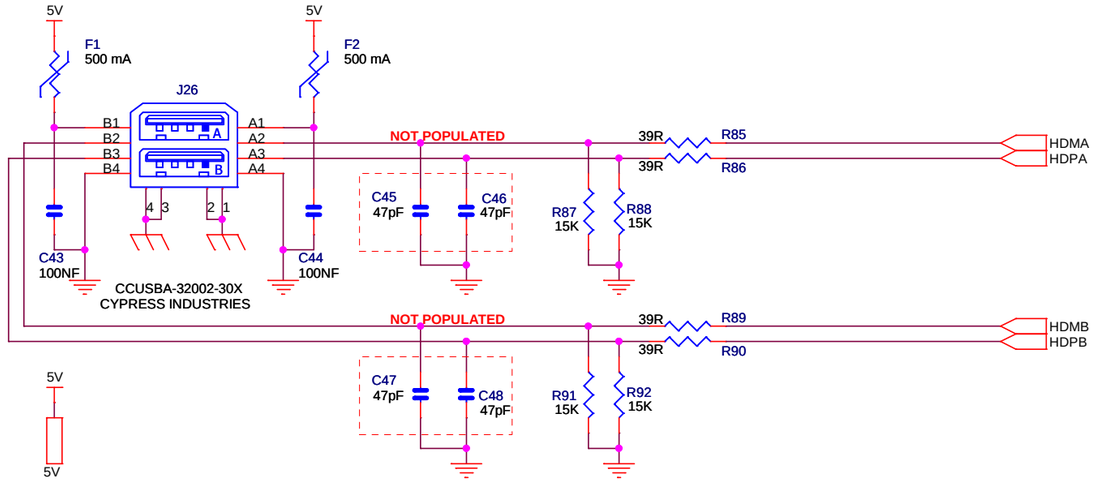
SERIAL DEBUG PORT



CAN BUS



USB HOST INTERFACE



REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	24-APR-07		
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX

AT91CAP-DKM

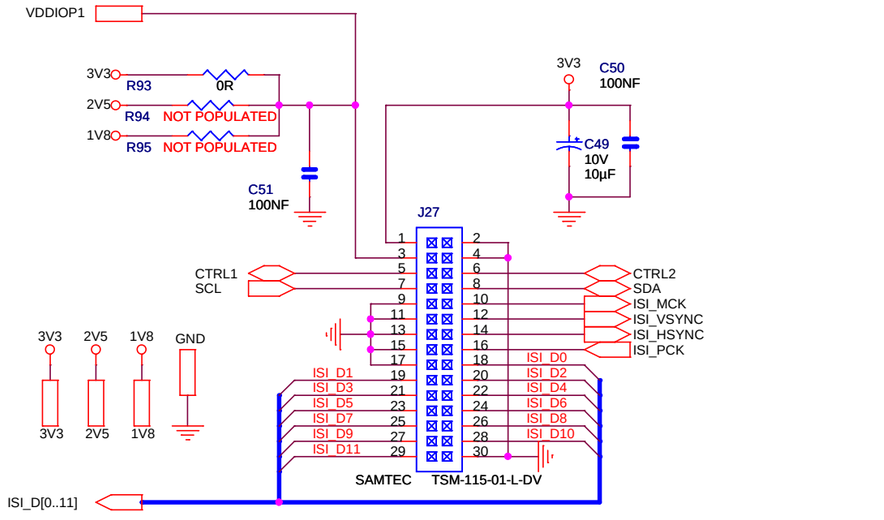
SERIAL INTERFACES

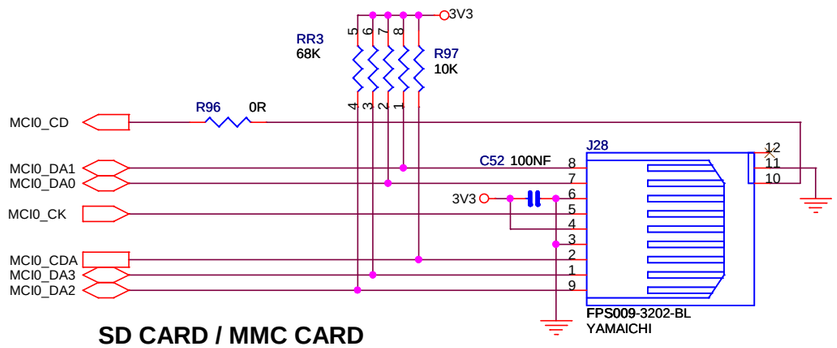
SCALE 1/1

REV. B

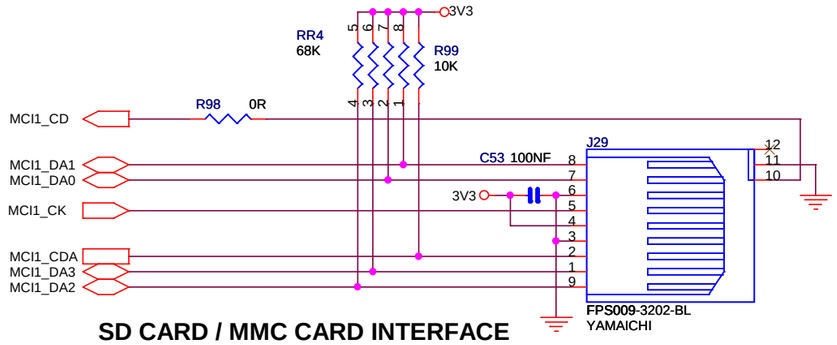
SHEET 8/13

IMAGE SENSOR CONNECTOR

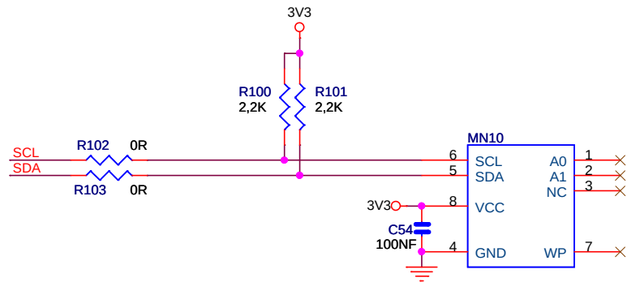




SD CARD / MMC CARD DATAFLASH CARD INTERFACE



SD CARD / MMC CARD INTERFACE



SERIAL EEPROM

REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	24-APR-07		
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX

AT91CAP-DKM

SERIAL DEVICES

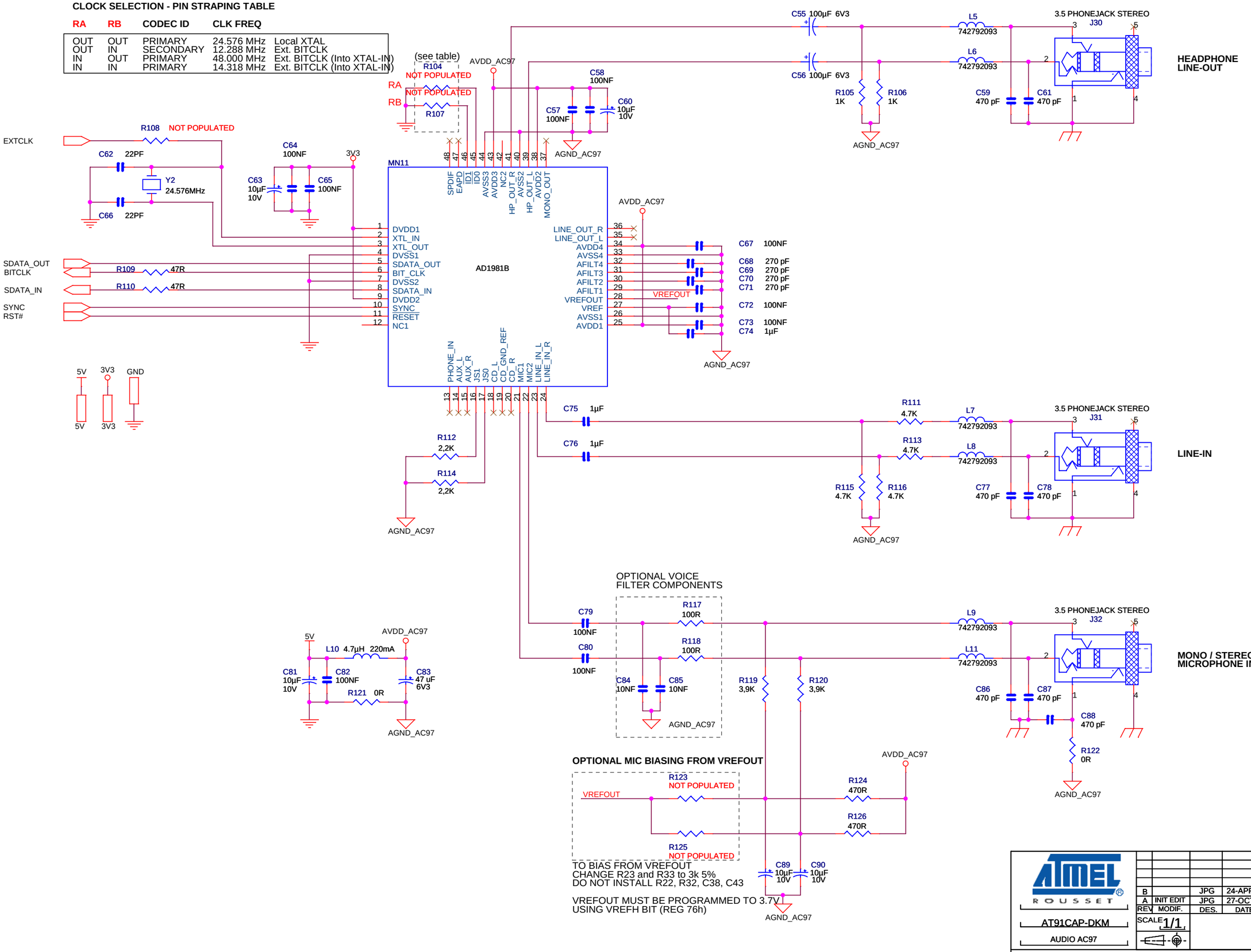
SCALE 1/1

REV. B

SHEET 9/13

CLOCK SELECTION - PIN STRAPING TABLE

RA	RB	CODEC ID	CLK FREQ	
OUT	OUT	PRIMARY	24.576 MHz	Local XTAL
OUT	IN	SECONDARY	12.288 MHz	Ext. BITCLK
IN	OUT	PRIMARY	48.000 MHz	Ext. BITCLK (Into XTAL-IN)
IN	IN	PRIMARY	14.318 MHz	Ext. BITCLK (Into XTAL-IN)



REV		DES.	DATE	VER.	DATE
B		JPG	24-APR-07		
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX

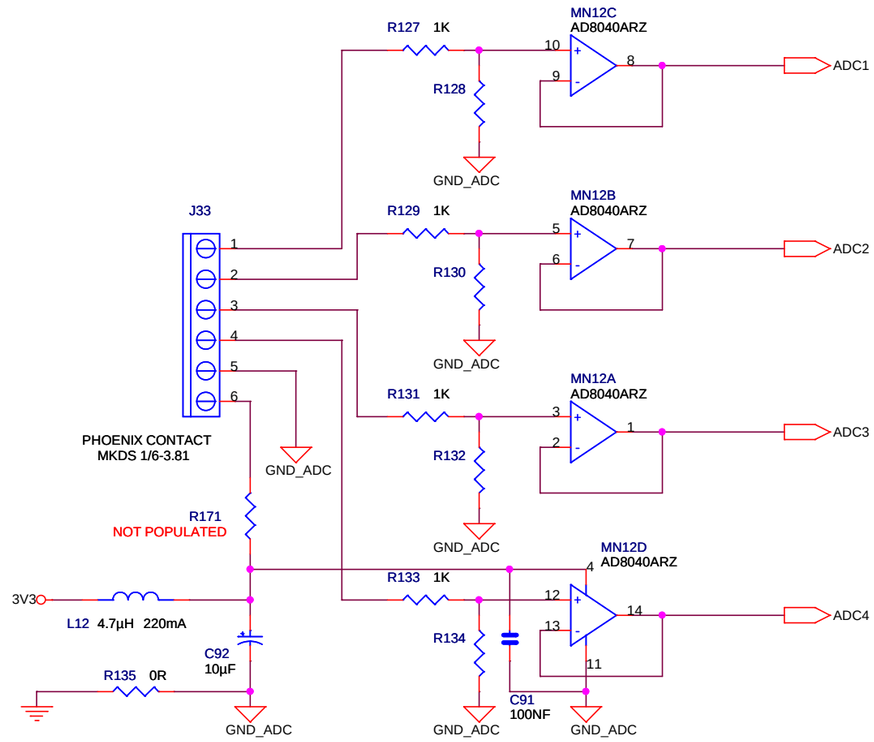
AT91CAP-DKM

AUDIO AC97

SCALE 1/1

REV. B

SHEET 10/13



REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	24-APR-07		
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX

ATMEL ROUSSET

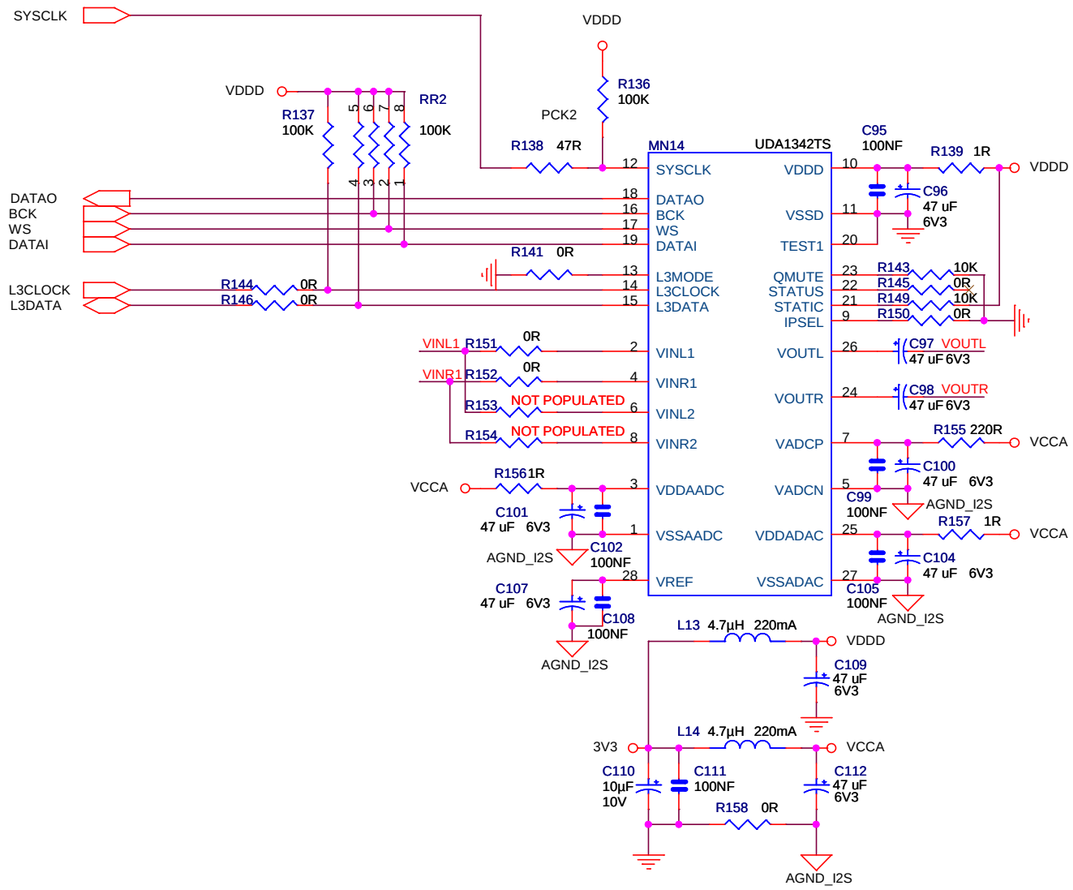
AT91CAP-DKM

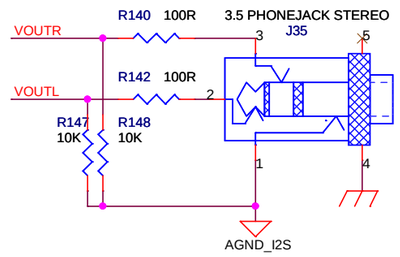
ADC INPUTS

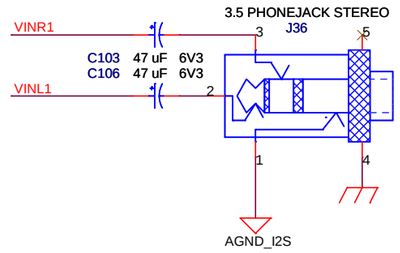
SCALE 1/1

REV. B

SHEET 11/13







B		JPG	24-APR-07		
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX
REV	MODIF.	DES.	DATE	VER.	DATE

ATMEL ROUSSET

AT91CAP-DKM

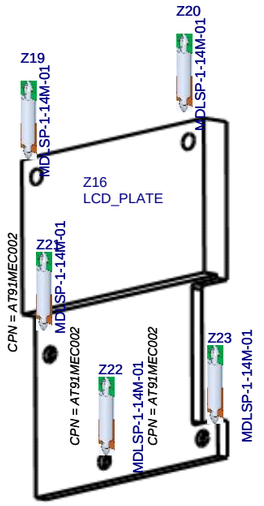
AUDIO I2S

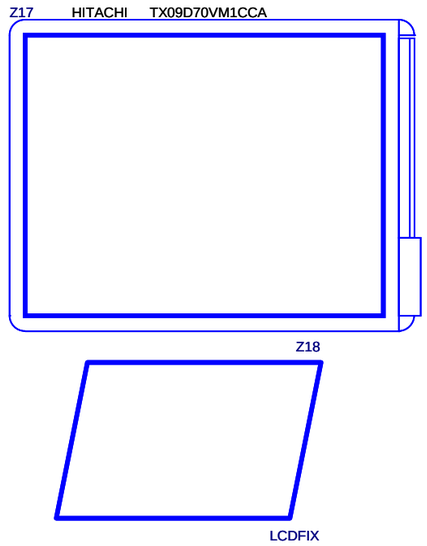
SCALE 1/1

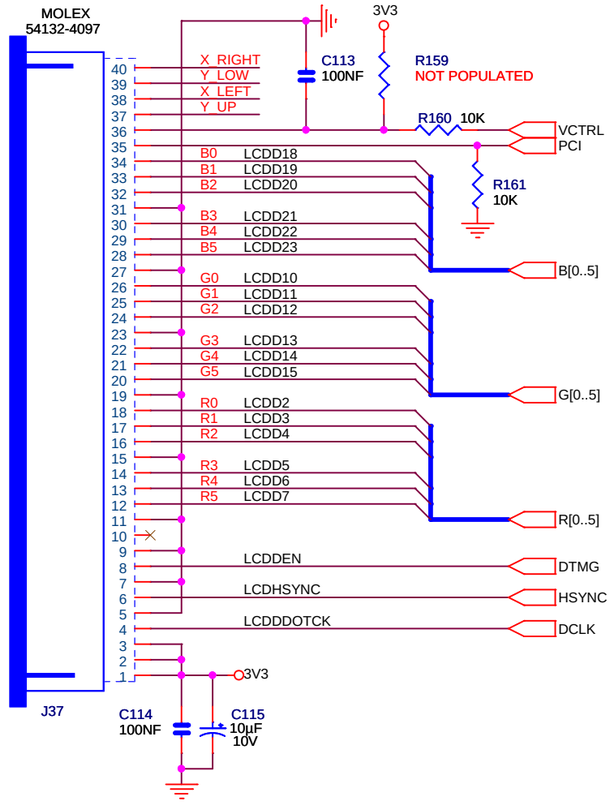
REV. B

SHEET 12/13

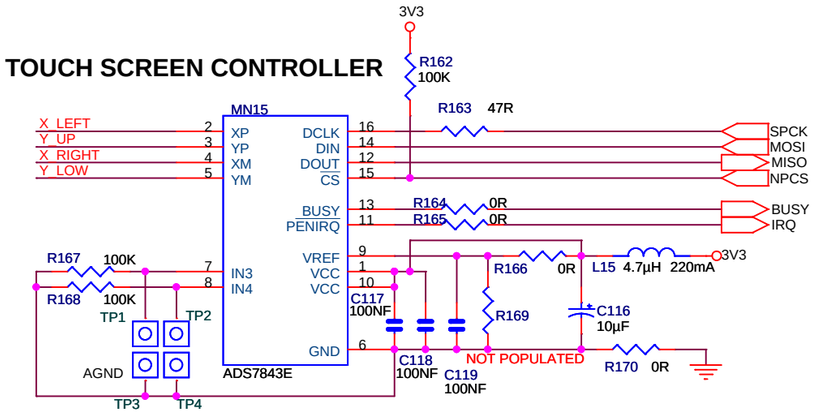
3.5-inch 1/4 VGA TFT LCD DISPLAY



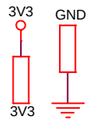




TOUCH SCREEN CONTROLLER



TWO USER'S ANALOG INPUTS
Full-Scale Input Span 0 to VREF



REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	24-APR-07		
A	INIT EDIT	JPG	27-OCT-06	XXX	XX-XXX-XX

ROUSSET

AT91CAP-DKM

LCD PANEL

SCALE 1/1

REV. B

SHEET 13/13

Section 16

AT91CAP9A-DKZ Schematics

16.1 Schematics

This section contains the following appended schematics:

- AT91CAP9A-DKZ Mezzanine Board (Top Level)
- FPGA User I/O Through-hole Grid
- Motherboard Connectors
- FPGA PISMO Connectors
- CAP Power Supply
- CAP Busses
- CAP
  - USB
  - PLL
  - ICE
- CAP SODIMM EBI
- FPGA Power 1/2
- FPGA Power 2/2
- FPGA I/Os
- FPGA I/Os Configuration
  - Banks 1 - 6
- FPGA I/Os Configuration
  - Banks 7 - 8
- FPGA I/Os Configuration
  - JTAG
  - AS Mode
- FPGA SODIMM EBI

TOP LEVEL

PCB1

CAP_SODIMM

J3
page 8

CAP

U2
pages 5, 6, 7

05_AT91CAP

FPGA_SODIMM

J4
page 14

14_FPGA_SODIMM

FPGA

U7
pages 9, 10, 11, 12

09_FPGA

USER_GRID

page 2

02_USER_GRID

MOTHERBOARD CONNECTORS

J1 & J2
page 3

03_MOTHERBOARD_CONNECTORS

PISMO2

J5
page 4

04_PISMO2_CONNECTOR

CONFIG

U8
page 13

13_CONFIG

08_CAP_SODIMM

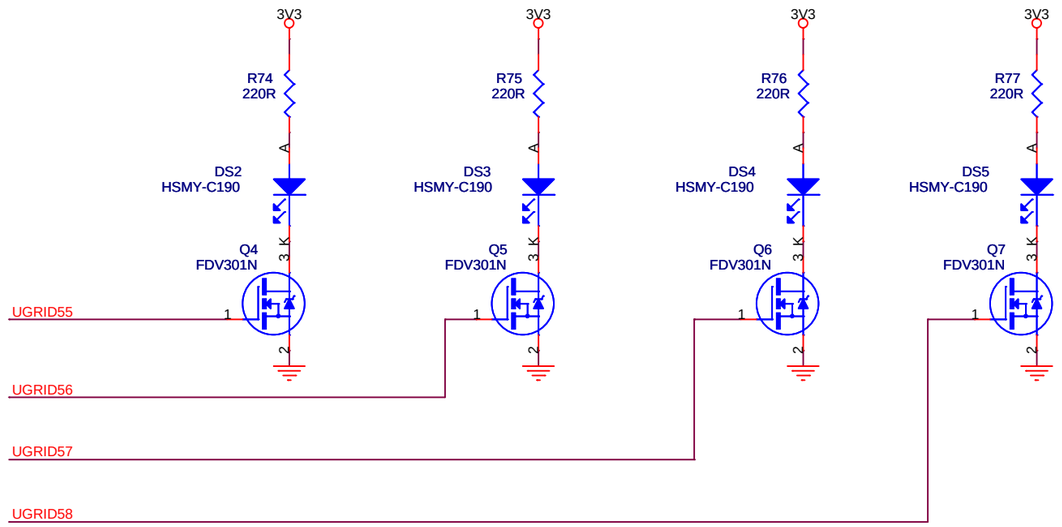
FIDU FD1_2007_05_04_15H00 — FEED = NO
FIDU FD1 — FEED = NO
FIDU FD4 — FEED = NO
FIDU FD2 — FEED = NO
FIDU FD3 — FEED = NO
FIDU FD5 — FEED = NO

REV	MODIF.	DES.	DATE	VER.	DATE
B		YRDE	04-MAY-07		
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06

AT91CAP9A-DKZ
MEZZANINE BOARD
SCALE 1/1
REV. B
SHEET 1/14

FPGA user I/O - through-hole grid

UGRID[0..75]



B		YRDE	04-MAY-07		
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06
REV	MODIF.	DES.	DATE	VER.	DATE

AT91CAP9A-DKZ

MEZZANINE BOARD

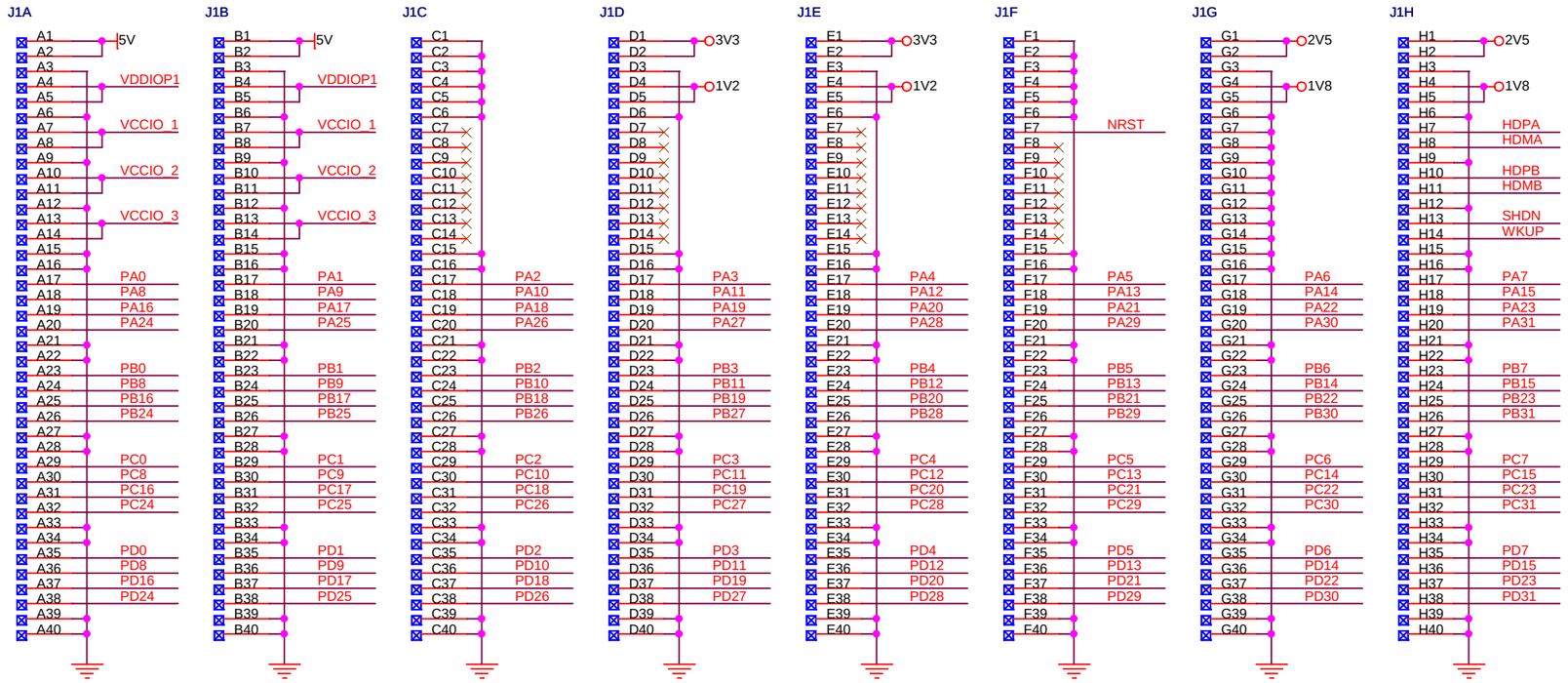
SCALE 1/1

REV. B

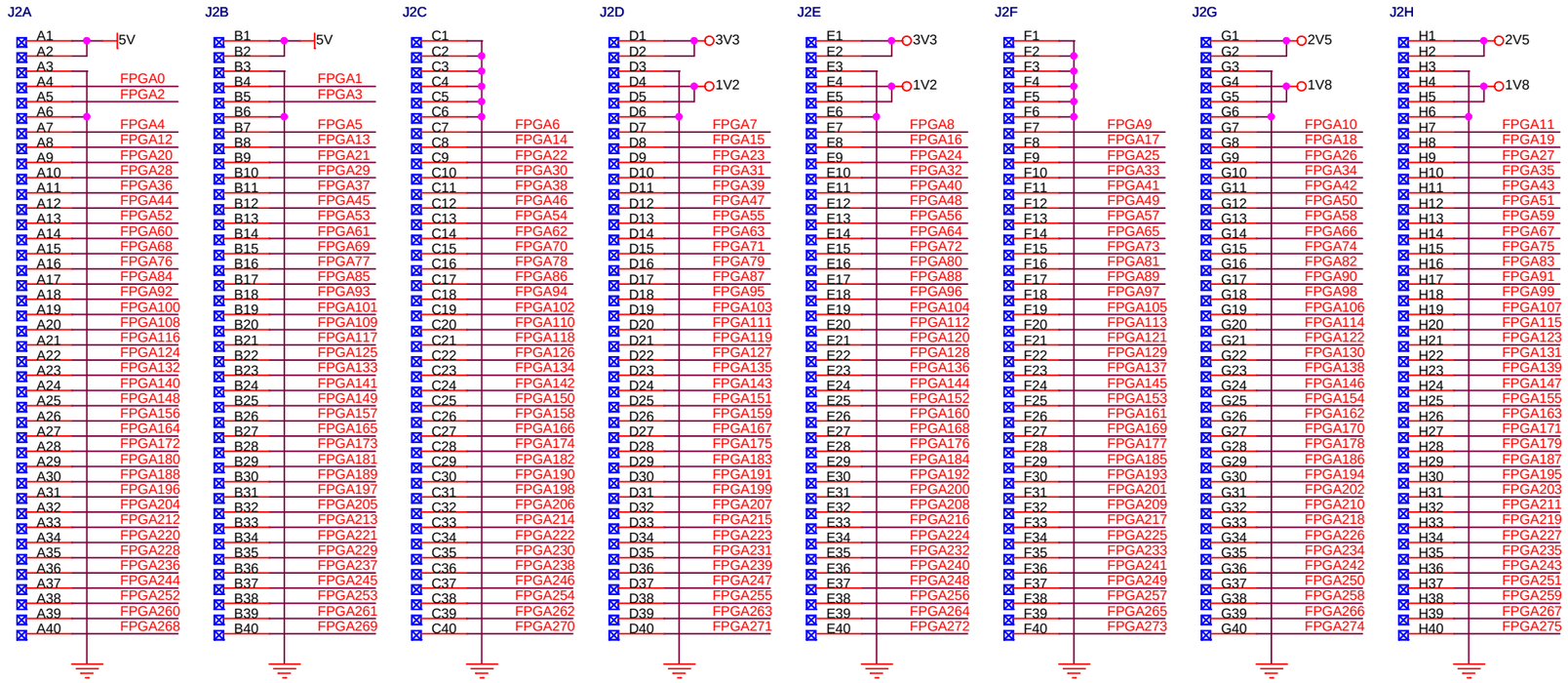
SHEET 2/14

Motherboard connectors

SEAF_40_050_SM_8_2_A_K 320 pins SAMTEC



SEAF_40_050_SM_8_2_A_K 320 pins SAMTEC



REV	MODIF.	DES.	DATE	VER.	DATE
B		YRDE	04-MAY-07		
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06

ATMEL ROUSSET

AT91CAP9A-DKZ

MEZZANINE BOARD

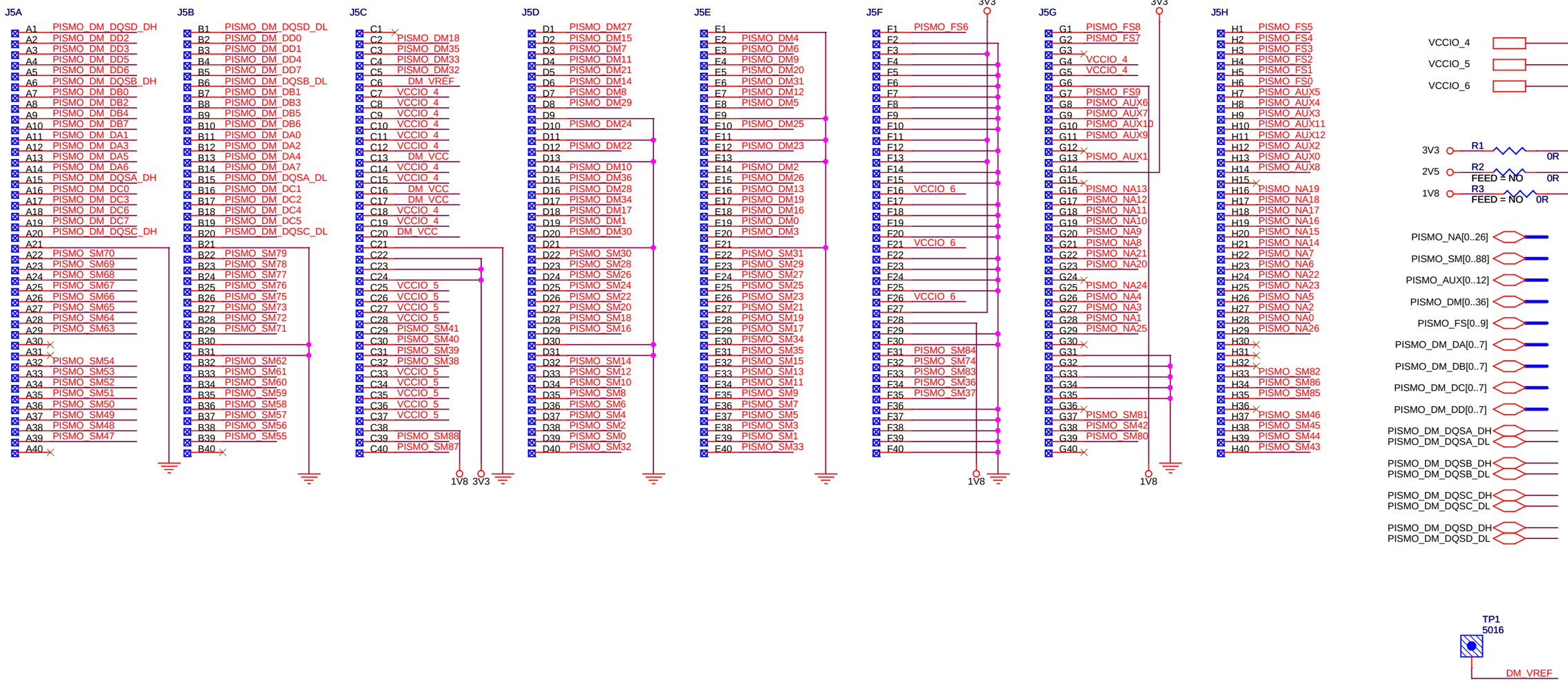
SCALE 1/1

REV. B

SHEET 3/14

FPGA - PISMO connector

SEAF_40_050_SM_8_2_A_K 320 pins SAMTEC



REV	MODIF.	DES.	DATE	VER.	DATE
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A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06

ATMEL ROUSSET

AT91CAP9A-DKZ

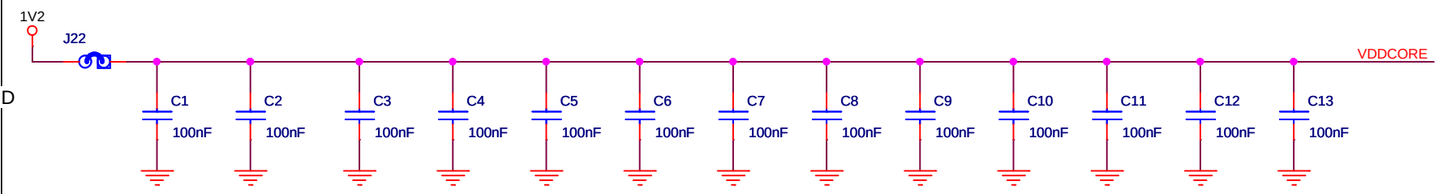
MEZZANINE BOARD

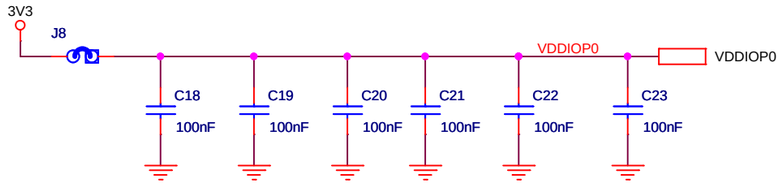
SCALE 1/1

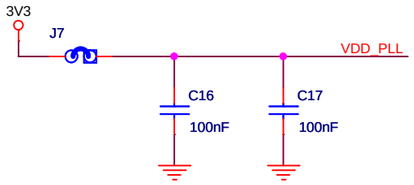
REV. B

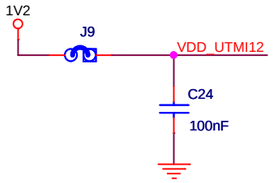
SHEET 4/14

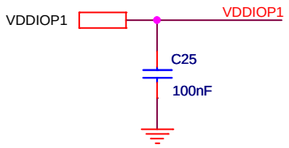
CAP - Power supply

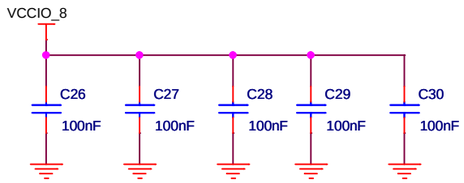


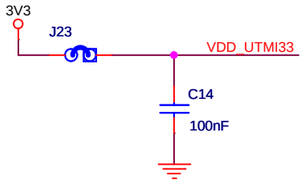


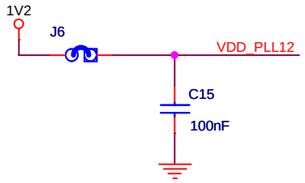


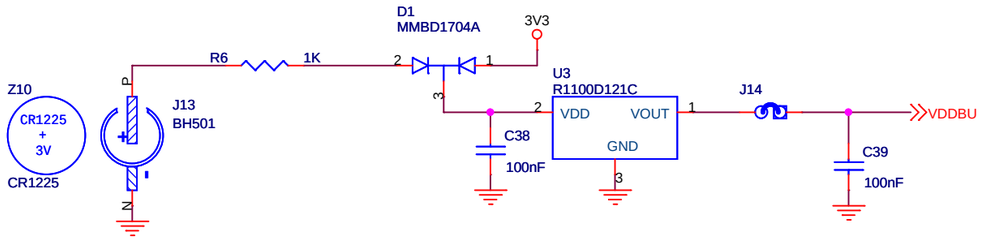


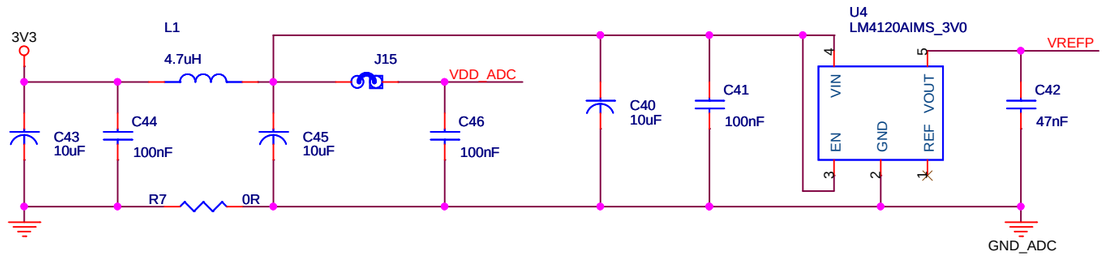


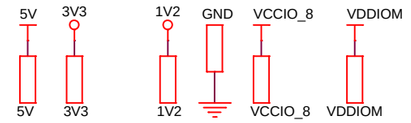


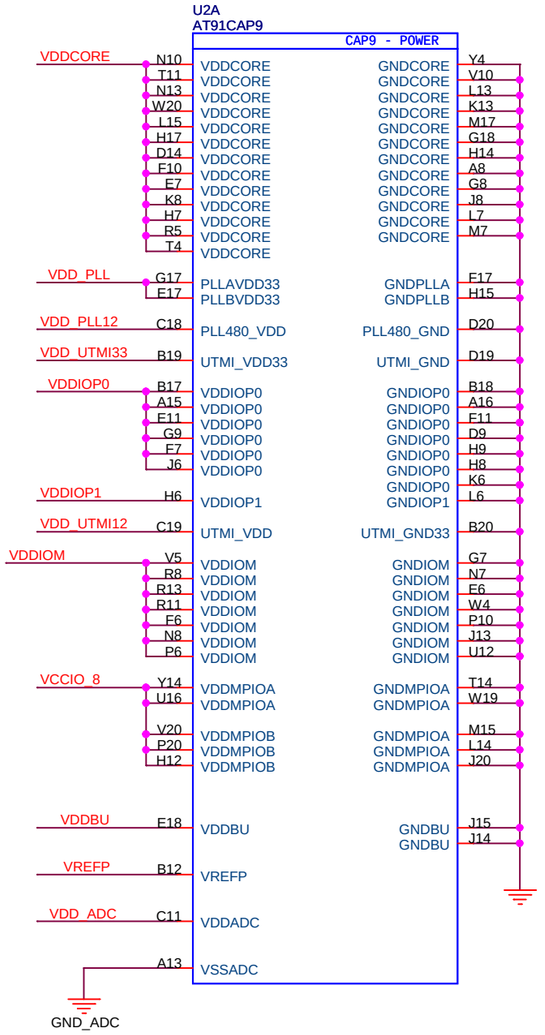












B		YRDE	04-MAY-07			
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06	
REV	MODIF.	DES.	DATE	VER.	DATE	

AT91CAP9A-DKZ

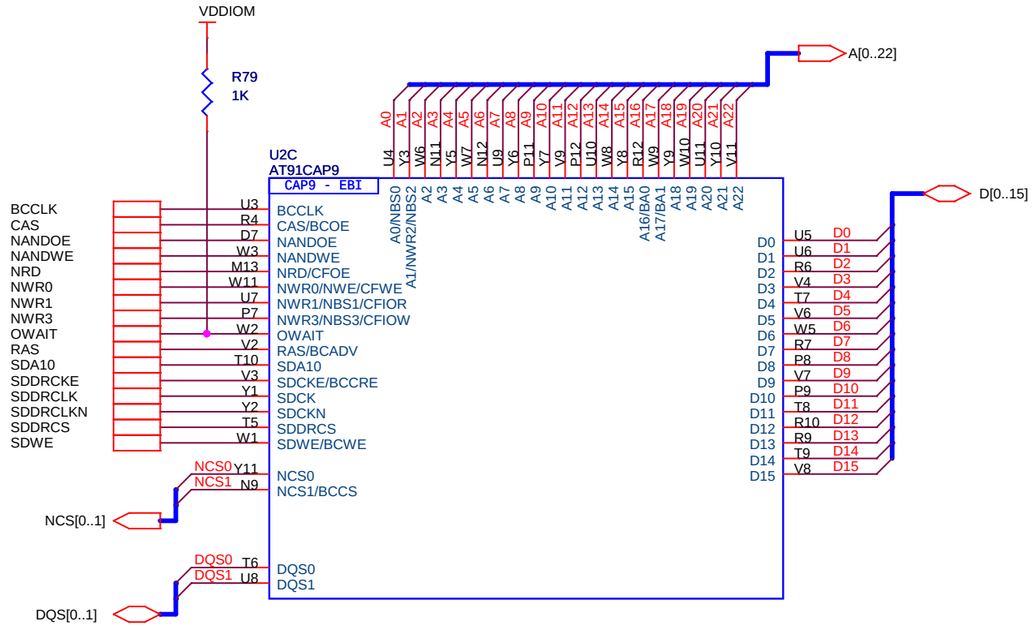
MEZZANINE BOARD

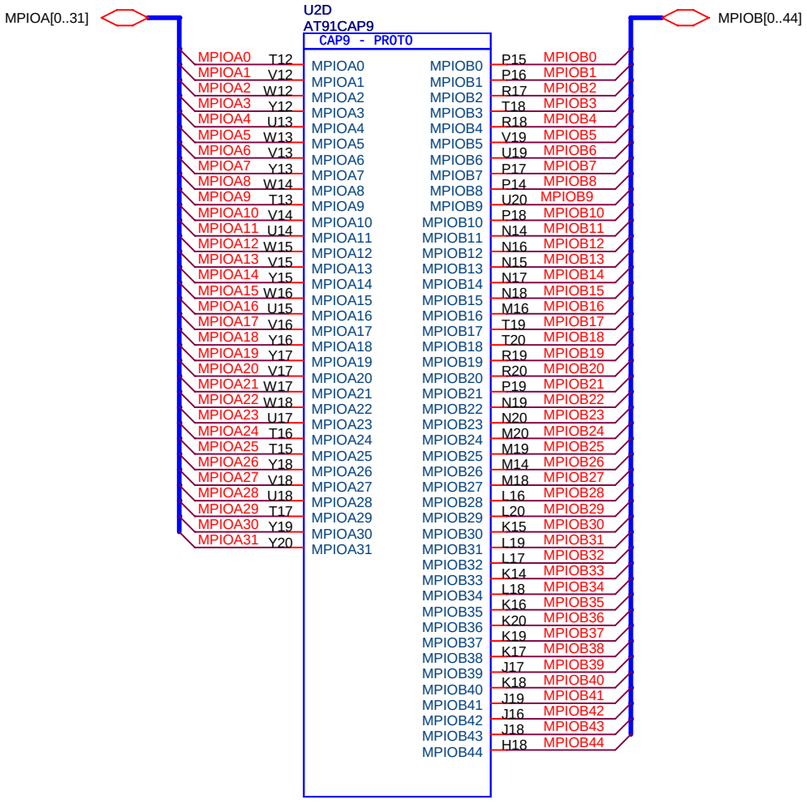
SCALE 1/1

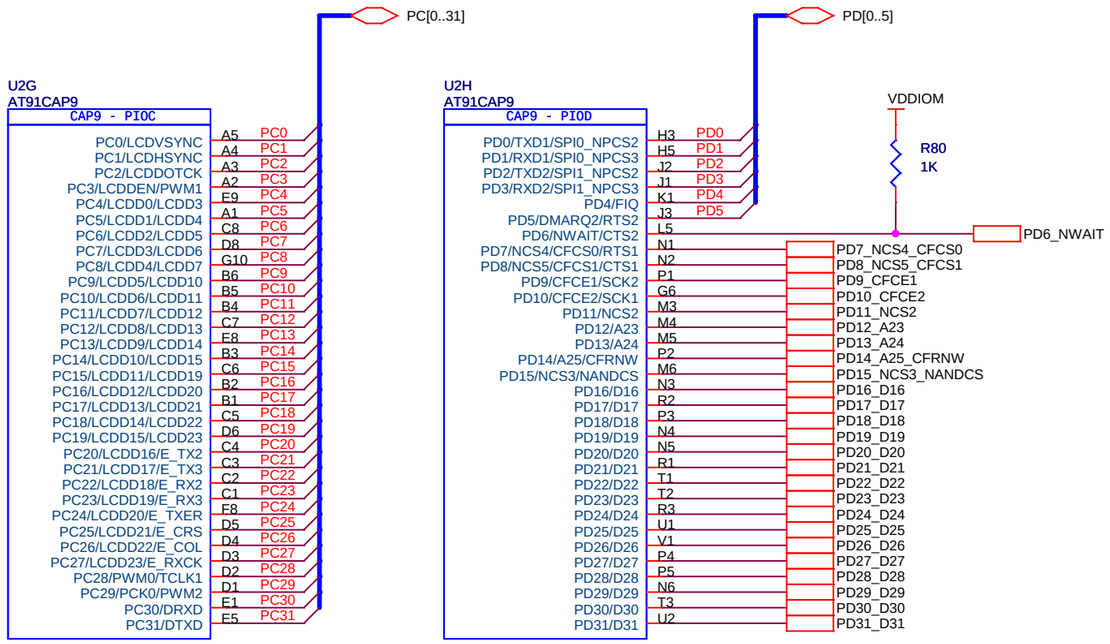
REV. B

SHEET 5/14

CAP - Busses







REV	MODIF.	DES.	DATE	VER.	DATE
B		YRDE	04-MAY-07		
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06

AT91CAP9A-DKZ

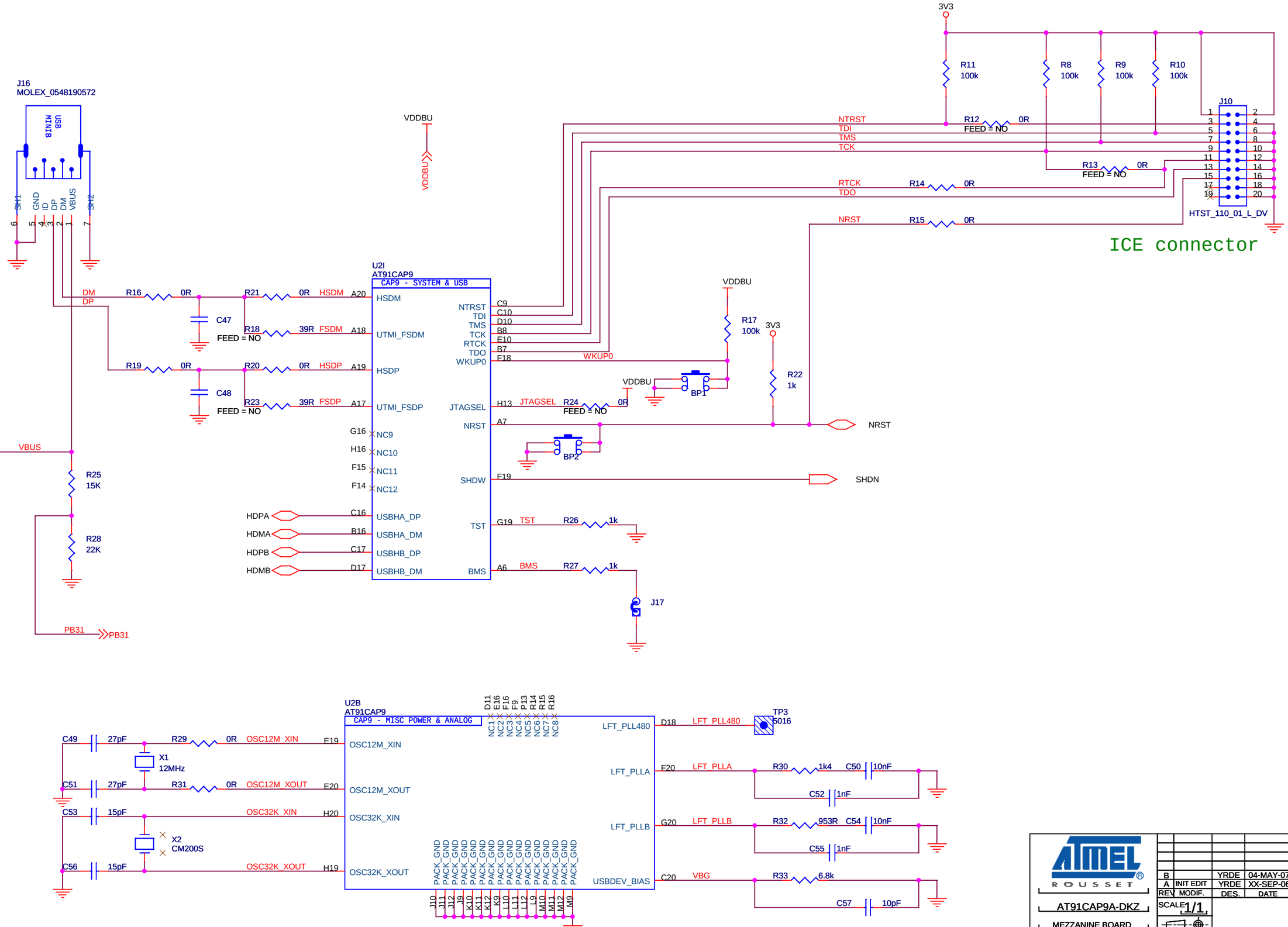
MEZZANINE BOARD

SCALE 1/1

REV. B

SHEET 6/14

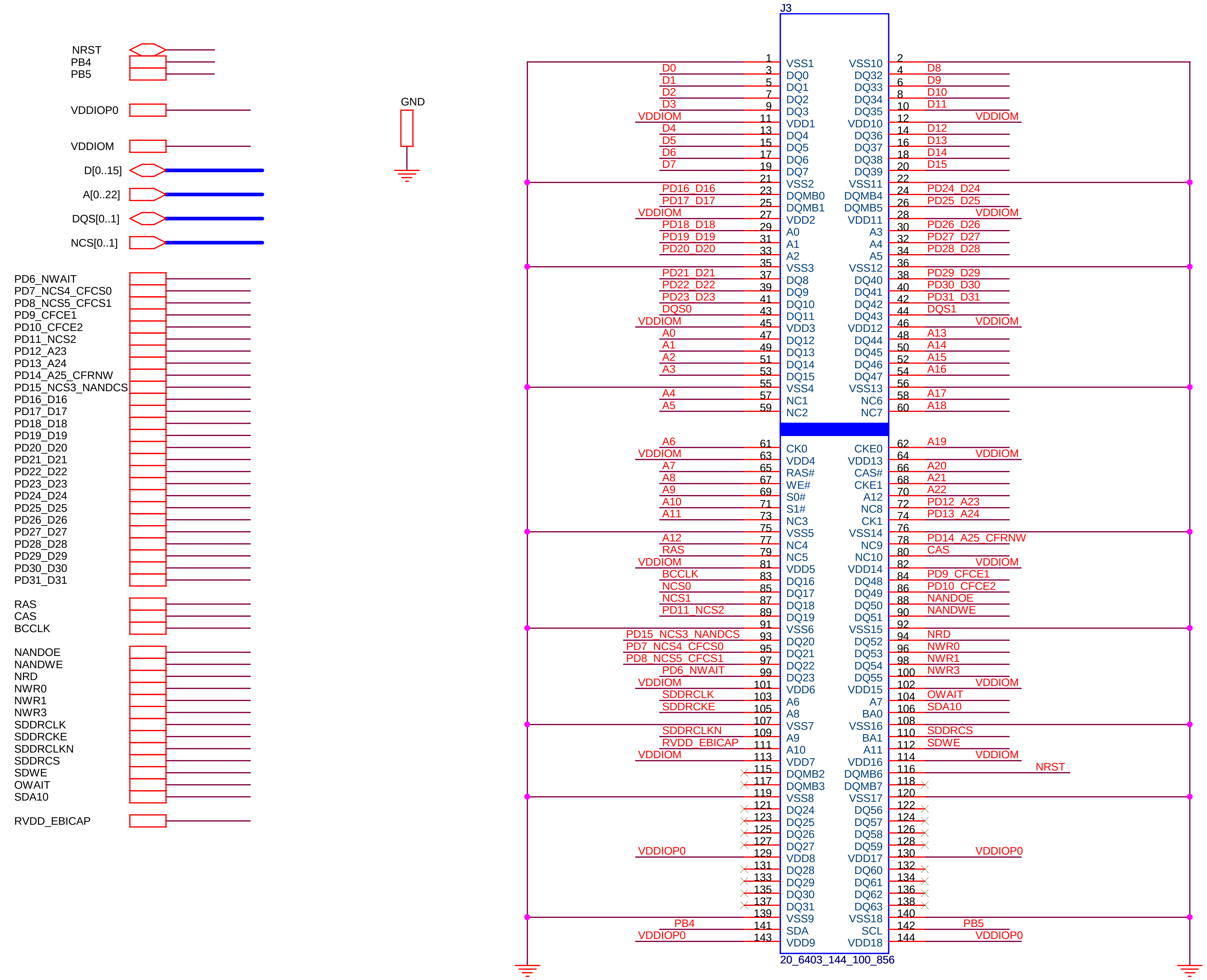
CAP - USB, PLL, ICE



REV	MODIF.	DES.	DATE	VER.	DATE
B		YRDE	04-MAY-07		
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06

AT91CAP9A-DKZ
MEZZANINE BOARD
SCALE 1/1
REV. B
SHEET 7/14

CAP - SODIMM EBI



REV	MODIF.	DES.	DATE	VER.	DATE
B		YRDE	04-MAY-07		
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06

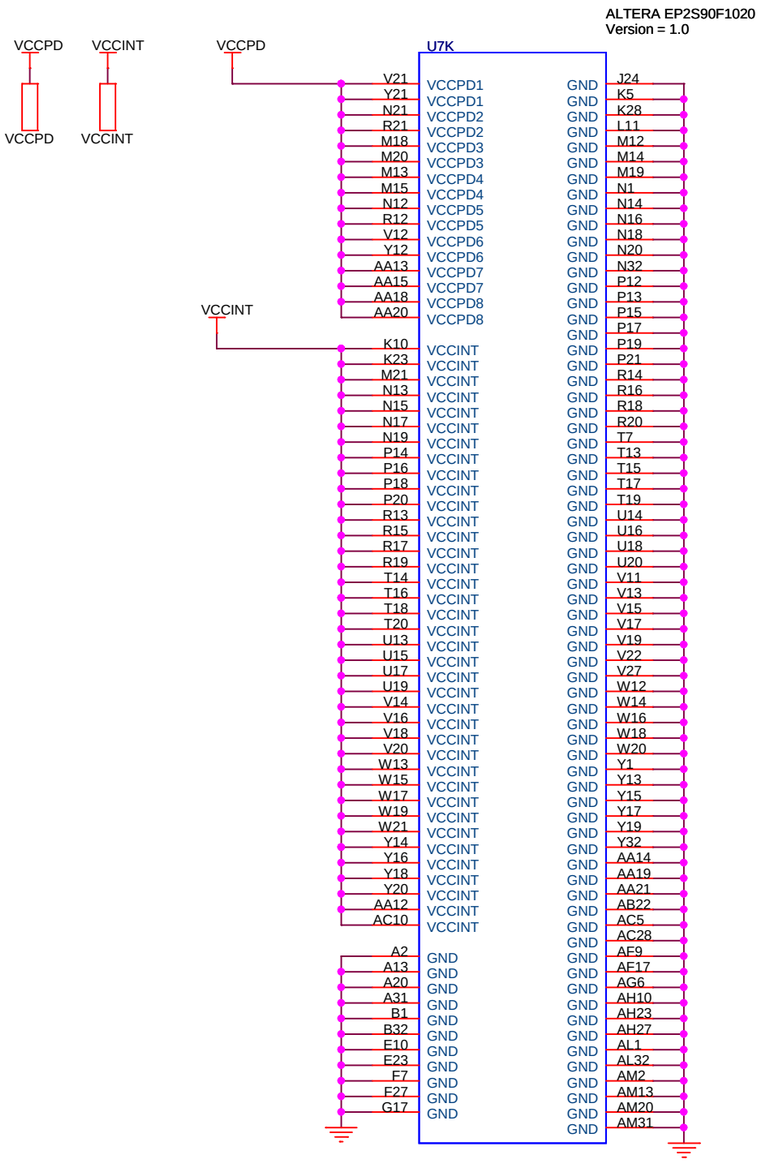
ATMEL ROUSSET

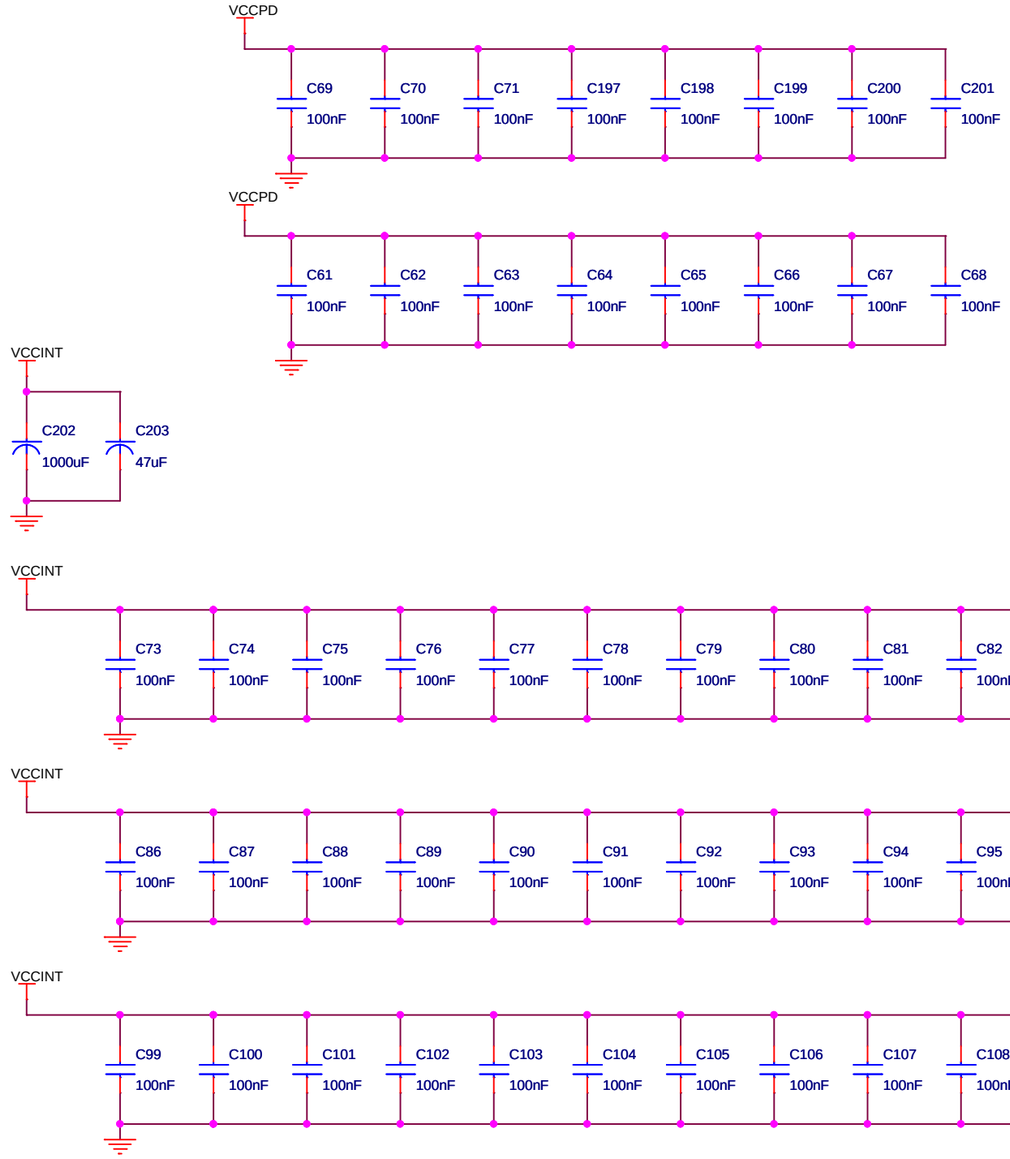
AT91CAP9A-DKZ

MEZZANINE BOARD

SCALE 1/1 | REV. B | SHEET 8/14

FPGA power 1/2





REV	MODIF.	DES.	DATE	VER.	DATE
B		YRDE	04-MAY-07		
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06

ATMEL ROUSSET

AT91CAP9A-DKZ

MEZZANINE BOARD

SCALE 1/1

REV. B

SHEET 9/14

FPGA power 2/2

3V3 C204 1000uF
2V5 C208 1000uF
1V8 C206 1000uF

VCCIO_1: C113 100nF, C114 100nF, C115 100nF, C111 100nF
VCCIO_2: C112 100nF, C116 100nF, C117 100nF, C118 100nF
VCCIO_3: C119 100nF, C120 100nF, C121 100nF, C122 100nF
VCCIO_4: C123 100nF, C124 100nF, C125 100nF, C126 100nF
VCCIO_5: C127 100nF, C128 100nF, C129 100nF, C130 100nF
VCCIO_6: C131 100nF, C132 100nF, C133 100nF, C134 100nF
VCCIO_7: C135 100nF, C136 100nF, C137 100nF, C138 100nF
VCCIO_8: C139 100nF, C140 100nF, C141 100nF, C142 100nF

VCCIO_1 C205 47uF
VCCIO_2 C207 47uF
VCCIO_3 C209 47uF
VCCIO_4 C211 47uF

VCCIO_5 C213 47uF
VCCIO_6 C215 47uF
VCCIO_7 C217 47uF
VCCIO_8 C219 47uF

L2 3V3 220mA → VCC_PLL5: 4.7uH C143, 1uF, C144 2.2uF, C145 100nF, C146 10nF
L3 3V3 → VCC_PLL6: 4.7uH C147, 1uF, C148 2.2uF, C149 100nF, C150 10nF
L4 3V3 220mA → VCC_PLL11: 4.7uH C163, 1uF, C164 2.2uF, C165 100nF, C166 10nF
L5 3V3 → VCC_PLL12: 4.7uH C167, 1uF, C168 2.2uF, C169 100nF, C170 10nF
L6 1V2 220mA → VCCA_PLL: 4.7uH C183, 1uF, C184 2.2uF, C185 100nF, C186 10nF
L7 1V2 → VCCD_PLL: 4.7uH C187, 1uF, C188 2.2uF, C189 100nF, C190 10nF

ALTERA EP2S90F1020
Version = 1.0

U7L

T25	GNDA_PLL1	VREFB1N0	W30
T26	GNDA_PLL1	VREFB1N1	AD28
U25	GNDA_PLL2	VREFB1N2	AG28
U26	GNDA_PLL2	VREFB2N0	F28
U8	GNDA_PLL3	VREFB2N1	J28
V8	GNDA_PLL3	VREFB2N2	P30
R8	GNDA_PLL4	VREFB3N0	C19
T8	GNDA_PLL4	VREFB3N1	D24
G16	GNDA_PLL5	VREFB3N2	C31
H16	GNDA_PLL5	VREFB4N0	C2
AD16	GNDA_PLL6	VREFB4N1	D9
AE16	GNDA_PLL6	VREFB4N2	C14
F26	GNDA_PLL7	VREFB5N0	P3
G26	GNDA_PLL7	VREFB5N1	J5
AG26	GNDA_PLL8	VREFB5N2	F5
AG27	GNDA_PLL8	VREFB6N0	AG5
AE7	GNDA_PLL9	VREFB6N1	AD5
AG7	GNDA_PLL9	VREFB6N2	W3
G7	GNDA_PLL10	VREFB7N0	AK14
G8	GNDA_PLL10	VREFB7N1	AJ9
G18	GNDA_PLL11	VREFB7N2	AK2
H18	GNDA_PLL11	VREFB8N0	AK31
AD17	GNDA_PLL12	VREFB8N1	AJ24
AE17	GNDA_PLL12	VREFB8N2	AK19
J16	VCC_PLL5_OUT		
AF15	VCC_PLL6_OUT		
J17	VCC_PLL11_OUT		
AF16	VCC_PLL12_OUT		
T24	VCCA_PLL1		
V26	VCCA_PLL2		
U9	VCCA_PLL3		
R9	VCCA_PLL4		
G15	VCCA_PLL5		
AE15	VCCA_PLL6		
H26	VCCA_PLL7		
AF26	VCCA_PLL8		
AE7	VCCA_PLL9		
H8	VCCA_PLL10		
H17	VCCA_PLL11		
AF18	VCCA_PLL12		
U24	VCCD_PLL1		
V25	VCCD_PLL2		
U7	VCCD_PLL3		
T9	VCCD_PLL4		
H15	VCCD_PLL5		
AD15	VCCD_PLL6		
H25	VCCD_PLL7		
AF25	VCCD_PLL8		
AE8	VCCD_PLL9		
H7	VCCD_PLL10		
J18	VCCD_PLL11		
AE18	VCCD_PLL12		
B3	TEMPDIODEn		
G9	TEMPDIODEp		
		U21	VCCIO1
		V32	VCCIO1
		AA28	VCCIO1
		AK32	VCCIO1
		C32	VCCIO2
		M28	VCCIO2
		R32	VCCIO2
		T21	VCCIO2
		A18	VCCIO3
		A30	VCCIO3
		E21	VCCIO3
		M17	VCCIO3
		A3	VCCIO4
		A15	VCCIO4
		E12	VCCIO4
		M16	VCCIO4
		C1	VCCIO5
		M5	VCCIO5
		R1	VCCIO5
		T12	VCCIO5
		U12	VCCIO6
		V1	VCCIO6
		AA5	VCCIO6
		AK1	VCCIO6
		AA16	VCCIO7
		AH12	VCCIO7
		AM3	VCCIO7
		AM15	VCCIO7
		AA17	VCCIO7
		AH21	VCCIO8
		AM30	VCCIO8
		AM18	VCCIO8

3V3
VREFB1 R36 0R CPN = AT91RES014
VREFB2 R37 0R CPN = AT91RES014
VREFB3 R38 0R CPN = AT91RES014
VREFB4 R39 0R CPN = AT91RES014
VREFB5 R40 0R CPN = AT91RES014
VREFB6 R41 0R CPN = AT91RES014
VREFB7 R42 0R CPN = AT91RES014
VREFB8 R43 0R CPN = AT91RES014

VCCIO_1
VCCIO_2
VCCIO_3
VCCIO_4
VCCIO_5
VCCIO_6
VCCIO_7
VCCIO_8

GND 3V3 2V5 1V8

VCCIO_1 … VCCIO_8

VCCIO_4: 3V3 R44 0R, 2V5 R45 0R, 1V8 R46 0R — FEED = NO
VCCIO_5: 3V3 R47 0R, 2V5 R48 0R, 1V8 R49 0R — FEED = NO
VCCIO_6: 3V3 R50 0R, 2V5 R51 0R, 1V8 R52 0R — FEED = NO
VCCIO_8: 3V3 R53 0R, 2V5 R54 0R, 1V8 R55 0R — FEED = NO

VCCA_PLL: C151 100nF, C152 1nF, C153 100nF, C154 1nF, C155 100nF, C156 1nF, C157 100nF, C158 1nF, C159 100nF, C160 1nF, C161 100nF, C162 1nF
VCCA_PLL: C171 100nF, C172 1nF, C173 100nF, C174 1nF, C175 100nF, C176 1nF, C177 100nF, C178 1nF, C179 100nF, C180 1nF, C181 100nF, C182 1nF

ATMEL ROUSSET

REV	MODIF.	DES.	DATE	VER.	DATE
B		YRDE	04-MAY-07		
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06

AT91CAP9A-DKZ
MEZZANINE BOARD
SCALE 1/1
REV. B
SHEET 10/14

FPGA I/Os

BANK 1

ALTERA EP2S90F1020
Version = 1.0

U7A

FPGA7	U22	IO_VB1N0_U22			
FPGA6	U23	IO_VB1N0_U23	IO_VB1N1_AB23	AB23	FPGA75
FPGA11	U27	IO_VB1N0_U27	IO_VB1N1_AB24	AB24	FPGA74
FPGA10	U28	IO_VB1N0_U28	IO_VB1N1_AB25	AB25	FPGA67
FPGA19	V23	IO_VB1N0_V23	IO_VB1N1_AB26	AB26	FPGA66
FPGA18	V24	IO_VB1N0_V24	IO_VB1N1_AB27	AB27	FPGA41
FPGA15	V28	IO_VB1N0_V28	IO_VB1N1_AB28	AB28	FPGA40
FPGA14	V29	IO_VB1N0_V29	IO_VB1N1_AC24	AC24	FPGA79
FPGA5	V30	IO_VB1N0_V30	IO_VB1N1_AC25	AC25	FPGA78
FPGA4	V31	IO_VB1N0_V31	IO_VB1N1_AC26	AC26	FPGA55
FPGA31	W24	IO_VB1N0_W24	IO_VB1N1_AC27	AC27	FPGA54
FPGA30	W25	IO_VB1N0_W25	IO_VB1N1_AC29	AC29	FPGA61
FPGA27	W26	IO_VB1N0_W26	IO_VB1N1_AC30	AC30	FPGA60
FPGA26	W27	IO_VB1N0_W27	IO_VB1N1_AD26	AD26	FPGA51
FPGA23	W28	IO_VB1N0_W28	IO_VB1N1_AD27	AD27	FPGA50
FPGA22	W29	IO_VB1N0_W29	IO_VB1N1_AD29	AD29	FPGA65
FPGA9	W31	IO_VB1N0_W31	IO_VB1N1_AD30	AD30	FPGA64
FPGA8	W32	IO_VB1N0_W32	IO_VB1N1_AD31	AD31	FPGA45
FPGA35	Y26	IO_VB1N0_Y26	IO_VB1N1_AD32	AD32	FPGA44
FPGA34	Y27	IO_VB1N0_Y27	IO_VB1N1_AE29	AE29	FPGA73
FPGA29	Y28	IO_VB1N0_Y28	IO_VB1N1_AE30	AE30	FPGA72
FPGA28	Y29	IO_VB1N0_Y29	IO_VB1N1_AE31	AE31	FPGA49
FPGA17	Y30	IO_VB1N0_Y30	IO_VB1N1_AE32	AE32	FPGA48
FPGA16	Y31	IO_VB1N0_Y31	IO_VB1N1_AF31	AE31	FPGA53
FPGA39	AA26	IO_VB1N0_AA26	IO_VB1N1_AF32	AE32	FPGA52
FPGA38	AA27	IO_VB1N0_AA27	IO_VB1N1_AG31	AG31	FPGA57
FPGA25	AA29	IO_VB1N0_AA29	IO_VB1N1_AG32	AG32	FPGA56
FPGA24	AA30	IO_VB1N0_AA30	IO_VB1N1_AH31	AH31	FPGA69
FPGA13	AA31	IO_VB1N0_AA31	IO_VB1N1_AH32	AH32	FPGA68
FPGA12	AA32	IO_VB1N0_AA32	IO_VB1N1_AJ31	AJ31	FPGA77
FPGA33	AB29	IO_VB1N0_AB29	IO_VB1N1_AJ32	AJ32	FPGA76
FPGA32	AB30	IO_VB1N0_AB30			
FPGA21	AB31	IO_VB1N0_AB31	IO_VB1N2_AD24	AD24	FPGA83
FPGA20	AB32	IO_VB1N0_AB32	IO_VB1N2_AD25	AD25	FPGA82
FPGA37	AC31	IO_VB1N0_AC31	IO_VB1N2_AE25	AE25	FPGA87
FPGA36	AC32	IO_VB1N0_AC32	IO_VB1N2_AE26	AE26	FPGA86
			IO_VB1N2_AE27	AE27	FPGA91
FPGA47	W22	IO_VB1N1_W22	IO_VB1N2_AE28	AE28	FPGA90
FPGA46	W23	IO_VB1N1_W23	IO_VB1N2_AF27	AF27	FPGA93
FPGA59	Y22	IO_VB1N1_Y22	IO_VB1N2_AF28	AF28	FPGA92
FPGA58	Y23	IO_VB1N1_Y23	IO_VB1N2_AF29	AF29	FPGA81
FPGA43	Y24	IO_VB1N1_Y24	IO_VB1N2_AF30	AF30	FPGA80
FPGA42	Y25	IO_VB1N1_Y25	IO_VB1N2_AG29	AG29	FPGA85
FPGA71	AA22	IO_VB1N1_AA22	IO_VB1N2_AG30	AG30	FPGA84
FPGA70	AA23	IO_VB1N1_AA23	IO_VB1N2_AH29	AH29	FPGA89
FPGA63	AA24	IO_VB1N1_AA24	IO_VB1N2_AH30	AH30	FPGA88
FPGA62	AA25	IO_VB1N1_AA25			

BANK 2

ALTERA EP2S90F1020
Version = 1.0

U7B

FPGA105	E29	IO_VB2N0_E29			
FPGA104	E30	IO_VB2N0_E30			
FPGA101	G27	IO_VB2N0_G27			
FPGA100	G28	IO_VB2N0_G28			
FPGA103	H27	IO_VB2N0_H27			
FPGA102	H28	IO_VB2N0_H28	IO_VB2N2_K29	K29	FPGA149
FPGA99	K24	IO_VB2N0_K24	IO_VB2N2_K30	K30	FPGA148
FPGA98	K25	IO_VB2N0_K25	IO_VB2N2_K31	K31	FPGA153
FPGA107	K26	IO_VB2N0_K26	IO_VB2N2_K32	K32	FPGA152
FPGA106	K27	IO_VB2N0_K27	IO_VB2N2_L29	L29	FPGA157
			IO_VB2N2_L30	L30	FPGA156
FPGA109	D31	IO_VB2N1_D31	IO_VB2N2_L31	L31	FPGA169
FPGA108	D32	IO_VB2N1_D32	IO_VB2N2_L32	L32	FPGA168
FPGA129	E31	IO_VB2N1_E31	IO_VB2N2_M29	M29	FPGA165
FPGA128	E32	IO_VB2N1_E32	IO_VB2N2_M30	M30	FPGA164
FPGA113	F29	IO_VB2N1_F29	IO_VB2N2_M31	M31	FPGA177
FPGA112	F30	IO_VB2N1_F30	IO_VB2N2_M32	M32	FPGA176
FPGA133	F31	IO_VB2N1_F31	IO_VB2N2_N26	N26	FPGA151
FPGA132	F32	IO_VB2N1_F32	IO_VB2N2_N27	N27	FPGA150
FPGA117	G29	IO_VB2N1_G29	IO_VB2N2_N28	N28	FPGA161
FPGA116	G30	IO_VB2N1_G30	IO_VB2N2_N29	N29	FPGA160
FPGA137	G31	IO_VB2N1_G31	IO_VB2N2_N30	N30	FPGA173
FPGA136	G32	IO_VB2N1_G32	IO_VB2N2_N31	N31	FPGA172
FPGA121	H29	IO_VB2N1_H29	IO_VB2N2_P24	P24	FPGA163
FPGA120	H30	IO_VB2N1_H30	IO_VB2N2_P25	P25	FPGA162
FPGA141	H31	IO_VB2N1_H31	IO_VB2N2_P26	P26	FPGA159
FPGA140	H32	IO_VB2N1_H32	IO_VB2N2_P27	P27	FPGA158
FPGA111	J26	IO_VB2N1_J26	IO_VB2N2_P28	P28	FPGA155
FPGA110	J27	IO_VB2N1_J27	IO_VB2N2_P29	P29	FPGA154
FPGA125	J29	IO_VB2N1_J29	IO_VB2N2_P31	P31	FPGA181
FPGA124	J30	IO_VB2N1_J30	IO_VB2N2_P32	P32	FPGA180
FPGA145	J31	IO_VB2N1_J31	IO_VB2N2_R22	R22	FPGA171
FPGA144	J32	IO_VB2N1_J32	IO_VB2N2_R23	R23	FPGA170
FPGA123	L23	IO_VB2N1_L23	IO_VB2N2_R24	R24	FPGA191
FPGA122	L24	IO_VB2N1_L24	IO_VB2N2_R25	R25	FPGA174
FPGA119	L25	IO_VB2N1_L25	IO_VB2N2_R26	R26	FPGA167
FPGA118	L26	IO_VB2N1_L26	IO_VB2N2_R27	R27	FPGA166
FPGA115	L27	IO_VB2N1_L27	IO_VB2N2_R28	R28	FPGA179
FPGA114	L28	IO_VB2N1_L28	IO_VB2N2_R29	R29	FPGA178
FPGA131	M22	IO_VB2N1_M22	IO_VB2N2_R30	R30	FPGA185
FPGA130	M23	IO_VB2N1_M23	IO_VB2N2_R31	R31	FPGA184
FPGA127	M24	IO_VB2N1_M24	IO_VB2N2_T22	T22	FPGA187
FPGA126	M25	IO_VB2N1_M25	IO_VB2N2_T23	T23	FPGA186
FPGA135	M26	IO_VB2N1_M26	IO_VB2N2_T27	T27	FPGA183
FPGA134	M27	IO_VB2N1_M27	IO_VB2N2_T28	T28	FPGA182
FPGA143	N22	IO_VB2N1_N22			
FPGA142	N23	IO_VB2N1_N23			
FPGA139	N24	IO_VB2N1_N24			
FPGA138	N25	IO_VB2N1_N25			
FPGA147	P22	IO_VB2N1_P22			
FPGA146	P23	IO_VB2N1_P23			

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FPGA213	A21	IO_VB3N0_A21	IO_VB3N1_D25	D25	FPGA245
FPGA215	A22	IO_VB3N0_A22	IO_VB3N1_D26	D26	FPGA241
FPGA203	B20	IO_VB3N0_B20	IO_VB3N1_E22	E22	FPGA225
FPGA212	B21	IO_VB3N0_B21	IO_VB3N1_E24	E24	FPGA246
FPGA216	B22	IO_VB3N0_B22	IO_VB3N1_E27	E27	FPGA248
FPGA205	C20	IO_VB3N0_C20	IO_VB3N1_F22	F22	FPGA224
FPGA214	C21	IO_VB3N0_C21	IO_VB3N1_F23	F23	FPGA226
FPGA217	C22	IO_VB3N0_C22	IO_VB3N1_G21	G21	FPGA244
FPGA202	D19	IO_VB3N0_D19	IO_VB3N1_H20	H20	FPGA219
FPGA206	D20	IO_VB3N0_D20	IO_VB3N1_H21	H21	FPGA236
FPGA204	E19	IO_VB3N0_E19	IO_VB3N1_J20	J20	FPGA228
FPGA207	E20	IO_VB3N0_E20	IO_VB3N1_J21	J21	FPGA237
	F17	IO_VB3N0_F17	IO_VB3N1_K20	K20	FPGA220
	G19	IO_VB3N0_G19	IO_VB3N1_K21	K21	FPGA235
FPGA210	J19	IO_VB3N0_J19	IO_VB3N1_L21	L21	FPGA227
FPGA196	K18	IO_VB3N0_K18			
FPGA211	K19	IO_VB3N0_K19	IO_VB3N2_A27	A27	FPGA253
FPGA209	L18	IO_VB3N0_L18	IO_VB3N2_A28	A28	FPGA254
FPGA208	L19	IO_VB3N0_L19	IO_VB3N2_A29	A29	FPGA262
FPGA218	L20	IO_VB3N0_L20	IO_VB3N2_B27	B27	FPGA252
			IO_VB3N2_B28	B28	FPGA256
FPGA230	A23	IO_VB3N1_A23	IO_VB3N2_B29	B29	FPGA261
FPGA234	A24	IO_VB3N1_A24	IO_VB3N2_C27	C27	FPGA257
FPGA239	A25	IO_VB3N1_A25	IO_VB3N2_C28	C28	FPGA260
FPGA240	A26	IO_VB3N1_A26	IO_VB3N2_C29	C29	FPGA264
FPGA229	B23	IO_VB3N1_B23	IO_VB3N2_D27	D27	FPGA255
FPGA233	B24	IO_VB3N1_B24	IO_VB3N2_D28	D28	FPGA263
FPGA238	B25	IO_VB3N1_B25	IO_VB3N2_E25	E25	FPGA249
FPGA242	B26	IO_VB3N1_B26	IO_VB3N2_E26	E26	FPGA250
FPGA231	C23	IO_VB3N1_C23	IO_VB3N2_E28	E28	FPGA265
FPGA232	C24	IO_VB3N1_C24	IO_VB3N2_F21	F21	FPGA251
FPGA247	C25	IO_VB3N1_C25	IO_VB3N2_F25	F25	FPGA267
FPGA243	C26	IO_VB3N1_C26	IO_VB3N2_G22	G22	FPGA268
FPGA223	D21	IO_VB3N1_D21	IO_VB3N2_H22	H22	FPGA258
FPGA221	D22	IO_VB3N1_D22	IO_VB3N2_J22	J22	FPGA259
FPGA222	D23	IO_VB3N1_D23	IO_VB3N2_K22	K22	FPGA266

ASDO
nCSO

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U7D

PISMO_DM_DA3	A4	IO_VB4N0_A4	IO_VB4N1_D11	D11	PISMO_DM20
PISMO_DM_DA4	A5	IO_VB4N0_A5	IO_VB4N1_D12	D12	PISMO_DM_DD5
PISMO_DM9	A6	IO_VB4N0_A6	IO_VB4N1_E8	E8	PISMO_DM_DC1
PISMO_DM_DB3	A7	IO_VB4N0_A7	IO_VB4N1_E9	E9	PISMO_DM_DQSC_DL
PISMO_DM_DA0	B4	IO_VB4N0_B4	IO_VB4N1_E11	E11	PISMO_DM_DD0
PISMO_DM8	B5	IO_VB4N0_B5	IO_VB4N1_F8	F8	PISMO_DM_DC2
PISMO_DM_DA7	B6	IO_VB4N0_B6	IO_VB4N1_F9	F9	PISMO_DM_DQSC_DH
PISMO_DM_DB0	B7	IO_VB4N0_B7	IO_VB4N1_F10	F10	PISMO_DM_DC3
PISMO_DM_DQSA_DH	C4	IO_VB4N0_C4	IO_VB4N1_F11	F11	PISMO_DM_DQSD_DH
PISMO_DM_DQSA_DL	C5	IO_VB4N0_C5	IO_VB4N1_F12	F12	PISMO_DM_DQSD_DL
PISMO_DM_DA6	C6	IO_VB4N0_C6	IO_VB4N1_G10	G10	PISMO_DM_DD1
PISMO_DM_DQSB_DL	C7	IO_VB4N0_C7	IO_VB4N1_G11	G11	PISMO_DM_DD2
PISMO_DM_DA1	D5	IO_VB4N0_D5	IO_VB4N1_G12	G12	PISMO_DM_DD3
PISMO_DM_DA5	D6	IO_VB4N0_D6	IO_VB4N1_H12	H12	PISMO_DM15
PISMO_DM_DQSB_DH	D7	IO_VB4N0_D7	IO_VB4N1_H13	H13	PISMO_DM22
PISMO_DM_DA2	E5	IO_VB4N0_E5	IO_VB4N1_J13	J13	PISMO_DM17
PISMO_DM_DB2	E6	IO_VB4N0_E6	IO_VB4N1_J14	J14	PISMO_DM23
PISMO_DM_DB1	E7	IO_VB4N0_E7	IO_VB4N1_K14	K14	PISMO_DM16
PISMO_DM0	H9	IO_VB4N0_H9	IO_VB4N1_K15	K15	PISMO_DM21
PISMO_DM4	H11	IO_VB4N0_H11	IO_VB4N1_L16	L16	PISMO_DM18
PISMO_DM1	J11	IO_VB4N0_J11			
PISMO_DM12	J12	IO_VB4N0_J12	IO_VB4N2_A12	A12	PISMO_DM25
PISMO_DM5	K12	IO_VB4N0_K12	IO_VB4N2_A14	A14	PISMO_FS3
PISMO_DM11	K13	IO_VB4N0_K13	IO_VB4N2_B12	B12	PISMO_DM24
PISMO_DM6	L13	IO_VB4N0_L13	IO_VB4N2_B13	B13	PISMO_FS2
PISMO_DM7	L14	IO_VB4N0_L14	IO_VB4N2_B14	B14	PISMO_DM36
PISMO_DM10	L15	IO_VB4N0_L15	IO_VB4N2_C13	C13	PISMO_DM35
			IO_VB4N2_D13	D13	PISMO_FS1
PISMO_DM_DB5	A8	IO_VB4N1_A8	IO_VB4N2_D14	D14	PISMO_FS0
PISMO_DM14	A9	IO_VB4N1_A9	IO_VB4N2_E13	E13	PISMO_DM28
PISMO_DM_DC5	A10	IO_VB4N1_A10	IO_VB4N2_E14	E14	PISMO_DM31
PISMO_DM_DD6	A11	IO_VB4N1_A11	IO_VB4N2_F13	F13	PISMO_DM29
PISMO_DM13	B8	IO_VB4N1_B8	IO_VB4N2_F14	F14	PISMO_DM27
PISMO_DM_DB7	B9	IO_VB4N1_B9	IO_VB4N2_F15	F15	PISMO_DM32
PISMO_DM_DC6	B10	IO_VB4N1_B10	IO_VB4N2_G13	G13	PISMO_DM30
PISMO_DM_DD7	B11	IO_VB4N1_B11	IO_VB4N2_G14	G14	PISMO_DM26
PISMO_DM_DB6	C8	IO_VB4N1_C8	IO_VB4N2_H14	H14	PISMO_DM33
PISMO_DM_DB4	C9	IO_VB4N1_C9	IO_VB4N2_J15	J15	PISMO_FS4
PISMO_DM_DC4	C10	IO_VB4N1_C10	IO_VB4N2_K16	K16	PISMO_FS5
PISMO_DM19	C11	IO_VB4N1_C11	IO_VB4N2_K17	K17	PISMO_FS6
PISMO_DM_DD4	C12	IO_VB4N1_C12	IO_VB4N2_L17	L17	PISMO_DM34
PISMO_DM_DC0	D8	IO_VB4N1_D8			
PISMO_DM_DC7	D10	IO_VB4N1_D10		L12	PISMO_DM2
			RUP4	K11	PISMO_DM3
			RDN4		

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			IO_VB5N1_D1	D1	PISMO_SM81
			IO_VB5N1_D2	D2	PISMO_SM80
			IO_VB5N1_E1	E1	PISMO_SM73
			IO_VB5N1_E2	E2	PISMO_SM72
			IO_VB5N1_E3	E3	PISMO_SM77
			IO_VB5N1_E4	E4	PISMO_SM76
PISMO_SM37	K1	IO_VB5N0_K1	IO_VB5N1_F1	F1	PISMO_SM65
PISMO_SM36	K2	IO_VB5N0_K2	IO_VB5N1_F2	F2	PISMO_SM64
PISMO_SM41	K3	IO_VB5N0_K3	IO_VB5N1_F3	F3	PISMO_SM69
PISMO_SM40	K4	IO_VB5N0_K4	IO_VB5N1_F4	F4	PISMO_SM68
PISMO_SM21	L1	IO_VB5N0_L1	IO_VB5N1_G1	G1	PISMO_SM57
PISMO_SM20	L2	IO_VB5N0_L2	IO_VB5N1_G2	G2	PISMO_SM56
PISMO_SM33	L3	IO_VB5N0_L3	IO_VB5N1_G3	G3	PISMO_SM61
PISMO_SM32	L4	IO_VB5N0_L4	IO_VB5N1_G4	G4	PISMO_SM60
PISMO_SM13	M1	IO_VB5N0_M1	IO_VB5N1_H1	H1	PISMO_SM49
PISMO_SM12	M2	IO_VB5N0_M2	IO_VB5N1_H2	H2	PISMO_SM48
PISMO_SM25	M3	IO_VB5N0_M3	IO_VB5N1_J1	J1	PISMO_SM45
PISMO_SM24	M4	IO_VB5N0_M4	IO_VB5N1_J2	J2	PISMO_SM44
PISMO_SM17	N2	IO_VB5N0_N2	IO_VB5N1_J3	J3	PISMO_SM53
PISMO_SM16	N3	IO_VB5N0_N3	IO_VB5N1_J4	J4	PISMO_SM52
PISMO_SM29	N4	IO_VB5N0_N4	IO_VB5N1_K6	K6	PISMO_SM79
PISMO_SM28	N5	IO_VB5N0_N5	IO_VB5N1_K7	K7	PISMO_SM78
PISMO_SM39	N8	IO_VB5N0_N8	IO_VB5N1_K8	K8	PISMO_SM75
PISMO_SM38	N9	IO_VB5N0_N9	IO_VB5N1_K9	K9	PISMO_SM74
PISMO_SM5	P1	IO_VB5N0_P1	IO_VB5N1_L5	L5	PISMO_SM59
PISMO_SM4	P2	IO_VB5N0_P2	IO_VB5N1_L6	L6	PISMO_SM58
PISMO_SM27	P4	IO_VB5N0_P4	IO_VB5N1_L7	L7	PISMO_SM71
PISMO_SM26	P5	IO_VB5N0_P5	IO_VB5N1_L8	L8	PISMO_SM70
PISMO_SM31	P6	IO_VB5N0_P6	IO_VB5N1_L9	L9	PISMO_SM67
PISMO_SM30	P7	IO_VB5N0_P7	IO_VB5N1_L10	L10	PISMO_SM66
PISMO_SM35	P8	IO_VB5N0_P8	IO_VB5N1_M6	M6	PISMO_SM47
PISMO_SM34	P9	IO_VB5N0_P9	IO_VB5N1_M7	M7	PISMO_SM46
PISMO_SM23	P10	IO_VB5N0_P10	IO_VB5N1_M8	M8	PISMO_SM63
PISMO_SM22	P11	IO_VB5N0_P11	IO_VB5N1_M9	M9	PISMO_SM62
PISMO_SM9	R2	IO_VB5N0_R2	IO_VB5N1_M10	M10	PISMO_SM55
PISMO_SM8	R3	IO_VB5N0_R3	IO_VB5N1_M11	M11	PISMO_SM54
PISMO_SM15	R4	IO_VB5N0_R4	IO_VB5N1_N6	N6	PISMO_SM43
PISMO_SM14	R5	IO_VB5N0_R5	IO_VB5N1_N7	N7	PISMO_SM42
PISMO_SM19	R6	IO_VB5N0_R6	IO_VB5N1_N10	N10	PISMO_SM51
PISMO_SM18	R7	IO_VB5N0_R7	IO_VB5N1_N11	N11	PISMO_SM50
PISMO_SM11	R10	IO_VB5N0_R10			
PISMO_SM10	R11	IO_VB5N0_R11			
PISMO_SM7	T5	IO_VB5N0_T5	IO_VB5N2_G5	G5	PISMO_AUX9
PISMO_SM6	T6	IO_VB5N0_T6	IO_VB5N2_G6	G6	PISMO_AUX8
PISMO_SM3	T10	IO_VB5N0_T10	IO_VB5N2_H3	H3	PISMO_SM85
PISMO_SM2	T11	IO_VB5N0_T11	IO_VB5N2_H4	H4	PISMO_SM84
			IO_VB5N2_H5	H5	PISMO_AUX11
			IO_VB5N2_H6	H6	PISMO_AUX10
			IO_VB5N2_J6	J6	PISMO_AUX7
			IO_VB5N2_J7	J7	PISMO_SM86
			IO_VB5N2_J8	J8	PISMO_SM83
			IO_VB5N2_J9	J9	PISMO_SM82

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PISMO_NA11	AC6	IO_VB6N0_AC6	IO_VB6N1_AF1	AF1	SODIMM_S3
PISMO_NA10	AC7	IO_VB6N0_AC7	IO_VB6N1_AF2	AF2	SODIMM_S2
PISMO_NA3	AD6	IO_VB6N0_AD6	IO_VB6N1_AF3	AF3	PISMO_NA25
PISMO_NA2	AD7	IO_VB6N0_AD7	IO_VB6N1_AF4	AF4	PISMO_NA24
PISMO_NA7	AD8	IO_VB6N0_AD8	IO_VB6N1_AG1	AG1	PISMO_AUX2
PISMO_NA6	AD9	IO_VB6N0_AD9	IO_VB6N1_AG2	AG2	PISMO_AUX1
PISMO_NA1	AF5	IO_VB6N0_AF5	IO_VB6N1_AH1	AH1	PISMO_NA21
PISMO_NA0	AF6	IO_VB6N0_AF6	IO_VB6N1_AH2	AH2	PISMO_NA20
PISMO_NA9	AG3	IO_VB6N0_AG3			
PISMO_NA8	AG4	IO_VB6N0_AG4			
PISMO_NA5	AH3	IO_VB6N0_AH3	IO_VB6N2_U5	U5	UGRID56
PISMO_NA4	AH4	IO_VB6N0_AH4	IO_VB6N2_U6	U6	UGRID55
PISMO_NA13	AJ1	IO_VB6N0_AJ1	IO_VB6N2_U10	U10	UGRID52
PISMO_NA12	AJ2	IO_VB6N0_AJ2	IO_VB6N2_U11	U11	UGRID51
			IO_VB6N2_V2	V2	UGRID58
SODIMM_S13	W10	IO_VB6N1_W10	IO_VB6N2_V3	V3	UGRID57
SODIMM_S12	W11	IO_VB6N1_W11	IO_VB6N2_V4	V4	UGRID40
SODIMM_S17	Y8	IO_VB6N1_Y8	IO_VB6N2_V5	V5	UGRID39
SODIMM_S16	Y9	IO_VB6N1_Y9	IO_VB6N2_V6	V6	UGRID44
SODIMM_S5	Y10	IO_VB6N1_Y10	IO_VB6N2_V7	V7	UGRID43
SODIMM_S4	Y11	IO_VB6N1_Y11	IO_VB6N2_V9	V9	UGRID48
SODIMM_S9	AA6	IO_VB6N1_AA6	IO_VB6N2_V10	V10	UGRID47
SODIMM_S8	AA7	IO_VB6N1_AA7	IO_VB6N2_W1	W1	UGRID54
PISMO_AUX4	AA8	IO_VB6N1_AA8	IO_VB6N2_W2	W2	UGRID53
PISMO_AUX3	AA9	IO_VB6N1_AA9	IO_VB6N2_W4	W4	UGRID28
SODIMM_S1	AA10	IO_VB6N1_AA10	IO_VB6N2_W5	W5	UGRID27
SODIMM_S0	AA11	IO_VB6N1_AA11	IO_VB6N2_W6	W6	UGRID32
PISMO_AUX0	AB5	IO_VB6N1_AB5	IO_VB6N2_W7	W7	UGRID31
PISMO_NA26	AB6	IO_VB6N1_AB6	IO_VB6N2_W8	W8	UGRID36
PISMO_NA19	AB7	IO_VB6N1_AB7	IO_VB6N2_W9	W9	UGRID35
PISMO_NA18	AB8	IO_VB6N1_AB8	IO_VB6N2_Y2	Y2	UGRID50
PISMO_NA23	AB9	IO_VB6N1_AB9	IO_VB6N2_Y3	Y3	UGRID49
PISMO_NA22	AB10	IO_VB6N1_AB10	IO_VB6N2_Y4	Y4	UGRID38
UGRID22	AC3	IO_VB6N1_AC3	IO_VB6N2_Y5	Y5	UGRID37
SODIMM_S18	AC4	IO_VB6N1_AC4	IO_VB6N2_Y6	Y6	UGRID24
PISMO_NA15	AC8	IO_VB6N1_AC8	IO_VB6N2_Y7	Y7	UGRID23
PISMO_NA14	AC9	IO_VB6N1_AC9	IO_VB6N2_AA1	AA1	UGRID46
SODIMM_S15	AD1	IO_VB6N1_AD1	IO_VB6N2_AA2	AA2	UGRID45
SODIMM_S14	AD2	IO_VB6N1_AD2	IO_VB6N2_AA3	AA3	UGRID42
PISMO_AUX6	AD3	IO_VB6N1_AD3	IO_VB6N2_AA4	AA4	UGRID41
PISMO_AUX5	AD4	IO_VB6N1_AD4	IO_VB6N2_AB1	AB1	UGRID34
SODIMM_S11	AE1	IO_VB6N1_AE1	IO_VB6N2_AB2	AB2	UGRID33
SODIMM_S10	AE2	IO_VB6N1_AE2	IO_VB6N2_AB3	AB3	UGRID30
SODIMM_S7	AE3	IO_VB6N1_AE3	IO_VB6N2_AB4	AB4	UGRID29
SODIMM_S6	AE4	IO_VB6N1_AE4	IO_VB6N2_AC1	AC1	UGRID26
PISMO_NA17	AE5	IO_VB6N1_AE5	IO_VB6N2_AC2	AC2	UGRID25
PISMO_NA16	AE6	IO_VB6N1_AE6			

FPGA[0..275]
FPGA[0..275]
PISMO_DM_DQSA_DH
PISMO_DM_DQSA_DL
PISMO_DM_DQSB_DH
PISMO_DM_DQSB_DL
PISMO_DM_DQSC_DH
PISMO_DM_DQSC_DL
PISMO_DM_DQSD_DH
PISMO_DM_DQSD_DL
PISMO_NA[0..26]
PISMO_SM[0..88]
PISMO_SM[0..88]
PISMO_DM[0..36]
PISMO_DM_DA[0..7]
PISMO_DM_DB[0..7]
PISMO_DM_DC[0..7]
PISMO_DM_DD[0..7]
PISMO_AUX[0..12]
PISMO_AUX[0..12]
PISMO_FS[0..9]
PISMO_FS[0..9]
SODIMM_C[0..53]
SODIMM_C[0..53]
SODIMM_D[0..31]
SODIMM_D[0..31]
SODIMM_DQS[0..1]
SODIMM_DQS[0..1]
SODIMM_S[0..18]
MPIOA[0..31]
MPIOA[0..31]
MPIOB[0..44]
MPIOB[0..44]
UGRID[0..75]
UGRID[0..75]

REV	MODIF.	DES.	DATE	VER.	DATE
B		YRDE	04-MAY-07		
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06

AT91CAP9A-DKZ
MEZZANINE BOARD
SCALE 1/1
REV. B
SHEET 11/14

FPGA I/Os, config

CONFIG_DONE
NRST
FPGA[0..275]
PISMO_AUX[0..12]
PISMO_SM[0..88]
PISMO_FS[0..9]
UGRID[0..75]
SODIMM_C[0..53]
SODIMM_D[0..31]
SODIMM_DQS[0..1]
MPIOA[0..31]
MPIOB[0..44]

3V3
R56 220R
DS1 HSMG-C170
Q3 FDV301N
CONFIG_DONE
VCCPD
R57 0R
VCCSEL
R59 0R *FEED = NO*

3V3
R58 10k
nSTATUS
TP4 5016
TP5 5016
TP6 5016
TP7 5016
TP8 5016
TP9 5016
TP10 5016

ALTERA EP2S90F1020
Version = 1.0

U7J

UGRID1	AD23	CLKUSR	nCE C30
	J25	CONF_DONE	nCEO AL3
FPGA200	G20	CRC_ERROR	nCONFIG AL30
UGRID0	AC22	CS	nCS AG18 UGRID7
DATA0	H19	DATA0	nIO_PULLUP AK3
FPGA201	F20	DATA1	AF23 UGRID3
FPGA269	G23	DATA2	nRS B30
FPGA270	H23	DATA3	nSTATUS AE23 UGRID2
FPGA271	J23	DATA4	nWS E17 FPGA199
FPGA272	L22	DATA5	PGM0 F19 FPGA198
FPGA273	F24	DATA6	PGM1 F18 FPGA197
FPGA274	G24	DATA7	PGM2 AL2
	B31	DCLK	PORSEL H24 FPGA275
UGRID6	AG19	DEV_CLRn	RDYnBSY AG17 UGRID4
UGRID5	AH17	DEV_OE	RUnLU AF24
UGRID75	G25	INIT_DONE	TCK AL31
	B2	MSEL0	TDI C3
	F6	MSEL1	TDO AE24
	J10	MSEL2	TMS AK30
	H10	MSEL3	TRST AC23 VCCSEL

DATA0
DCLK
nCE
nCONFIG
nCEO
nIO_PULLUP
nSTATUS
PORSEL
S2_TCK
S2_TDI
S2_TDO
S2_TMS
TRST
VCCSEL

VCCPD
R60 0R MSEL0 FEED = NO
R62 0R MSEL1 FEED = NO
R63 0R MSEL2 FEED = NO
R64 0R MSEL3

VCCPD
R78 1k

J19 903-NM415J-51P
R61 0R
Y1 EN VDD GND OUT CO4305-12
C191 100nF

TP11 5016
PLL_ENA

ALTERA EP2S90F1020
Version = 1.0

U7I

FPGA188	T31	CLK0n	PLL5_OUT1p C16 UGRID68
FPGA189	T32	CLK0p	PLL5_OUT1n D16 UGRID67
FPGA190	T29	CLK1n	PLL5_OUT0p B15 UGRID66
FPGA175	T30	CLK1p	PLL5_OUT0n C15 UGRID65
FPGA1	U31	CLK2n	PLL5_FBp D15 UGRID64
FPGA0	U32	CLK2p	PLL5_FBn E15 UGRID63
FPGA3	U29	CLK3n	
FPGA2	U30	CLK3p	PLL6_OUT1p AJ15 UGRID14
MPIOB44	AL17	CLK4n	PLL6_OUT1n AH15 UGRID15
MPIOB24	AM17	CLK4p	PLL6_OUT0p AK16 UGRID16
MPIOB43	AJ17	CLK5n	PLL6_OUT0n AJ16 UGRID17
NRST	AK17	CLK5p	PLL6_FBp AL15 UGRID18
SODIMM_C53	AL16	CLK6n	PLL6_FBn AK15 UGRID19
SODIMM_C52	AM16	CLK6p	
SODIMM_C51	AG16	CLK7n	PLL11_OUT1p D18 UGRID71
SODIMM_C50	AH16	CLK7p	PLL11_OUT1n E18 UGRID72
UGRID61	U2	CLK8n	PLL11_OUT0p B18 UGRID69
UGRID62	U1	CLK8p	PLL11_OUT0n C18 UGRID70
UGRID59	U4	CLK9n	PLL11_FBp A19 UGRID73
UGRID60	U3	CLK9p	PLL11_FBn B19 UGRID74
PISMO_SM1	T2	CLK10n	
PISMO_SM0	T1	CLK10p	PLL12_OUT1p AJ18 UGRID11
EXT_CLK	T4	CLK11n	PLL12_OUT1n AH18 UGRID10
XTAL_CLK	T3	CLK11p	PLL12_OUT0p AL18 UGRID13
PISMO_FS7	B16	CLK12n	PLL12_OUT0n AK18 UGRID12
PISMO_FS8	A16	CLK12p	PLL12_FBp AM19 UGRID9
PISMO_FS9	F16	CLK13n	PLL12_FBn AL19 UGRID8
PISMO_AUX12	E16	CLK13p	
FPGA193	B17	CLK14n	PLL_ENA AF8 PLL_ENA
FPGA192	A17	CLK14p	
FPGA195	D17	CLK15n	FPLL7CLKp D30 FPGA96
FPGA194	C17	CLK15p	FPLL7CLKn D29 FPGA97
			FPLL8CLKp AJ30 FPGA95
			FPLL8CLKn AJ29 FPGA94
			FPLL9CLKp AJ3 UGRID20
			FPLL9CLKn AJ4 UGRID21
			FPLL10CLKp D3 PISMO_SM88
			FPLL10CLKn D4 PISMO_SM87

BANK 7

ALTERA EP2S90F1020
Version = 1.0

U7G

SODIMM_C17	AB15	IO_VB7N0_AB15	IO_VB7N1_AK10 AK10 SODIMM_C23
SODIMM_C0	AB16	IO_VB7N0_AB16	IO_VB7N1_AK11 AK11 SODIMM_C22
SODIMM_C2	AC15	IO_VB7N0_AC15	IO_VB7N1_AK12 AK12 SODIMM_D3
SODIMM_C1	AC16	IO_VB7N0_AC16	IO_VB7N1_AL7 AL7 SODIMM_C34
SODIMM_C9	AD14	IO_VB7N0_AD14	IO_VB7N1_AL8 AL8 SODIMM_D16
SODIMM_C10	AE14	IO_VB7N0_AE14	IO_VB7N1_AL9 AL9 SODIMM_C29
SODIMM_C13	AF13	IO_VB7N0_AF13	IO_VB7N1_AL10 AL10 SODIMM_D5
SODIMM_C18	AF14	IO_VB7N0_AF14	IO_VB7N1_AL11 AL11 SODIMM_C20
SODIMM_C14	AG13	IO_VB7N0_AG13	IO_VB7N1_AM7 AM7 SODIMM_D19
SODIMM_C16	AG14	IO_VB7N0_AG14	IO_VB7N1_AM8 AM8 SODIMM_C33
SODIMM_C11	AG15	IO_VB7N0_AG15	IO_VB7N1_AM9 AM9 SODIMM_D12
SODIMM_C15	AH13	IO_VB7N0_AH13	IO_VB7N1_AM10 AM10 SODIMM_D4
SODIMM_C12	AH14	IO_VB7N0_AH14	IO_VB7N1_AM11 AM11 SODIMM_D1
SODIMM_C5	AJ13	IO_VB7N0_AJ13	
SODIMM_C6	AJ14	IO_VB7N0_AJ14	IO_VB7N2_AB12 AB12 SODIMM_C45
SODIMM_C8	AK13	IO_VB7N0_AK13	IO_VB7N2_AB13 AB13 SODIMM_C35
SODIMM_D0	AL12	IO_VB7N0_AL12	IO_VB7N2_AC11 AC11 SODIMM_C44
SODIMM_C4	AL13	IO_VB7N0_AL13	IO_VB7N2_AC12 AC12 SODIMM_C42
SODIMM_C7	AL14	IO_VB7N0_AL14	IO_VB7N2_AD11 AD11 SODIMM_C41
SODIMM_C19	AM12	IO_VB7N0_AM12	IO_VB7N2_AD12 AD12 SODIMM_C36
SODIMM_C3	AM14	IO_VB7N0_AM14	IO_VB7N2_AE9 AE9 SODIMM_C49
			IO_VB7N2_AE10 AE10 SODIMM_C46
SODIMM_C28	AB14	IO_VB7N1_AB14	IO_VB7N2_AE11 AE11 SODIMM_C38
SODIMM_C31	AC13	IO_VB7N1_AC13	IO_VB7N2_AG8 AG8 SODIMM_C40
SODIMM_C21	AC14	IO_VB7N1_AC14	IO_VB7N2_AG9 AG9 SODIMM_D27
SODIMM_C24	AD13	IO_VB7N1_AD13	IO_VB7N2_AH5 AH5 SODIMM_D29
SODIMM_C32	AE12	IO_VB7N1_AE12	IO_VB7N2_AH6 AH6 SODIMM_D26
SODIMM_C25	AE13	IO_VB7N1_AE13	IO_VB7N2_AH7 AH7 SODIMM_D25
SODIMM_D9	AE10	IO_VB7N1_AF10	IO_VB7N2_AH8 AH8 SODIMM_D24
SODIMM_C27	AF11	IO_VB7N1_AF11	IO_VB7N2_AH9 AH9 SODIMM_C39
SODIMM_D11	AF12	IO_VB7N1_AF12	IO_VB7N2_AJ5 AJ5 SODIMM_D30
SODIMM_D10	AG10	IO_VB7N1_AG10	IO_VB7N2_AJ6 AJ6 SODIMM_D21
SODIMM_D8	AG11	IO_VB7N1_AG11	IO_VB7N2_AK4 AK4 SODIMM_DQS0
SODIMM_C26	AG12	IO_VB7N1_AG12	IO_VB7N2_AK5 AK5 SODIMM_C43
SODIMM_D6	AH11	IO_VB7N1_AH11	IO_VB7N2_AK6 AK6 SODIMM_D22
SODIMM_D17	AJ7	IO_VB7N1_AJ7	IO_VB7N2_AL4 AL4 SODIMM_D31
SODIMM_D13	AJ8	IO_VB7N1_AJ8	IO_VB7N2_AL5 AL5 SODIMM_DQS1
SODIMM_D15	AJ10	IO_VB7N1_AJ10	IO_VB7N2_AL6 AL6 SODIMM_C37
SODIMM_D7	AJ11	IO_VB7N1_AJ11	IO_VB7N2_AM4 AM4 SODIMM_D28
SODIMM_D2	AJ12	IO_VB7N1_AJ12	IO_VB7N2_AM5 AM5 SODIMM_D23
SODIMM_D18	AK7	IO_VB7N1_AK7	IO_VB7N2_AM6 AM6 SODIMM_D20
SODIMM_D14	AK8	IO_VB7N1_AK8	
SODIMM_C30	AK9	IO_VB7N1_AK9	RDN7 AB11 SODIMM_C47
			RUP7 AD10 SODIMM_C48

BANK 8

ALTERA EP2S90F1020
Version = 1.0

U7H

MPIOA1	AB21	IO_VB8N0_AB21	IO_VB8N1_AH26 AH26 MPIOA29
MPIOA11	AC21	IO_VB8N0_AC21	IO_VB8N1_AJ22 AJ22 MPIOB17
MPIOA4	AD22	IO_VB8N0_AD22	IO_VB8N1_AJ23 AJ23 MPIOB16
MPIOA2	AE22	IO_VB8N0_AE22	IO_VB8N1_AJ25 AJ25 MPIOB0
MPIOA19	AF21	IO_VB8N0_AF21	IO_VB8N1_AJ26 AJ26 MPIOA22
MPIOA3	AF22	IO_VB8N0_AF22	IO_VB8N1_AK22 AK22 MPIOB15
MPIOA12	AG21	IO_VB8N0_AG21	IO_VB8N1_AK23 AK23 MPIOB8
MPIOA0	AG25	IO_VB8N0_AG25	IO_VB8N1_AK24 AK24 MPIOB7
MPIOA5	AH28	IO_VB8N0_AH28	IO_VB8N1_AK25 AK25 MPIOA31
MPIOA15	AJ27	IO_VB8N0_AJ27	IO_VB8N1_AL23 AL23 MPIOB10
MPIOA7	AJ28	IO_VB8N0_AJ28	IO_VB8N1_AL24 AL24 MPIOB6
MPIOA20	AK26	IO_VB8N0_AK26	IO_VB8N1_AL25 AL25 MPIOA25
MPIOA13	AK27	IO_VB8N0_AK27	IO_VB8N1_AM23 AM23 MPIOB9
MPIOA10	AK28	IO_VB8N0_AK28	IO_VB8N1_AM24 AM24 MPIOB5
MPIOA6	AK29	IO_VB8N0_AK29	IO_VB8N1_AM25 AM25 MPIOA23
MPIOA21	AL26	IO_VB8N0_AL26	IO_VB8N1_AM26 AM26 MPIOA24
MPIOA18	AL27	IO_VB8N0_AL27	
MPIOA14	AL28	IO_VB8N0_AL28	IO_VB8N2_AB17 AB17 MPIOB41
MPIOA9	AL29	IO_VB8N0_AL29	IO_VB8N2_AB18 AB18 MPIOB32
MPIOA17	AM27	IO_VB8N0_AM27	IO_VB8N2_AC17 AC17 MPIOB42
MPIOA16	AM28	IO_VB8N0_AM28	IO_VB8N2_AC18 AC18 MPIOB39
MPIOA8	AM29	IO_VB8N0_AM29	IO_VB8N2_AC19 AC19 MPIOB21
			IO_VB8N2_AD18 AD18 MPIOB40
MPIOB19	AB19	IO_VB8N1_AB19	IO_VB8N2_AD19 AD19 MPIOB29
MPIOB1	AB20	IO_VB8N1_AB20	IO_VB8N2_AE19 AE19 MPIOB30
MPIOB18	AC20	IO_VB8N1_AC20	IO_VB8N2_AF19 AF19 MPIOB31
MPIOB11	AD20	IO_VB8N1_AD20	IO_VB8N2_AH19 AH19 MPIOB36
MPIOA26	AD21	IO_VB8N1_AD21	IO_VB8N2_AH20 AH20 MPIOB33
MPIOB20	AE20	IO_VB8N1_AE20	IO_VB8N2_AJ19 AJ19 MPIOB35
MPIOB2	AE21	IO_VB8N1_AE21	IO_VB8N2_AJ20 AJ20 MPIOB34
MPIOB4	AF20	IO_VB8N1_AF20	IO_VB8N2_AJ21 AJ21 MPIOB25
MPIOB3	AG20	IO_VB8N1_AG20	IO_VB8N2_AK20 AK20 MPIOB38
MPIOB14	AG22	IO_VB8N1_AG22	IO_VB8N2_AK21 AK21 MPIOB26
MPIOB12	AG23	IO_VB8N1_AG23	IO_VB8N2_AL20 AL20 MPIOB37
MPIOA27	AG24	IO_VB8N1_AG24	IO_VB8N2_AL21 AL21 MPIOB28
MPIOB13	AH22	IO_VB8N1_AH22	IO_VB8N2_AL22 AL22 MPIOB23
MPIOA30	AH24	IO_VB8N1_AH24	IO_VB8N2_AM21 AM21 MPIOB27
MPIOA28	AH25	IO_VB8N1_AH25	IO_VB8N2_AM22 AM22 MPIOB22

REV	MODIF.	DES.	DATE	VER.	DATE
B		YRDE	04-MAY-07		
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06

ATMEL ROUSSET

AT91CAP9A-DKZ

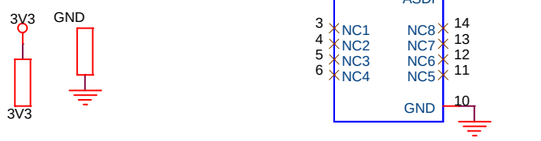
MEZZANINE BOARD

SCALE 1/1

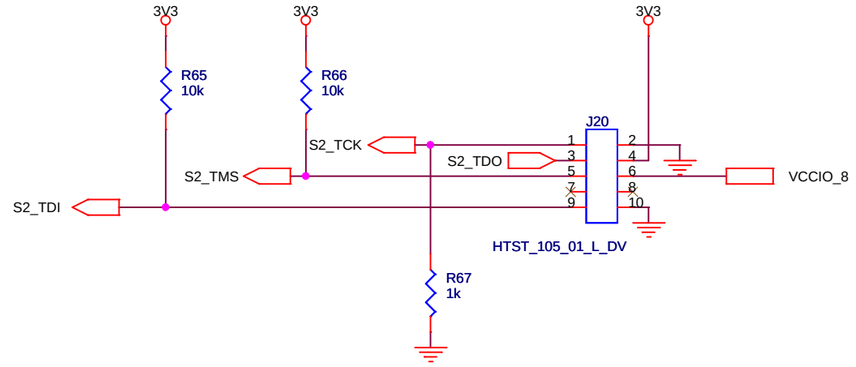
REV. B

SHEET 12/14

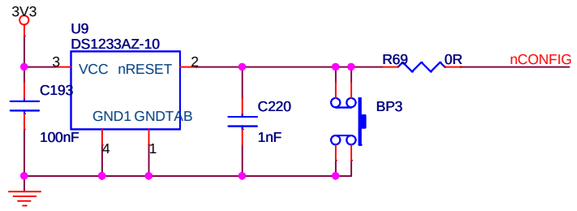
FPGA I/Os, config

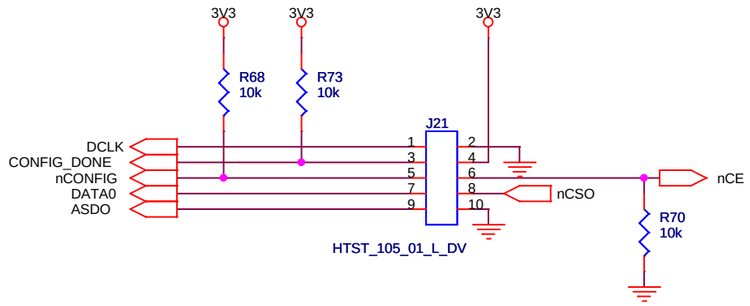


JTAG



AS Mode





REV	MODIF.	DES.	DATE	VER.	DATE
B		YRDE	04-MAY-07		
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06

ATMEL ROUSSET

AT91CAP9A-DKZ

MEZZANINE BOARD

SCALE 1/1

REV. B

SHEET 13/14

FPGA - SODIMM EBI

SODIMM_D[0..31]
SODIMM_DQS[0..1]
SODIMM_C[0..53]
SODIMM_S[0..18]
VCCIO_6
VCCIO_7

GND
5V
5V

J4

	1	VSS1	VSS10	2			
SODIMM_D0	3	DQ0	DQ32	4	SODIMM_D8		
SODIMM_D1	5	DQ1	DQ33	6	SODIMM_D9		
SODIMM_D2	7	DQ2	DQ34	8	SODIMM_D10		
SODIMM_D3	9	DQ3	DQ35	10	SODIMM_D11		
VCCIO_7	11	VDD1	VDD10	12	VCCIO_7		
SODIMM_D4	13	DQ4	DQ36	14	SODIMM_D12		
SODIMM_D5	15	DQ5	DQ37	16	SODIMM_D13		
SODIMM_D6	17	DQ6	DQ38	18	SODIMM_D14		
SODIMM_D7	19	DQ7	DQ39	20	SODIMM_D15		
	21	VSS2	VSS11	22			
SODIMM_D16	23	DQMB0	DQMB4	24	SODIMM_D24		
SODIMM_D17	25	DQMB1	DQMB5	26	SODIMM_D25		
VCCIO_7	27	VDD2	VDD11	28	VCCIO_7		
SODIMM_D18	29	A0	A3	30	SODIMM_D26		
SODIMM_D19	31	A1	A4	32	SODIMM_D27		
SODIMM_D20	33	A2	A5	34	SODIMM_D28		
	35	VSS3	VSS12	36			
SODIMM_D21	37	DQ8	DQ40	38	SODIMM_D29		
SODIMM_D22	39	DQ9	DQ41	40	SODIMM_D30		
SODIMM_D23	41	DQ10	DQ42	42	SODIMM_D31		
SODIMM_DQS0	43	DQ11	DQ43	44	SODIMM_DQS1		
VCCIO_7	45	VDD3	VDD12	46	VCCIO_7		
SODIMM_C0	47	DQ12	DQ44	48	SODIMM_C27		
SODIMM_C1	49	DQ13	DQ45	50	SODIMM_C28		
SODIMM_C2	51	DQ14	DQ46	52	SODIMM_C29		
SODIMM_C3	53	DQ15	DQ47	54	SODIMM_C30		
	55	VSS4	VSS13	56			
SODIMM_C4	57	NC1	NC6	58	SODIMM_C31		
SODIMM_C5	59	NC2	NC7	60	SODIMM_C32		
SODIMM_C6	61	CK0	CKE0	62	SODIMM_C33		
VCCIO_7	63	VDD4	VDD13	64	VCCIO_7		
SODIMM_C7	65	RAS#	CAS#	66	SODIMM_C34		
SODIMM_C8	67	WE#	CKE1	68	SODIMM_C35		
SODIMM_C9	69	S0#	A12	70	SODIMM_C36		
SODIMM_C10	71	S1#	NC8	72	SODIMM_C37		
SODIMM_C11	73	NC3	CK1	74	SODIMM_C38		
	75	VSS5	VSS14	76			
SODIMM_C12	77	NC4	NC9	78	SODIMM_C39		
SODIMM_C13	79	NC5	NC10	80	SODIMM_C40		
VCCIO_7	81	VDD5	VDD14	82	VCCIO_7		
SODIMM_C14	83	DQ16	DQ48	84	SODIMM_C41		
SODIMM_C15	85	DQ17	DQ49	86	SODIMM_C42		
SODIMM_C16	87	DQ18	DQ50	88	SODIMM_C43		
SODIMM_C17	89	DQ19	DQ51	90	SODIMM_C44		
	91	VSS6	VSS15	92			
SODIMM_C18	93	DQ20	DQ52	94	SODIMM_C45		
SODIMM_C19	95	DQ21	DQ53	96	SODIMM_C46		
SODIMM_C20	97	DQ22	DQ54	98	SODIMM_C47		
SODIMM_C21	99	DQ23	DQ55	100	SODIMM_C48		
VCCIO_7	101	VDD6	VDD15	102	VCCIO_7		
SODIMM_C22	103	A6	A7	104	SODIMM_C49		
SODIMM_C23	105	A8	BA0	106	SODIMM_C50		
	107	VSS7	VSS16	108			
SODIMM_C24	109	A9	BA1	110	SODIMM_C51		
RVDD_EBIFPGA	111	A10	A11	112	SODIMM_C52		
VCCIO_7	113	VDD7	VDD16	114	VCCIO_7		
SODIMM_C25	115	DQMB2	DQMB6	116	SODIMM_C53		
SODIMM_C26	117	DQMB3	DQMB7	118	SODIMM_S9		
	119	VSS8	VSS17	120			
SODIMM_S0	121	DQ24	DQ56	122	SODIMM_S10		
SODIMM_S1	123	DQ25	DQ57	124	SODIMM_S11		
SODIMM_S2	125	DQ26	DQ58	126	SODIMM_S12		
SODIMM_S3	127	DQ27	DQ59	128	SODIMM_S13		
VCCIO_6	129	VDD8	VDD17	130	VCCIO_6		
SODIMM_S4	131	DQ28	DQ60	132	SODIMM_S14		
SODIMM_S5	133	DQ29	DQ61	134	SODIMM_S15		
SODIMM_S6	135	DQ30	DQ62	136	SODIMM_S16		
SODIMM_S7	137	DQ31	DQ63	138	SODIMM_S17		
	139	VSS9	VSS18	140			
SODIMM_S8	141	SDA	SCL	142	SODIMM_S18		
VCCIO_6	143	VDD9	VDD18	144	VCCIO_6		

20_6403_144_100_856

5V
C194 10uF
C195 100nF
U10 LT1963AEQ
IN OUT
nSHDN ADJ
GND1 GND2
TAB
R71 3.32k
R72 1.96k
C196 10uF
VCCIO_7
D3
SMLVT3V3
RVDD_EBIFPGA

REV		DES.	DATE	VER.	DATE
B		YRDE	04-MAY-07		
A	INIT EDIT	YRDE	XX-SEP-06	XXX	XX-XXX-06

ATMEL ROUSSET

AT91CAP9A-DKZ

MEZZANINE BOARD

SCALE 1/1

REV. B

SHEET 14/14

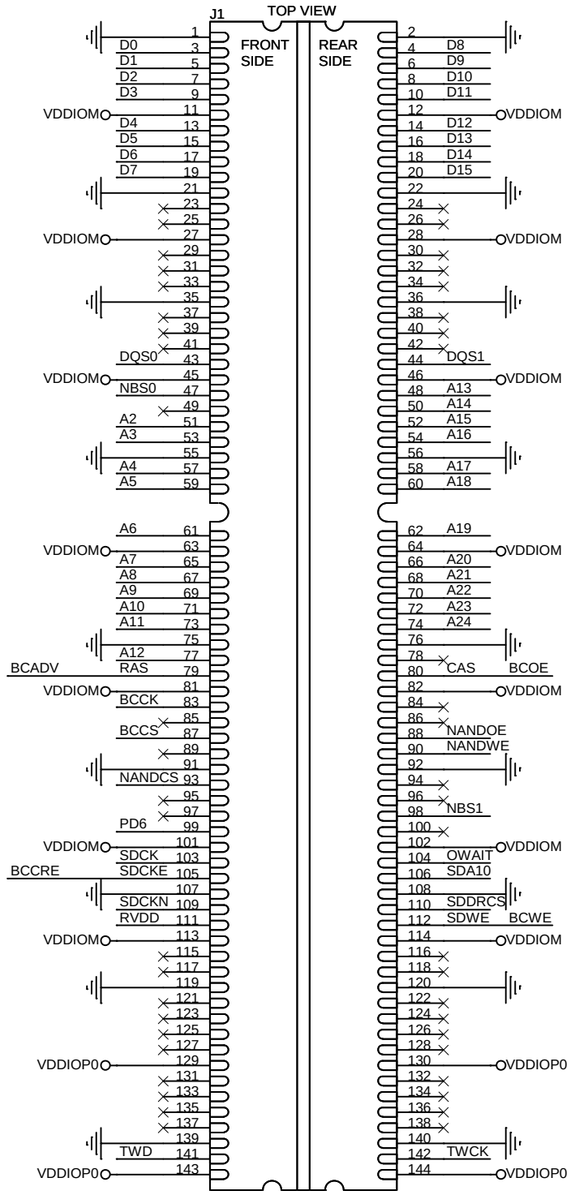
Section 17

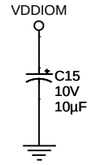
AT91CAP-MEM18 Schematics

17.1 Schematics

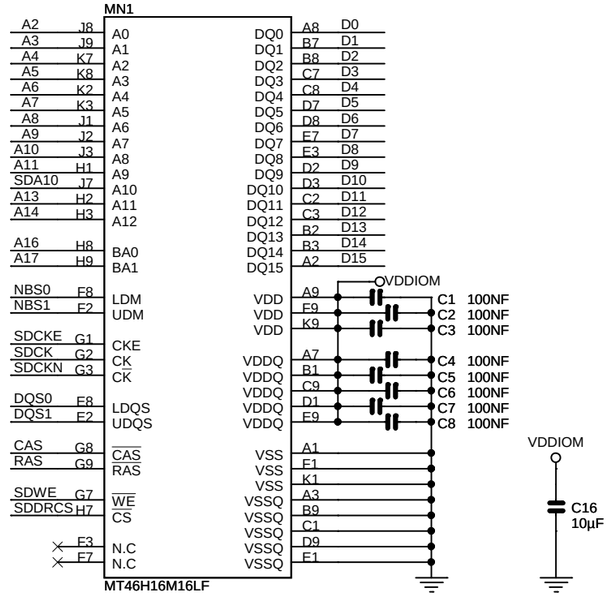
This section contains the following appended schematics:

- AT91CAP-MEM18

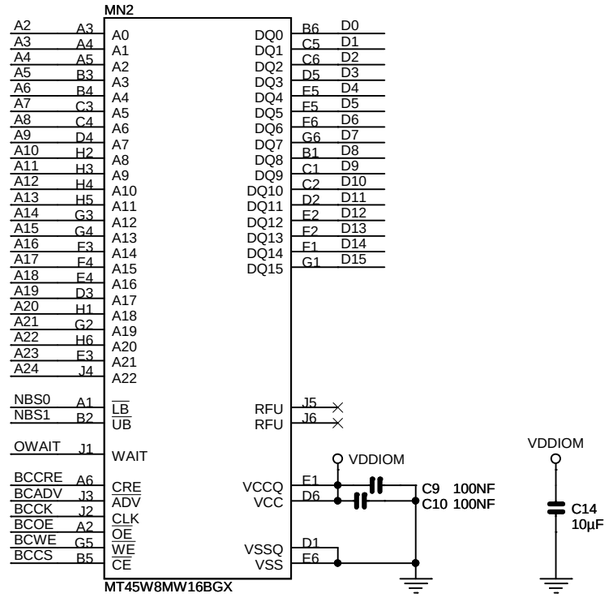




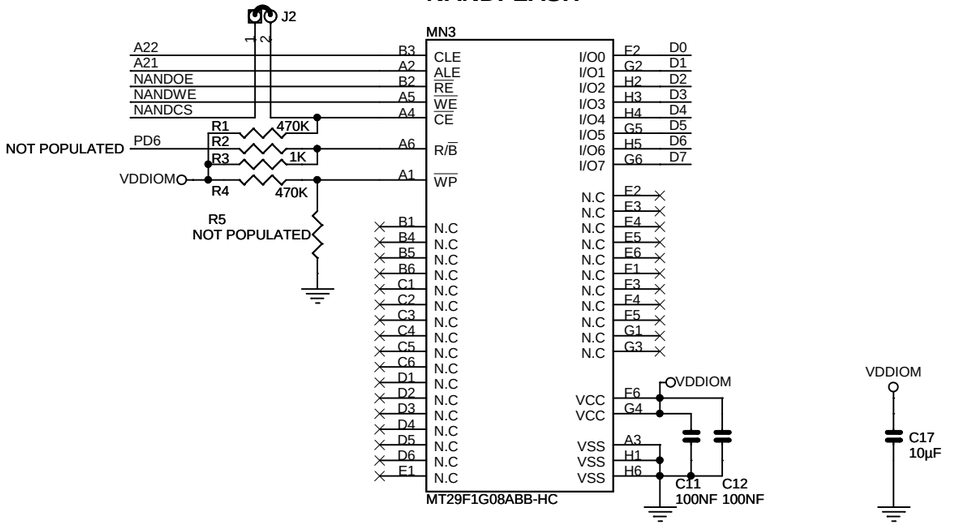
MOBILE DDR

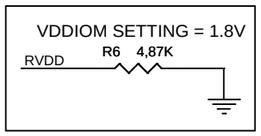


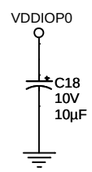
BURST CELLULAR RAM

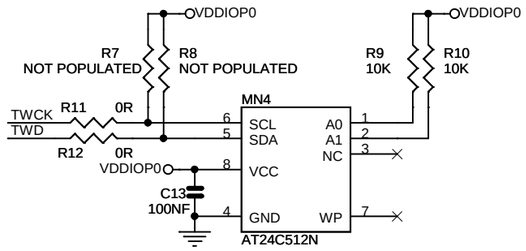


NANDFLASH









SERIAL EEPROM

A	INIT EDIT	JPG	07-JUN-07	XXX	XX-XXX-06
REV.	MODIF.	DES.	DATE	VER.	DATE

AT91CAP9-EMV

AT91CAP-MEM18

SCALE 1/1

REV. A

SHEET 1/1

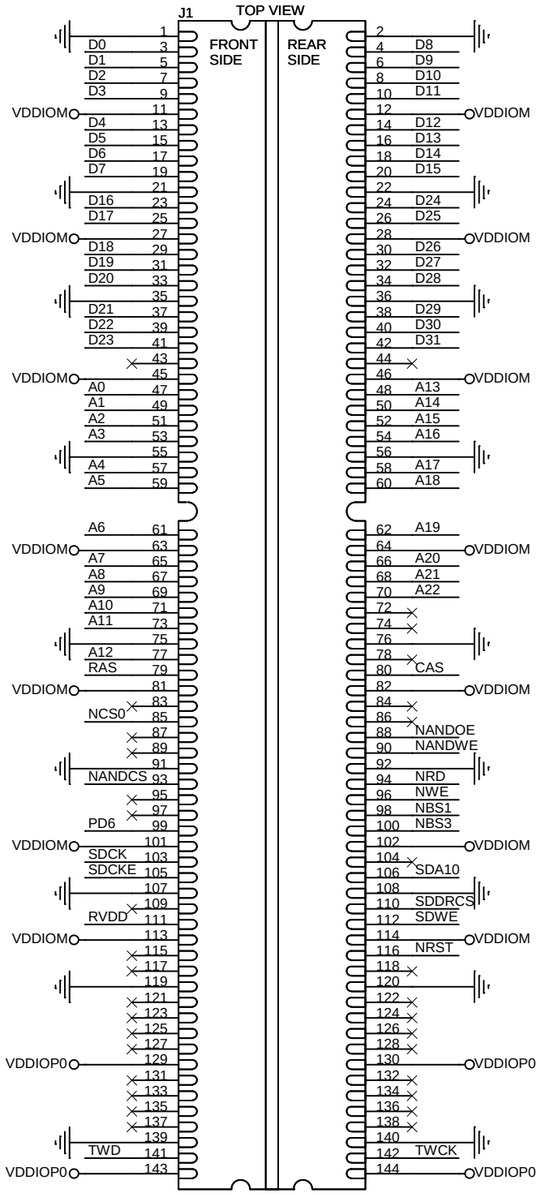
Section 18

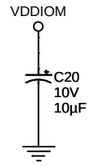
AT91CAP-MEM33 Schematics

18.1 Schematics

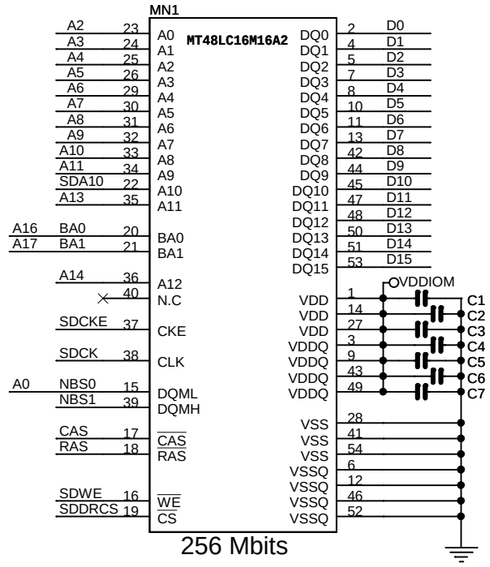
This section contains the following appended schematics:

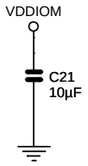
- AT91CAP-MEM33

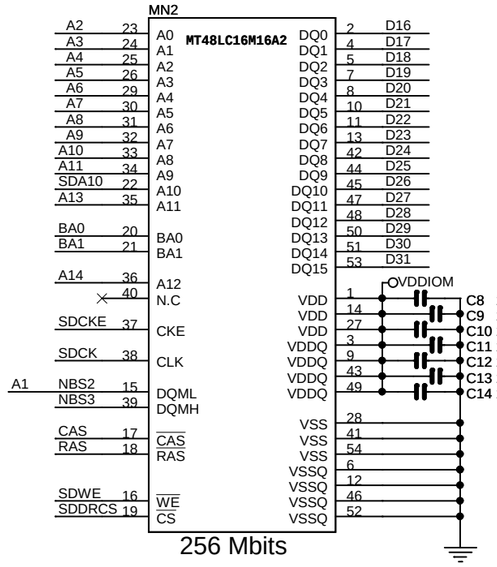




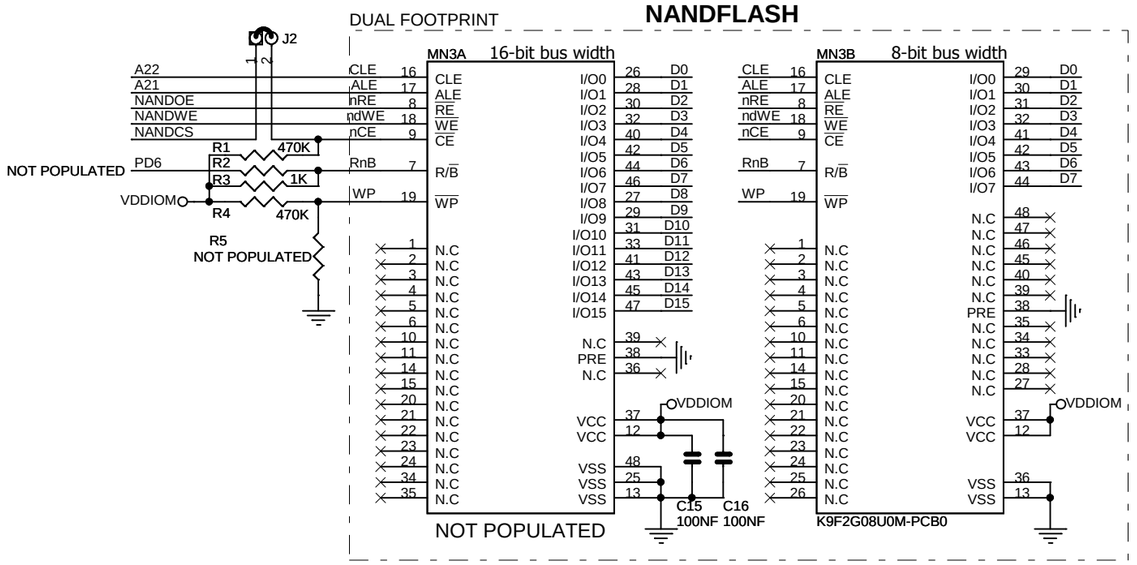
SDRAM



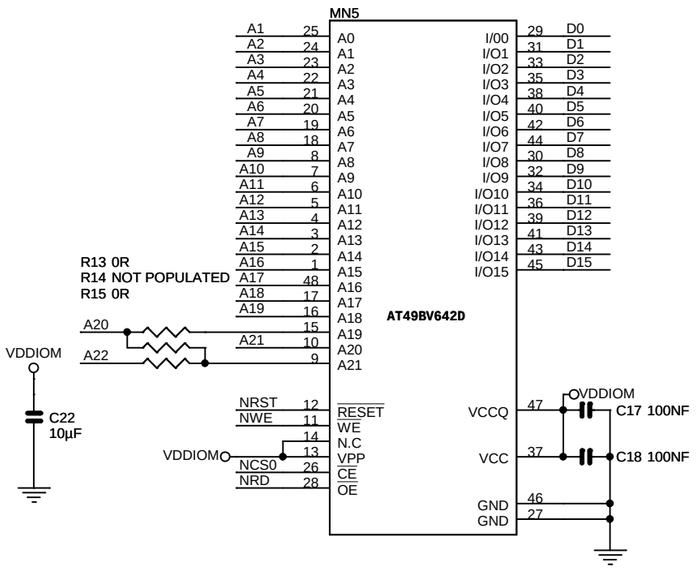


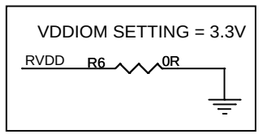


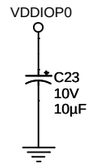
NANDFLASH

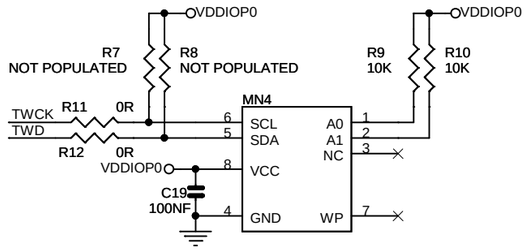


NORFLASH









SERIAL EEPROM

A	INIT EDIT	JPG	07-JUN-07	XXX	XX-XXX-XX	
REV	MODIF.	DES.	DATE	VER.	DATE	
AT91CAP9-EMV				REV.	SHEET	
AT91CAP-MEM33	SCALE 1/1			A	1/1	

Section 19

Errata

19.1 Known Errata

There are presently no known errata on any of the boards associated with the AT91CAP9A-DK development system.

Section 20

Revision History

20.1 Revision History

Document	Comments	Change Request Ref.
6321B	Section 3.14 ”FPGA Extension” on page 3-5, Warning updated.and update to Table 3-1, “FPGA IO Overlapping Table. Added Section 3.14.3, ” “Mistral” Extension Connectors” and updates to Table 3-2, “J-8 (male) Pin Assignment Table, Table 3-3, “J10 (female) Pin Assignment Table, Table 3-4, “PCI64 Extension Connector Table. Section 3.14.4, ” USB Device interfaces”, Warning updated and update to Table 3-5, “USB Interface and FPGA Connection.	4509
	Section 7.7.6, ” FPGA Pinout Tables” Updates to: Table 7-5, “FPGA Pins Sorted by Bank/Signal Name and Table 7-6, “FPGA Pins Sorted by Signal Name.	
	Section 15, “AT91CAP-DKM Schematics” updated	
	Section 16, “AT91CAP9A-DKZ Schematics” updated	
	Section 17, “AT91CAP-MEM18 Schematics” updated	
	Section 18, “AT91CAP-MEM33 Schematics” updated	
6321A	First issue.	

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