DATA SHEET

SCC2681T

Dual asynchronous receiver/transmitter (DUART)

Product data

2004 Apr 06

Philips
Semiconductors

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DESCRIPTION

The Philips Semiconductors SCC2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. The SCC2681T features a faster bus cycle time than the standard SCC2681. The quick bus cycle eliminates or reduces the need for wait states with fast CPUs and permits high throughput in I/O intensive systems. Higher external clock rates may be used with the transmitter, receiver and counter timer which in turn provide greater versatility in baud rate generation. The SCC2681T interfaces directly with microprocessors and may be used in a polled or interrupt driven system. It is manufactured in CMOS technology.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16× clock derived from a programmable counter/timer, or an external 1× or 16× clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruple buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

Also provided on the SCC2681T are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

For a complete functional description and programming information for the SCC2681T, refer to the SCC2681 product specification.

FEATURES

- Fast bus cycle times reduce or eliminate CPU wait states
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 22 fixed rates: 50 to 115.2 k baud
  - Non-standard rates to 115.2
  - Non-standard user-defined rate derived from programmable counter/timer
  - External 1× or 16× clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - 100 kΩ typical pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt/DMA signals
  - Auto 485 turn-around
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates:
  - 1× – 1 MB/sec transmitter and receiver
  - 16× – 500 kB/sec receiver and 250 kB/sec transmitter
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5 V power supply
- Commercial temperature range

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5 V ± 10%, T_{amb} = 0 °C to +70 °C	DWG #
44-Pin Plastic Lead Chip Carrier (PLCC)	SCC2681TC1A44	SOT187-2

NOTE: For a full register description and programming information see the SCC2681.

BLOCK DIAGRAM

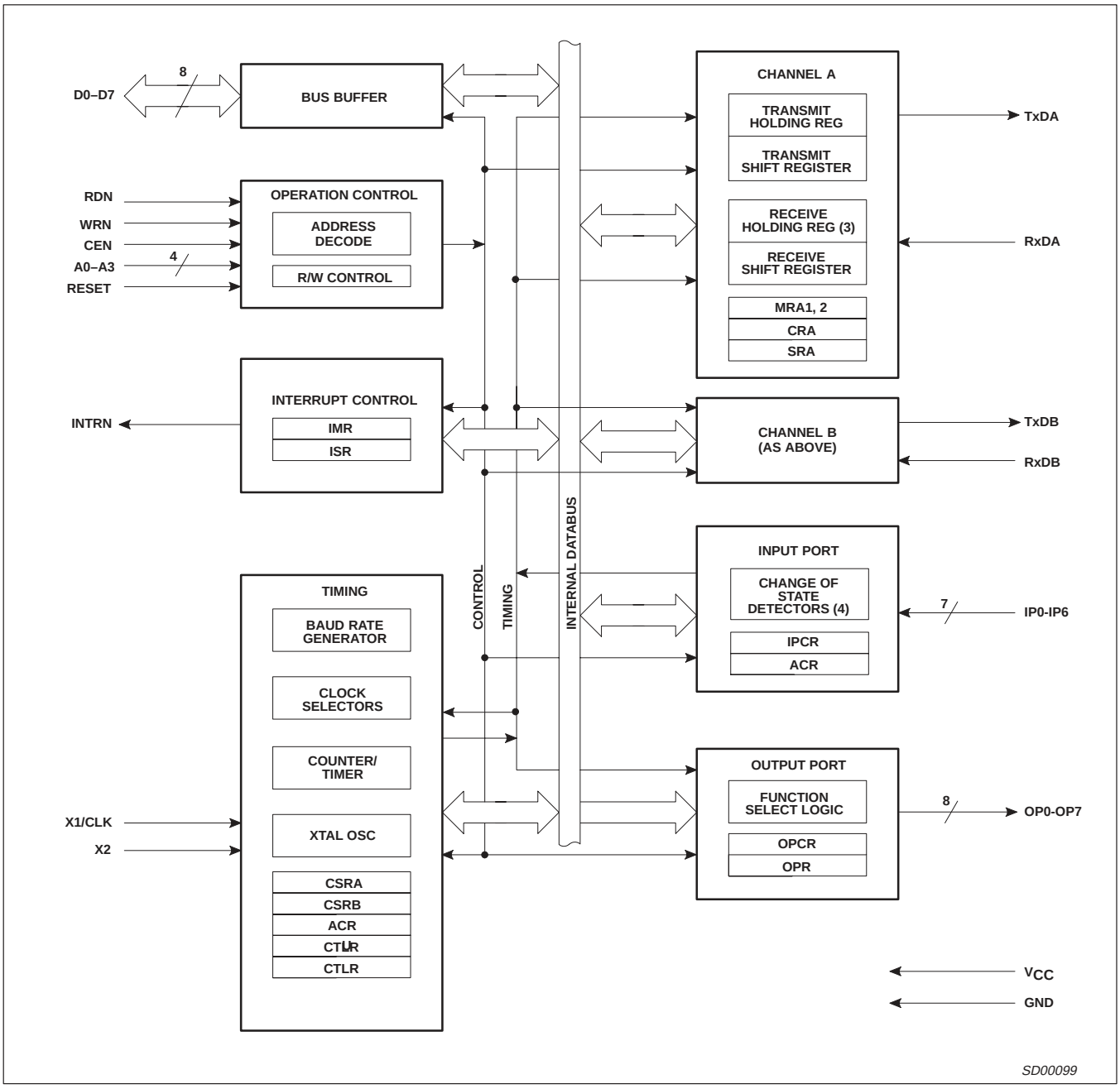


Figure 1. Block Diagram

NOTE:
Refer to SCC2681 for functional description.

PIN CONFIGURATION

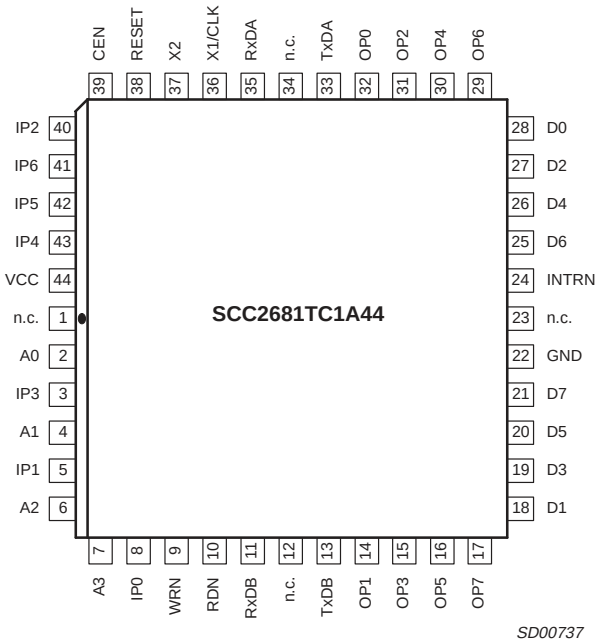


Figure 2. Pin configuration

PIN DESCRIPTION

MNEMONIC	PIN	TYPE	NAME AND FUNCTION
D0–D7	21, 25, 20, 26, 19, 27, 18, 28	I/O	**Data Bus:** Bidirectional three-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	39	I	**Chip Enable:** Active LOW input signal. When LOW, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the WRN, RDN, and A0–A3 inputs. When CEN is HIGH, the DUART places the D0–D7 lines in the three-state condition.
WRN	9	I	**Write Strobe:** When LOW and CEN is also LOW, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	10	I	**Read Strobe:** When low and CEN is also LOW, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	2, 4, 6, 7	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	38	I	**Reset:** A HIGH level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the HIGH state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (HIGH) state. Clears Test modes, sets MR pointer to MR1.
INTRN	24	O	**Interrupt Request:** Active-LOW, open-drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	36	I	**Crystal 1:** Crystal connection or an external clock input. A crystal of a clock the appropriate frequency (nominally 3.6864 MHz) must be supplied at all times. For crystal connections see Figure 7, Clock Timing.
X2	37	I	**Crystal 2:** Crystal connection. See Figure 7. If a crystal is not used it is best to keep this pin not connected. It **must not** be grounded.
RxDA	35	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. ‘Mark’ is HIGH, ‘space’ is LOW.
RxDB	11	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. ‘Mark’ is HIGH, ‘space’ is LOW.

MNEMONIC	PIN	TYPE	NAME AND FUNCTION
TxDA	33	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is HIGH, 'space' is LOW.
TxDB	13	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is HIGH, 'space' is LOW.
OP0	32	O	**Output 0:** General purpose output, or channel A request to send (RTSAN, active-LOW). Can be deactivated automatically on receive or transmit.
OP1	14	O	**Output 1:** General purpose output, or channel B request to send (RTSBN, active-LOW). Can be deactivated automatically on receive or transmit.
OP2	31	O	**Output 2:** General purpose output, or channel A transmitter 1× or 16× clock output, or channel A receiver 1× clock output.
OP3	15	O	**Output 3:** General purpose output, or open-drain, active-LOW counter/timer interrupt output, or channel B transmitter 1× clock output, or channel B receiver 1× clock output.
OP4	30	O	**Output 4:** General purpose output, or channel A open-drain, active-LOW, RxRDYA/FFULLA interrupt output.
OP5	16	O	**Output 5:** General purpose output, or channel B open-drain, active-LOW, RxRDYB/FFULLB interrupt output.
OP6	29	O	**Output 6:** General purpose output, or channel A open-drain, active-LOW, TxRDYA interrupt output.
OP7	17	O	**Output 7:** General purpose output, or channel B open-drain, active-LOW TxRDYB interrupt output.
IP0	8	I	**Input 0:** General purpose input, or channel A clear to send active-LOW input (CTSAN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP1	5	I	**Input 1:** General purpose input, or channel B clear to send active-LOW input (CTSBN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP2	40	I	**Input 2:** General purpose input, or counter/timer external clock input. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP3	3	I	**Input 3:** General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP4	43	I	**Input 4:** General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP5	42	I	**Input 5:** General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP6	41	I	**Input 6:** General purpose input, or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
V_{CC}	44	I	**Power Supply:** +5 V supply input.
GND	22	I	**Ground**
n.c.	1, 12, 23, 34		**not connected**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_{amb}	Operating ambient temperature range[2]	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C
	All voltages with respect to GND[3]	–0.5 to +6.0	V
	Pin voltage range	V_{SS} – 0.5 to V_{CC} + 0.5	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150 °C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

T_{amb} = 0 °C to +70 °C; V_{CC} = +5.0 V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage (except X1/CLK)	$T_{amb} \geq 0$ °C	2.0	–	–	V
V_{IH}	HIGH-level input voltage (except X1/CLK)	$T_{amb} <$ 0 °C	2.5	–	–	V
V_{IH}	HIGH-level input voltage (X1/CLK)		0.8 V_{CC}	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 2.4 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage (except open-drain outputs)[4]	I_{OH} = –400 µA	V_{CC} – 0.5	–	–	V
I_{IX1}	X1/CLK input current	V_{IN} = 0 V to V_{CC}	–10	–	+10	µA
I_{ILX1}	X1/CLK input LOW current – operating	V_{IN} = 0 V	–75	–	0	µA
I_{IHX1}	X1/CLK input HIGH current – operating	$V_{IN} = V_{CC}$	0	–	75	µA
I_{OHX2}	X2 output HIGH current – operating	$V_{OUT} = V_{CC}$; X1 = 0	0	–	+75	µA
I_{OHX2S}	X2 output HIGH short circuit current – operating	V_{OUT} = 0 V; X1 = 0	–10	–	–1	mA
I_{OLX2}	X2 output LOW current – operating	V_{OUT} = 0 V; X1 = V_{CC}	–75	–	0	µA
I_{OLX2S}	X2 output LOW short circuit current – operating	$V_{OUT} = V_{CC}$; X1 = V_{CC}	1	–	10	mA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 V to V_{CC}	–10	–	+10	µA
	Input port pins	V_{IN} = 0 V to V_{CC}	–20	–	+10	µA
I_{OZH}	Output off current HIGH, 3-state data bus	$V_{IN} = V_{CC}$	–	–	10	µA
I_{OZL}	Output off current LOW, 3-state data bus	V_{IN} = 0 V	–10	–	–	µA
I_{ODL}	Open-drain output LOW current in off-state	V_{IN} = 0 V	–10	–	–	µA
I_{ODH}	Open-drain output HIGH current in off-state	$V_{IN} = V_{CC}$	–	–	10	µA
I_{CC}	Power supply current[5]					
	Operating mode	CMOS input levels	–	–	10	mA

NOTES:

1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4 V and 2.4 V with a transition time of 5 ns maximum. For X1/CLK this swing is between 0.4 V and 4.4 V. All time measurements are referenced at input voltages of 0.8 V and 2.0 V and output voltages of 0.8 V and 2.0 V, as appropriate.
3. Typical values are at +25 °C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150 pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50 pF, R_L = 2.7 kΩ to V_{CC}.
5. All outputs are disconnected. Inputs are switching between CMOS levels of V_{CC} – 0.2 V and V_{SS} + 0.2 V.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4]

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Reset timing (see Figure 3)					
t_{RES}	Reset pulse width	1.0	–	–	µs
Bus timing (see Figure 4) (Note 5)					
t_{AVEL}	A0–A3 set-up to RDN and CEN, or WRN and CEN LOW	0	–	–	ns
t_{ELAX}	RDN and CEN, or WRN and CEN LOW to A0–A3 invalid	100	–	–	ns
t_{RLRH}	RDN and CEN LOW to RDN or CEN HIGH	120	–	–	ns
t_{EHEL}	CEN HIGH to CEN LOW[6, 7]	110	–	–	ns
t_{RLDA}	CEN and RDN LOW to data outputs active	15	–	–	ns
t_{RLDV}	CEN and RDN LOW to data valid	–	–	100	ns
t_{RHDI}	CEN or RDN HIGH to data invalid	10	–	–	ns
t_{RHDF}	CEN or RDN HIGH to data outputs floating	–	–	65	ns
t_{WLWH}	WRN and CEN LOW to WRN or CEN HIGH	75	–	–	ns
t_{DVWH}	Data input valid to WRN or CEN HIGH	35	–	–	ns
t_{WHDI}	WRN or CEN HIGH to data invalid	15	–	–	ns
Port timing (see Figure 5)					
t_{PS}	Port input set-up time before RDN LOW	0	–	–	ns
t_{PH}	Port input hold time after RDN HIGH	0	–	–	ns
t_{PD}	Port output valid after WRN HIGH	–	–	200	ns
Interrupt timing (see Figure 6)					
t_{IR}	INTRN (or OP3–OP7 when used as interrupts) negated from:				
	Read RHR (RxRDY/FFULL interrupt)	–	–	200	ns
	Write THR (TxRDY interrupt)	–	–	200	ns
	Reset command (delta break interrupt)	–	–	200	ns
	Stop C/T command (counter interrupt)	–	–	200	ns
	Read IPCR (input port change interrupt)	–	–	200	ns
	Write IMR (clear of interrupt mask bit)	–	–	200	ns
Clock timing (see Figure 7)					
t_{CLK}	X1/CLK HIGH or LOW time	90			ns
f_{CLK}	X1/CLK frequency	2		4	MHz
t_{CTC}	CTCLK (IP2) HIGH or LOW time	55			ns
f_{CTC}	CTCLK (IP2) frequency[8]	0		8	MHz
t_{RX}	RxC HIGH or LOW time	55			ns
f_{RX}	RxC frequency (16×)[8]	0	3.6864	8	MHz
	(1×)[8]	0		1	MHz
t_{TX}	TxC HIGH or LOW time	110			ns
f_{TX}	TxC frequency (16×)[8]	0		4	MHz
	(1×)[8]	0		1	MHz
Transmit timing (see Figure 8)					
t_{TXD}	TxD output delay from TxC external clock input on IP pin	–	–	300	ns
t_{TCS}	Output delay from TxC LOW at OP pin to TxD data output	0	–	100	ns
Receive timing (see Figure)					
t_{RXS}	RxD data set-up time before RxC HIGH at external clock input on IP pin	200	–	–	ns
t_{RXH}	RxD data hold time after RxC HIGH at external clock input on IP pin	25	–	–	ns

NOTES:

1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4 V and 2.4 V with a transition time of 20 ns maximum. For X1/CLK this swing is between 0.4 V and 4.0 V. All time measurements are referenced at input voltages of 0.8 V and 2.0 V and output voltages of 0.8 V and 2.0 V as appropriate.
3. Typical values are at +25 °C, typical supply voltages, and typical processing parameters.

4. Test conditions for outputs: C_L = 150 pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50 pF, R_L = 2.7 kΩ to V_{CC}.
5. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, the parameter defines the minimum HIGH times between one CEN and the next. The RDN signal must be negated for t_{EHEL} to guarantee that any status register changes are valid. As a consequence, this minimum time must be met for the RDN input even if the CEN is used as the strobing signal for bus operations.
7. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
8. Minimum frequencies are not tested but are guaranteed by design.

Figure 3. Reset Timing

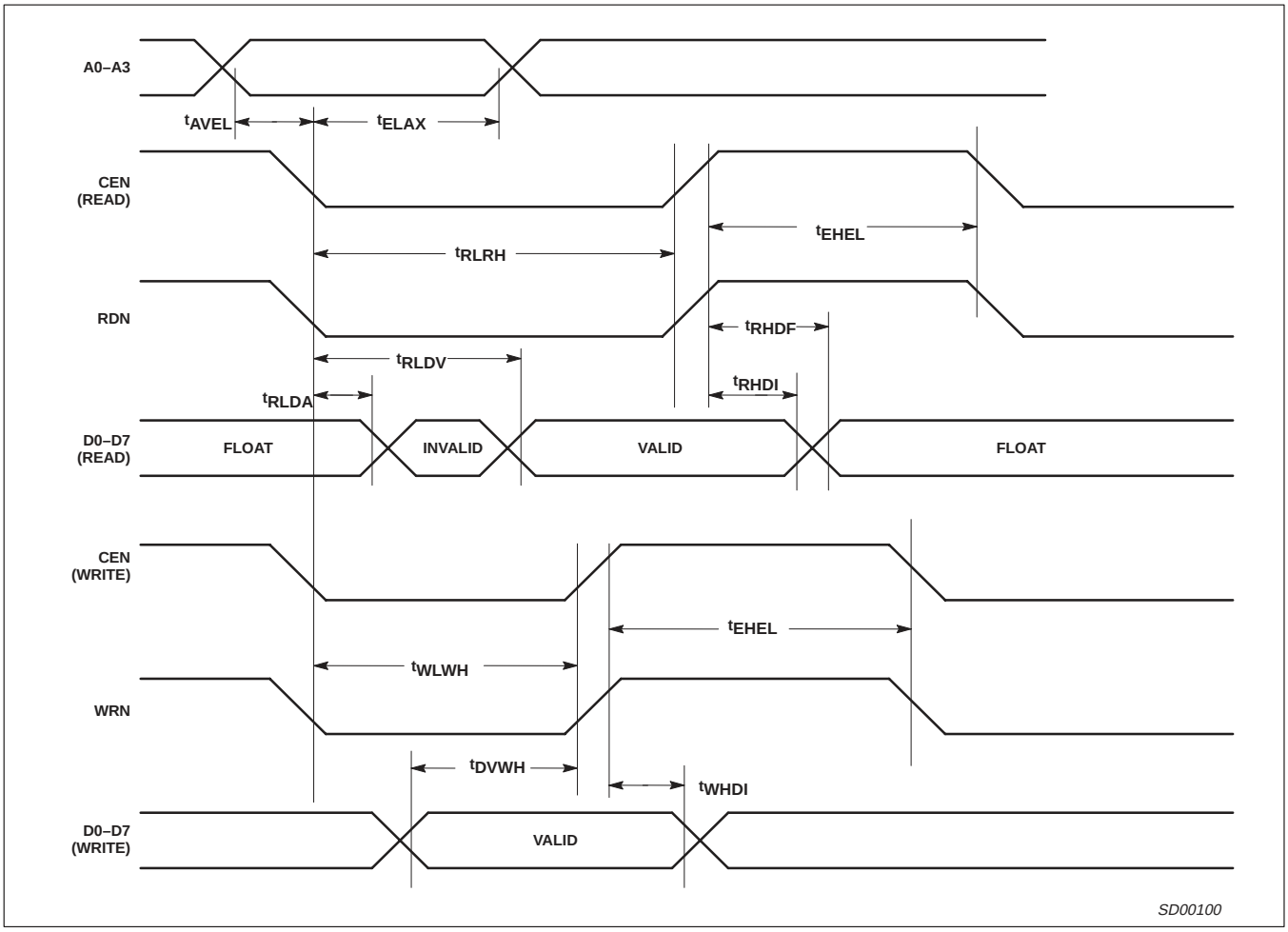


Figure 4. Bus Timing

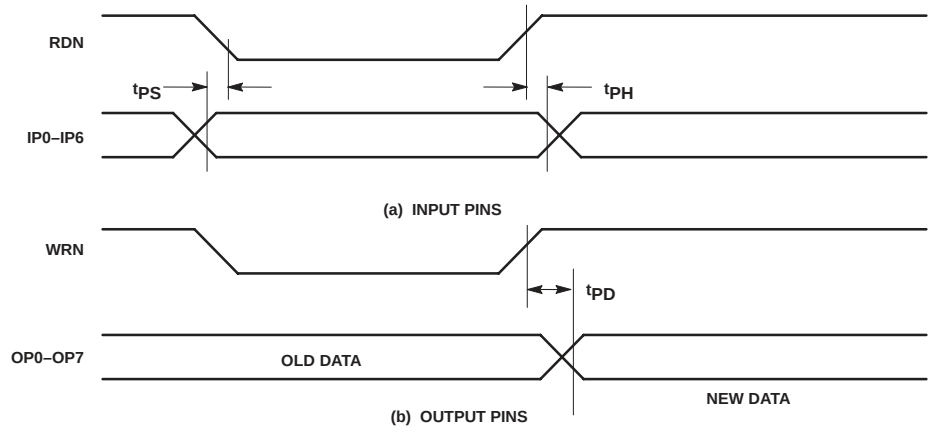
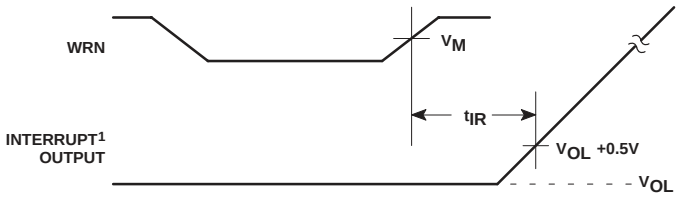


Figure 5. Port Timing



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

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Figure 6. Interrupt Timing

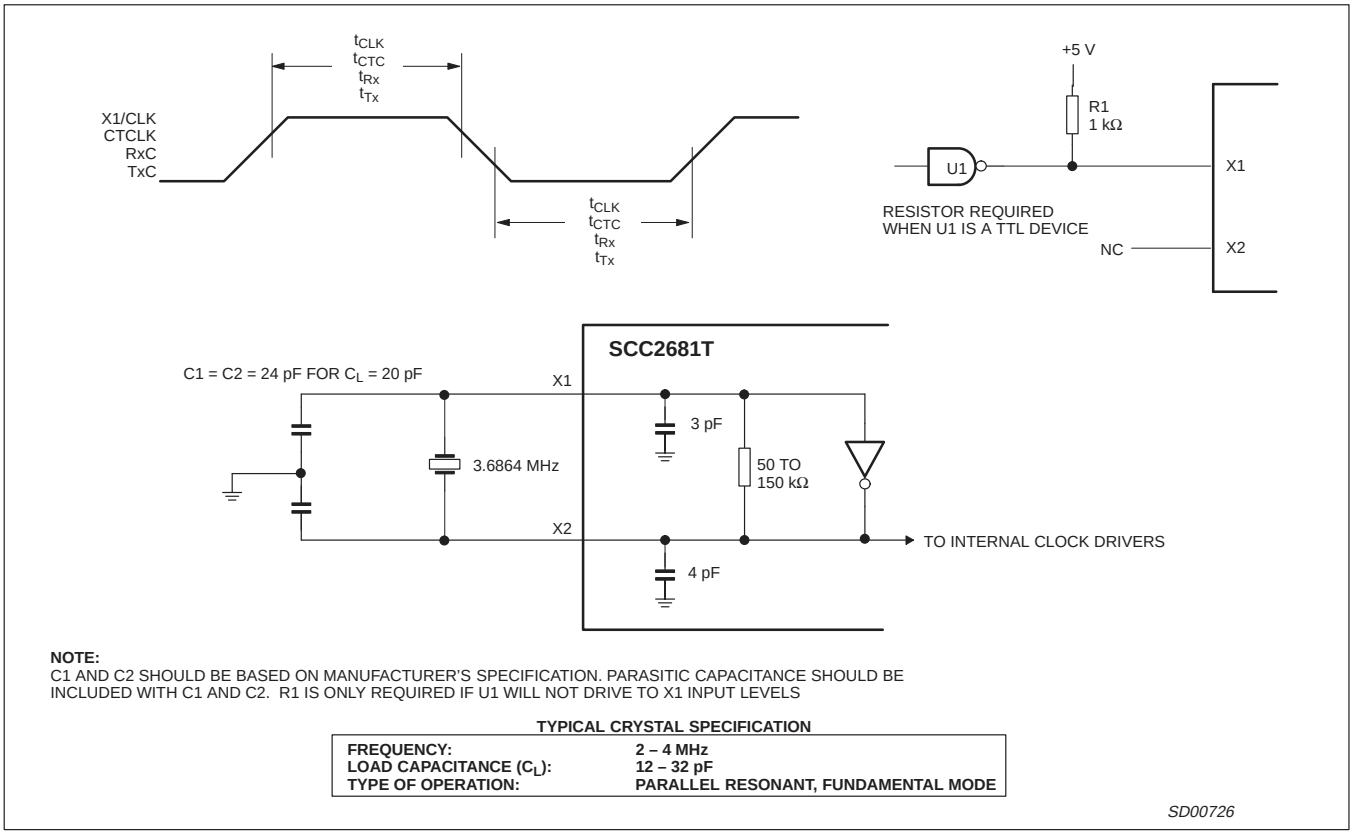


Figure 7. Clock Timing

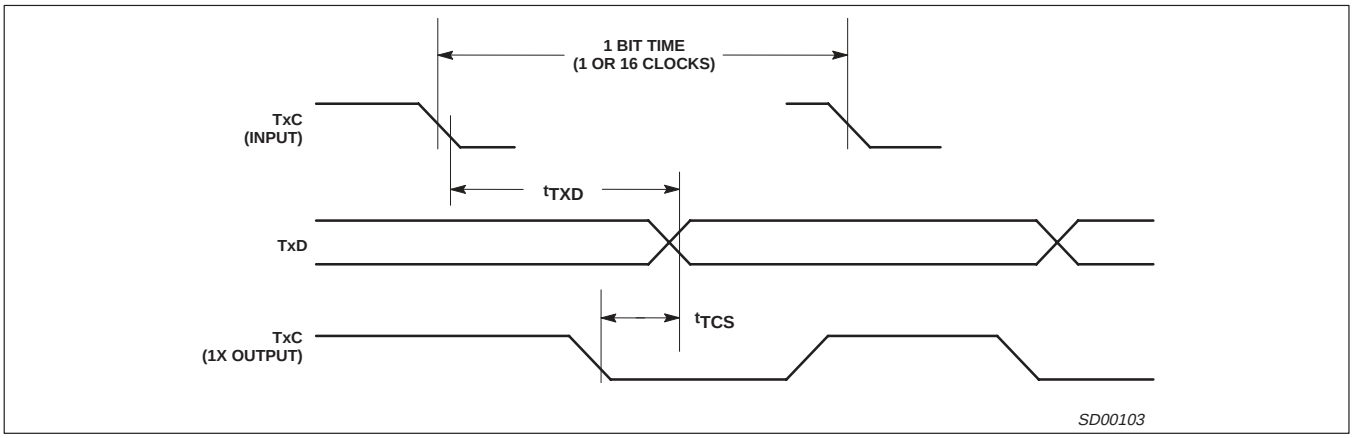


Figure 8. Transmit

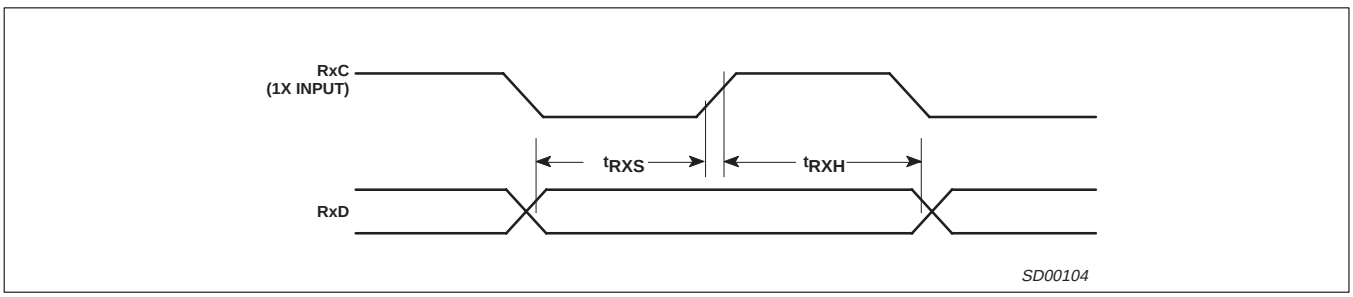
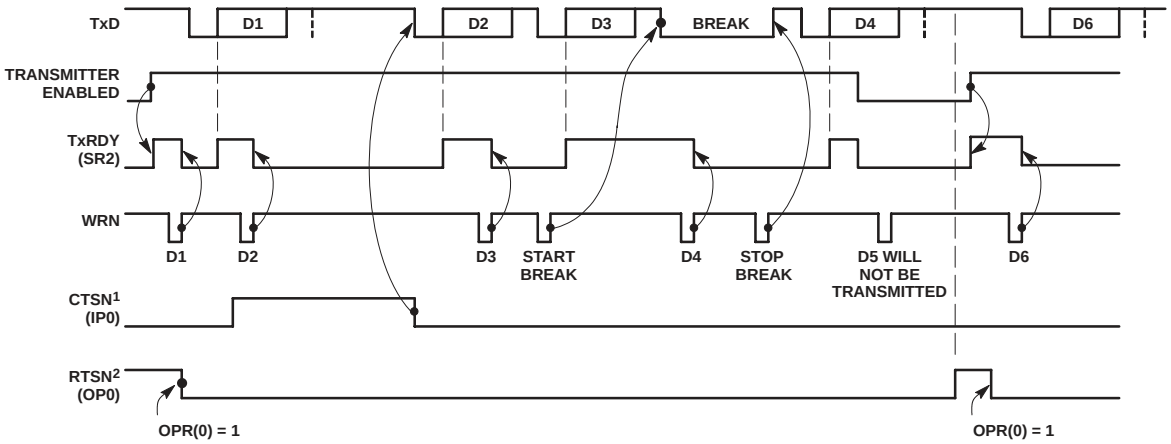


Figure 9. Receive



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

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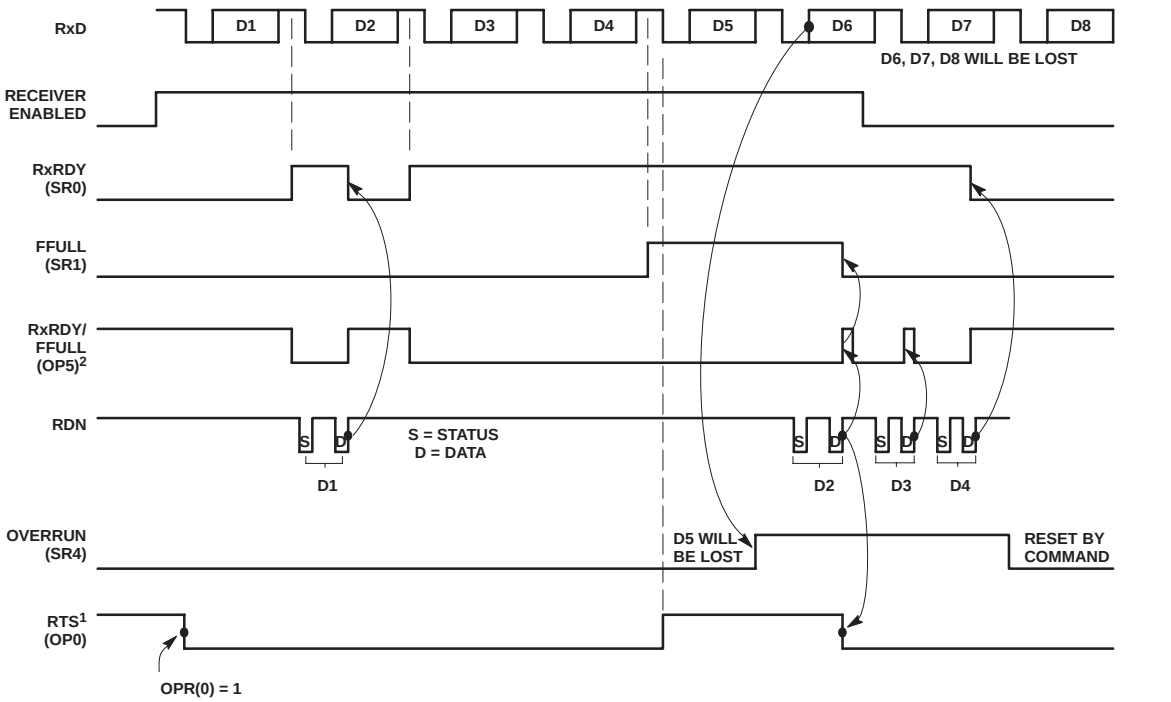
Figure 10. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR1(6) = 0.

SD00105

Figure 11. Receiver Timing

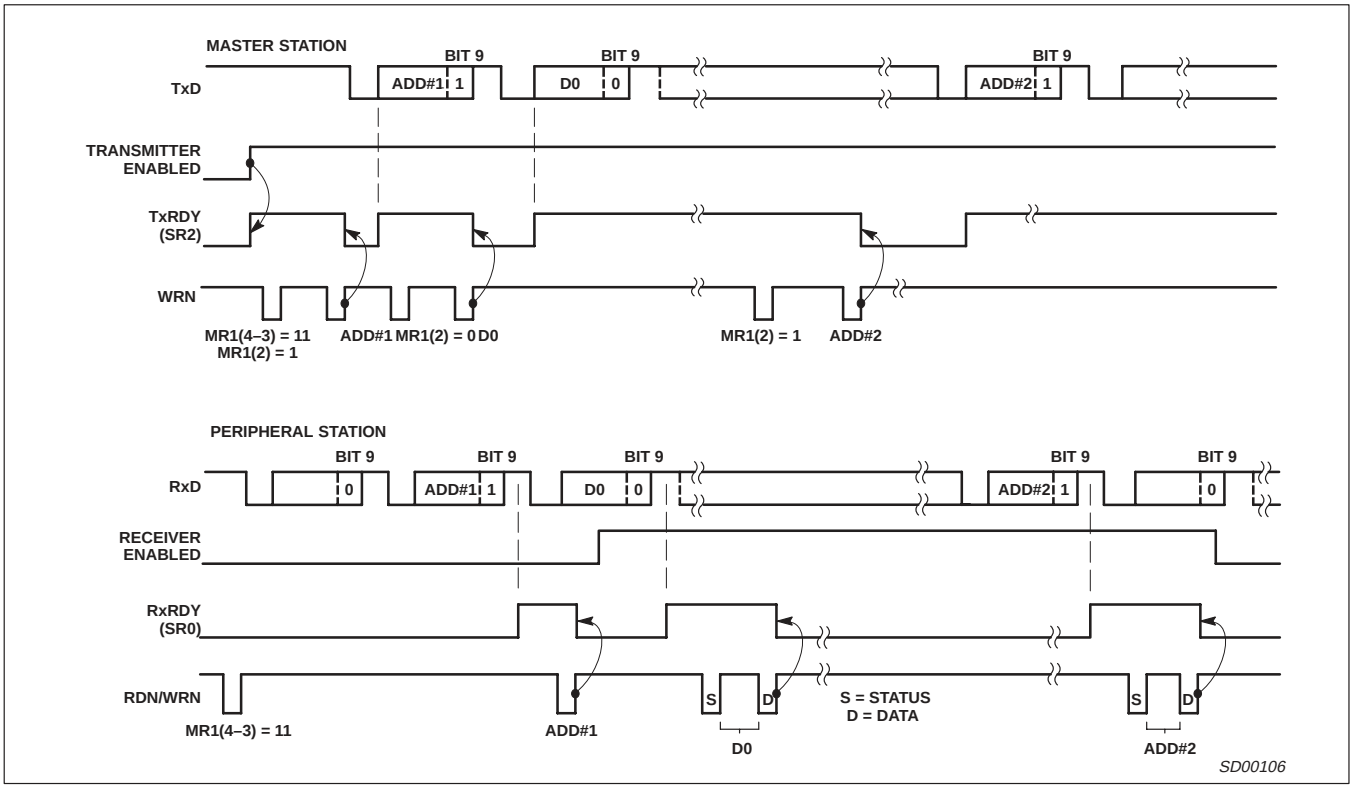
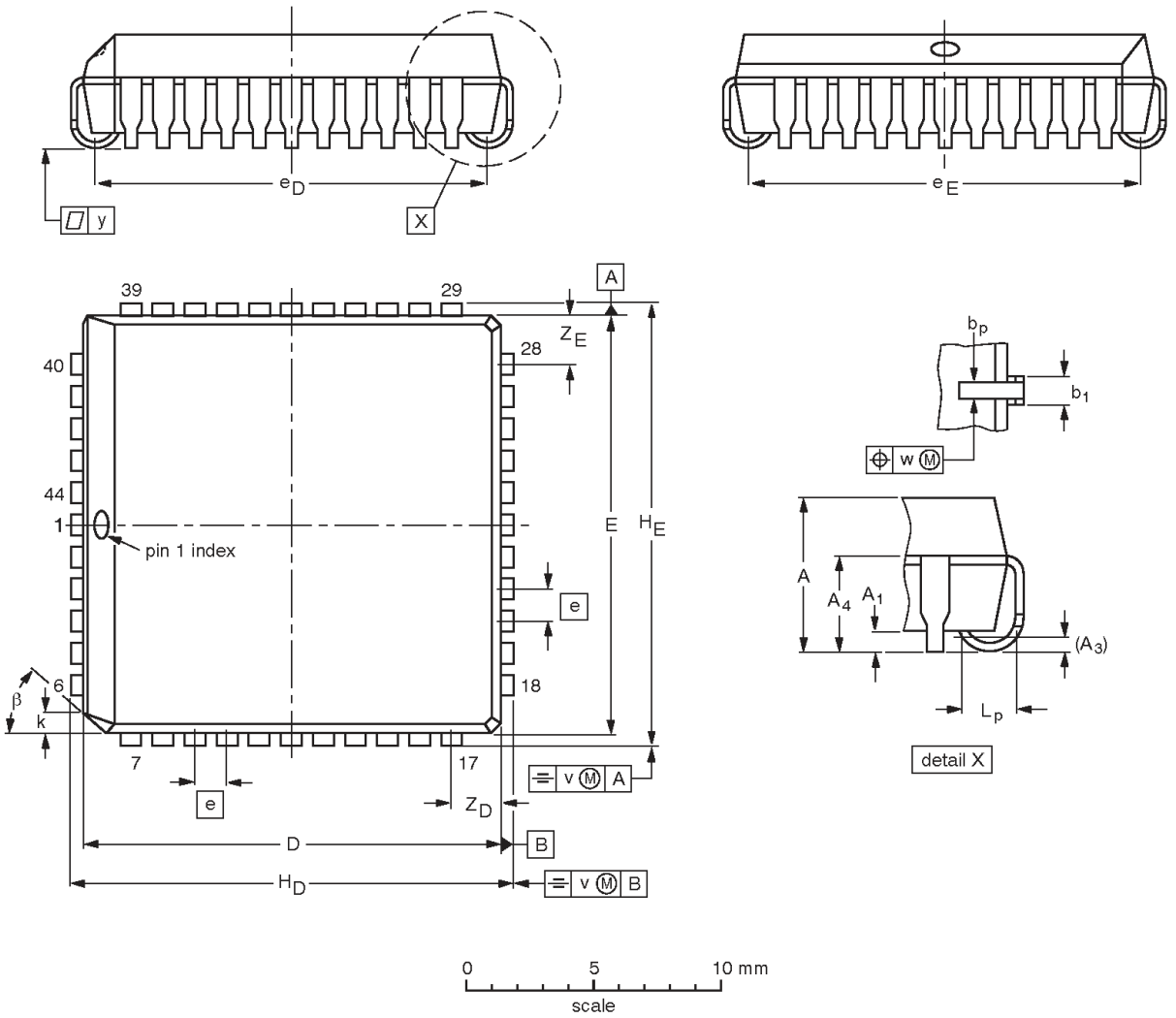


Figure 12. Wake-Up Mode

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

REVISION HISTORY

Rev	Date	Description
_1	20040406	**Product data (9397 750 12073). ECN 853-2446 01-A15014 of 15 December 2003.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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