

CM1263-02SE

Low Capacitance ESD Protection for High-Speed Serial Interfaces

Features

- 2 Channels of ESD Protection
- 0.85 pF Loading Capacitance per Channel Typical
- Provides ESD Protection to IEC61000-4-2 Level 4:
 - ± 8 kV Contact Discharge
 - ± 15 kV Air Discharge
- 5-Pin SOT-553 Package
- These Devices are Pb-Free and are RoHS Compliant

Applications

- LCD and Camera Data Lines in Wireless Handsets that Use High-speed Serial Interfaces such as MDDI, MIPI, MVI and MPL
- I/O Port Protection for Mobile Handsets, Notebook Computers, PDAs, etc.
- Wireless Handsets
- Handheld PCs/PDAs
- LCD and Camera Modules



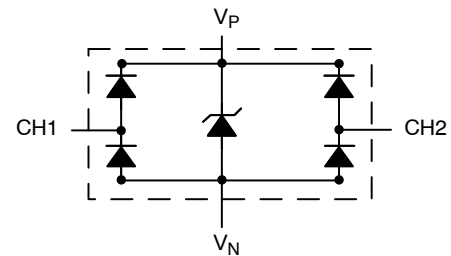
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SOT-553
SE SUFFIX
CASE 463B

BLOCK DIAGRAM



MARKING DIAGRAM



L63 = Specific Device Code
M = Date Code

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------|----------------------|------------------|
| CM1263-02SE | SOT-553 (Pb-Free) | 5000/Tape & Reel |

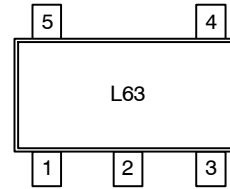
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

CM1263-02SE

Table 1. PIN DESCRIPTIONS

| 5-Pin, SOT-553 Package | |
|------------------------|----------------------|
| Pin | Description |
| 1 | V_P |
| 2 | V_N |
| 3 | NC |
| 4 | (CH1) ESD Channel #1 |
| 5 | (CH2) ESD Channel #2 |

PACKAGE / PINOUT DIAGRAM



SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

| Parameter | Rating | Units |
|--|--------------------------------|-------|
| Operating Supply Voltage ($V_P - V_N$) | 6.0 | V |
| Operating Temperature Range | -40 to +85 | °C |
| Storage Temperature Range | -65 to +150 | °C |
| DC Voltage at any channel input | $(V_N - 0.5)$ to $(V_P + 0.5)$ | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

CM1263-02SE

Table 3. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------|--|--|--------------|---------------|--------------|-------|
| V _P | Operating Supply Voltage (V _P - V _N) | | | 3.3 | 5.5 | V |
| I _P | Operating Supply Current | (V _P - V _N) = 3.3 V | | | 8.0 | μA |
| V _F | Diode Forward Voltage Top Diode Bottom Diode | I _F = 8 mA; T _A = 25°C | 0.60 0.60 | 0.80 0.80 | 0.95 0.95 | V |
| I _{LEAK} | Channel Leakage Current | T _A = 25°C; V _P = 5 V, V _N = 0 V, V _{TEST} = 0 to 5 V | | 0.1 | 1.0 | μA |
| C _{IN} | Channel Input Capacitance | At 1 MHz, V _P = 3.3 V, V _N = 0 V, V _{IN} = 1.65 V | | 0.85 | 1.2 | pF |
| ΔC _{IN} | Channel Input Capacitance Matching | At 1 MHz, V _P = 3.3 V, V _N = 0 V, V _{IN} = 1.65 V | | 0.02 | | pF |
| V _{ESD} | ESD Protection Peak Discharge Voltage at any channel input, in system: a) Contact Discharge per IEC 61000-4-2 standard b) Air Discharge per IEC 61000-4-2 standard | T _A = 25°C; (Notes 2 and 3) T _A = 25°C; (Note 3) | | ±8 ±15 | | kV |
| V _{CL} | Channel Clamp Voltage Positive Transients Negative Transients | T _A = 25°C, I _{PP} = 1 A, t _P = 8/20 μS (Note 3) | | +9.96 -1.6 | | V |
| R _{DYN} | Dynamic Resistance Positive Transients Negative Transients | I _{PP} = 1 A, t _P = 8/20 μS Any I/O pin to Ground; (Note 3) | | 0.96 0.5 | | Ω |

1. All parameters specified at T_A = -40°C to +85°C unless otherwise noted.
2. Standard IEC 61000-4-2 with C_{Discharge} = 150pF, R_{Discharge} = 330 Ω, V_P = 3.3 V, V_N grounded.
3. These measurements performed with no external capacitor on V_P (V_P floating).

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

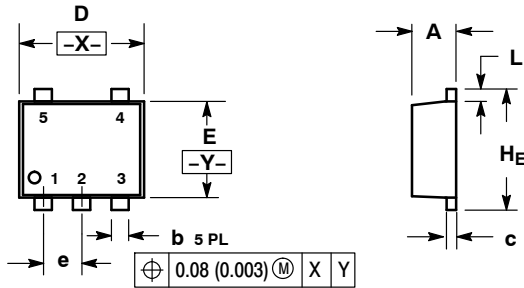
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SCALE 4:1

SOT-553, 5 LEAD CASE 463B ISSUE C

DATE 20 MAR 2013

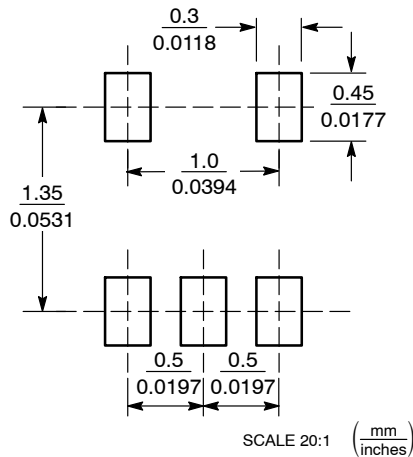


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | MILLIMETERS | | | INCHES | | |
|----------------|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.009 | 0.011 |
| c | 0.08 | 0.13 | 0.18 | 0.003 | 0.005 | 0.007 |
| D | 1.55 | 1.60 | 1.65 | 0.061 | 0.063 | 0.065 |
| E | 1.15 | 1.20 | 1.25 | 0.045 | 0.047 | 0.049 |
| e | 0.50 BSC | | | 0.020 BSC | | |
| L | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| H _E | 1.55 | 1.60 | 1.65 | 0.061 | 0.063 | 0.065 |

RECOMMENDED SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

STYLE 2:

- PIN 1. CATHODE
- 2. COMMON ANODE
- 3. CATHODE 2
- 4. CATHODE 3
- 5. CATHODE 4

STYLE 3:

- PIN 1. ANODE 1
- 2. N/C
- 3. ANODE 2
- 4. CATHODE 2
- 5. CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
- 2. DRAIN 1/2
- 3. SOURCE 1
- 4. GATE 1
- 5. GATE 2

STYLE 5:

- PIN 1. ANODE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. CATHODE

STYLE 6:

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. EMITTER 1
- 4. COLLECTOR 1
- 5. COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

STYLE 8:

- PIN 1. CATHODE
- 2. COLLECTOR
- 3. N/C
- 4. BASE
- 5. EMITTER

STYLE 9:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. ANODE
- 5. ANODE

| | | |
|-------------------------|----------------------------------|--|
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| NEW STANDARD: | | |
| DESCRIPTION: | SOT-553, 5 LEAD | PAGE 1 OF 2 |



| ISSUE | REVISION | DATE |
|-------|---|-------------|
| A | ADDED STYLES 3–9. REQ. BY D. BARLOW | 11 NOV 2003 |
| B | ADDED NOMINAL VALUES AND UPDATED GENERIC MARKING DIAGRAM. REQ. BY HONG XIAO | 27 MAY 2005 |
| C | UPDATED DIMENSIONS D, E, AND HE. REQ. BY J. LETTERMAN. | 20 MAR 2013 |
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