MP2661

4.65V System, 500mA, I^2C-Controlled Battery Charger with Power Path Management for Single-Cell Li-Ion Battery

The Future of Analog IC Technology

DESCRIPTION

The MP2661 is a highly integrated, single-cell, lithium-ion (Li-ion) and lithium-polymer (Li-polymer) battery charger with system power path management for space-limited, portable applications. The MP2661 uses input power from either an AC adapter or a USB port to supply the system load and charge the battery independently. The charger features constant current pre-charge (PRE.C), constant current (CC) fast charge, and constant voltage (CV) regulation, charge termination, and auto-recharge.

The power path management function ensures continuous power to the system by automatically selecting the input, the battery, or both to power the system. This power stage features a low dropout regulator from the input to the system and a 100mΩ switch from the battery to the system. Power path management separates the charging current from the system load, which allows for proper charge termination and keeps the battery in full-charge mode.

The MP2661 provides short-circuit protection (SCP) by limiting the current from the input to the system, and the battery to the system. SCP protects the Li-ion battery from being damaged by excessively high currents. If the battery voltage (V_{BATT}) drops below its configurable under-voltage lockout (UVLO) threshold, then the path between the battery and the system is cut off to prevent the Li-ion battery from being over-discharged. An integrated I^2C control interface allows the MP2661 to program the charging parameters, such as the input current limit (I_{IN_LIM}), minimum input voltage (V_{IN_MIN}) regulation, charging current, battery regulation voltage, safety timer, and battery UVLO.

The MP2661 is available in a WLCSP-9 (1.55mmx1.55mm) package.

FEATURES

- Fully Autonomous Charger for Single-Cell Li-Ion and Li-Polymer Batteries
- Complete Power Path Management for Simultaneously Powering the System and Charging the Battery
- ±0.5% Charging Voltage Accuracy
- 13V Maximum Voltage for the Input Source
- I^2C Interface for Setting Charging Parameters and Status Reporting
- Fully Integrated Power Switches and No External Blocking Diode Required
- Built-In Robust Charging Protection Including Battery Temperature Monitoring and Programmable Timer
- PCB Over-Temperature Protection (PCB_OTP)
- System Reset Function
- Integrated Battery Disconnect Function
- Thermal Limiting Regulation On-Chip
- Safety-Related Certification:
  - IEC 62368-1 CB Certification
- Available in a WLCSP-9 (1.55mmx1.55mm) Package

APPLICATIONS

- Wearable Devices
- Smart Handheld Devices
- Fitness Accessories
- Smartwatches

TYPICAL APPLICATION

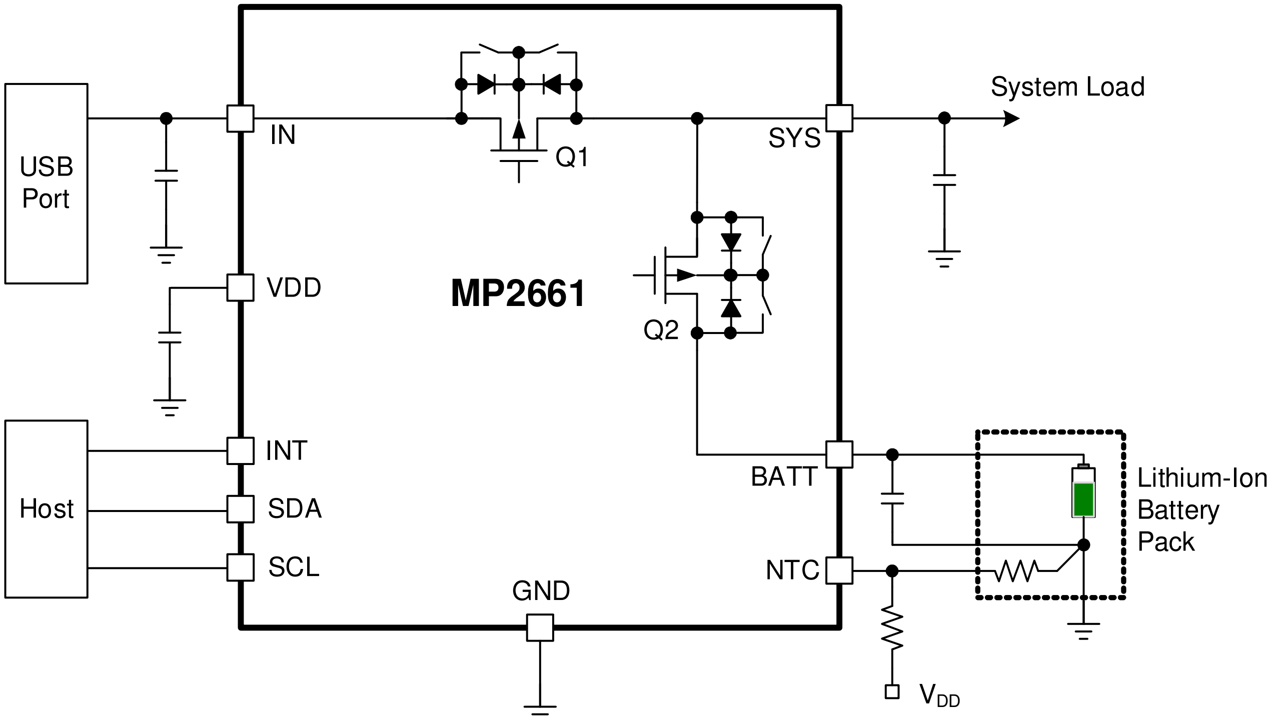


Table 1: Operation Modes (1)

Items	I²C Control			INT Pin	
	HIZ = 1	CEB = 1	FET_DIS = 1	H to L for 16s	H to L for 4s
LDO FET	Off	x	x	x	x
Battery FET (charging)	x	Off	Off	Off for 4s, then on	On
Battery FET (discharging)	x	x	Off	Off for 4s, then on	On

Note:

1) "x" means not applicable.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2661GC-xxxx**	WLCSP-9 (1.55mmx1.55mm)	*See Below*
EVKT-2661	Evaluation Kit	

* For Tape & Reel, add suffix -Z (e.g. MP2661GC-xxxx-Z).
**“xxxx” is the register setting option. The factory default is “0000”. This content can be viewed in the I²C register map. Please contact an MPS FAE to obtain an “xxxx” value.

TOP MARKING

EZY
LLL

EZ: Product code of MP2661GC
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-2661

EVKT-2661 kit contents (items listed below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2661-C-00A	MP2661 evaluation board	1
2	EVKT-USBI2C-02 bag	Includes one USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Includes datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

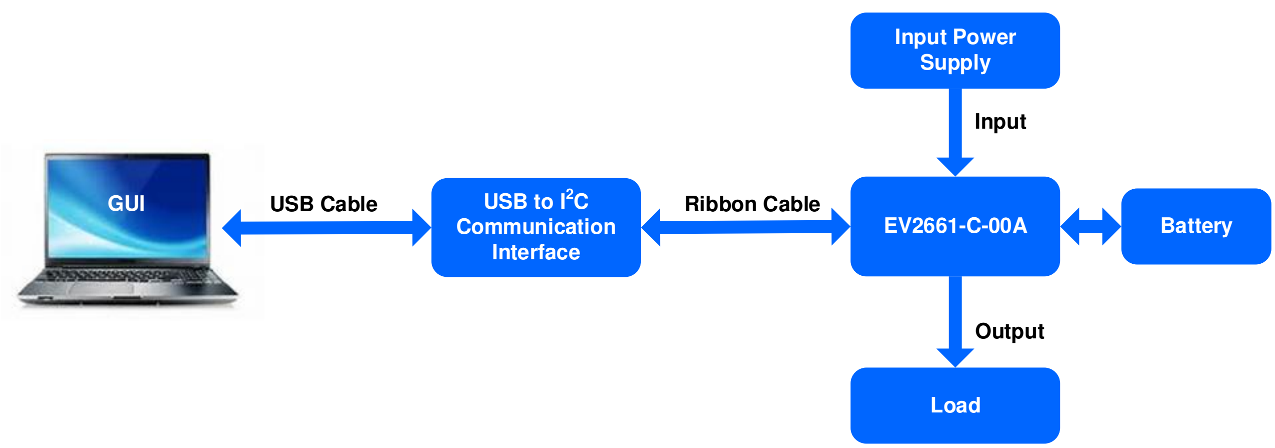
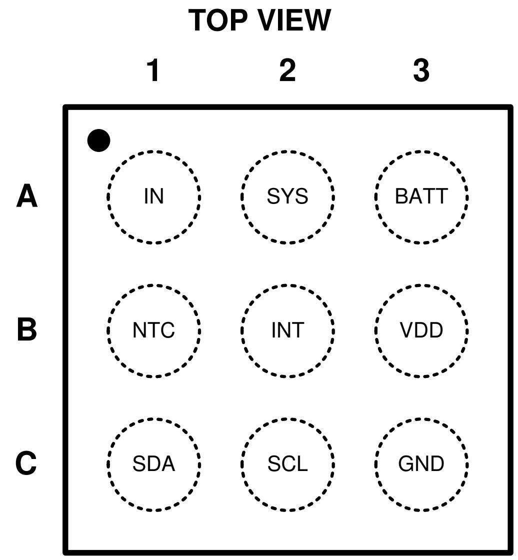


Figure 1: EVKT-2661 Evaluation Kit Set-Up

PACKAGE REFERENCE



WLCSP-9 (1.55mmx1.55mm)

PIN FUNCTIONS

Pin #	Name	I/O	Description
A1	IN	Power	**Input power.** Place a ceramic capacitor between the IN pin and GND, as close to the IC as possible.
A2	SYS	Power	**System power supply.** Place a ceramic capacitor between the SYS pin and GND, as close to the IC as possible.
A3	BATT	Power	**Battery.** Place a ceramic capacitor between the BATT pin and GND, as close to the IC as possible.
B1	NTC	I	**Temperature sense input.** Connect a negative temperature coefficient (NTC) thermistor to the NTC pin. Configure the hot and cold temperature windows via a resistor divider connected from VDD to NTC to GND. Charging is suspended when NTC is out of range.
B2	INT	I/O	**Interrupt signal.** The INT pin sends the charging status and fault interruption to the host. INT can also disconnect the system from the battery. Pull INT low for >16s. The battery FET turns off and on again after >4s, regardless of the INT state. The external INT pull-up resistor should be ≥300kΩ.
B3	VDD	Power	**Internal control power supply.** Connect a 0.1µF ceramic capacitor between the VDD pin to GND. No external load is allowed.
C1	SDA	I/O	**I²C interface data.** Connect the SDA pin to the logic rail via a 10kΩ resistor.
C2	SCL	I	**I²C interface clock.** Connect the SCL pin to the logic rail via a 10kΩ resistor.
C3	GND	Power	**Ground.**

ABSOLUTE MAXIMUM RATINGS (2)

V_{IN} .... -0.3V to +13V
All other pins to GND .... -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (3)
…………………………………………….0.88W
Junction temperature ………………………..150°C
Lead temperature (solder) .... 260°C
Storage temperature .... -65°C to +150°C

Recommended Operating Conditions (4)

Supply Voltage (V_{IN})…4.35V to 5.5V (USB Input)
I_{IN} .... Up to 455mA
I_{SYS} .... Up to 3.2A (6)
I_{CHG} .... Up to 455mA
V_{BATT} .... Up to 4.545V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

WLCSP-9 (1.55mmx1.55m) .... 114 ... 12 ... °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.
6) Guaranteed by design.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Source and Battery Protection						
Input voltage range	V_{IN}				13	V
Input operation voltage	V_{IN}		4.35	5	5.5	V
BATT input voltage (7)	V_{BATT}				4.5	V
Input over-voltage protection (OVP) threshold	V_{IN_OVP}	Input rising threshold	5.85	6	6.15	V
Input OVP hysteresis				350		mV
Input under-voltage lockout threshold	V_{IN_UVLO}	Input rising threshold	3.8	3.9	4	V
Input under-voltage lockout threshold hysteresis				170		mV
Input vs. battery headroom threshold	V_{HDRM}	Input rising vs. battery	100	130	160	mV
Input vs. battery headroom threshold hysteresis				85		mV
Battery under-voltage lockout threshold	V_{BATT_UVLO}	BATT voltage falling, configurable, REG01h, bits[2:0] = 100 - 2.8V	2.6	2.8	3	V
Battery UVLO Range		Configurable range	2.4		3.1	V
Battery under-voltage lockout threshold hysteresis				210		mV
Battery over-voltage protection	V_{BATT_OVP}	Rising, greater than V_{BATT_REG}		130		mV
		Falling, greater than V_{BATT_REG}		70		
Power Path Management						
Regulated system output voltage	V_{SYS_REG}	V_{IN} = 5.5V, I_{SYS} = 10mA, I_{CHG} = 0A	4.55	4.65	4.75	V
Input current limit	I_{IN_LIM}	REG00h, bits[2:0] = 000 - 85mA	65	75	85	mA
		REG00h, bits[2:0] = 001 - 130mA	102	116	130	
		REG00h, bits[2:0] = 100 - 265mA	230	247	265	
		REG00h, bits[2:0] = 111 - 455mA	400	428	455	
Input minimum voltage regulation	V_{IN_MIN}	I²C configurable range	3.88		5.08	V
		I²C setting V_{IN_MIN} = 4.2V	4.1	4.2	4.3	
SYS output voltage	V_{SYS}	Charging mode, V_{IN} = 5.5V, V_{BATT} = 3.7V	4.55	4.65	4.75	V
		Supplement mode, V_{BATT} = 3.7V, I_{BATT} = 100mA	3.6			
		$V_{IN} < V_{IN\_UVLO}$ and $V_{BATT} < V_{BATT\_UVLO}$		0		

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IN to SYS switch on resistance	R_{ON_SYS}	V_{IN} = 5V, I_{SYS} = 100mA		300	400	mΩ
Input quiescent current	I_{IN_Q}	V_{IN} = 5.5V, CEB = 0, charge enable, I_{CHG} = 0A, I_{SYS} = 0A		600		µA
		V_{IN} = 5.5V, CEB = 1, charge disable		480		
Battery quiescent current	I_{BATT_Q}	V_{IN} = 5V, CEB = 0, I_{SYS} = 0A, V_{BATT} = 4.3V		32		µA
		V_{IN} = 0V, CEB = 1, I_{SYS} = 0A, V_{BATT} = 4.35V, disable PCB_OTP, do not include the current from the external NTC resistor		11	13	
		V_{IN} = 0V, CEB = 1, I_{SYS} = 0A, V_{BATT} = 4.35V, enable PCB_OTP, do not include the current from the external NTC resistor		20	24	
		V_{BATT} = 4.5V, V_{IN} = V_{SYS} = GND, FET_DIS = 1, disconnect mode		4	5.5	
BATT input to SYS switch on resistance	R_{ON_BATT}	V_{IN} < 2V, V_{BATT} = 3.5V, I_{SYS} = 100mA		100	150	mΩ
Battery current regulation in discharge mode	I_{DSCHG}	Configurable range	400		3200 (7)	mA
BATT to SYS switch leakage		V_{BATT} = 4.5V, V_{IN} = V_{SYS} = GND, disconnect mode			1	µA
SYS reverse to BATT switch leakage		V_{SYS} = 6V, V_{IN} = 4.5V, V_{BATT} = GND, CEB = 1			1	µA
Battery discharge function controlled by INT (7)	t_{INT}	INT pull-low lasting time to turn off the battery discharge function		16		sec
		Battery FET lasts for the off time duration before auto-on		4		
Battery Charger						
Battery voltage regulation range	V_{BATT_REG}	Programmable range	3.6		4.545	V
Battery voltage (V_{BATT_REG} = 4.2V)	V_{BATT}	T_A = 25°C, I_{BATT} = 15mA	4.179	4.2	4.221	V
Battery charge voltage regulation	V_{BATT_REG}	V_{BATT_REG} = 4.2V, REG04h, bits[7:2] = 101000	4.179	4.2	4.221	V
		V_{BATT_REG} = 4.35V, REG04h, bits[7:2] = 110010	4.328	4.35	4.372	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Fast charge current	I_{CC}	V_{IN} = 5V, V_{BATT} = 3.8V, configurable range	8		535 (7)	mA
		V_{IN} = 5V, V_{BATT} = 3.8V, $I_{CC\_SETTING}$ = 93mA	88	93	98	
		V_{IN} = 5V, V_{BATT} = 3.8V, $I_{CC\_SETTING}$ = 246mA	232	248	263	
		V_{IN} = 5V, V_{BATT} = 3.8V, $I_{CC\_SETTING}$ = 399mA	376	401	426	
Junction temperature regulation (7)	T_{J_REG}	Junction temperature regulation, REG06h, bits[1:0] = 11 - 120°C		120		°C
Pre-charge current	I_{PRE}	Configurable range	6		27	mA
		$I_{PRE\_SETTING}$ = 6mA, REG03h, bits[1:0] = 00	2.5	4.7		
		$I_{PRE\_SETTING}$ = 20mA, REG03h, bits[1:0] = 10	14	18	22	
Charge termination current threshold	I_{TERM}	$I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), $I_{PRE\_SETTING}$ = 6mA	5	7	9	mA
		$I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), $I_{PRE\_SETTING}$ = 13mA	10	13.5	17	
		$I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), $I_{PRE\_SETTING}$ = 20mA	16	20	24	
		$I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), $I_{PRE\_SETTING}$ = 27mA	22	27	32	
		$I_{CC\_SETTING}$ ≥ 280mA, (REG02h, bit[4] = 1), $I_{PRE\_SETTING}$ = 6mA	10	13.5	17	
		$I_{CC\_SETTING}$ ≥ 280mA, (REG02h, bit[4] = 1), $I_{PRE\_SETTING}$ = 13mA	22	27	32	
		$I_{CC\_SETTING}$ ≥ 280mA, (REG02h, bit[4] = 1), $I_{PRE\_SETTING}$ = 20mA	34	42	49	
		$I_{CC\_SETTING}$ ≥ 280mA, (REG02h, bit[4] = 1), $I_{PRE\_SETTING}$ = 27mA	46	55	64	
Charge termination current threshold hysteresis	I_{TERM_HYS}	$I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), $I_{PRE\_SETTING}$= 20mA	7.5	11	15	mA
		$I_{CC\_SETTING}$ ≥ 280mA, (REG02h, bit[4] = 0), $I_{PRE\_SETTING}$ = 20mA	19	24	29	
Pre-charge threshold voltage	V_{BATT_PRE}	V_{BATT} rising, set V_{BATT_PRE} = 3V	2.8	3	3.1	V
Pre-charge threshold voltage hysteresis				90		mV
Recharge threshold below V_{BATT_REG}	V_{RECH}	REG04h, bit[0] = 0	120	160	200	mV
		REG04h, bit[0] = 1	260	300	350	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Protection						
Thermal shutdown rising threshold (7)	T_{J_SHDN}			150		°C
Thermal shutdown hysteresis (7)				20		°C
NTC output current	I_{NTC}	CEB = 0, NTC = 3V	-100	0	+100	nA
NTC cold temp rising threshold	V_{COLD}	As a percentage of V_{DD}	63	65	67	%
NTC cold temp rising threshold hysteresis				30		mV
NTC hot temp falling threshold	V_{HOT}	As a percentage of V_{DD}	31	33	35	%
NTC hot temp falling threshold hysteresis				70		mV
NTC hot temp falling threshold for PCB_OTP	V_{HOT_PCB}	As a percentage of V_{DD}	30	32	34	%
NTC hot temp falling threshold hysteresis for PCB_OTP				85		mV
Logic I/O Pin Characteristics						
Low logic voltage threshold	V_L				0.4	V
High logic voltage threshold	V_H		1.3			V
I²C Interface(SDA, SCL)						
Input high threshold level	V_{IH}	V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold level	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 5mA			0.4	V
I²C clock frequency	f_{SCL}				400	kHz
Digital Clock and Watchdog Timer						
Digital clock 2	f_{DIG2}			32		kHz
Watchdog timer	t_{WDT}	Configurable, REG05h, bits[5:4] = 11		160		sec

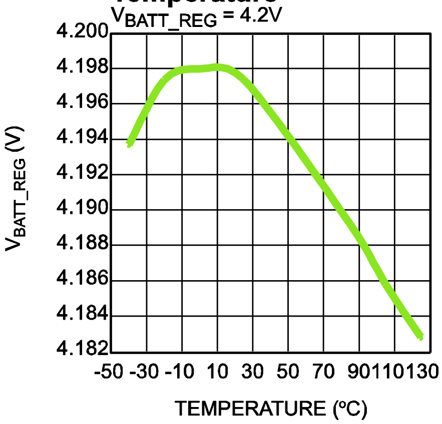
Note:

7) Guaranteed by design.

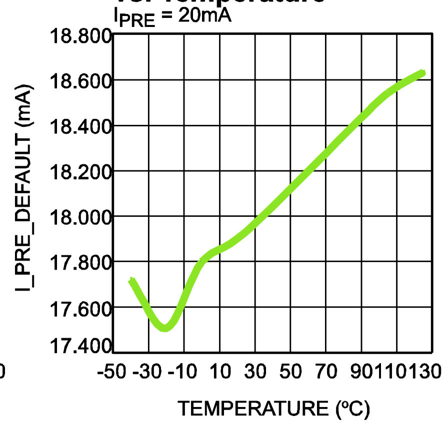
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 246mA, V_{IN_MIN} = 4.76V, unless otherwise noted.

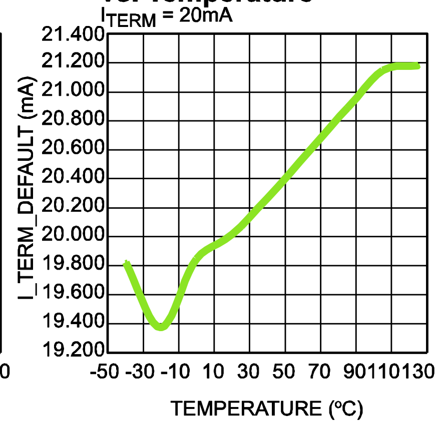
VBATT Regulation Voltage vs. Temperature



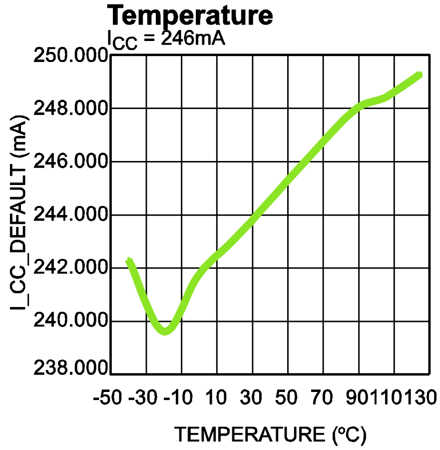
Pre-Charge Current vs. Temperature



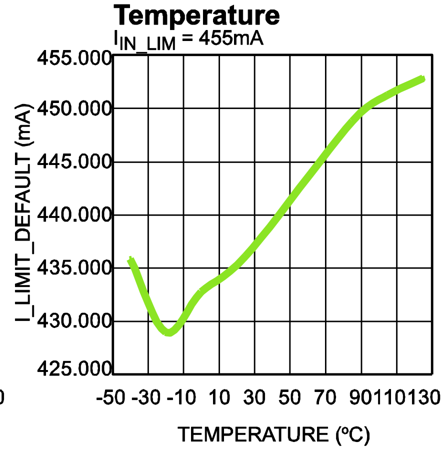
Battery Termination Current vs. Temperature



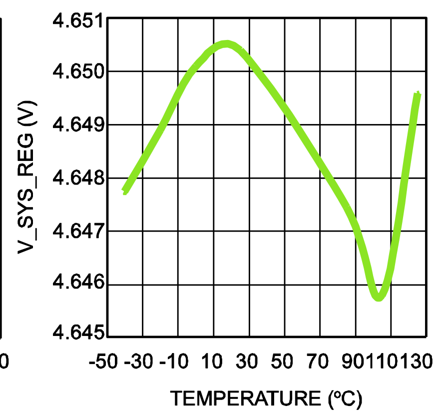
Charge Current vs. Temperature



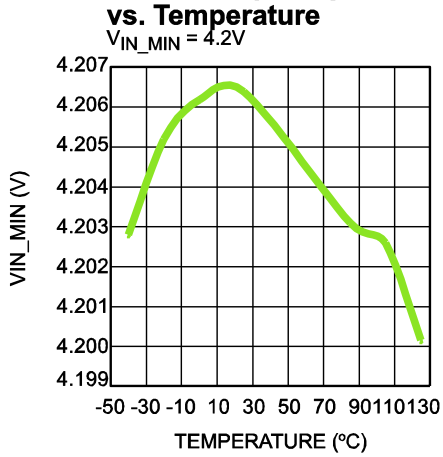
Input Current Limit vs. Temperature



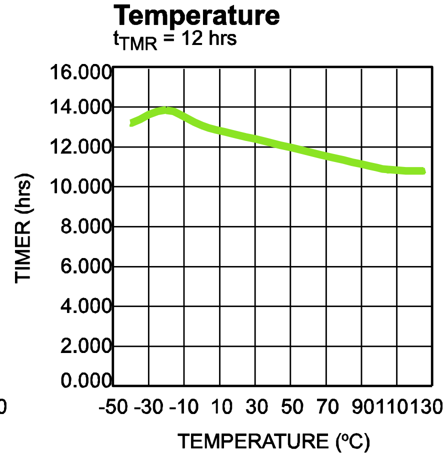
System Regulation Voltage vs. Temperature



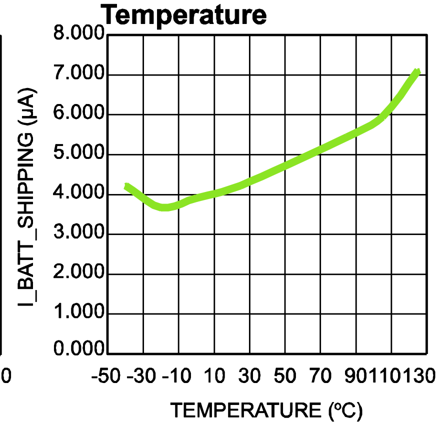
Input Voltage Regulation vs. Temperature



Timer Period vs. Temperature



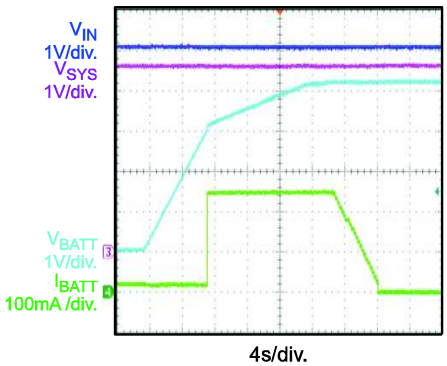
Battery Leakage Current Under Shipping vs. Temperature



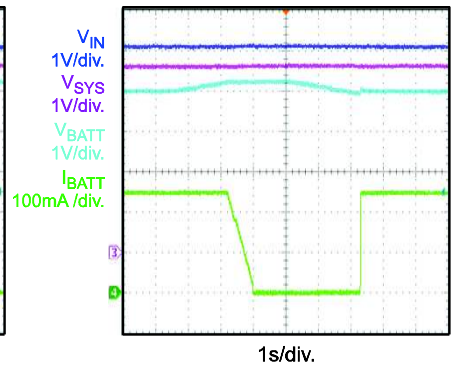
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 246mA, V_{IN_MIN} = 4.76V, unless otherwise noted.

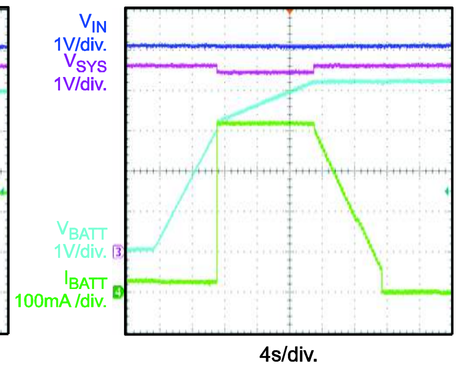
Battery Charge Curve
I_{SYS} = 0A



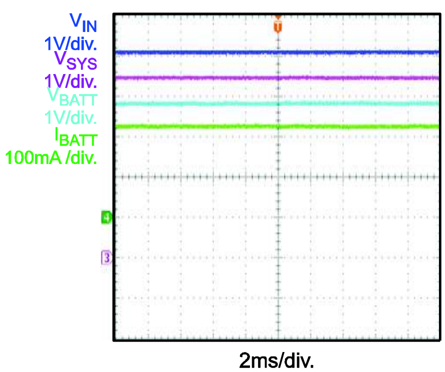
Auto-Recharge
I_{SYS} = 0A



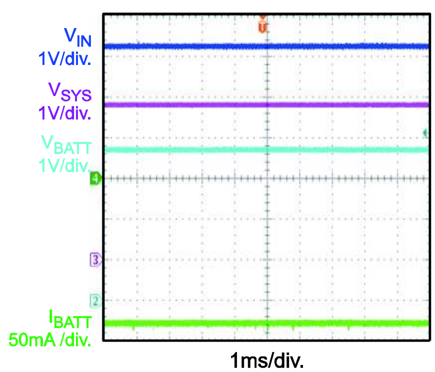
Battery Charge Curve
I_{CC} = 399mA



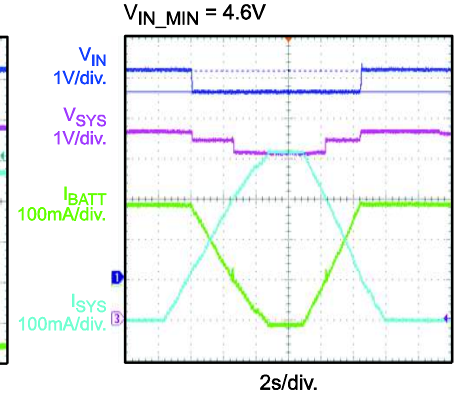
CC Charge Steady State
V_{BATT} = 3.7V, I_{SYS} = 200mA



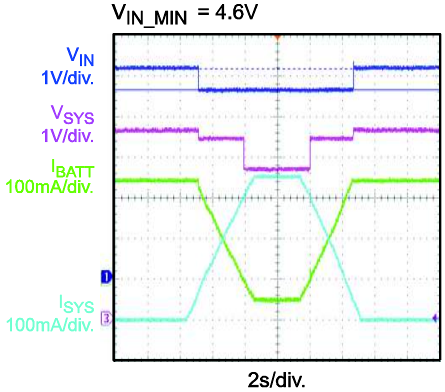
Supplement Mode Steady State
V_{BATT} = 3.7V, I_{SYS} = 600mA



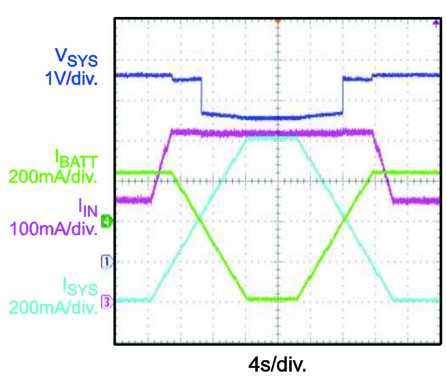
Input Voltage Regulation based PPM
V_{IN} = 5V/300mA, V_{BATT} = 4.2V, V_{IN_MIN} = 4.6V



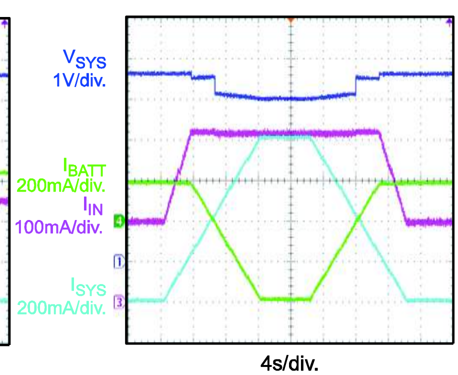
Input Voltage Regulation based PPM
V_{IN} = 5V/300mA, V_{BATT} = 3.7V
V_{IN_MIN} = 4.6V



Input Current Limit based PPM
V_{BATT} = 3.7V



Input Current Limit based PPM
V_{BATT} = 4.2V, I_{BATT} = 100mA,

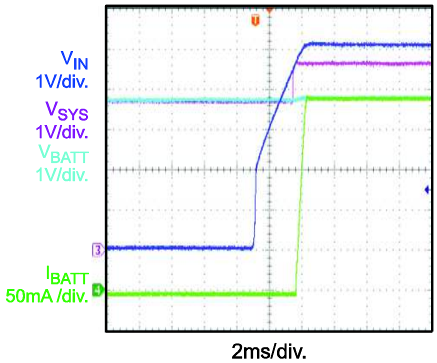


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 246mA, V_{IN_MIN} = 4.76V, unless otherwise noted.

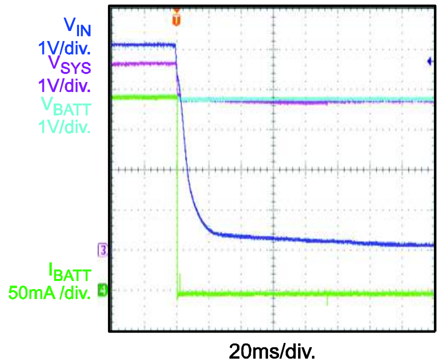
Power On

V_{BATT} = 3.7V, I_{SYS} = 0A



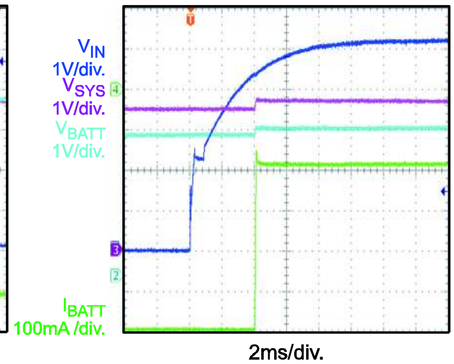
Power Off

V_{BATT} = 3.7V, I_{SYS} = 0A



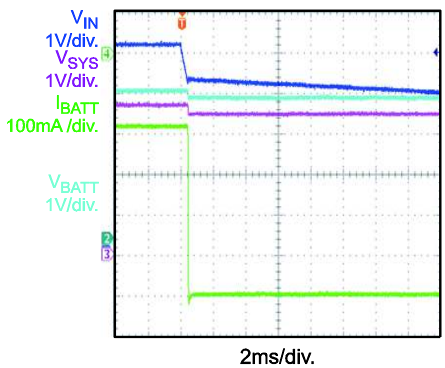
Power On @ Supplement Mode

V_{BATT} = 3.7V, I_{SYS} = 600mA



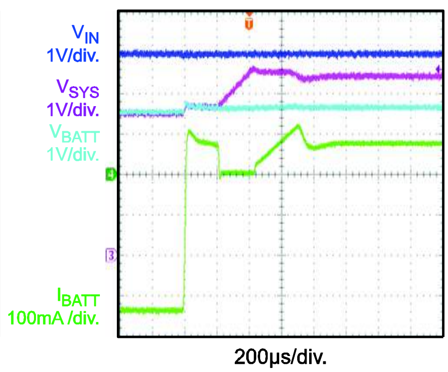
Power Off @ Supplement Mode

V_{BATT} = 3.7V, I_{SYS} = 600mA



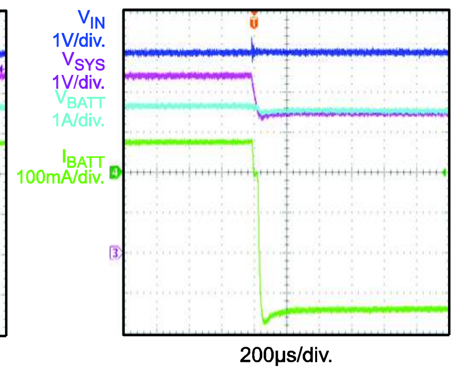
EN On @ Input Current Limit Based PPM

V_{BATT} = 3.7V, I_{SYS} = 350mA



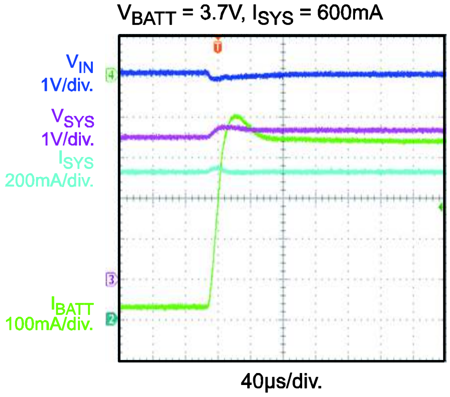
EN Off @ Input Current Limit Based PPM

V_{BATT} = 3.7V, I_{SYS} = 350mA



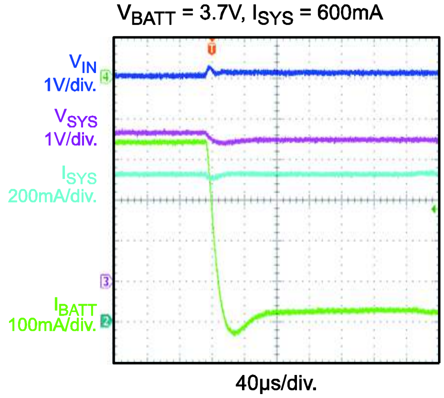
EN On @ Supplement Mode

V_{BATT} = 3.7V, I_{SYS} = 600mA



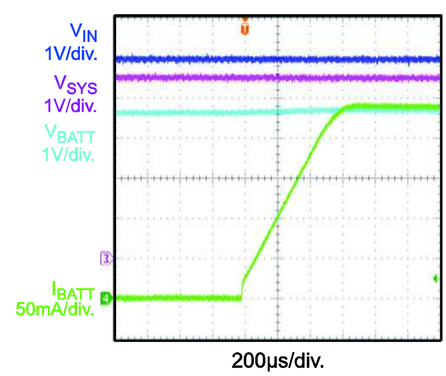
EN Off @ Supplement Mode

V_{BATT} = 3.7V, I_{SYS} = 600mA



Charge On

V_{BATT} = 3.7V, I_{SYS} = 0A

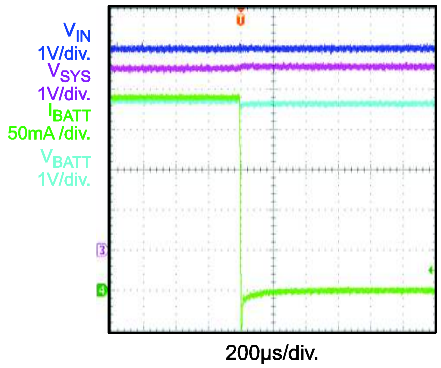


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 246mA, V_{IN_MIN} = 4.76V, unless otherwise noted.

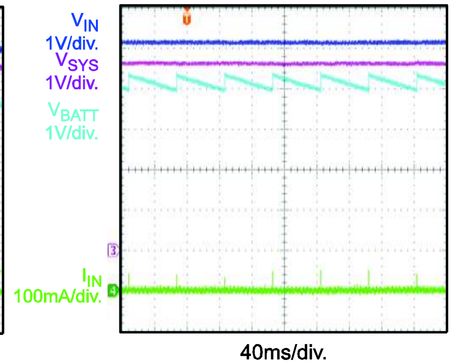
Charge Off

V_{BATT} = 3.7V, I_{SYS}=0A



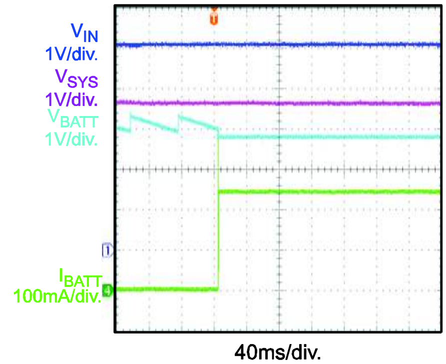
BATT Float Operation

I_{SYS} = 0A



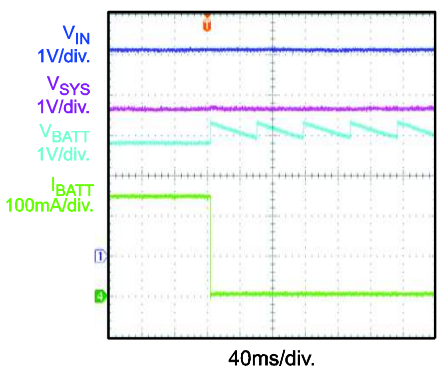
BATT Insertion

V_{BATT} = 3.7V, I_{SYS} = 0A



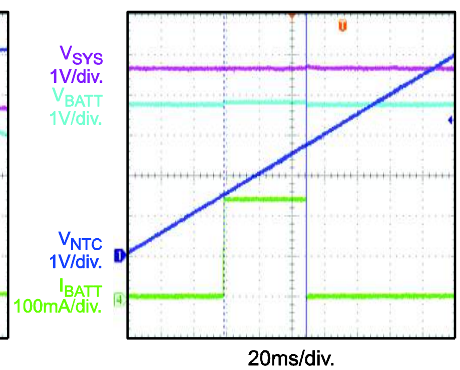
BATT Removal

V_{BATT} = 3.7V, I_{SYS} = 0A



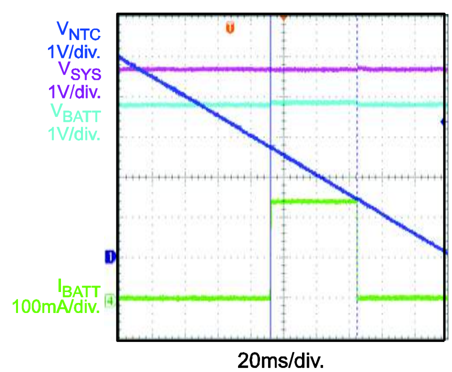
NTC On/Off

V_{BATT} = 3.7V, I_{SYS} = 0A



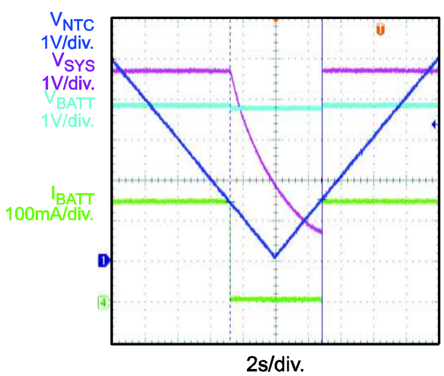
NTC On/Off

V_{BATT} = 3.7V, I_{SYS} = 0A



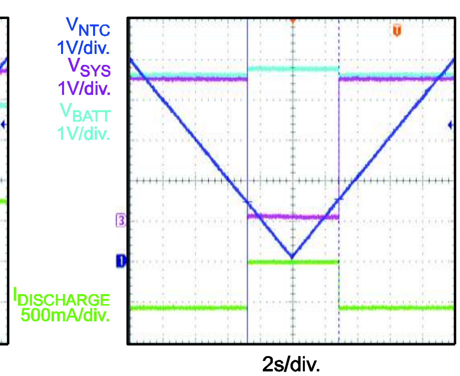
PCB OTP @ Charge Mode

V_{BATT} = 3.7V, I_{SYS} = 0A



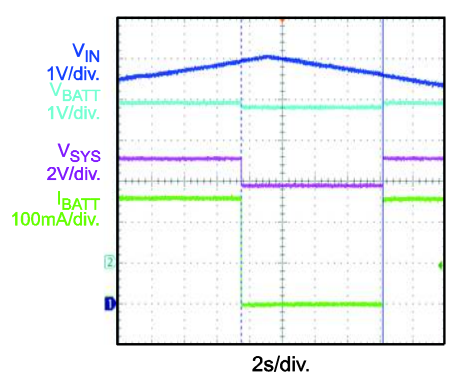
PCB OTP @ Discharge Mode

V_{IN} = 0V, V_{BATT} = 3.7V, I_{SYS} = 500mA



V_{IN} OVP Operation

V_{BATT} = 3.7V, I_{SYS} = 0A



FUNCTIONAL BLOCK DIAGRAM

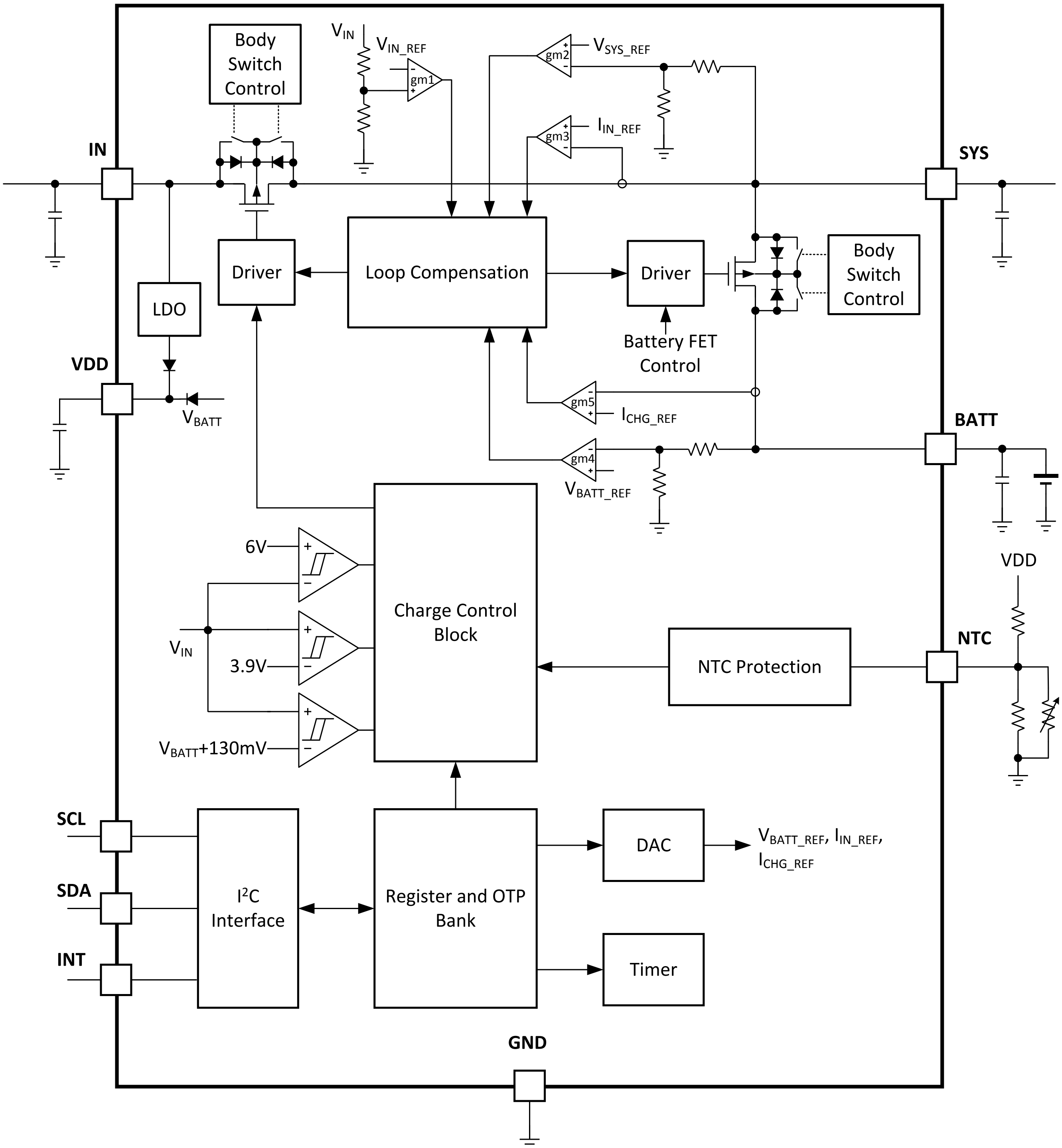


Figure 2: Functional Block Diagram

OPERATION

Introduction

The MP2661 is an I²C-controlled, single-cell, lithium-ion (Li-ion) and lithium-polymer (Li-polymer) battery charger with complete power path management. The charge functions include constant current pre-charge (PRE.C) mode, constant current (CC) fast-charge mode, constant voltage (CV) regulation, charge termination, auto-recharge, and an integrated timer. The power path function allows the input source to power the system and charge the battery simultaneously. If there is conflict in meeting both the system load and battery charging current, then the IC reduces the charging current automatically or uses the battery as a supplemental power to satisfy the system load.

The IC integrates a 300mΩ LDO FET between the IN and SYS pins, and a 100mΩ battery FET between the SYS and BATT pins.

In charge mode, the on-chip 100mΩ battery FET operates as a full-featured linear charger with pre-charging, CC charging, CV charging, charge termination, auto-recharging, NTC monitoring, integrated timer control, and thermal protection. The charge current (I_{CHG}) can be configured via the I²C interface. If the die temperature exceeds the thermal regulation threshold (typically 120°C), then the IC limits I_{CHG}.

In supplement mode, if the input power is not enough to power the system load, then the 100mΩ battery FET turns on to connect the battery to the system load. If the input is removed, then the 100mΩ battery FET turns on to allow the battery to power up the system.

Once the system load is satisfied, the remaining current is used to charge the smart power path management battery. The IC reduces I_{CHG} or uses power from the battery to satisfy the system load when its demand exceeds the input power capacity.

Figure 3 shows the MP2661 power path management structure.

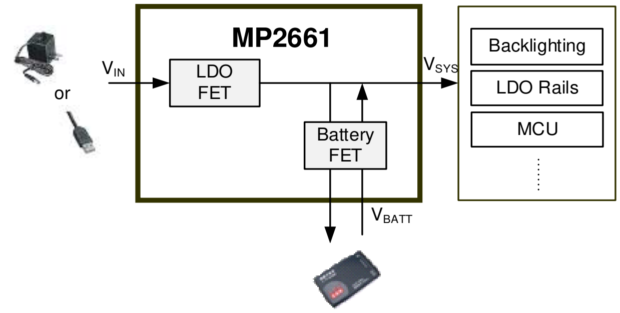


Figure 3: Power Path Management Structure

Power Supply

The IC's internal bias circuit is powered by V_{IN} or V_{BATT}, whichever is the higher voltage. If either V_{IN} or V_{BATT} exceeds its respective under-voltage lockout (UVLO) threshold, then the sleep comparator, battery depletion comparator, and the battery FET driver are enabled. At this point, the I²C interface is ready for communication and all registers are reset to the default value. The host can access all registers.

Input Over-Voltage Protection (OVP) and Under-Voltage Lockout (UVLO) Protection

The MP2661 has an input over-voltage protection (OVP) threshold and an input UVLO threshold. Once V_{IN} exceeds the normal V_{IN} range, the Q1 FET turns off.

Once V_{IN} is identified as a good source, a 200µs immunity timer begins. If the input power is still sufficient after the 200µs timer expires, then the system starts up. Otherwise, Q1 remains off.

Figure 4 shows the input power detection operation profile.

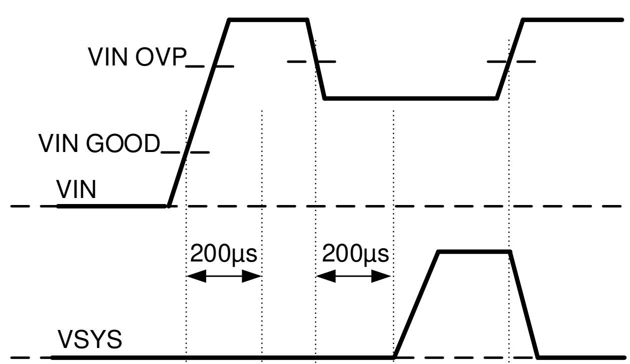


Figure 4: Input Power Detection Operation Profile

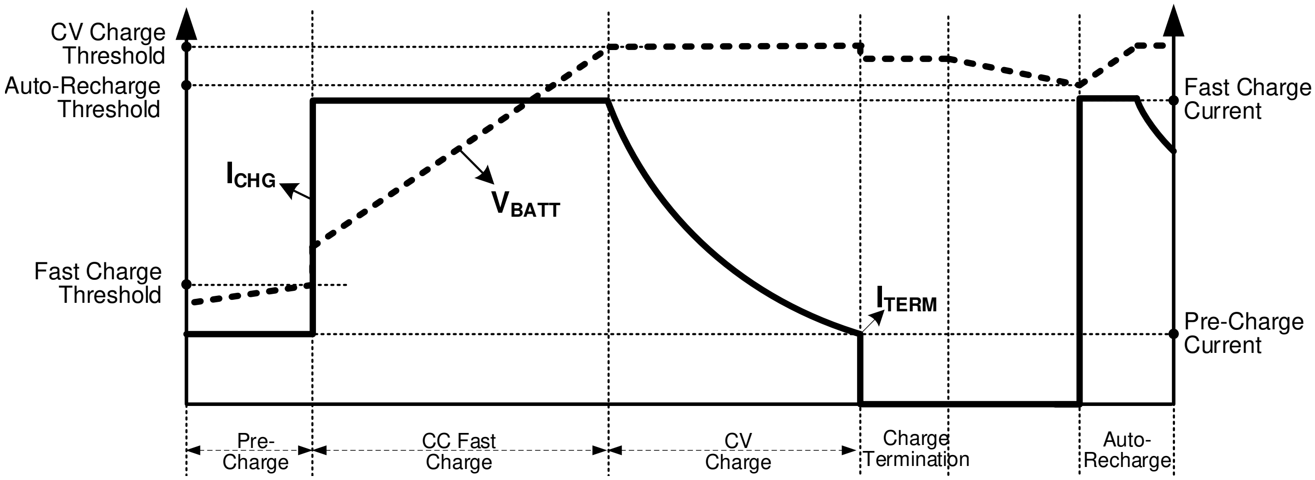


Figure 5: Battery Charge Profile

Power Path Management

The IC employs a direct power path structure with a battery FET that decouples the system from the battery, which allows for separate control between the system and the battery. The system is given priority start-up, even with a deeply discharged or missing battery. Once the input power is available, even with a depleted battery, the system voltage (V_{SYS}) is regulated to V_{SYS_REG} via the integrated LDO FET.

The direct power structure is composed of a frond-end LDO FET connected between IN and SYS, and a battery FET connected between SYS and BATT.

The input LDO (using an LDO FET) provides power to the system, which drives the system load directly and charges the battery through the battery FET.

If V_{IN} exceeds V_{SYS_REG}, then V_{SYS} is regulated to V_{SYS_REG}. If V_{IN} drops below V_{SYS_REG}, then the LDO FET turns on with the input current limit (I_{IN_LIM}).

Battery Charge Profile

The IC provides three main charging phases: pre-charge, constant current charge, and constant voltage charge (see Figure 5). These phases are described below:

1. Phase 1 (PRE.C mode): The IC can safely pre-charge the deeply depleted battery until the battery voltage (V_{BATT}) reaches the pre-charge to fast charge threshold (V_{BATT_PRE}). The pre-charge current is configurable via REG03h (bits[1:0]). If V_{BATT_PRE} is not reached before the 1hr pre-charge timer expires, then the charge cycle stops and a corresponding timeout fault signal is asserted.
2. Phase 2 (CC fast charge mode): If V_{BATT} exceeds V_{BATT_PRE}, the IC enters a constant-current charge (fast charge) phase. The fast charge current can be programmable via REG02h, bits[4:0].
3. Phase 3 (constant voltage charge): If V_{BATT} reaches the pre-configurable charge full voltage (V_{BATT_REG}) set via REG04h (bits[7:2]), then the charge mode changes from CC mode to CV mode. Then I_{CHG} begins to taper off.

Assuming the termination function (EN_TERM) is set via REG05h (bit[6] = 1), then the charge cycle is considered complete once the following conditions are met:

- The charge current (I_{CHG}) reaches the end of charge (EOC) current threshold (I_{TERM}), and the 2.5ms delay timer is initiated.
- During the 2.5ms delay period, I_{BATT} is below I_{TERM} + I_{TERM_HYS}.

The charge status is marked as complete once the 2.5ms delay timer expires.

If TERM_TMR is set via REG05h (bit[0] = 0), then I_{CHG} is terminated once the timer expires. Otherwise, I_{CHG} continues to drop.

If EN_TERM = 0, then the termination function is disabled and the conditions described above do not occur. During the charge process, I_{CHG} may be below the register setting due to other loop regulations (such as dynamic power management (DPM) regulation for V_{IN} and I_{IN} or thermal regulation). If I_{IN} or V_{IN} reaches their respective limits during CV charge mode, then the charge-full termination should not be influenced once I_{CHG} is not near to the EOC current specification.

A new charge cycle begins once the following conditions are met:

- The input power has been recycled.
- The I²C has enabled battery charging.
- The device enters auto-recharge mode.
- There is not a thermistor fault present at NTC.
- There is not a safety timer fault present.
- Battery over-voltage protection (OVP) has not been triggered.
- The Battery FET is not forced to turn off.

Automatic Recharge

If the battery is fully charged and charging has ceased, then the battery may be discharged due to system consumption or self-discharge. If V_{BATT} is discharged below the recharge threshold, and V_{IN} remains within the operation range, then the IC begins a new charging cycle automatically without restarting a charge cycle manually.

The auto-recharge function is valid when EN_TERM = 1 and TERM_TMR = 0.

Battery Over-Voltage Protection (OVP)

The IC's integrated battery over-voltage (OV) limit is about 130mV above V_{BATT_REG}. If a battery OV event occurs, then the IC suspends charging immediately and asserts a fault.

Input Current-Based and Input Voltage-Based Power Management

The IC uses input current-based power management by monitoring I_{IN} continuously to meet the input source's (typically a USB) maximum current limit specification. I_{IN_LIM} can be configured via the I²C to prevent the input source from overloading.

If the preset I_{IN_LIM} exceeds the input source rating, then the backup V_{IN}-based power management also works to prevent the input source from overloading. If either I_{IN_LIM} or the input voltage limit (V_{IN_LIM}) is reached, then the Q1 FET between IN and SYS is regulated to limit the total input power, which causes V_{SYS} to drop. Once the system drops to the minimum value (4.56V or V_{IN} - 160mV), I_{CHG} decreases to prevent V_{SYS} from dropping further.

Voltage-based DPM regulates V_{IN} to V_{IN_MIN} once the load exceeds the input power capacity. V_{IN_MIN} set via the I²C should be at least 400mV above V_{BATT_REG} to ensure the regulator's stable operation.

Battery Supplement Mode

If DPM occurs, I_{CHG} is reduced to maintain I_{IN} or V_{IN} in regulation. If I_{CHG} is 0A and the input source is still overloaded due to a heavy system load, then V_{SYS} starts to drop. Once V_{SYS} falls below V_{BATT}, the IC enters battery supplement mode. When V_{SYS} is 30mV below V_{BATT}, ideal diode mode is enabled. The battery FET is regulated to maintain V_{BATT} - V_{SYS} at 22.5mV. If the supplement current (I_{DSCHG} x R_{ON_BATT}) exceeds 22.5mV, then the battery FET turns on to maintain the ideal forward voltage. Once V_{SYS} exceeds V_{BATT} + 20mV, if the system load decreases, then ideal diode mode is disabled.

Figure 6 on page 18 shows the dynamic power management and battery supplement mode operation profile.

If V_{IN} is not available, then the IC operates in discharge mode, and the battery FET is turned on to reduce loss.

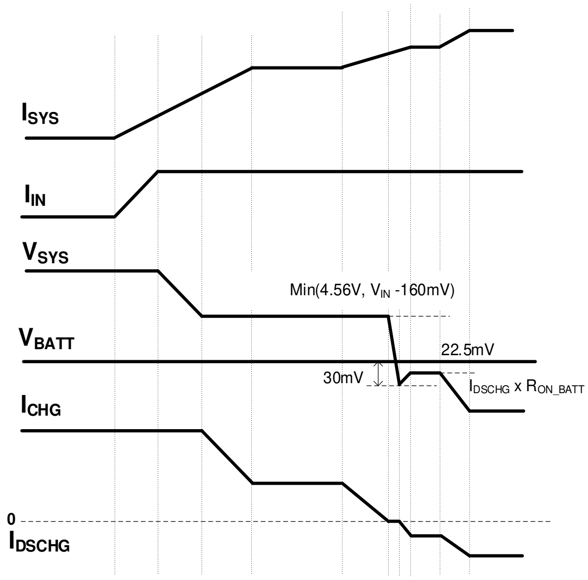


Figure 6: Dynamic Power Management and Battery Supplement Operation Profile

Battery Charge-Full Voltage

V_{BATT} for the constant voltage regulation phase in V_{BATT_REG}. Once V_{BATT_REG} is 4.2V, it has a ±0.5% accuracy over the ambient temperature range (0°C to 50°C). If the battery is removed, then V_{BATT} should be between V_{BATT_REG} - V_{RECH} and V_{BATT_REG}.

Thermal Regulation and Thermal Shutdown

The IC monitors the internal junction temperature (T_J) to maximize power delivery (PD) and prevent the chip from overheating. If the internal T_J reaches the T_{J_REG} preset limit (default 120°C), the IC reduces I_{CHG} to prevent higher power dissipation. The multiple thermal regulation thresholds (from 60°C to 120°C) help the system design meet different applications' thermal requirements. The T_J regulation threshold can be set via REG06h (bits[1:0]).

When the junction temperature reaches 150°C, both Q1 and Q2 are turned off.

Negative Temperature Coefficient (NTC) Temperature Sensor

The negative temperature coefficient (NTC) allows the IC to sense the battery temperature via the thermistor (typically available in the battery pack) to ensure a safe operating environment for the chip. A resistor with an appropriate value should be connected from VDD to NTC, and the thermistor should be connected from NTC to ground. The NTC voltage is determined by the resistor divider. The divider ratio depends on the temperature. The IC internally sets the predetermined divider ratio's upper and lower bounds for NTC cold and NTC hot. The MP2661's default I²C setting is PCB_OTP, which is configurable via the I²C (see Table 2).

Table 2: NTC Function Selection

I²C Control		Function
EN_NTC	ENB_PCB_OTP	
0	x	Disabled
1	1	NTC
1	0	PCB_OTP

If PCB_OTP is selected, then the NTC voltage (V_{NTC}) should be below the NTC hot threshold, and both the LDO FET and Battery FET are off. The PCB_OTP fault sets the NTC_FAULT status (REG08h, bit[1]) to 1 to indicate the fault. Operation resumes once V_{NTC} exceeds the NTC hot threshold.

The NTC function only works in charge mode. Once V_{NTC} drops below of the divider ratio and the temperature is outside the safe operating range, the IC stops charging and reports this on the status bits. Charging resumes automatically once the temperature is within the safe range again.

Safety Timer

The IC provides both a pre-charge and a fast-charge safety timer to prevent extended charging cycles due to abnormal battery conditions. If V_{BATT} is below V_{BATT_PRE}, then the safety timer is 1 hour. The fast-charge safety timer begins once the battery enters fast-charge mode. The fast-charge safety timer can be configured via the I²C. The safety timer feature can be disabled via the I²C.

The following actions can reset the safety timer:

- A new charge cycle is initiated
- Charge enable toggling
- Hi-Z disable toggling

Host Mode and Default Mode

The IC is a host-controlled device. After the power-on reset (POR), the IC starts in the watchdog timer expiration state or default mode. All registers are in the default settings.

Any write to the IC changes it to host mode. All charge parameters are configurable. If the watchdog timer (REG05h, bits[5:4]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to the REG01h, bit[6] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the IC returns to default mode. The watchdog timer limit can also be programmed or disabled by the host control. When there is no V_{IN}, the watchdog timer is suspended. (Figure 19)

The operation can also be changed to default mode when one of the following conditions occur:

- Refresh input without battery
- Reinsert battery with no V_{IN}
- Register reset REG01h, bit[7] is reset

Battery Discharge Function

If the battery is connected and the input source is missing, the battery FET is fully on when V_{BATT} is above the V_{BATT_UVLO} threshold. The 100mΩ battery FET minimizes conduction loss during discharge. The quiescent current of the IC is as low as 11μA in this mode. The low on resistance and low quiescent current help extend the running time of the battery.

Over-Discharge Current Protection

The IC has over-discharge current protection in discharge mode and supplement mode. Once I_{BATT} exceeds the programmable discharge current limit (default 2A), the battery FET turns off after a 60μs delay, and the MP2661 enters hiccup mode in over-current protection (OCP). The discharge current can be programmed high to 3.2A via the I²C. If the discharge current goes high to reach the internal fixed current limit (about 3.7A), the battery FET is turned off and starts hiccup mode immediately.

Similarly, when the V_{BATT} falls below the programmable V_{BATT_UVLO} threshold (default 2.8V), the battery FET is turned off to prevent over-discharge.

System Short-Circuit Protection (SCP)

The MP2661 features SYS node short-circuit protection (SCP) for the IN to SYS path and the BATT to SYS path.

V_{SYS} is continuously monitored. If V_{SYS} is below 1.5V, the system (SCP) for the IN to SYS path and the BATT to SYS path are active. I_{DSCHG} is decreased to half of the original value.

1) IN to SYS path: Once I_{IN} exceeds the protection threshold, both the LDO FET and the battery FET turn off immediately, and the IC enters hiccup mode. Otherwise, the max current limit and the setting I_{IN_LIM} are not reached, and I_{IN} is regulated at I_{IN_LIM}. Hiccup mode also starts after a 60μs delay. The interval of the hiccup mode is 800μs.
2) BATT to SYS path: Once I_{BATT} exceeds the 3.7A protection threshold, both the LDO FET and the battery FET turn off immediately, and the IC enters hiccup mode. When the battery discharge current limit threshold is reached, hiccup mode starts after a 60μs delay. The interval of the hiccup mode is 800μs.

If a system short-circuit occurs when both the input and battery are present, the protection mechanism of both paths work, with the faster one dominating hiccup operation (see Figure 22).

Interrupt to Host (INT)

The IC has an alert mechanism that can output an interrupt signal via INT to notify the system of the operation by outputting a 256μs low-state INT pulse. All of the below events can trigger the INT output:

- Good input source detected (PG_STAT)
- Charge completed
- Charging status change
- Any fault in REG08h (watchdog timer fault, input fault, thermal fault, safety timer fault, battery OVP fault, NTC fault)

When any fault occurs, the IC sends out an INT pulse and latches the fault state in REG08h. After the IC exits the fault state, the fault bit could be released to 0 after the host reads REG08h. The NTC fault is not latched and always reports the current thermistor conditions.

Note that the INT needs the external pull-up resistor for its open-drain connection. Suggest the resistance not lower than 300kΩ.

Battery Disconnection Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system to prevent excessive capacity discharge during shipping and storage, and to allow the system power to reset.

The MP2661 provides both shipping mode (see Figure 23 on page 34) and system reset mode for different application requirements.

Shipping Mode

The register bit FET_DIS (REG06h, bit[5]) controls when the IC enters shipping mode.

During normal operation, the battery FET turns on and FET_DIS is set to 0. If this bit is set to 1, then the Battery FET turns off and the MP2661 enters shipping mode. The FET_DIS bit is reset to 0 automatically after the BATT turns off (see Figure 7).

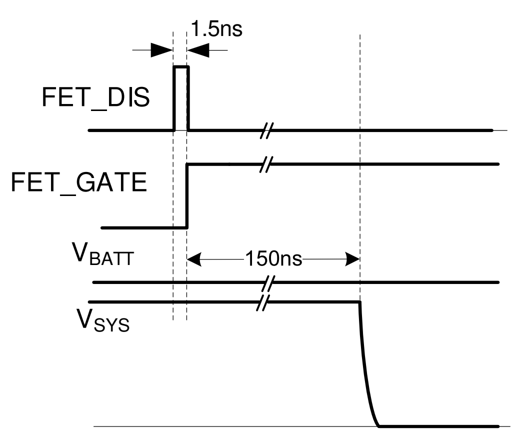


Figure 7: Time Delay from FET_DIS = 1 to the Battery FET Turn-Off

The IC exits shipping mode by pulling INT low.

If the IC is in the shipping mode and only the battery is present, then pull INT down by pushing PB make the MP2661 exit shipping mode (see Table 3 and Figure 25 on page 36).

Table 3: INT Exit Shipping Mode with Only V_{BATT} Present

	INT Signal	IC Exits Shipping Mode
Case 1	INT is low twice with the rising edge >600ns	At once
Case 2	INT is low once with the rising edge >600ns	After 4s
Case 3	INT is low for 4s	Once after the 4s
Case 4	INT is low with the rising edge in ms level	At once

If the IC is in shipping mode and V_{IN} is not present, then the MP2661 can exit shipping mode. Once V_{IN} is preset and within the operation range, the MP2661 pulls INT low to indicate a good input source has been detected. Then the MP2661 can exit shipping mode via the INT signal (see Figure 8).

Table 4: INT Exit Shipping Mode during Start-Up through VIN

	INT signal	IC Exits Shipping Mode
Case 1	INT is low twice with the rising edge >600ns	At once
Case 2	INT is low once with the rising edge >600ns	After 4s
Case 3	INT is low with the rising edge in ms level	At once

If FET_DIS is set to 1 during shipping mode, then the IC can exit sleep mode once INT is low for 4s. In this case, the FET_DIS bit cannot be reset to 0 automatically. It must be reset to 0 manually via the I²C.

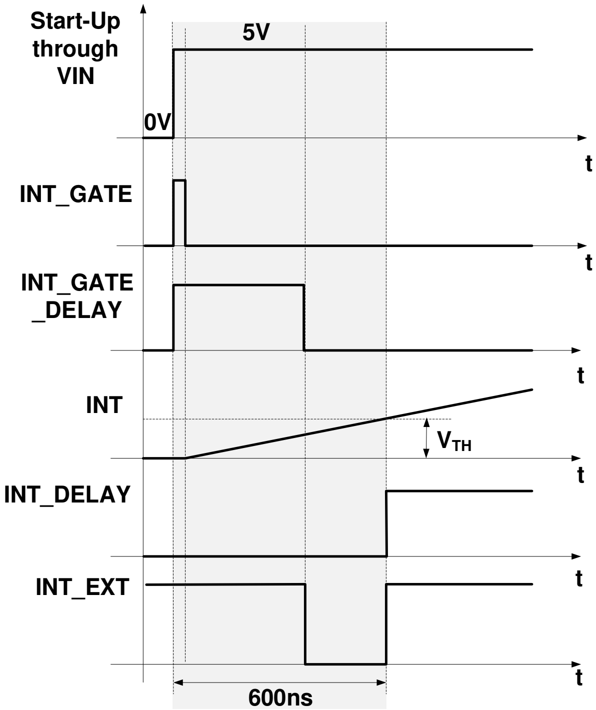


Figure 8: INT Signal during V_{IN} Start-Up

Reset Mode

If a system reset is required, the IC can use INT to cut off the path from the battery to the system.

If the INT logic is set to low for more than 16s, then the battery is disconnected from the system by turning off the battery FET.

The off state lasts for 4s, then the battery FET turns on automatically, and the system is powered by the battery again. During the 4s off time, the INT pin voltage can be high or low. The IC can reset the system by configuring INT (see Figure 9).

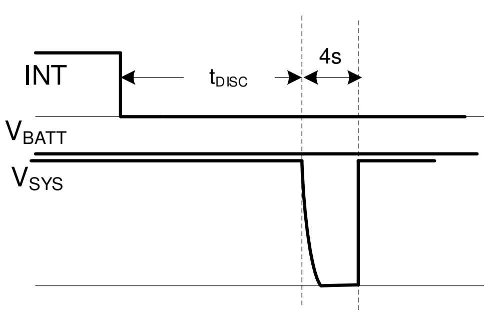


Figure 9: System Reset Function Operation Profile

Serial Interface

The IC uses an I²C interface for the flexible charging parameter settings and instantaneous device status reporting. The I²C is a two-wire serial interface with two required bus lines: a serial data line (SDA) and a serial clock line (SCL). Both the SDA and SCL lines are open-drain, and must to be connected to the positive supply voltage via a pull-up resistor.

The IC operates as a slave device, receiving control inputs from the master device (e.g. a microcontroller). The SCL line is always driven by the master device. The I²C interface supports both standard mode (up to 100kbit/s), and fast mode (up to 400kbit/s).

All transactions begin with a start (S) command and are terminated with a stop (P) command. The start and stop commands are always generated by the master. A start command is defined as a high-to-low transition on the SDA line while SCL is high. A stop command is defined as a low-to-high transition on the SDA line while SCL is high.

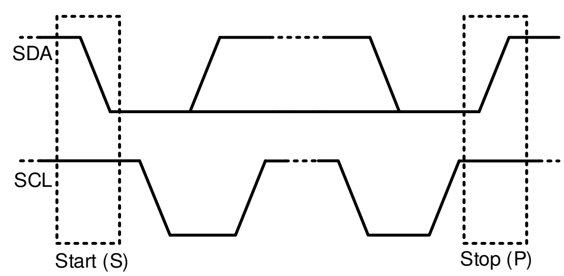


Figure 10: Start and Stop Commands

For data validity, the data on the SDA line must be stable during the clock's high period. The SDA line's high and low states can only change once the SCL line's clock signal is low. Every byte on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.

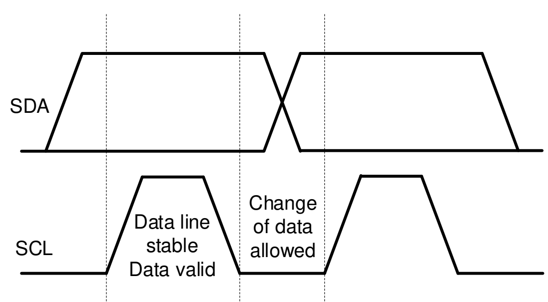


Figure 11: Bit Transfer on the I²C Bus

Each byte has to be followed by an acknowledge (ACK) bit generated by the receiver to signal the transmitter that the byte was successfully received.

The ACK signal is defined as the transmitter releasing the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line low. It remains low during the 9th clock pulse's high period.

A not acknowledged (NACK) signal is defined as a the SDA line being high during the 9th clock pulse. Then the master can generate either a stop to abort the transfer or a repeated start (Sr) command to begin a new transfer.

After the start signal, a slave address is sent. This address is 7 bits long, and is followed by an 8th data direction bit (bit R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). The address bit arrangement is shown below.

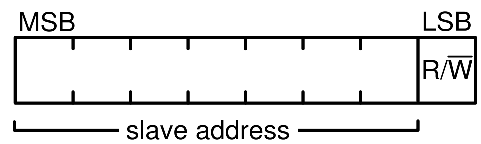


Figure 12: 7-Bit Address

For more details on the signal sequences, see Figure 13, Figure 14, Figure 15, Figure 16, and Figure 17 on page 23.

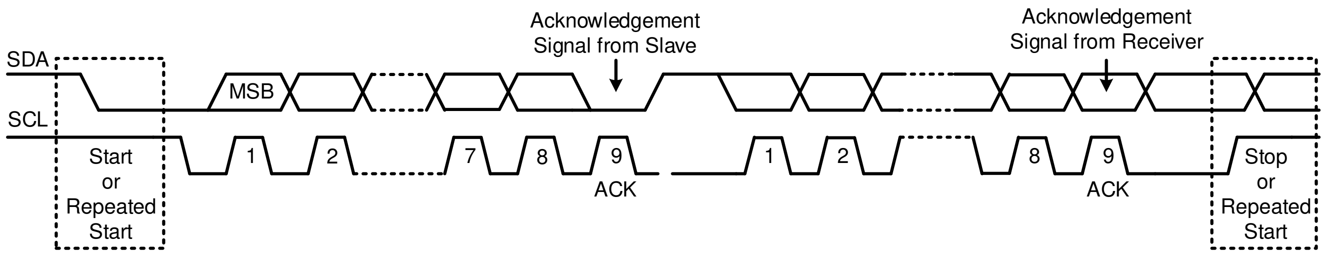


Figure 13: Data Transfer on the I²C Bus

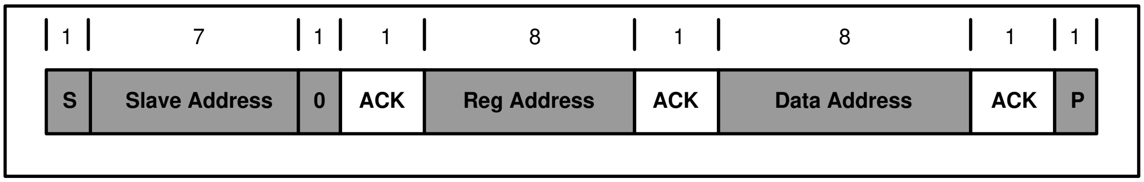


Figure 14: Single Write

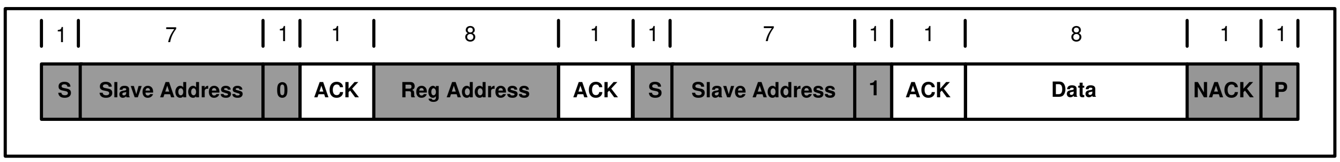


Figure 15: Single Read

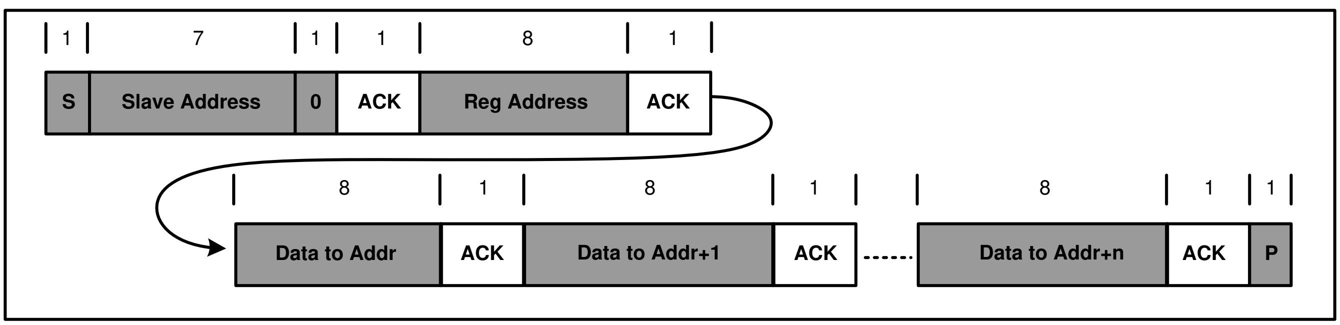


Figure 16: Multiple-Write

Figure 17: Multiple-Read

I²C REGISTER MAP

IC Address: 09h (some trim options are reserved)

Input Source Control Register/Address: 00h (Default: 01001111)

Bit	Symbol	Description	Read/Write	Default
Bit[7]	EN_HIZ (8)	0: Disabled (default) 1: Enabled	Read/write	0
Input Voltage Regulation				
Bit[6]	V_{IN_MIN} [3]	640mV	Read/write	Offset: 3.88V Range: 3.88V to 5.08V Default: 4.60V (1001)
Bit[5]	V_{IN_MIN} [2]	320mV		
Bit[4]	V_{IN_MIN} [1]	160mV		
Bit[3]	V_{IN_MIN} [0]	80mV		
Input Current Limit				
Bit[2]	I_{IN_LIM} [2]	000: 85mA 001: 130mA 010: 175mA 011: 220mA 100: 265mA 101: 310mA 110: 355mA 111: 455mA (default)	Read/write	111
Bit[1]	I_{IN_LIM} [1]			
Bit[0]	I_{IN_LIM} [0]			

Note:

8) This bit enables and disables the LDO FET.

Power-On Configuration Register/Address: 01h (Default: 0000 0100)

Bit	Symbol	Description	Read/Write	Default
Bit[7]	Register reset	0: Keep current setting (default) 1: Reset	Read/write	0
Bit[6]	I²C watchdog timer reset	0: Normal (default) 1: Reset	Read/write	0
Bit[5]	Reserved			
Bit[4]	Reserved			
Charger Configuration				
Bit[3]	CEB	0: Charge enabled (default) 1: Charge disabled	Read/write	0
Battery UVLO Threshold				
Bit[2]	V_{BATT_UVLO} [2]	0.4V	Read/write	Offset: 2.4V Range: 2.4V to 3.1V Default: 2.8V (100)
Bit[1]	V_{BATT_UVLO} [1]	0.2V		
Bit[0]	V_{BATT_UVLO} [0]	0.1V		

I²C REGISTER MAP *(continued)*

Charge Current Control Register/Address: 02h (Default: 000 01110)

Bit	Symbol	Description	Read/Write	Default
Bit[7]	Reserved			
Bit[6]	Reserved			
Bit[5]	Reserved			
Charge Current Setting				
Bit[4]	I_{CC} [4]	272mA	Read/write	Offset: 8mA Range: 8mA to 535mA Default: 246mA (01110)
Bit[3]	I_{CC} [3]	136mA		
Bit[2]	I_{CC} [2]	68mA		
Bit[1]	I_{CC} [1]	34mA		
Bit[0]	I_{CC} [0]	17mA		

Pre-Charge/Termination Current/Address: 03h (Default: 01001 010)

Bit	Symbol	Description	Read/Write	Default
Bit[7]	Reserved			
BATT to SYS Discharge Current Limit				
Bit[6]	I_{DSCHG} [3]	1600mA	Read/write	Offset: 200mA Range: 400mA to 3.2A Valid range: 0001 to 1111 Default: 2000mA (1001)
Bit[5]	I_{DSCHG} [2]	800mA		
Bit[4]	I_{DSCHG} [1]	400mA		
Bit[3]	I_{DSCHG} [0]	200mA		
PCB_OTP Enable				
Bit[2]	ENB_PCB_OTP	0: Enabled (default) 1: Disabled	Read/write	0
Pre-Charge Current				
Bit[1]	I_{PRE} [1]	14mA	Read/write	Offset: 6mA Range: 6mA to 27mA Default: 20mA (10)
Bit[0]	I_{PRE} [0]	7mA		

I²C REGISTER MAP *(continued)*

Charge Voltage Control Register/Address: 04h (Default: 1010 0011)

Bit	Symbol	Description	Read/Write	Default
Battery Regulation Voltage				
Bit[7]	V_{BATT_REG} [5]	480mV	Read/write	Offset: 3.6V Range: 3.6V to 4.545V Default: 4.2V (101000)
Bit[6]	V_{BATT_REG} [4]	240mV		
Bit[5]	V_{BATT_REG} [3]	120mV		
Bit[4]	V_{BATT_REG} [2]	60mV		
Bit[3]	V_{BATT_REG} [1]	30mV		
Bit[2]	V_{BATT_REG} [0]	15mV		
Pre-Charge Threshold				
Bit[1]	V_{BATT_PRE}	0: 2.8V 1: 3V (default)	Read/write	1
Battery Recharge Threshold (below V_{BATT_REG})				
Bit[0]	V_{RECH}	0: 150mV 1: 300mV (default)	Read/write	1

Charge Termination/Timer Control Register/Address: 05h (Default: 0100 1010)

Bit	Symbol	Description	Read/Write	Default
Bit[7]	Reserved			
Termination Setting (if Termination is Enabled)				
Bit[6]	EN_TERM	0: Disabled 1: Enabled (default)	Read/write	1
I²C Watchdog Timer Limit				
Bit[5]	WATCHDOG [1]	00: Timer disabled (default) 01: 40s 10: 80s 11: 160s	Read/write	00
Bit[4]	WATCHDOG [0]			
Safety Timer Setting				
Bit[3]	EN_TIMER	0: Disabled 1: Enabled (default)	Read/write	1
Fast Charge Timer				
Bit[2]	CHG_TMR [1]	00: 3hrs 01: 5hrs (default) 10: 8hrs 11: 12hrs	Read/write	01
Bit[1]	CHG_TMR [0]			
Termination Timer Control (If TERM_TMR is Enabled, the IC Does Not Suspend I_{CHARGE} after Termination)				
Bit[0]	TERM_TMR	0: Disabled (default) 1: Enabled	Read/write	0

I2C REGISTER MAP *(continued)*

Miscellaneous Operation Control Register/Address: 06h (Default: 0100 1011)

Bit	Symbol	Description	Read/Write	Default
Bit[7]	Reserved			
Bit[6]	TMR2X_EN	0: Disabled, 2X extended safety timer during PPM 1: Enabled 2X, extended safety timer during PPM (default)	Read/write	1
Bit[5]	FET_DIS (9)	0: Enabled (default) 1: Disabled	Read/write	0
Bit[4]	Reserved			
Bit[3]	EN_NTC	0: Disabled 1: Enabled (default)	Read/write	1
Bit[2]	Reserved			
Thermal Regulation Threshold				
Bit[1]	T_{J_REG} [1]	00: 60°C 01: 80°C 10: 100°C 11: 120°C (default)	Read/write	11
Bit[0]	T_{J_REG} [0]			

Note:

9) This bit controls the turn off function of the battery FET, including the charging and discharging.

System Status Register/Address: 07h (Default: 0000 0000)

Bit	Symbol	Description	Read/Write	Default
Bit[7]	Reserved			
Revision				
Bit[6]	Rev [1]	Revision number	Read-only	00
Bit[5]	Rev [0]			
Bit[4]	CHG_STAT [1]	00: Not charging (default) 01: Pre-charge mode 10: Charge mode 11: Charge complete	Read-only	00
Bit[3]	CHG_STAT [0]			
Bit[2]	PPM_STAT	0: No PPM (default) 1: PPM	Read-only	0 (no power-path management occurs)
Bit[1]	PG_STAT	0: Power fail (default) 1: Power good	Read-only	0
Bit[0]	THERM_STAT	0: No thermal regulation (default) 1: Thermal regulation	Read-only	0

I²C REGISTER MAP *(continued)*

Fault Register/Address: 08h (Default: 0000 0000)

Bit	Symbol	Description	Read/Write	Default
Bit[7]	Reserved			
Bit[6]	WATCHDOG_FAULT	0: Normal (default) 1: Watchdog timer expiration	Read-only	0
Bit[5]	VIN_FAULT	0: Normal (default) 1: Input fault (OVP or bad source)	Read-only	0
Bit[4]	THEM_SD	0: Normal (default) 1: Thermal shutdown	Read-only	0
Bit[3]	BAT_FAULT	0: Normal (default) 1: Battery OVP	Read-only	0
Bit[2]	STMR_FAULT	0: Normal (default) 1: Safety timer expired	Read-only	0
Bit[1]	NTC_FAULT [1]	0: Normal (default) 1: NTC hot	Read-only	0
Bit[0]	NTC_FAULT [0]	0: Normal (default) 1: NTC cold	Read-only	0

OTP MAP [(10)]

#	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x02	N/A			I_{CC}: 8mA to 535mA, 17mA/step				
0x03	N/A					PCB_OTP	I_{PRE}: 6mA to 27mA, 7mA/step	
0x04	V_{BATT_REG}: 3.6V to 4.545V, 15mV/step						N/A	
0x05	N/A		WATCHDOG		N/A			

OTP DEFAULT [(10)]

OTP Items [(10)]	Default
I_{CC}	246mA
PCB_OTP	Enabled
I_{PRE}	20mA
V_{BATT_REG}	4.2V
WATCHDOG	Disabled

Note:

10) OTP means one-time programmable.

STATE CONVERSION CHART

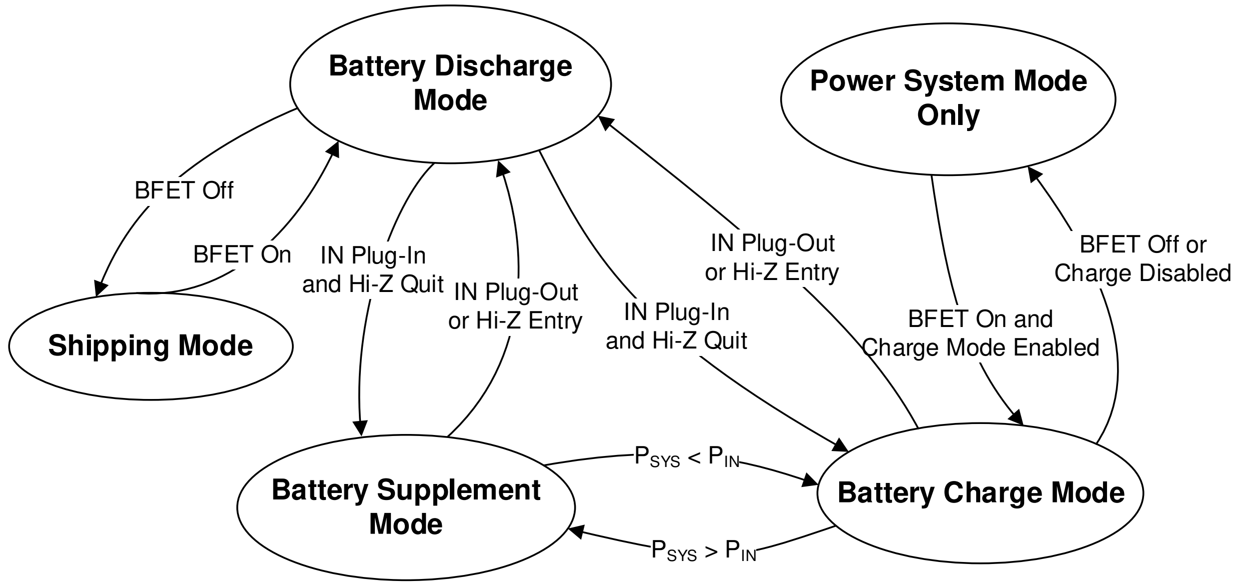


Figure 18: State Machine Conversion

CONTROL FLOWCHART

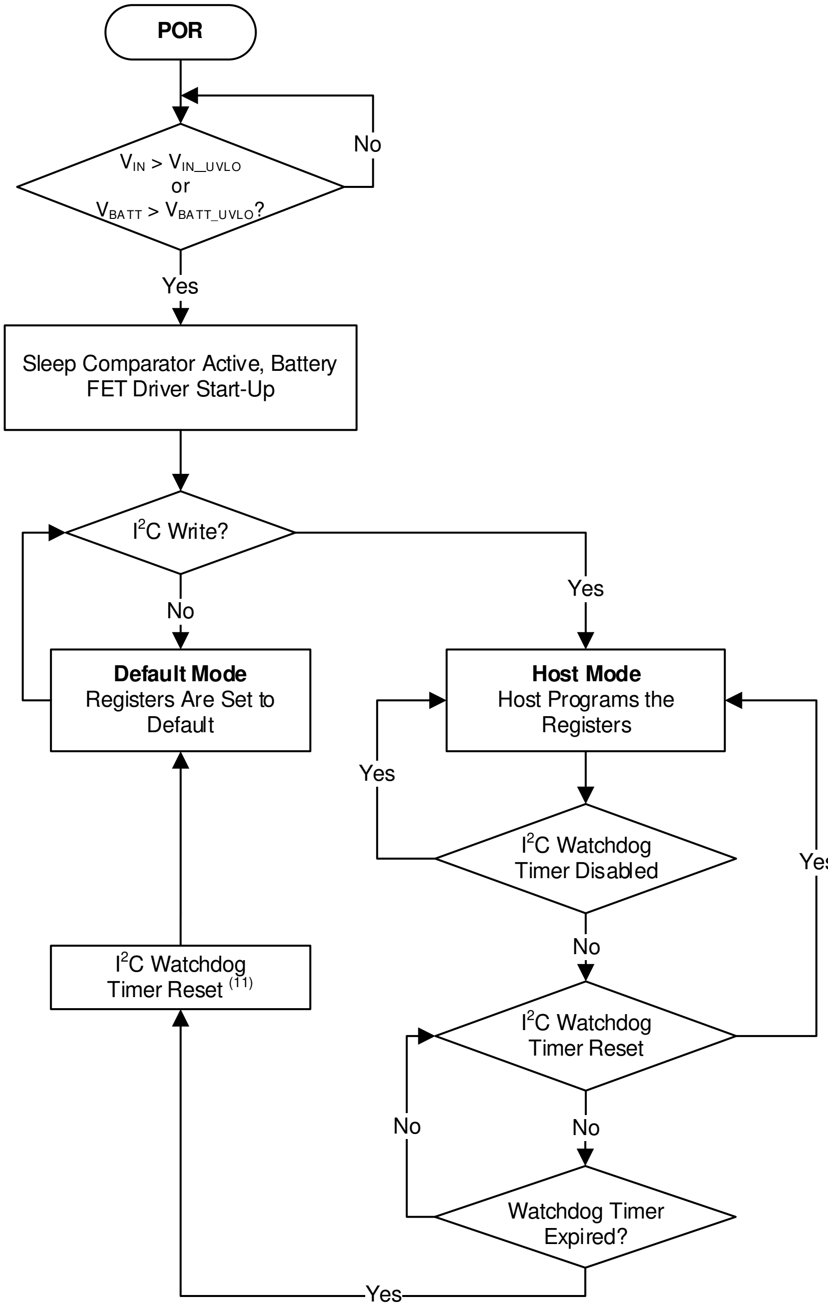


Figure 19: Default Mode and Host Mode Selection (12)

Notes:

11) Once the watchdog timer expires, the I²C watchdog timer must be reset, or the watchdog timer is not valid in the next cycle.
12) The watchdog timer is held when V_{IN} is not present.

CONTROL FLOWCHART *(continued)*

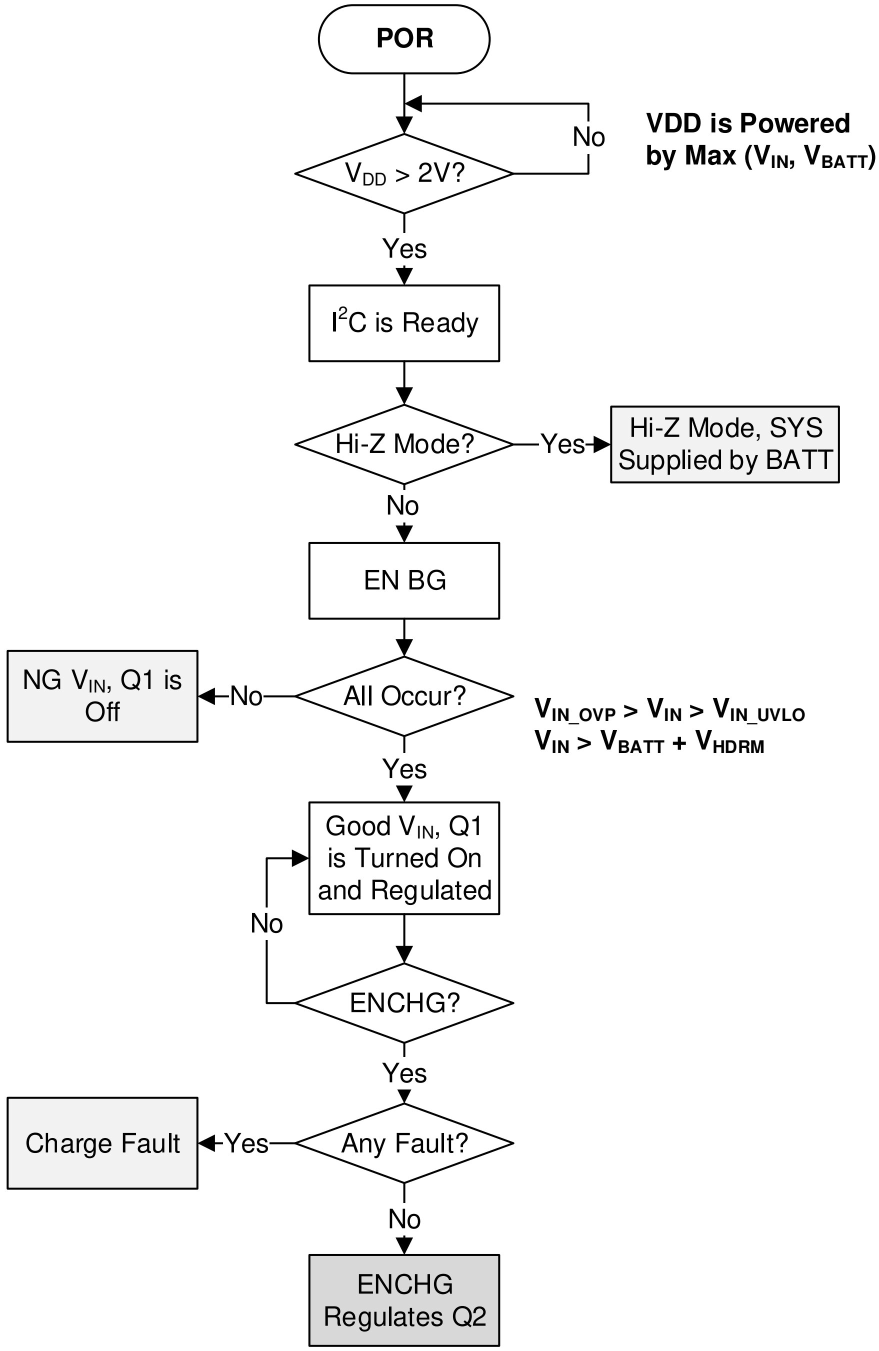


Figure 20: Input Power Start-Up Flowchart

CONTROL FLOWCHART *(continued)*

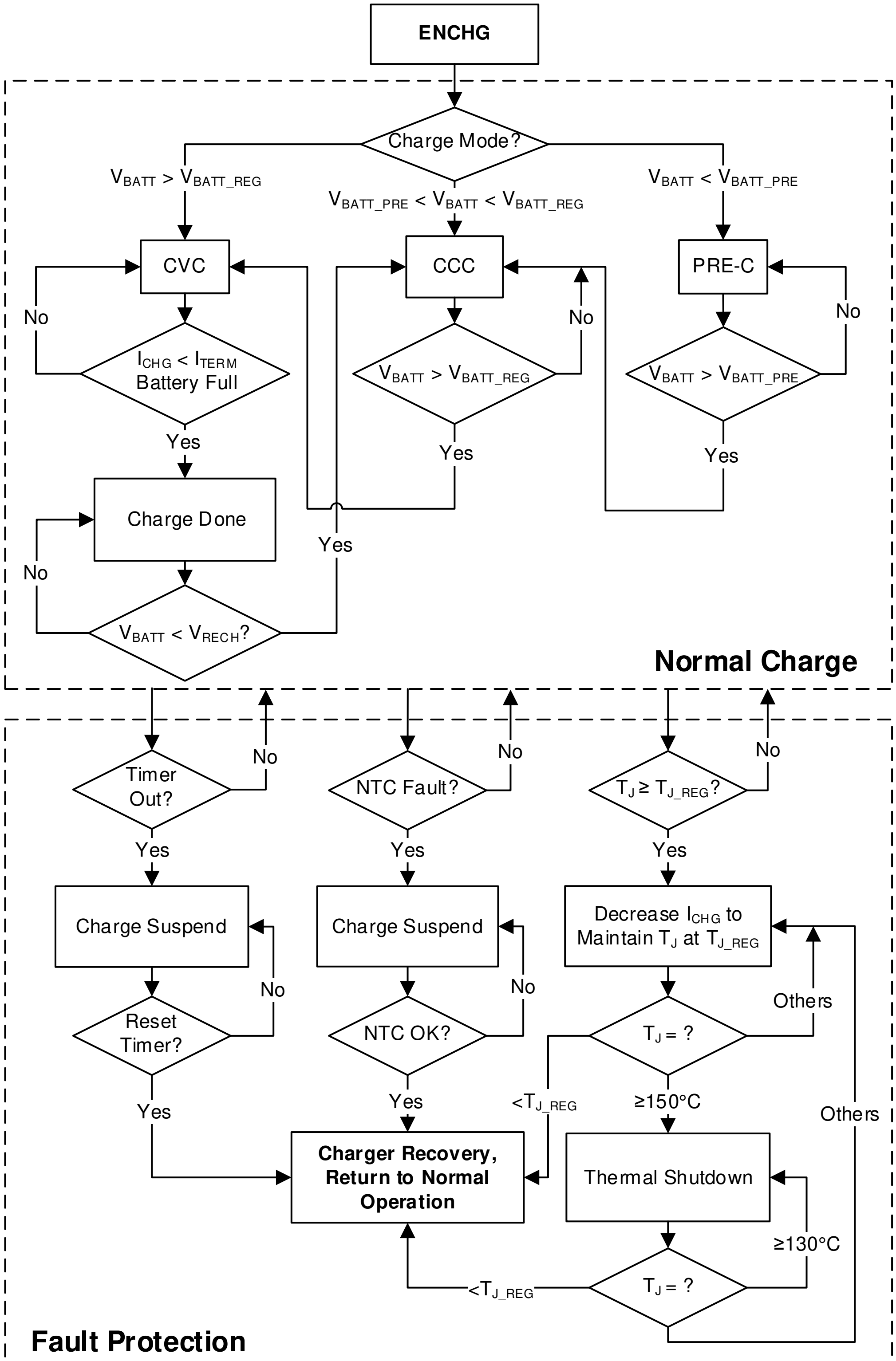


Figure 21: Charging Process

CONTROL FLOWCHART *(continued)*

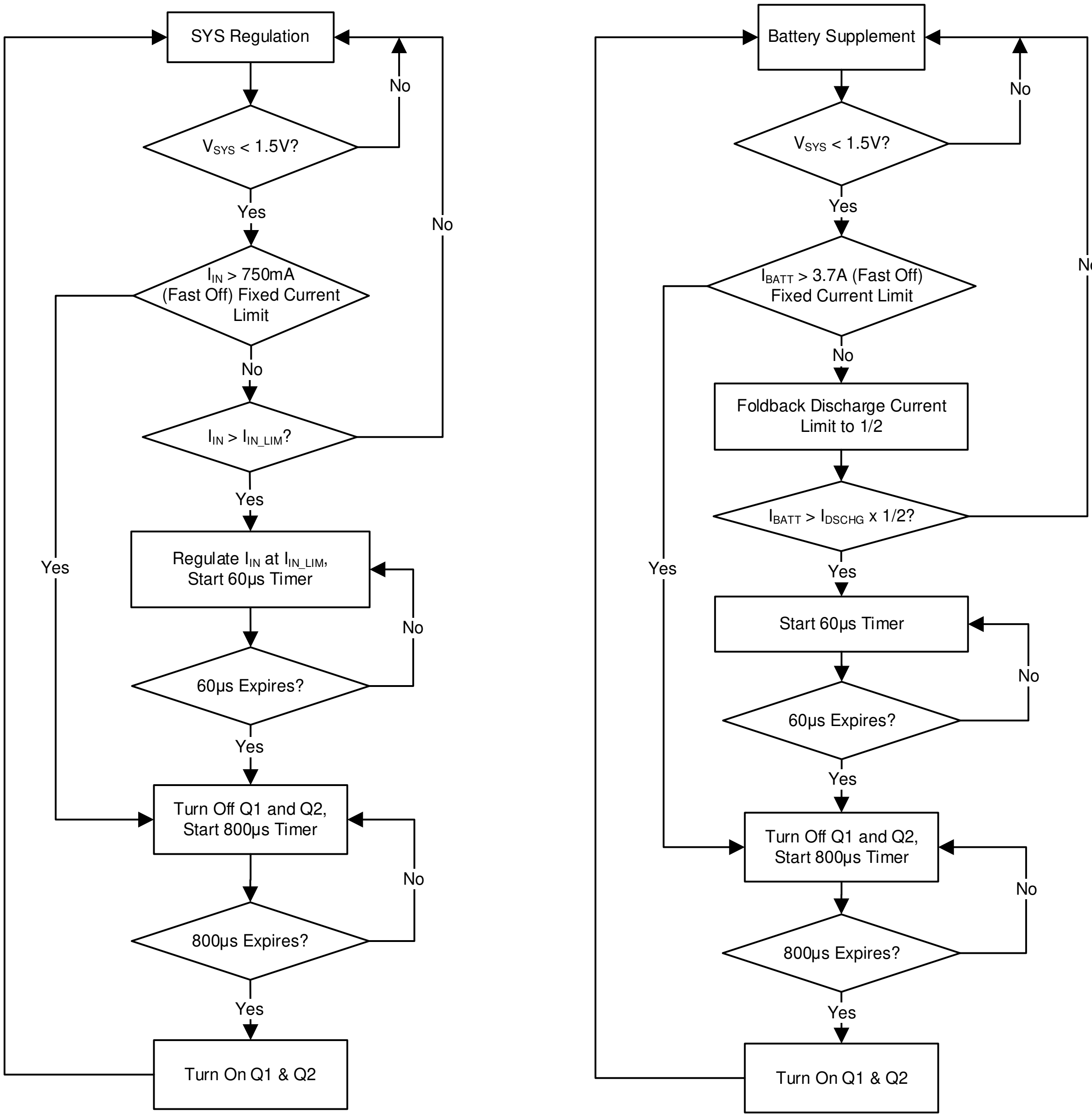


Figure 22: System Short-Circuit Protection (SCP)

CONTROL FLOWCHART *(continued)*

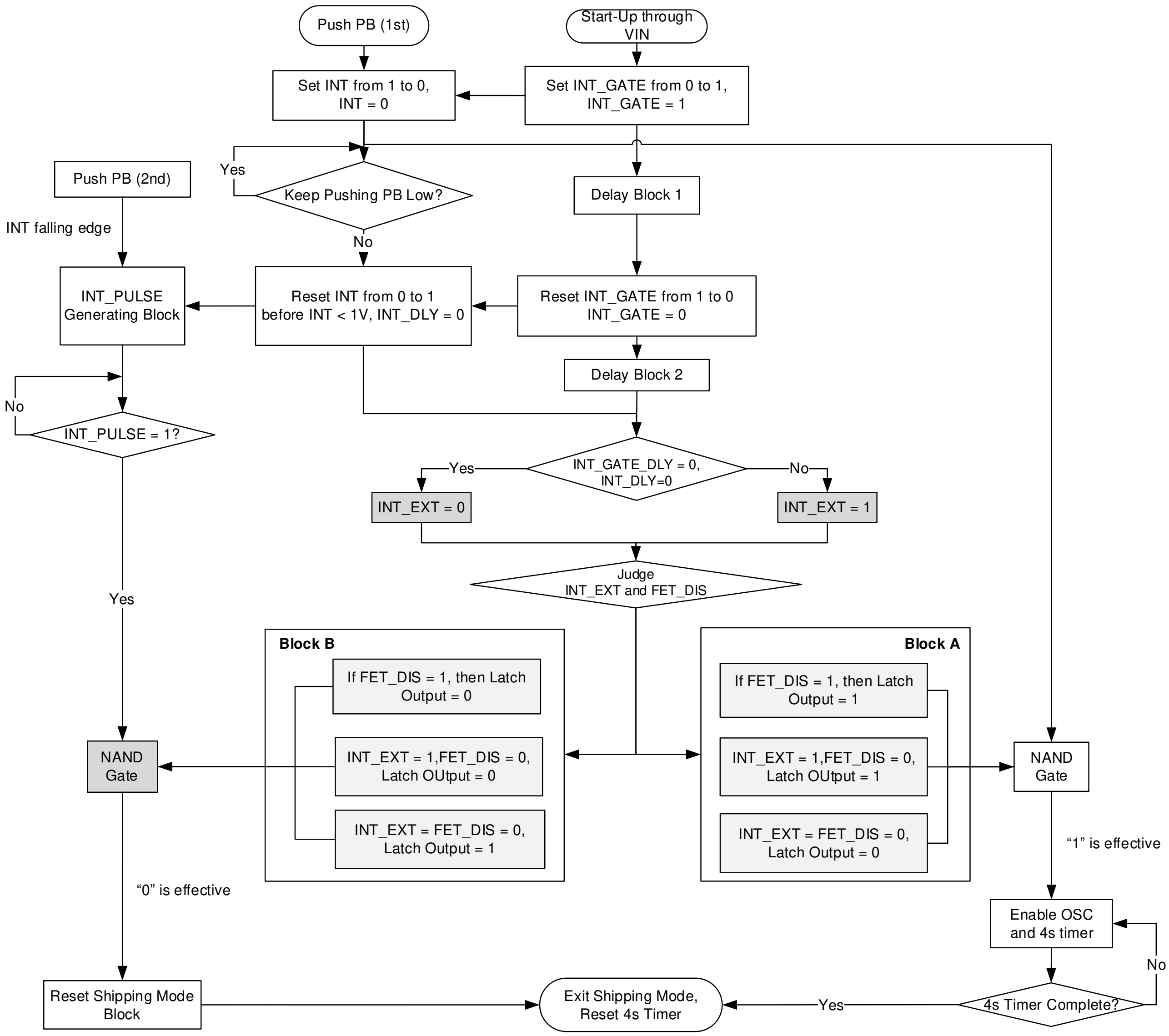


Figure 23: MP2661 Exits Shipping Mode

APPLICATION INFORMATION

Selecting a Resistor for the NTC Sensor

NTC uses a resistor divider from the input source (VDD) to sense the battery temperature. The two resistors (R_{T1} and R_{T2}) allow the high temperature limit and low temperature limit to be programmed independently. In other words, the IC can fit most types of NTC resistors and different temperature operation range requirements with the two extra resistors. R_{T1} and R_{T2} depends on the NTC resistor. R_{T2} can be calculated with Equation (1):

$$R_{T2} = \frac{(V_{COLD} - V_{HOT}) \times R_{NTCH} \times R_{NTCL}}{(V_{HOT} - V_{COLD}V_{HOT}) \times R_{NTCL} - (V_{COLD} - V_{COLD}V_{HOT}) \times R_{NTCH}} \quad (1)$$

R_{T1} can be calculated with Equation (2):

$$R_{T1} = \frac{1\text{-}V_{COLD}}{V_{COLD}} \times (R_{T2} // R_{NTCL}) \quad (2)$$

Where R_{NTCH} is the NTC resistance at a high temperature of the required temperature operation range, and R_{NTCL} is the value of the NTC resistance at a low temperature.

Selecting the External Capacitor

As with most low-dropout (LDO) regulators, the MP2661 requires external capacitors for regulator stability and voltage spike immunity. The device is specifically designed for portable applications requiring minimum board space and small components. These capacitors must be correctly selected for optimal performance.

An input capacitor is required for stability. A capacitor at least 1µF must be connected between IN and GND for stable operation over the entire load current range. There can be more output capacitance than input as long as the input is at least 1µF.

The IC is designed specifically to work with a very small ceramic output capacitor. A ceramic capacitor with X5R or X7R type dielectrics at least 10µF is suitable in the MP2661 application circuit. For the MP2661, the output capacitor should be connected between SYS and GND with thick traces and a small loop area.

A capacitor from BATT to GND is also necessary for the MP2661, and the typical capacitance value is 4.7µF. A ceramic capacitor with X5R or X7R type dielectrics at least 4.7µF is suitable for the application circuit.

A capacitor between VDD and GND is used to stabilize the VDD voltage to power the internal control and logic circuit. The typical value of this capacitor is 100nF.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 24, follow the guidelines below:

1. To ensure a small input inductance and ground impedance, place the external capacitors as close to the IC as possible.
2. Place the PCB trace connecting the capacitor between VDD and GND as close to the IC as possible.
3. Keep the AGND I2C wire clean and away from PGND.
4. Place the I2C wire in parallel.

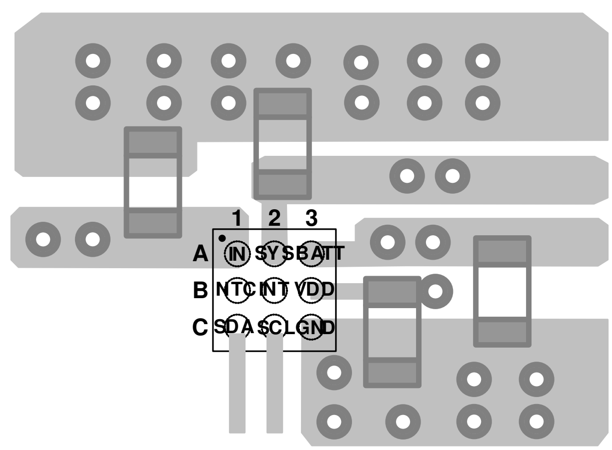


Figure 24: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

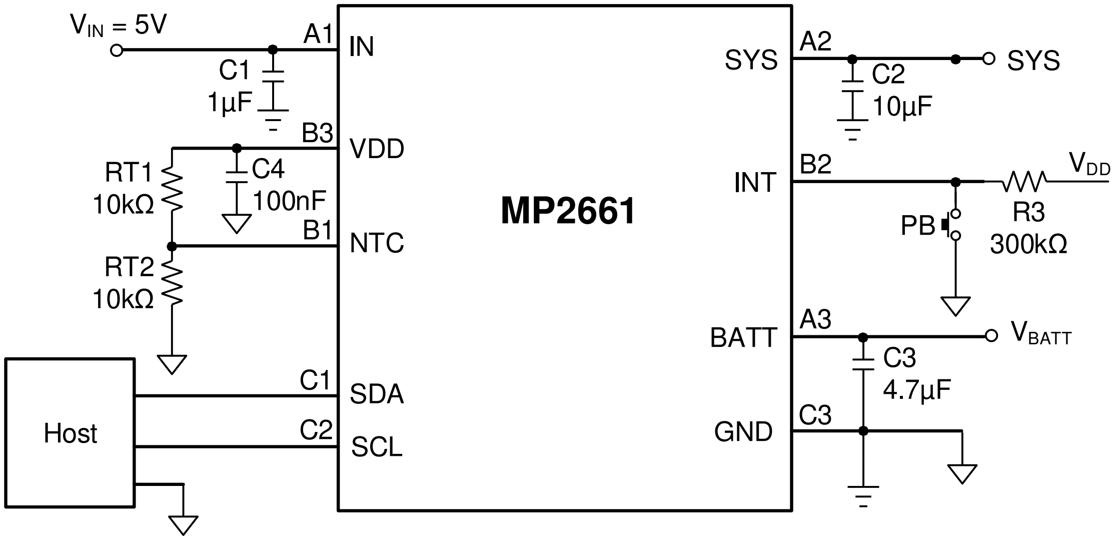


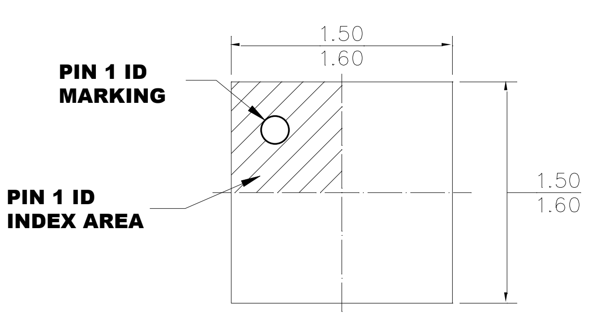
Figure 25: Typical Application Circuit with 5V Input

Table 5: Bill of Materials

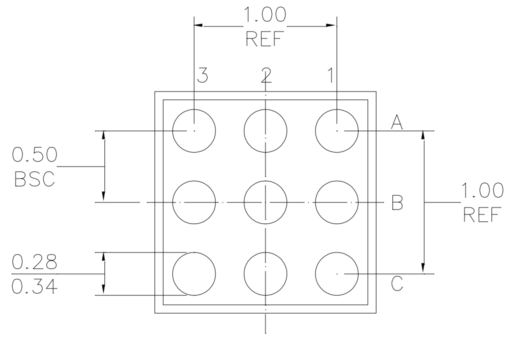
Qty	Ref	Value	Description	Package	Manufacturer
1	C1	1µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C2	10µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C3	4.7µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C4	100nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any

PACKAGE INFORMATION

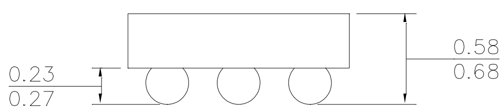
WLCSP-9 (1.55mmx1.55mm)



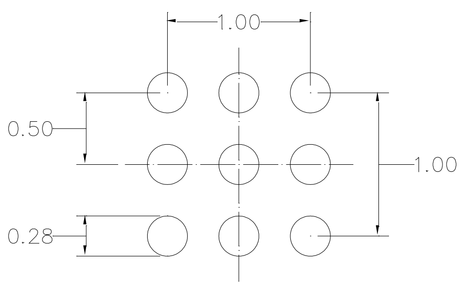
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211, VARIATION BC.
4) DRAWING IS NOT TO SCALE.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/14/2017	Initial Release	-
1.1	06/22/2021	Added “IEC 62368-1 CB Certified” to the Features section	1
		Update descriptions in the Pin Functions section	4
		Updated “CE=L” to “CEB = 0” and “CE=H” to “CEB = 1”	6–8
		Updated “I_{TC}” to “I_{PRE}”, “I_{BF}” to “I_{TERM}” and “V_{IN_REG}” to “V_{IN_MIN}”	6–32
		Updated the Typical Performance Characteristics section	10–13
		Updated the Operation section; added I2C section	15–23
		Updated the Control Flowchart section	31–34
		Updated the Equation 1 and Equation 2 introduction sentences	35
		Formatting, grammar and clerical updates; updated figure titles; updated note numbers.	All