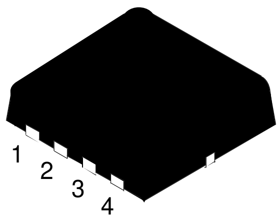
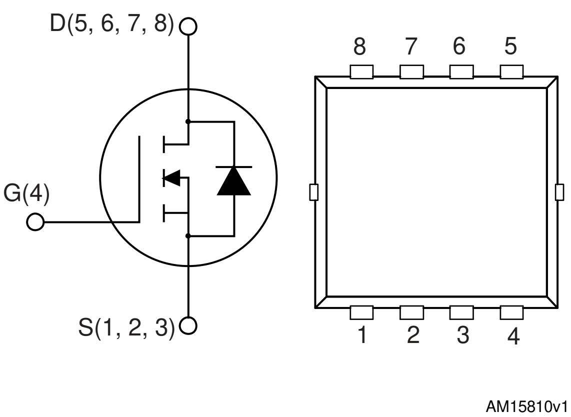
N-channel 60 V, 0.0046 Ω typ., 20 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 3.3x3.3 package

Datasheet - production data



PowerFLAT™ 3.3x3.3 HV

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STL20N6F7	60 V	0.0054 Ω	20 A

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STL20N6F7	20N6F	PowerFLAT™ 3.3x3.3	Tape and reel

This is information on a product in full production.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D [(1)]	Drain current (continuous) at T_C = 25 °C	100	A
I_D [(1)]	Drain current (continuous) at T_C = 100 °C	61	A
I_{DM} [(1)(2)]	Drain current (pulsed)	400	A
I_D [(3)]	Drain current (continuous) at T_{pcb} = 25 °C	20	A
I_D [(3)]	Drain current (continuous) at T_{pcb} = 100 °C	12	A
I_{DM} [(2)(3)]	Drain current (pulsed)	80	A
P_{TOT} [(1)]	Total dissipation at T_C = 25 °C	78	W
P_{TOT} [(3)]	Total dissipation at T_{pcb} = 25 °C	3	W
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Operating junction temperature		

Notes:

(1)This value is rated according to R_{thj-c}.

(2)Pulse width limited by safe operating area.

(3)This value is rated according to $R_{thj-pcb}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}$ [(1)]	Thermal resistance junction-pcb max.	42.8	°C/W
$R_{thj-case}$	Thermal resistance junction-case max.	1.6	°C/W

Notes:

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V V_{DS} = 60 V			1	µA
I_{GSS}	Gate-body leakage current	V_{GS} = 20 V, V_{DS} = 0			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10 A		0.0046	0.0054	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1600	-	pF
C_{oss}	Output capacitance		-	880	-	pF
C_{rss}	Reverse transfer capacitance		-	66	-	pF
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 20 A, V_{GS} = 10 V	-	25	-	nC
Q_{gs}	Gate-source charge		-	7.2	-	nC
Q_{gd}	Gate-drain charge		-	8.1	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 10 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	15	-	ns
t_r	Rise time		-	17.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	24.4	-	ns
t_f	Fall time		-	7.8	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 20 A, V_{GS} = 0	-		1.2	V
t_{rr}	Reverse recovery time	I_D = 20 A, di/dt = 100 A/µs V_{DD} = 48 V	-	39.6		ns
Q_{rr}	Reverse recovery charge		-	36		nC
I_{RRM}	Reverse recovery current		-	1.8		A

Notes:

(1) Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics

Figure 2: Safe operating area

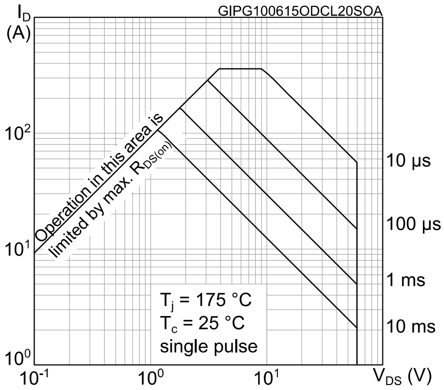


Figure 3: Thermal impedance

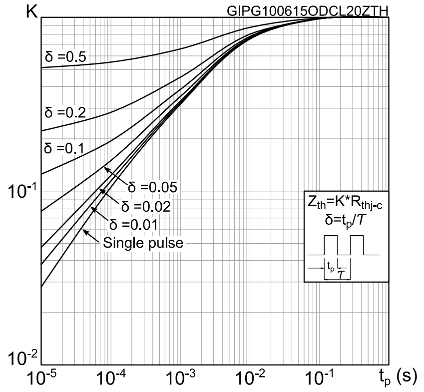


Figure 4: Output characteristics

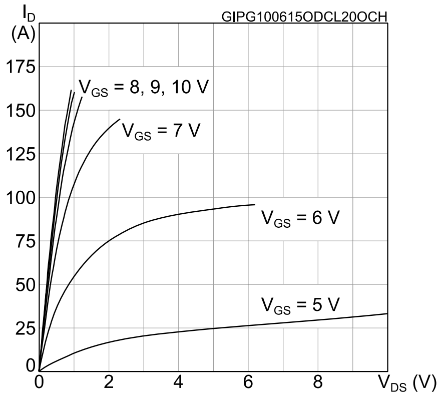


Figure 5: Transfer characteristics

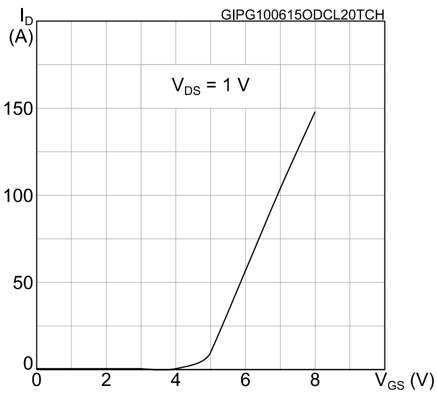


Figure 6: Gate charge vs gate-source voltage

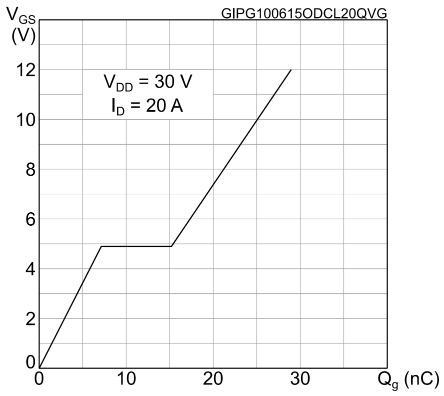


Figure 7: Static drain-source on-resistance

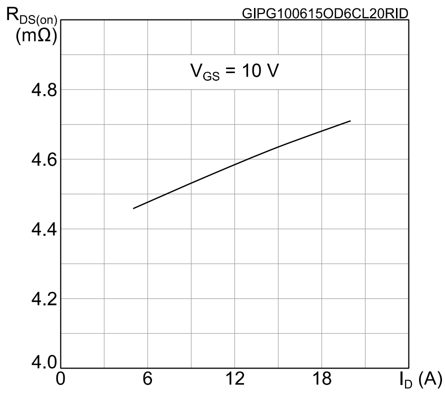


Figure 8: Capacitance variations

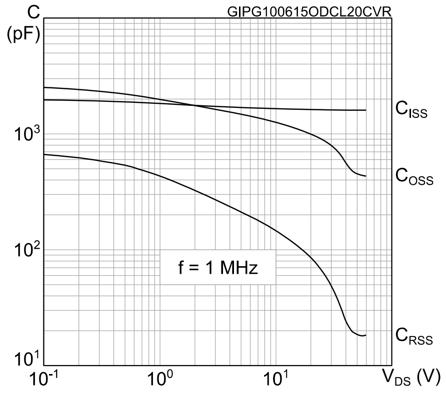


Figure 9: Normalized gate threshold voltage vs temperature

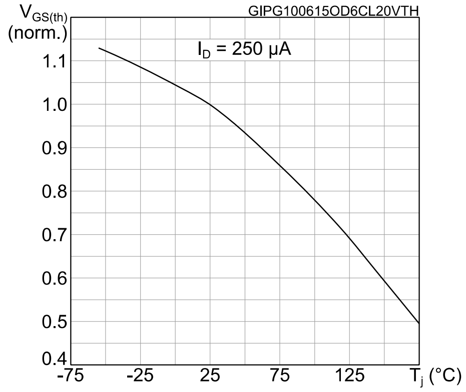


Figure 10: Normalized on-resistance vs temperature

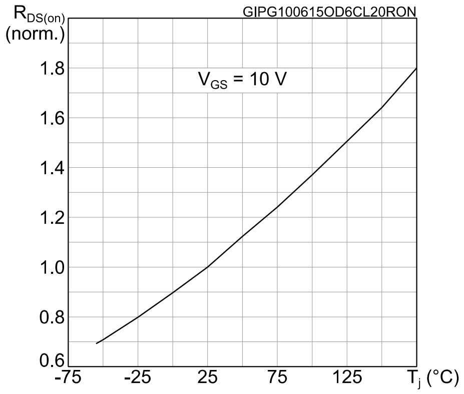


Figure 11: Normalized V(BR)DSS vs temperature

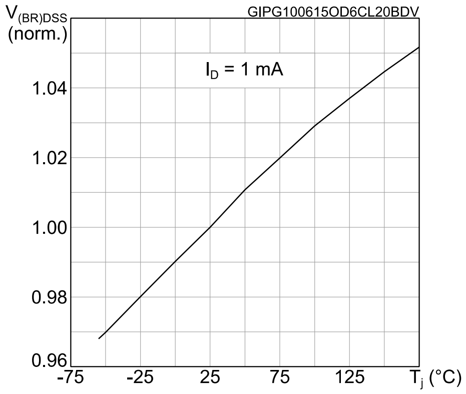
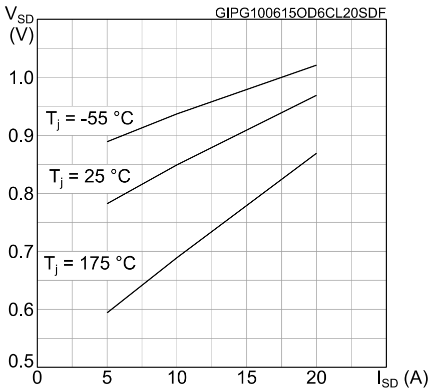


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

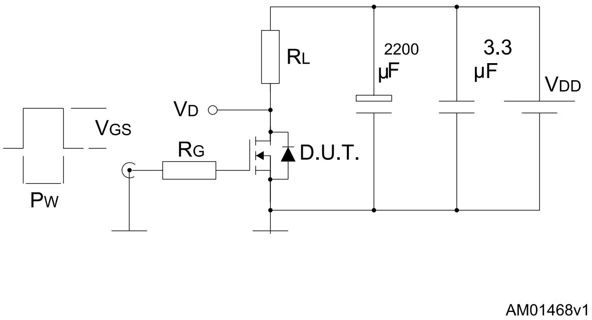


Figure 14: Gate charge test circuit

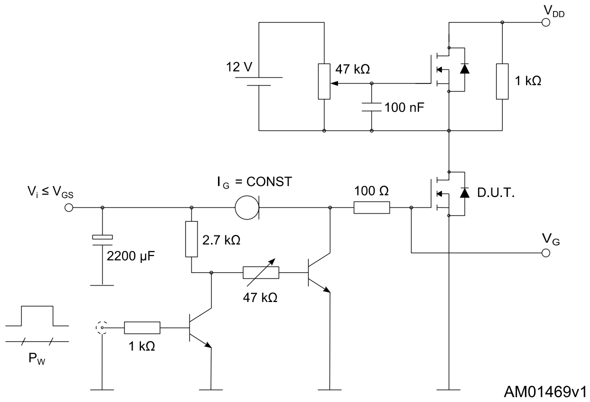


Figure 15: Test circuit for inductive load switching and diode recovery times

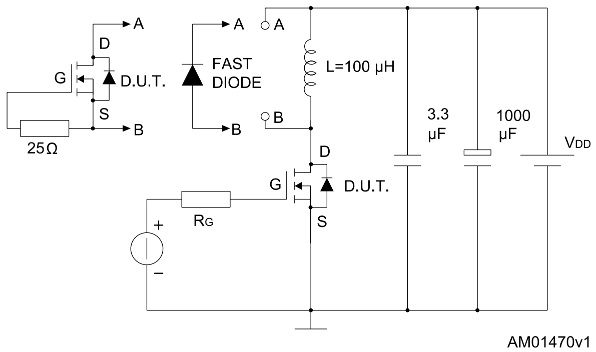


Figure 16: Unclamped inductive load test circuit

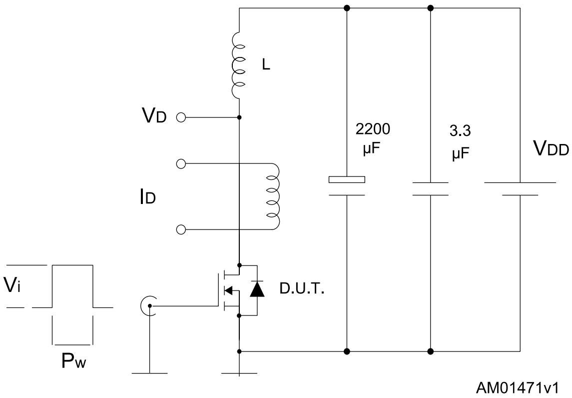


Figure 17: Unclamped inductive waveform

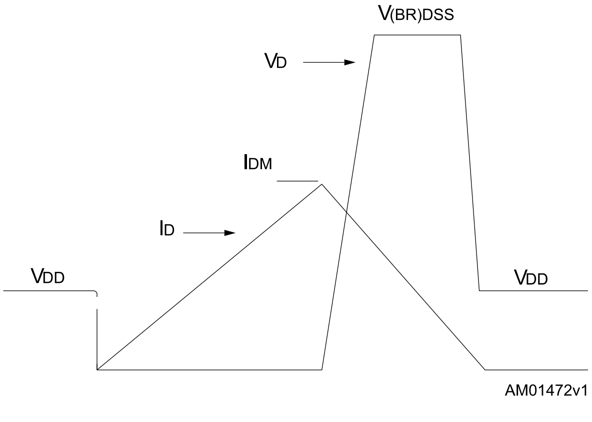
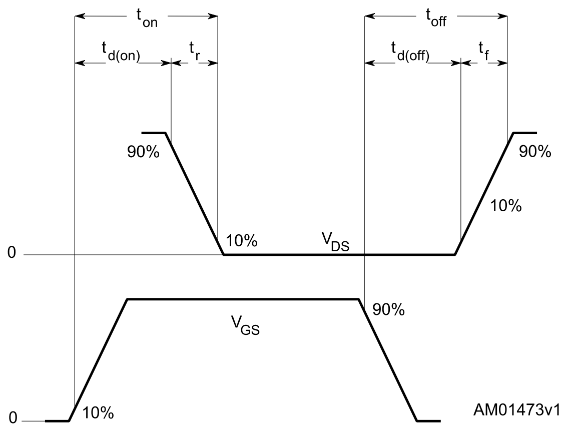


Figure 18: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT 3.3x3.3 package information

Figure 19: PowerFLAT™ 3.3x3.3 HV package outline

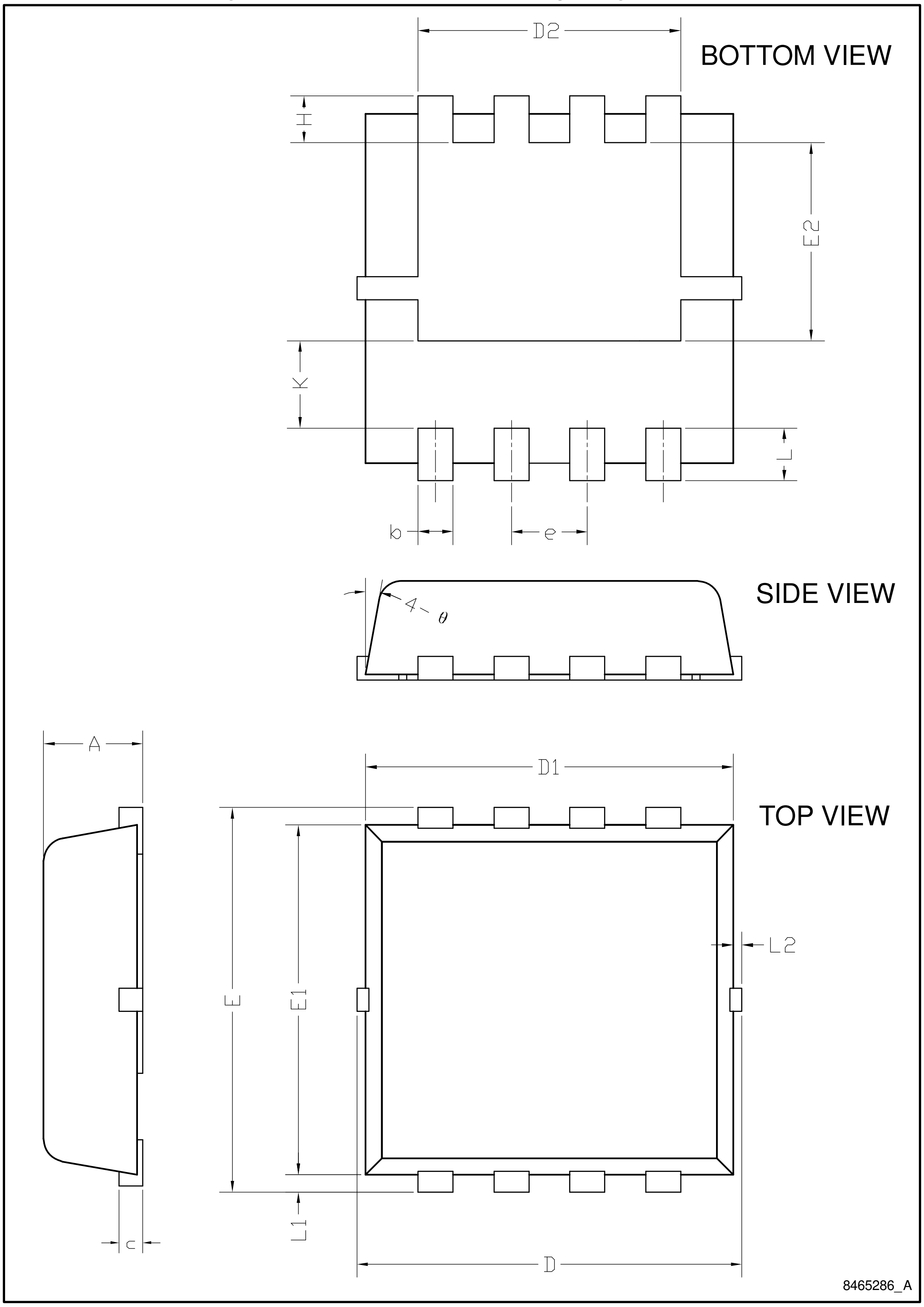
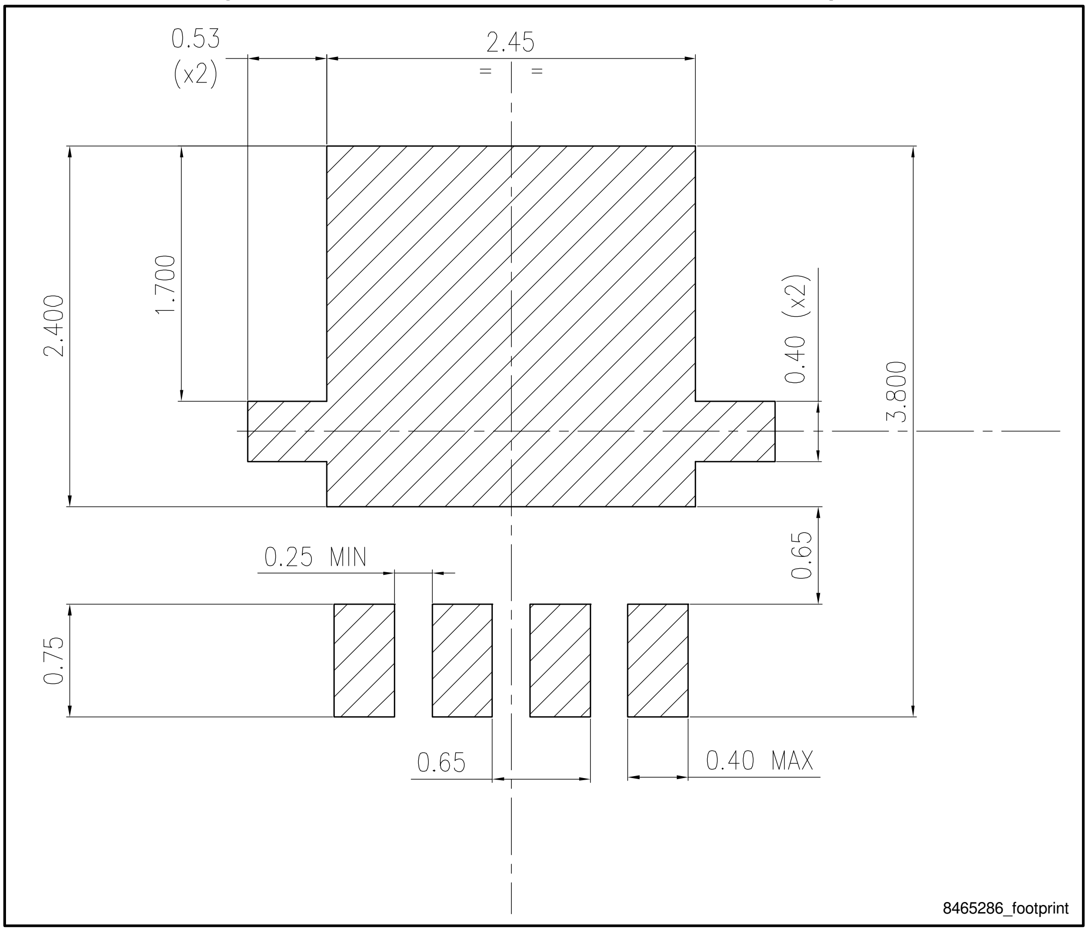


Table 8: PowerFLAT™ 3.3x3.3 HV package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	030	0.45	0.60
L1	0.05	0.15	0.25
L2			0.5
ϑ	8°	10°	12°

Figure 20: PowerFLAT™ 3.3x3.3 HV recommended footprint



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
28-Jan-2015	1	First release.
03-Feb-2015	2	Updated *Table 2: "Absolute maximum ratings"*
10-Jun-2015	3	In Section 2 Electrical characteristics: - updated Table 5: Dynamic - updated Table 6: Switching times - updated Table 7: Source-drain diode Added Section 2.1 Electrical characteristics (curves)