

ISL9016A

150mA Dual LDO with Low Noise, High PSRR and Low I<sub>Q</sub>

FN8865  
Rev 0.00  
August 3, 2016

The [ISL9016A](#) is a high performance dual LDO capable of providing up to 150mA current on each channel. It features a low standby current and very high PSRR and is stable with output capacitance of 1μF to 4.7μF with an ESR of up to 200mΩ.

The device integrates a separate enable function for each output. The quiescent current is typically 49μA when only one LDO is enabled and typically 80μA when both LDOs are enabled. When both LDOs are under shutdown condition, the drawing current is typically less than 1μA.

The ISL9016A provides a wide input voltage range from 1.8V to 6.5V. It also has a high PSRR of 80dB at 1kHz and 45dB at 1MHz. The ISL9016A also provides output current limit, overheat protection, reverse current protection, as well as excellent load transient response.

The ISL9016A is offered in a tiny 1.6mmx1.6mm 6 Ld UTDFN package. Output voltage options are available from 1.2V to 2.8V. Several combinations of voltage outputs are standard and others may be available upon request.

**Features**

- Dual integrated 150mA high performance LDOs
- High PSRR: 80dB at 1kHz and 45dB at 1MHz
- Reverse current protection
- Low quiescent current
  - 49μA (single LDO enabled)/80μA (dual LDOs enabled)
- Excellent load transient response
- Typically ±0.8% output voltage accuracy
- Low output noise: typically 25μV<sub>RMS</sub>
- Wide input voltage capability: 1.8V to 6.5V
- Low dropout voltage: typically 120mV at 150mA
- Separate enable control for each LDO
- Stable with 1μF to 4.7μF ceramic output capacitors
- Soft-start to limit input current surge during enable
- Current limit and overheat protection
- Tiny 6 Ld 1.6mmx1.6mm UTDFN package
- Pb-free (RoHS Compliant)

**Applications**

- PDAs, cell phones and smart phones
- Portable instruments, MP3/4 players, PMP, DSC
- Handheld devices including medical handhelds

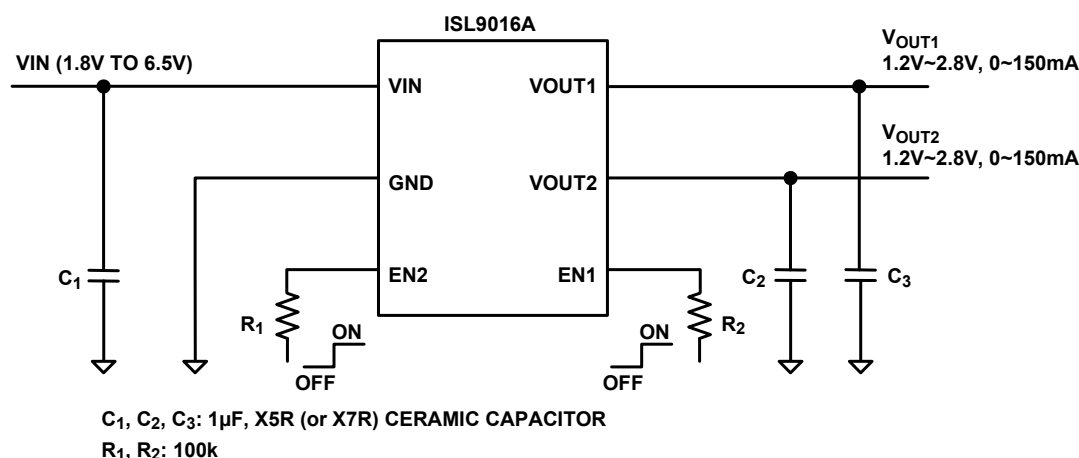
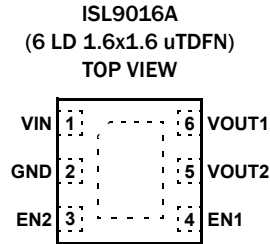


FIGURE 1. TYPICAL APPLICATION DIAGRAM

## Pin Configuration



## Pin Descriptions

| PIN # | PIN NAME | DESCRIPTION  |
|-------|----------|--|
| 1     | VIN      | Supply Voltage/LDO input. Connect a 1 $\mu$ F capacitor to GND.  |
| 2     | GND      | GND is the connection to system ground. Connect to PCB ground plane.   |
| 3     | EN2      | LDO2 Enable pin. Enable = High, Disable = Low. A 100k resistor should be connected between EN2 and the control voltage rail. Do NOT leave it floating. |
| 4     | EN1      | LDO1 Enable pin. Enable = High, Disable = Low. A 100k resistor should be connected between EN1 and the control voltage rail. Do NOT leave it floating. |
| 5     | VOUT2    | LDO2 Output. Connect capacitor with a value from 1 $\mu$ F to 4.7 $\mu$ F to GND (1 $\mu$ F recommended).  |
| 6     | VOUT1    | LDO1 Output. Connect capacitor with a value from 1 $\mu$ F to 4.7 $\mu$ F to GND (1 $\mu$ F recommended).  |
| -     | E-Pad    | Connect the e-pad to the system ground.  |

## Ordering Information

| PART NUMBER<br>(Notes 1, 3) | PART MARKING | V <sub>OUT1</sub> VOLTAGE<br>(V) (Note 2) | V <sub>OUT2</sub> VOLTAGE<br>(V) (Note 2) | TEMP RANGE<br>(°C) | TAPE AND REEL<br>(UNITS) | PACKAGE<br>(RoHS COMPLIANT) | PKG<br>DWG. # |
|-----------------------------|--------------|---|---|--------------------|--------------------------|-----------------------------|---------------|
| ISL9016AIRUWJZ-T            | W2           | 1.2                                       | 2.8                                       | -40 to +85         | 3k                       | 6 Ld UTDFN                  | L6.1.6x1.6A   |
| ISL9016AIRUJCZ-T            | W1           | 2.8                                       | 1.8                                       | -40 to +85         | 3k                       | 6 Ld UTDFN                  | L6.1.6x1.6A   |
| ISL9016AIRUNCZ-T            | W3           | 3.3                                       | 1.8                                       | -40 to +85         | 3k                       | 6 Ld UTDFN                  | L6.1.6x1.6A   |

### NOTES:

- Please refer to [TB347](#) for details on reel specifications.
- For other output voltages, contact Intersil marketing or local sales office.
- These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), please see device information page for [ISL9016A](#). For more information on MSL please see techbrief [TB363](#).

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

| PART NUMBER | DUAL /SINGLE | MAXIMUM OUTPUT CURRENT<br>(mA) | OUTPUT VOLTAGES<br>(V) |
|-------------|--------------|--------------------------------|------------------------|
| ISL9016A    | Dual         | 150                            | 1.2 to 2.8             |
| ISL9021A    | Single       | 250                            | 0.9 to 3.3             |
| ISL9008A    | Single       | 150                            | 1.5 to 3.3             |

**Absolute Maximum Ratings**

|                       |                             |
|-----------------------|-----------------------------|
| $V_{IN}$ to GND       | -0.3V to +7.1V              |
| All Other Pins to GND | -0.3 to ( $V_{IN} + 0.3$ )V |
| ESD Rating            |                             |
| Human Body Model      | 2kV                         |
| Charged Device Model  | 1.5kV                       |
| Machine Model         | 200V                        |

**Thermal Information**

|                             |                           |
|-----------------------------|---------------------------|
| Thermal Resistance          | $\theta_{JA}$ (°C/W)      |
| 6 Ld uTDFN Package (Note 5) | 117.5                     |
| Junction Temperature Range  | -40°C to +125°C           |
| Operating Temperature Range | -40°C to +85°C            |
| Storage Temperature Range   | -65°C to +150°C           |
| Pb-Free Reflow Profile (*)  | see <a href="#">TB487</a> |

**Recommended Operating Conditions**

|                                     |                |
|-------------------------------------|----------------|
| Supply Voltage ( $V_{IN}$ )         | 1.8V to 6.5V   |
| Each LDO Load Current               | up to 150mA    |
| Ambient Temperature Range ( $T_A$ ) | -40°C to +85°C |

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**NOTE:**

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief [TB379](#).

**Electrical Specifications** Typical specifications are measured at the following conditions:  $T_A = +25^\circ\text{C}$ ;  $V_{IN} = (V_{OUT} + 0.5\text{V})$  to 6.5V with a minimum  $V_{IN}$  of 1.8V;  $C_{IN} = 1\mu\text{F}$ ;  $C_O = 1\mu\text{F}$ . **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

| PARAMETER                    | SYMBOL    | TEST CONDITIONS  | MIN<br>(Note 8) | TYP   | MAX<br>(Note 8) | UNIT                |
|------------------------------|-----------|--|-----------------|-------|-----------------|---------------------|
| <b>DC CHARACTERISTICS</b>    |           |  |                 |       |                 |                     |
| Supply Voltage               | $V_{IN}$  |  | <b>1.8</b>      |       | <b>6.5</b>      | V                   |
| UVLO Threshold               | $V_{UV+}$ |  |                 | 1.710 | <b>1.775</b>    | V                   |
|                              | $V_{UV-}$ |  | <b>1.55</b>     | 1.62  |                 |                     |
| Input Quiescent Current      |           | Quiescent condition: $I_{OUT1} = 0\mu\text{A}$ ; $I_{OUT2} = 0\mu\text{A}$                                       |                 |       |                 |                     |
|                              | $I_{DD1}$ | One LDO active   |                 | 49    | <b>67</b>       | $\mu\text{A}$       |
|                              | $I_{DD2}$ | Both LDO active  |                 | 80    | <b>100</b>      | $\mu\text{A}$       |
| Shutdown Current             | $I_{DDS}$ | At +25°C   |                 | 0.1   | 1.0             | $\mu\text{A}$       |
| Regulation Voltage Accuracy  |           | $V_{IN} = V_{OUT} + 0.5\text{V}$ to 6.5V, $I_{OUT} = 10\mu\text{A}$ to 150mA, $T_A = +25^\circ\text{C}$          | -0.8            |       | +0.8            | %                   |
|                              |           | $V_{IN} = V_{OUT} + 0.5\text{V}$ to 6.5V, $I_{OUT} = 10\mu\text{A}$ to 150mA, $T_A = -40^\circ\text{C}$ to +85°C | <b>-1.8</b>     |       | <b>+1.8</b>     | %                   |
| Maximum Output Current       | $I_{MAX}$ | Each LDO, Continuous   | 150             |       |                 | mA                  |
| Internal Current Limit       | $I_{LIM}$ |  | 175             | 265   | <b>355</b>      | mA                  |
| Dropout Voltage (Note 6)     | $V_{D01}$ | $I_{OUT} = 150\text{mA}$ ; $1.2\text{V} \leq V_{OUT} \leq 2.1\text{V}$   |                 | 250   | <b>425</b>      | mV                  |
|                              | $V_{D02}$ | $I_{OUT} = 150\text{mA}$ ; $2.1\text{V} \leq V_{OUT} \leq 2.8\text{V}$   |                 | 200   | <b>325</b>      | mV                  |
|                              | $V_{D03}$ | $I_{OUT} = 150\text{mA}$ ; $2.8\text{V} \leq V_{OUT}$  |                 | 120   | <b>200</b>      | mV                  |
| Thermal Shutdown Temperature | $T_{SD+}$ |  |                 | 145   |                 | °C                  |
|                              | $T_{SD-}$ |  |                 | 110   |                 | °C                  |
| <b>AC CHARACTERISTICS</b>    |           |  |                 |       |                 |                     |
| Ripple Rejection             |           | $I_{OUT} = 10\text{mA}$ , $V_{IN} = 3.7\text{V}$ (minimum), $V_{OUT} = 2.7\text{V}$ , $T_A = +25^\circ\text{C}$  |                 |       |                 |                     |
|                              |           | At 1kHz  |                 | 80    |                 | dB                  |
|                              |           | At 10kHz   |                 | 60    |                 | dB                  |
|                              |           | At 100kHz  |                 | 50    |                 | dB                  |
|                              |           | At 1MHz  |                 | 45    |                 | dB                  |
| Output Noise Voltage         |           | $V_{IN} = 4.2\text{V}$ , $I_{OUT} = 10\text{mA}$ , $T_A = +25^\circ\text{C}$ , BW = 10Hz to 100kHz               |                 | 25    |                 | $\mu\text{V}_{RMS}$ |

**Electrical Specifications** Typical specifications are measured at the following conditions:  $T_A = +25^\circ\text{C}$ ;  $V_{IN} = (V_{OUT} + 0.5\text{V})$  to 6.5V with a minimum  $V_{IN}$  of 1.8V;  $C_{IN} = 1\mu\text{F}$ ;  $C_O = 1\mu\text{F}$ . **Boldface limits apply across the operating temperature range,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .** (Continued)

| PARAMETER                               | SYMBOL           | TEST CONDITIONS  | MIN<br>(Note 8) | TYP | MAX<br>(Note 8)                  | UNIT                   |
|---|------------------|--|-----------------|-----|----------------------------------|------------------------|
| <b>DEVICE START-UP CHARACTERISTICS</b>  |                  |  |                 |     |                                  |                        |
| Device Enable Time                      | $t_{EN}$         | Time from assertion of the ENx pin to when the output voltage reaches 95% of the $V_{OUT}$ (nominal) |                 | 400 | <b>600</b>                       | $\mu\text{s}$          |
| LDO Soft-Start Ramp Rate                | $t_{SSR}$        | Slope of linear portion of LDO output voltage ramp during start-up                                   |                 | 30  | <b>60</b>                        | $\mu\text{s}/\text{V}$ |
| <b>EN PIN CHARACTERISTICS</b>           |                  |  |                 |     |                                  |                        |
| Input Low Voltage                       | $V_{IL}$         | $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$   | -0.3            |     | 0.4                              | V                      |
| Input High Voltage                      | $V_{IH}$         |  | <b>1.1</b>      |     | <b><math>V_{IN} + 0.3</math></b> | V                      |
| Input Leakage Current                   | $I_{IL}, I_{IH}$ |  |                 |     | <b>0.1</b>                       | $\mu\text{A}$          |
| <b>REVERSE CURRENT CHARACTERISTICS</b>  |                  |  |                 |     |                                  |                        |
| Output Reverse Leakage Current (Note 7) | $I_{ORLC}$       | $V_{IN} = 0\text{V}, V_{OUT} = 5.5\text{V}$  |                 | 8   | <b>15</b>                        | $\mu\text{A}$          |

## NOTES:

- $V_{OX} = 0.98 \cdot V_{OX}(\text{NOM})$ ; Valid for  $V_{OX}$  greater than 1.80V.
- Output reverse leakage current is measured with  $V_{IN}$  pin grounded and  $V_{OUT}$  pin connected to 5.5V.
- Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ\text{C}$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

## Typical Operating Performance

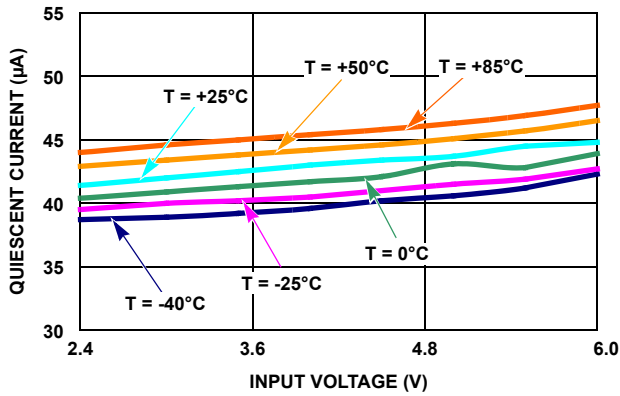


FIGURE 2. QUIESCENT CURRENT vs INPUT VOLTAGE ( $V_{OUT1} = 2.8V$ , ONLY LDO1 ENABLED)

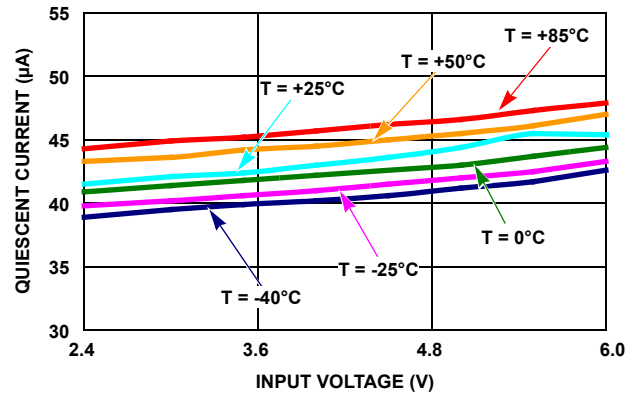


FIGURE 3. QUIESCENT CURRENT vs INPUT VOLTAGE ( $V_{OUT2} = 2.8V$ , ONLY LDO2 ENABLED)

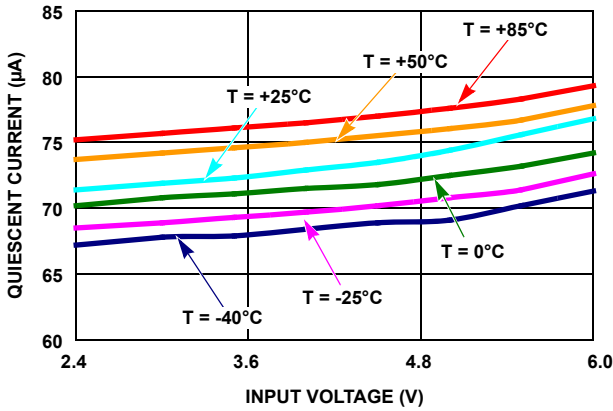


FIGURE 4. QUIESCENT CURRENT vs INPUT VOLTAGE ( $V_{OUT1} = 1.2V$ ,  $V_{OUT2} = 2.8V$ , LDO1 AND LDO2 ENABLED)

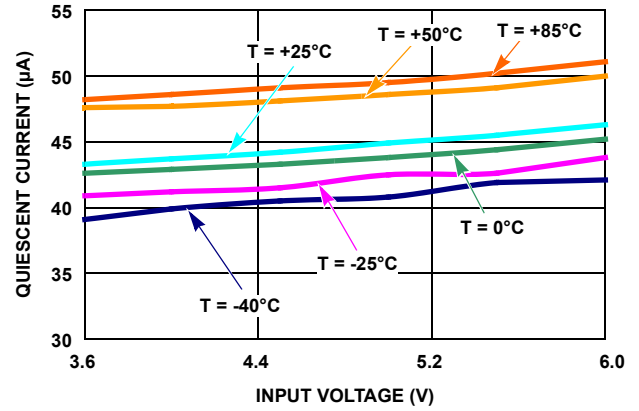


FIGURE 5. QUIESCENT CURRENT vs INPUT VOLTAGE ( $V_{OUT1} = 2.8V$ , ONLY LDO1 ENABLED)

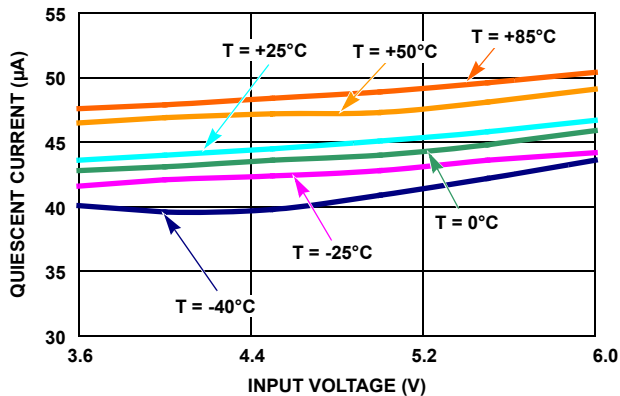


FIGURE 6. QUIESCENT CURRENT vs INPUT VOLTAGE ( $V_{OUT2} = 2.8V$ , ONLY LDO2 ENABLED)

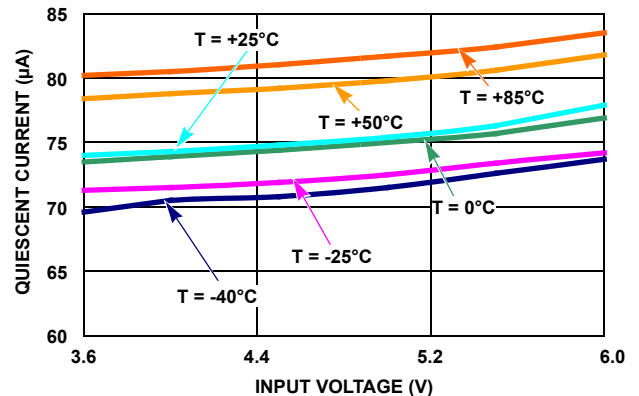


FIGURE 7. QUIESCENT CURRENT vs INPUT VOLTAGE ( $V_{OUT1} = 1.2V$ ,  $V_{OUT2} = 2.8V$ , LDO1 AND LDO2 ENABLED)

## Typical Operating Performance (Continued)

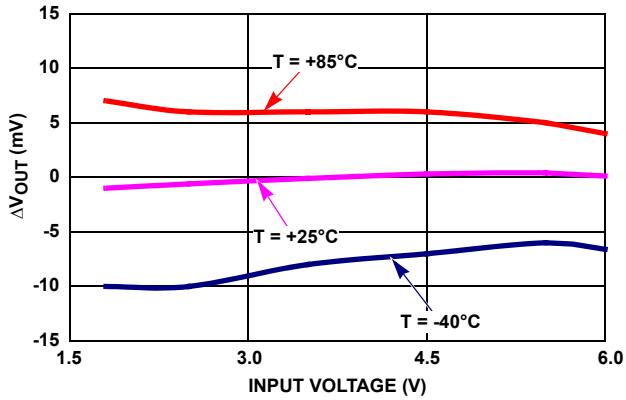


FIGURE 8.  $\Delta V_{OUT}$  vs INPUT VOLTAGE ( $V_{OUT\_NOMINAL} = 1.2V$ ,  $I_{OUT} = 50mA$ )

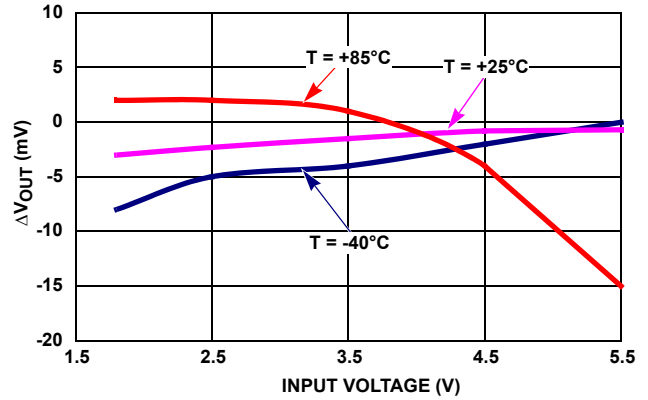


FIGURE 9.  $\Delta V_{OUT}$  vs INPUT VOLTAGE ( $V_{OUT\_NOMINAL} = 1.2V$ ,  $I_{OUT} = 150mA$ )

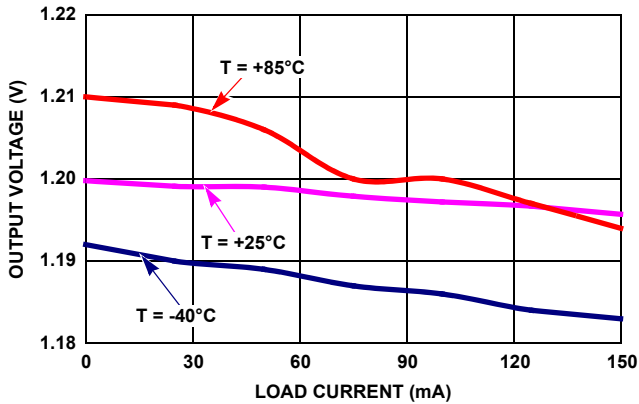


FIGURE 10. LOAD REGULATION ( $V_{IN} = 1.8V$ ,  $V_{OUT} = 1.2V$ )

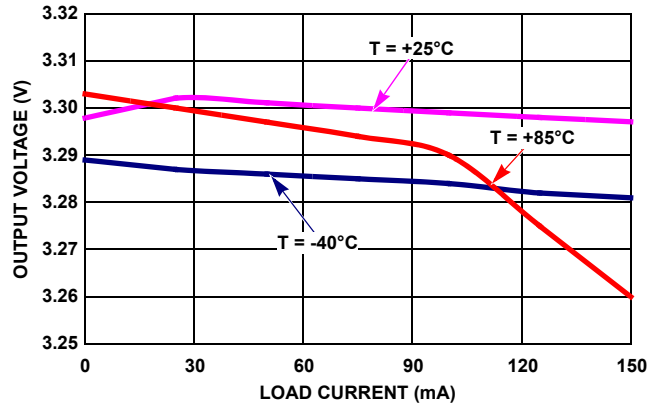


FIGURE 11. LOAD REGULATION ( $V_{IN} = 4.5V$ ,  $V_{OUT} = 2.8V$ )

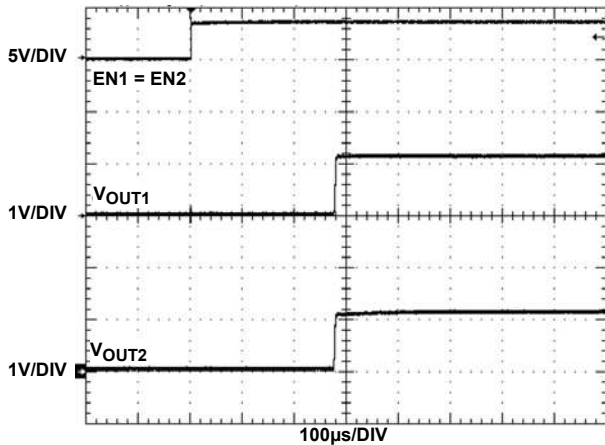


FIGURE 12. ENABLE OPERATION ( $V_{IN} = 3.6V$ ,  $V_{OUT1} = V_{OUT2} = 1.2V$ )

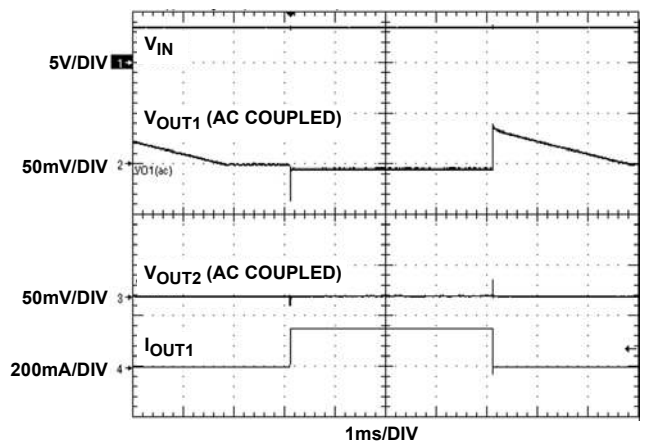


FIGURE 13. LOAD TRANSIENT RESPONSE ( $V_{IN} = 3.6V$ ,  $V_{OUT1} = 1.2V$ ,  $V_{OUT2} = 2.8V$ ,  $I_{OUT1}$  0.01mA TO 150mA)

## Typical Operating Performance (Continued)

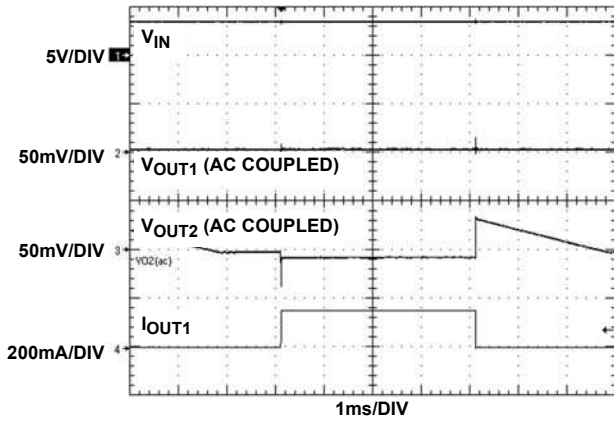


FIGURE 14. LOAD TRANSIENT RESPONSE ( $V_{IN} = 3.6V$ ,  $V_{OUT1} = 1.2V$ ,  $V_{OUT2} = 2.8V$ ,  $I_{OUT2}$  0.01mA TO 150mA)

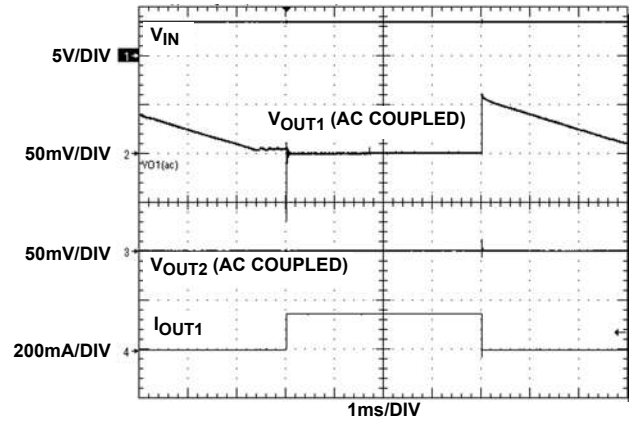


FIGURE 15. LOAD TRANSIENT RESPONSE ( $V_{IN} = 3.6V$ ,  $V_{OUT1} = 2.8V$ ,  $V_{OUT2} = 1.8V$ ,  $I_{OUT1}$  0.01mA TO 150mA)

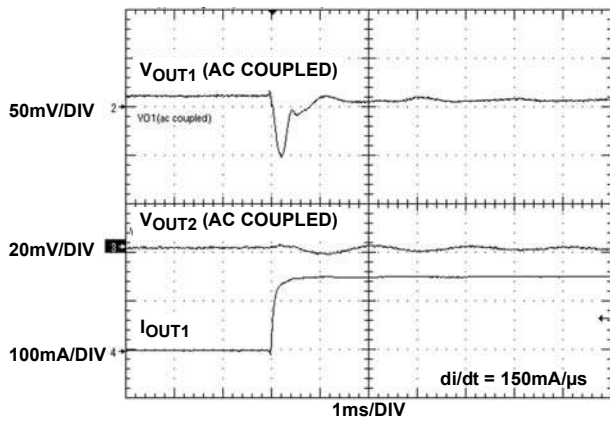


FIGURE 16. LOAD TRANSIENT RESPONSE ( $V_{IN} = 1.8V$ ,  $V_{OUT1} = 1.2V$ ,  $V_{OUT2} = 2.8V$ ,  $I_{OUT1}$  0.01mA TO 150mA)

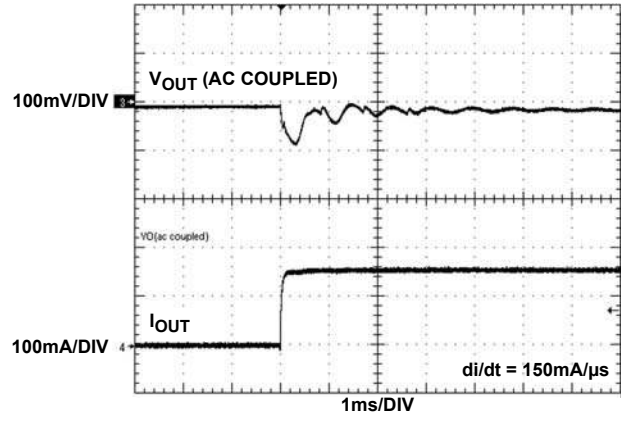


FIGURE 17. LOAD TRANSIENT RESPONSE ( $V_{IN} = 3.3V$ ,  $V_{OUT1} = 1.8V$ ,  $V_{OUT2} = 2.8V$ ,  $I_{OUT1}$  0.01mA TO 150mA)

## Block Diagram

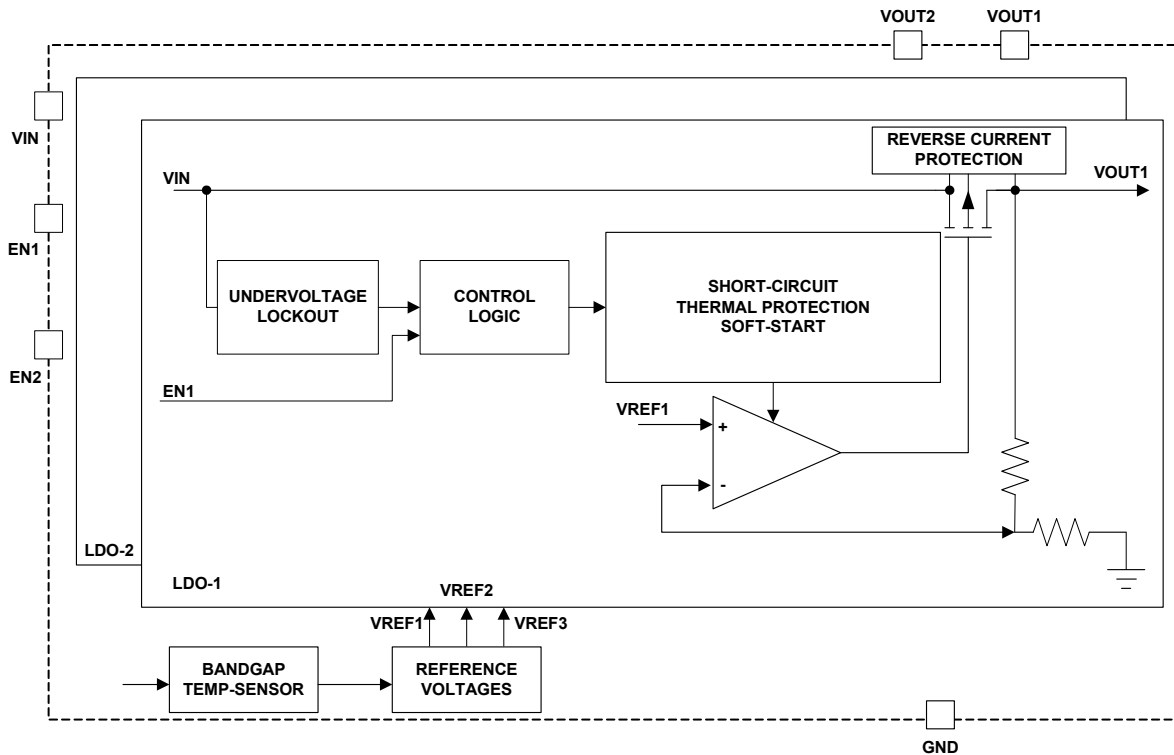


FIGURE 18. BLOCK DIAGRAM

## Functional Description

The ISL9016A contains two high performance LDOs. High performance is achieved through a circuit, which delivers fast transient response to varying load conditions. In a quiescent condition, the ISL9016A adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, thermal shutdown protection, reverse current protection and soft-start. Thermal shutdown protects the device against overheating. Soft-start limits the start-up input current surges. In some certain application circuits, the output voltage may be externally held up, meanwhile, the input voltage could be connected to ground, or connected to some voltage lower than the output side, or be left open circuit. The ISL9016A features the reverse current protection; it can limit the current flow from output to input. This protection will automatically initiate when  $V_{OUT}$  is detected to be higher than  $V_{IN}$ . When  $V_{IN}$  is pulled to ground and  $V_{OUT}$  is held at 5.5V, the current flow from  $V_{OUT}$  to  $V_{IN}$  is typically less than  $8\mu\text{A}$ .

### Enable Control

The ISL9016A has two separate enable pins, EN1 and EN2, which independently enable/disable each of the LDO outputs. When both EN1 and EN2 are low, the whole device is in shutdown mode. In this condition, all on-chip circuits are off, and the device draws minimum current, typically less than 0.1mA. When one or both the EN pins go high, the LDO1 and/or LDO2 will be enabled accordingly based on the voltage signal applied on its related EN pin and start from the soft-start. Likewise, when one or both EN pins go low, LDO1 and/or LDO2 will be disabled based on the signal applied on its related EN

pin. A 100k $\Omega$  (or above) pull-up resistor should be connected between ENx pin and the external control voltage (as shown in the [Figure 1 on page 1](#)).

### LDO Protections

The ISL9016A offers several protections, which make it ideal for using in battery-powered application circuits.

The ISL9016A provides short-circuit protection by limiting the output current to typical 265mA. When a short-circuit happens, the circuit is limited at 265mA (typical). If the short-circuit lasts long enough, the die temperature increases, and the over-temperature protection circuit will turn off the output.

When the die temperature reaches about  $+145^{\circ}\text{C}$ , the thermal protection starts working. Under the overheat condition, only the LDO sourcing more than 50mA will be shut off. This does not affect the operation of the other LDO. If both LDOs source more than 50mA and an overheat condition occurs, both LDO outputs will be disabled. Once the die temperature falls back to about  $+110^{\circ}\text{C}$ , the disabled LDOs are re-enabled and soft-start automatically takes place.

In certain applications, the following input/output situations may occur, with output voltage externally held up higher than the input voltage:

1. Input is pulled to ground
2. Input is left open circuit
3. Input is pulled to some intermediate voltage



The ISL9016A provides the reverse current protection to limit the current flow from output to input under these situations. When input is pulled to ground and output is held to 5.5V, the typical reverse current from output to input side is less than 8 $\mu$ A.

### **Input and Output Capacitors**

The ISL9016A provides a linear regulator that has low quiescent current, fast transient response, and overall stability across the recommended operating conditions. A ceramic capacitor (X5R or X7R) with a capacitance of 1 $\mu$ F to 4.7 $\mu$ F with an ESR up to 200m $\Omega$  is suitable for the ISL9016A to maintain its output stability. The ground connection of the output capacitor should be connected directly to the GND pin of the device, and also placed close to the device. Similarly for the input capacitor, usually a 1 $\mu$ F ceramic capacitor (X5R or X7R) is suitable for most cases, but if large, fast rising-time load transient condition is expected, a higher value input capacitor may be necessary to achieve better performance.

### **Board Layout Recommendations**

A good PCB layout will be an important step to achieve good performance. It is recommended to design the board with separate ground planes for input and output, and connect both ground planes at the GND pin of the device. Consideration should be taken when placing the components and route the trace to minimize the ground impedance, as well as keep the parasitic inductance low. Usually the input/output capacitors should be placed close to the device with good ground connection.

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE           | REVISION | CHANGE          |
|----------------|----------|-----------------|
| August 3, 2016 | FN8865.0 | Initial Release |

## About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at [www.intersil.com](http://www.intersil.com).

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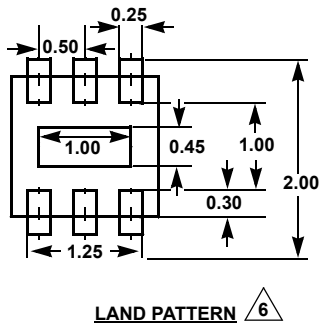
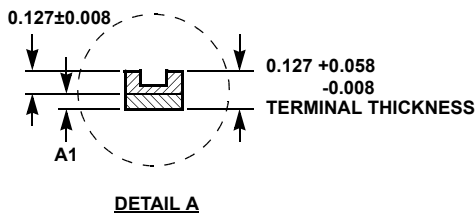
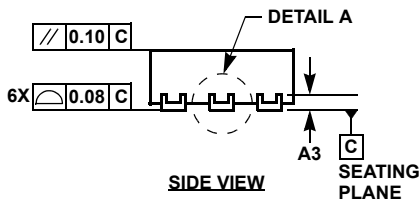
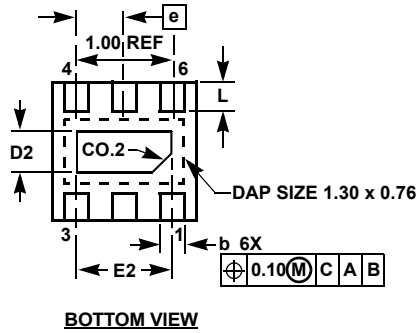
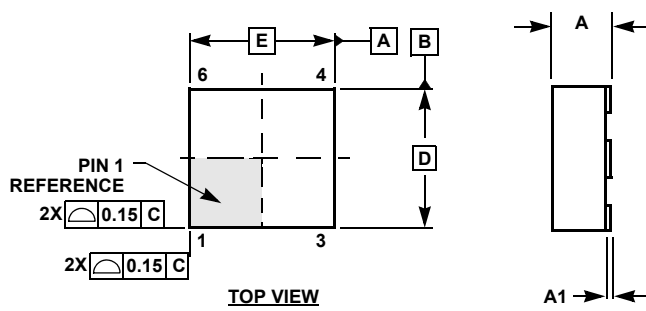
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**Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)**



**L6.1.6x1.6A**

**6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE**

| SYMBOL | MILLIMETERS |         |      | NOTES |
|--------|-------------|---------|------|-------|
|        | MIN         | NOMINAL | MAX  |       |
| A      | 0.45        | 0.50    | 0.55 | -     |
| A1     | -           | -       | 0.05 | -     |
| A3     | 0.127 REF   |         |      | -     |
| b      | 0.15        | 0.20    | 0.25 | -     |
| D      | 1.55        | 1.60    | 1.65 | 4     |
| D2     | 0.40        | 0.45    | 0.50 | -     |
| E      | 1.55        | 1.60    | 1.65 | 4     |
| E2     | 0.95        | 1.00    | 1.05 | -     |
| e      | 0.50 BSC    |         |      | -     |
| L      | 0.25        | 0.30    | 0.35 | -     |

Rev. 1 6/06

**NOTES:**

1. Dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08mm.
3. Warpage shall not exceed 0.10mm.
4. Package length/package width are considered as special characteristics.
5. JEDEC Reference MO-229.
6. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.