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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR **2SJ601**

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ601 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

• Low on-state resistance:

RDS(on)1 = 31 m Ω MAX. (VGS = -10 V, ID = -18 A)

 $R_{DS(on)2} = 46 \text{ m}\Omega \text{ MAX.} (V_{GS} = -4.0 \text{ V}, I_{D} = -18 \text{ A})$

· Low input capacitance:

 $C_{iss} = 3300 \text{ pF TYP.} (V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V})$

- · Built-in gate protection diode
- TO-251/TO-252 package

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	-60	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	I _{D(DC)}	∓36	Α
Drain Current (pulse) Note1	ID(pulse)	∓120	Α
Total Power Dissipation (Tc = 25°C)	Рт	65	W
Total Power Dissipation (T _A = 25°C)	Рт	1.0	W
Channel Temperature	T_ch	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current Note2	las	-35	Α
Single Avalanche Energy Note2	Eas	123	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = -30 V, R_G = 25 Ω , V_{GS} = -20 \rightarrow 0 V

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ601	TO-251 (MP-3)
2SJ601-Z	TO-252 (MP-3Z)

(TO-251)



(TO-252



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ELECTRICAL CHARACTERISTICS (TA = 25°C)

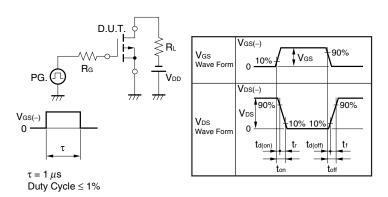
		-				
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = -60 V, V _{GS} = 0 V			-10	μA
Gate Leakage Current	lgss	V _{GS} = ∓20 V, V _{DS} = 0 V			∓10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	-1.5	-2.0	-2.5	V
Forward Transfer Admittance Note	yfs	V _{DS} = -10 V, I _D = -18 A	15	30		S
Drain to Source On-state Resistance Note	RDS(on)1	Vgs = -10 V, ID = -18 A		25	31	mΩ
	RDS(on)2	Vgs = -4.0 V, ID = -18 A		32	46	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V		3300		pF
Output Capacitance	Coss	Vgs = 0 V		580		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		230		pF
Turn-on Delay Time	td(on)	I _D = -18 A		11		ns
Rise Time	tr	V _{GS} = −10 V		12		ns
Turn-off Delay Time	td(off)	$V_{DD} = -30 \text{ V}$		80		ns
Fall Time	t f	$R_G = 0 \Omega$		53		ns
Total Gate Charge	QG	VDD = -48 V		63		nC
Gate to Source Charge	Qgs	V _G S = −10 V		10		nC
Gate to Drain Charge	Q _{GD}	I□ = -36 A		16		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	IF = 36 A, VGS = 0 V		1.0		٧
Reverse Recovery Time	trr	IF = 36 A, VGS = 0 V		52		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		108		nC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$V_{GS} = -20 \rightarrow 0 \text{ V}$ V_{DD} V_{DD}

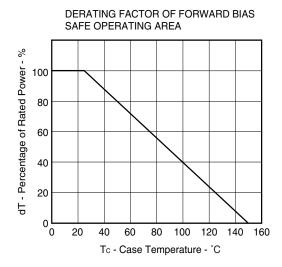
TEST CIRCUIT 2 SWITCHING TIME

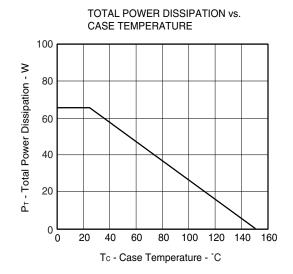


TEST CIRCUIT 3 GATE CHARGE

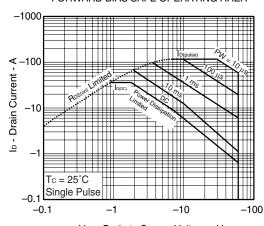
$$\begin{array}{c|c} D.U.T. \\ \hline \\ IG = -2 \text{ mA} \\ \hline \\ PG. \\ \hline \end{array}$$

TYPICAL CHARACTERISTICS (TA = 25°C)



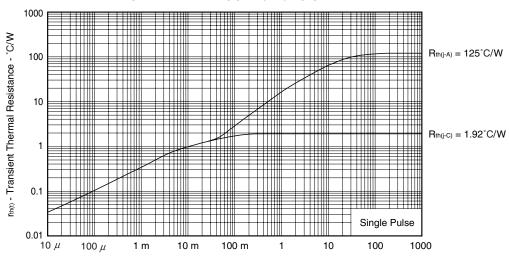


FORWARD BIAS SAFE OPERATING AREA



 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

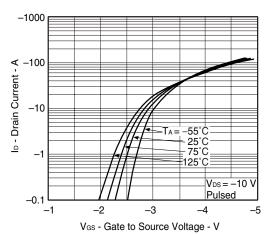
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



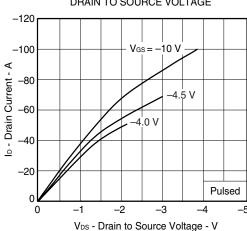
PW - Pulse Width - s

3

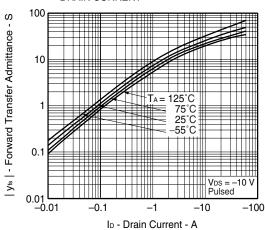
FORWARD TRANSFER CHARACTERISTICS



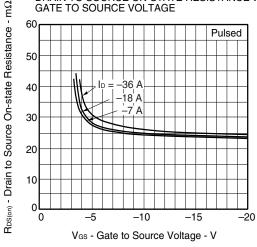




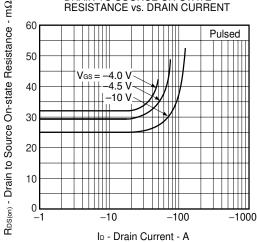
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



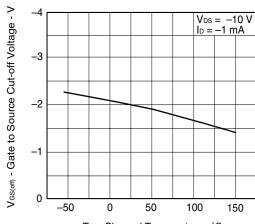
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



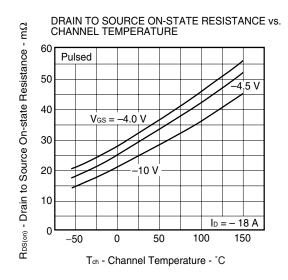
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

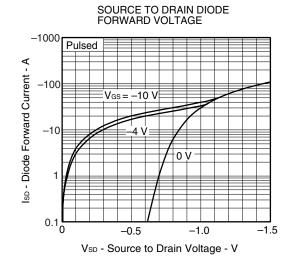


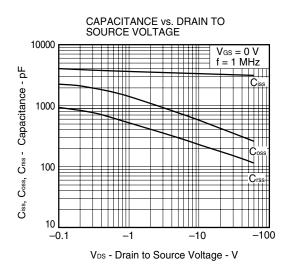
GATE TO SOURCE CUT-OFF VOLTAGE vs. **CHANNEL TEMPERATURE**

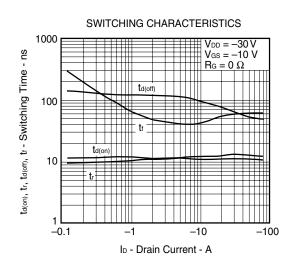


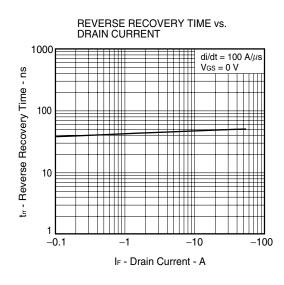
Tch - Channel Temperature - °C

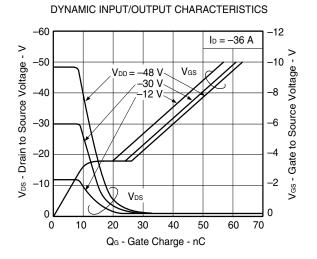


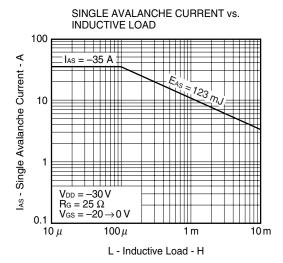


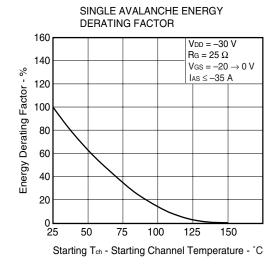






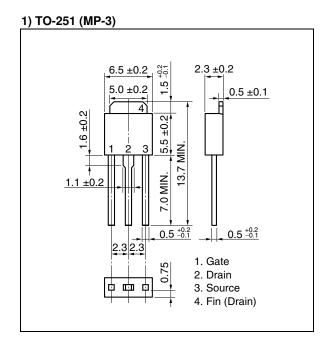


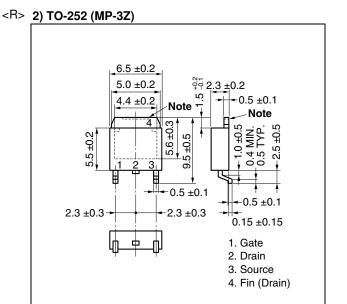






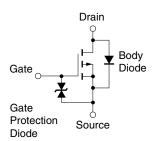
PACKAGE DRAWINGS (Unit: mm)





Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Data Sheet D14646EJ5V0DS 7

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