



### ORDERING INFORMATION

Part Number	Package	Top Marking
MP6905GS*	SOIC-8	See Below

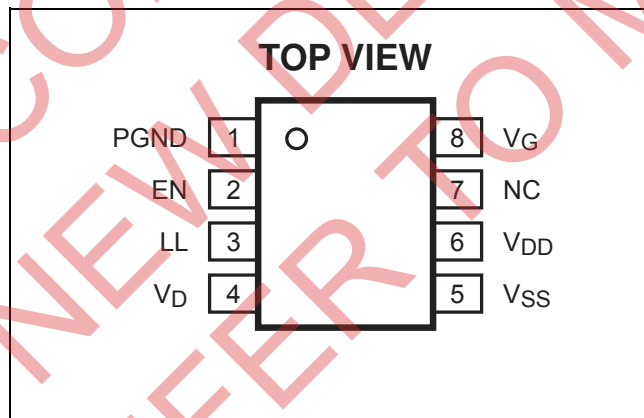
\* For Tape & Reel, RoHS Compliant Packaging, add suffix -Z (e.g. MP6905GS-Z);

### TOP MARKING

\_\_\_\_\_  
**MP6905**  
**LLLLLLLL**  
**MPSYWW**

MP6905: part number;  
 LLLLLLLL: lot number;  
 MPS: MPS prefix;  
 Y: year code;  
 WW: week code:

### PACKAGE REFERENCE



**ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

V <sub>DD</sub> to V <sub>SS</sub> .....	-0.3V to +27V
PGND to V <sub>SS</sub> .....	-0.3V to +0.3V
V <sub>G</sub> to V <sub>SS</sub> .....	-0.3V to V <sub>CC</sub>
V <sub>D</sub> to V <sub>SS</sub> .....	-0.7V to +180V
LL, EN to V <sub>SS</sub> .....	-0.3V to +6.5V
Continuous Power Dissipation (T <sub>A</sub> = +25°C) <sup>(2)</sup>	
SOIC8.....	1.4W
Junction Temperature .....	150°C
Lead Temperature (Solder).....	260°C
Storage Temperature .....	-55°C to +150°C

**Recommended Operation Conditions <sup>(3)</sup>**

V <sub>DD</sub> to V <sub>SS</sub> .....	8V to 24V
Maximum Junction Temp. (T <sub>J</sub> ).....	+125°C

**Thermal Resistance <sup>(4)</sup>**

	<b>θ<sub>JA</sub></b>	<b>θ<sub>JC</sub></b>
SOIC8 .....	90	45 ...°C/W

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub>(MAX)=(T<sub>J</sub>(MAX)-T<sub>A</sub>)/θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

NOT RECOMMENDED FOR NEW DESIGNERS REFER TO MP6906

## ELECTRICAL CHARACTERISTICS

$V_{DD}=12V$ ,  $T_J=-40^{\circ}C\sim 125^{\circ}C$ , Min & Max are guaranteed by characterization, typical is tested under  $25^{\circ}C$ , unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
$V_{DD}$ Voltage Range			8		24	V
$V_{DD}$ UVLO Rising			5.0	6.0	7.0	V
$V_{DD}$ UVLO Hysteresis			0.8	1	1.25	V
Operating Current	$I_{CC}$	$C_{LOAD}=5nF$ , $F_{SW}=100kHz$		8	10	mA
Quiescent Current	$I_q$	$V_{SS}-V_D=0.5V$		2	3.6	mA
Shutdown Current		$V_{DD}=4V$			260	$\mu A$
		$V_{DD}=20V$ , $EN=0V$			500	
Light-Load Mode Current				300	400	$\mu A$
Thermal Shutdown <sup>(5)</sup>				150		$^{\circ}C$
Thermal Shutdown Hysteresis <sup>(5)</sup>				30		$^{\circ}C$
Enable UVLO Rising	$V_{EN-R}$		1.1	1.5	1.9	V
Enable UVLO Hysteresis				0.2	0.4	V
Internal Pull-Up Current On EN				10	15	$\mu A$
<b>CONTROL CIRCUITRY SECTION</b>						
$V_{SS}-V_D$ Forward Voltage	$V_{fwd}$		20	32	44	mV
Turn-On Delay	$T_{Don}$	$C_{LOAD} = 5nF$	$-20^{\circ}C \leq T_J \leq 125^{\circ}C$	150	250	ns
			$-40^{\circ}C \leq T_J < -20^{\circ}C$	250		
	$T_{Don}$	$C_{LOAD} = 10nF$	$-20^{\circ}C \leq T_J \leq 125^{\circ}C$	250	350	ns
			$-40^{\circ}C \leq T_J < -20^{\circ}C$	350		
Input Bias Current On $V_D$		$V_D = 180V$			1	$\mu A$
Minimum On Time	$T_{MIN}$	$C_{LOAD} = 5nF$	0.6	1.2	1.9	$\mu s$
Light-Load-Enter Delay	$T_{LL-Delay}$	$R_{LL}=100k\Omega$	70	100	130	$\mu s$
Light-Load-Enter Pulse Width	$T_{LL}$	$R_{LL}=100k\Omega$	1.2	1.9	2.6	$\mu s$
Light-Load-Enter Pulse Width Hysteresis	$T_{LL-H}$	$R_{LL}=100k\Omega$		0.2		$\mu s$
Light-Load Resistor Value	$R_{LL}$		30		300	$k\Omega$
Light-Load Mode Exit-Pulse Width Threshold ( $V_{DS}$ )	$V_{LL-DS}$		-380	-250	-120	mV
<b>GATE DRIVER SECTION</b>						
$V_G$ (Low)	$V_{G-L}$	$I_{LOAD}=1mA$		0.05	0.1	V
$V_G$ (High)		$V_{DD} > 17V$	13	14.8	16.5	V
		$V_{DD} < 17V$		$V_{DD}-2.2$		
Turn-Off Threshold ( $V_{SS}-V_D$ )	$V_{off}$		-23	-5	13	mV
Turn-Off Propagation Delay		$V_D=V_{SS}$		15		ns
Turn-Off Total Delay	$T_{Doff}$	$V_D=V_{SS}$ , $C_{LOAD}=5nF$ , $R_{GATE}=0\Omega$		35	70	ns
		$V_D=V_{SS}$ , $C_{LOAD}=10nF$ , $R_{GATE}=0\Omega$		45	70	ns
Pull-Down Impedance				1	2	$\Omega$
Pull-Down Current <sup>(5)</sup>		$3V < V_G < 10V$		2		A

**Notes:**

5) Guaranteed by Characterization

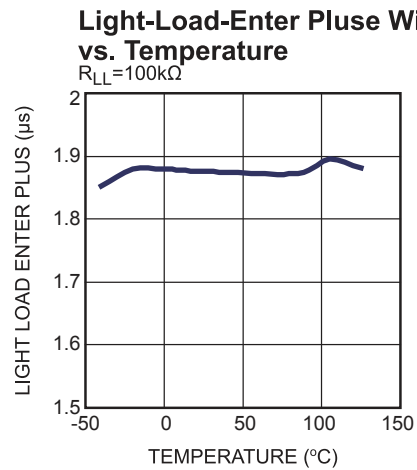
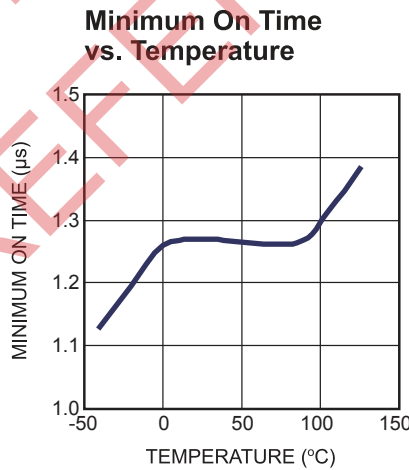
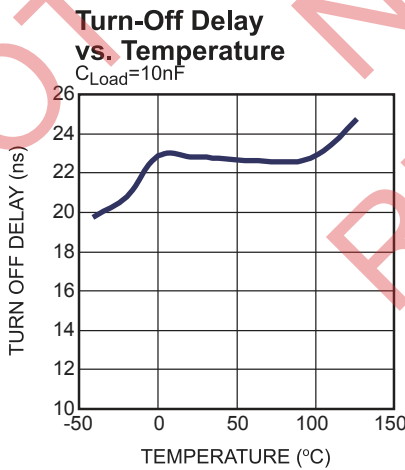
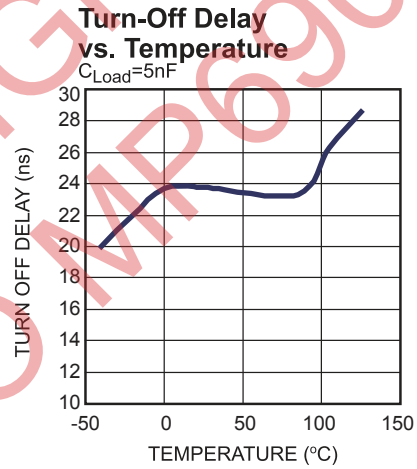
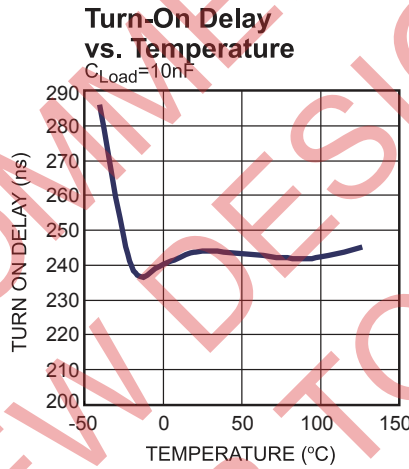
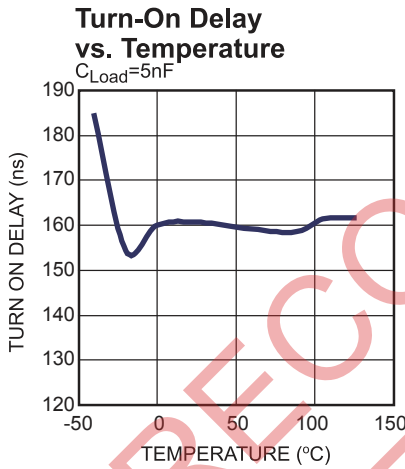
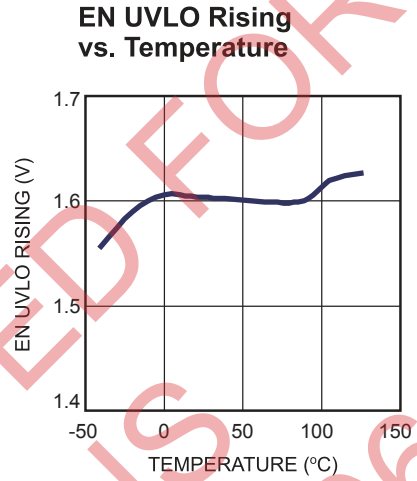
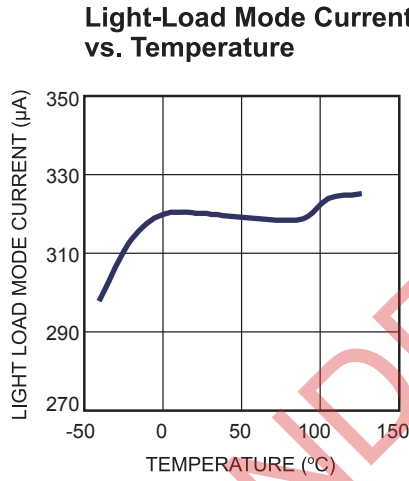
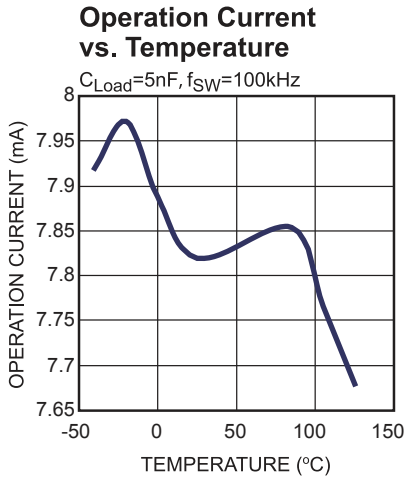
**PIN FUNCTIONS**

Pin #	Name	Description
1	PGND	Power Ground. The return for the driver switch.
2	EN	Enable ( active high)
3	LL	Light-load timing setting. Connect a resistor to set the light-load timing.
4	VD	FET (drain-voltage sense)
5	VSS	Ground, also used as reference for VD.
6	VDD	Supply Voltage
7	NC	No connection
8	VG	Gate drive output

NOT RECOMMENDED FOR  
NEW DESIGNS  
REFER TO MP6906

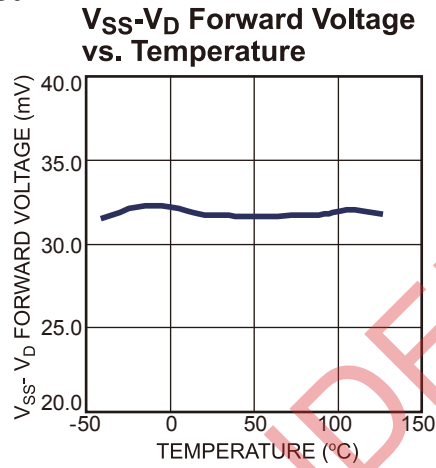
**TYPICAL PERFORMANCE CHARACTERISTICS**

$V_{DD} = 12V$ , unless otherwise noted.



**TYPICAL PERFORMANCE CHARACTERISTICS** *(continued)*

$V_{DD} = 12V$ , unless otherwise noted.



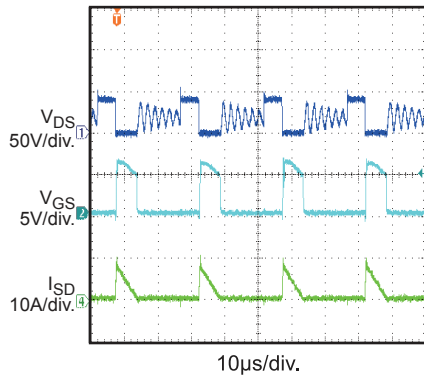
NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP6906

**TYPICAL PERFORMANCE CHARACTERISTICS** (continued)

$V_{DD} = 12V$ , unless otherwise noted.

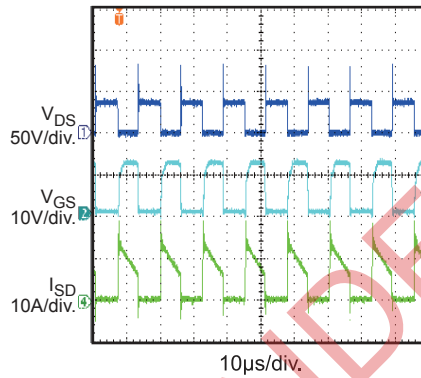
**Operation in 90W Flyback Application<sup>(6)</sup>**

$V_{IN} = 90Vac, I_{OUT} = 1A$



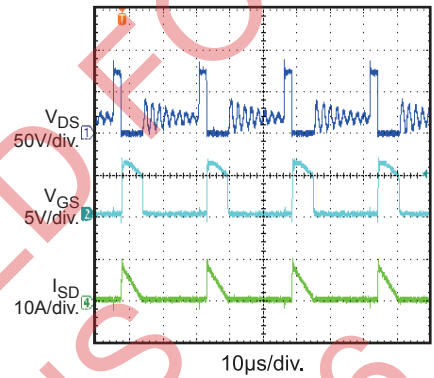
**Operation in 90W Adapter Application**

$V_{IN} = 90Vac, I_{OUT} = 4.7A$



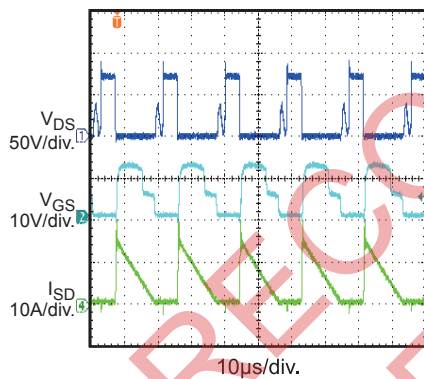
**Operation in 90W Flyback Application**

$V_{IN} = 250Vac, I_{OUT} = 1A$



**Operation in 90W Adapter Application**

$V_{IN} = 250Vac, I_{OUT} = 4.7A$



**Notes:**

6) See Figure 14 for the test circuit



BLOCK DIAGRAM

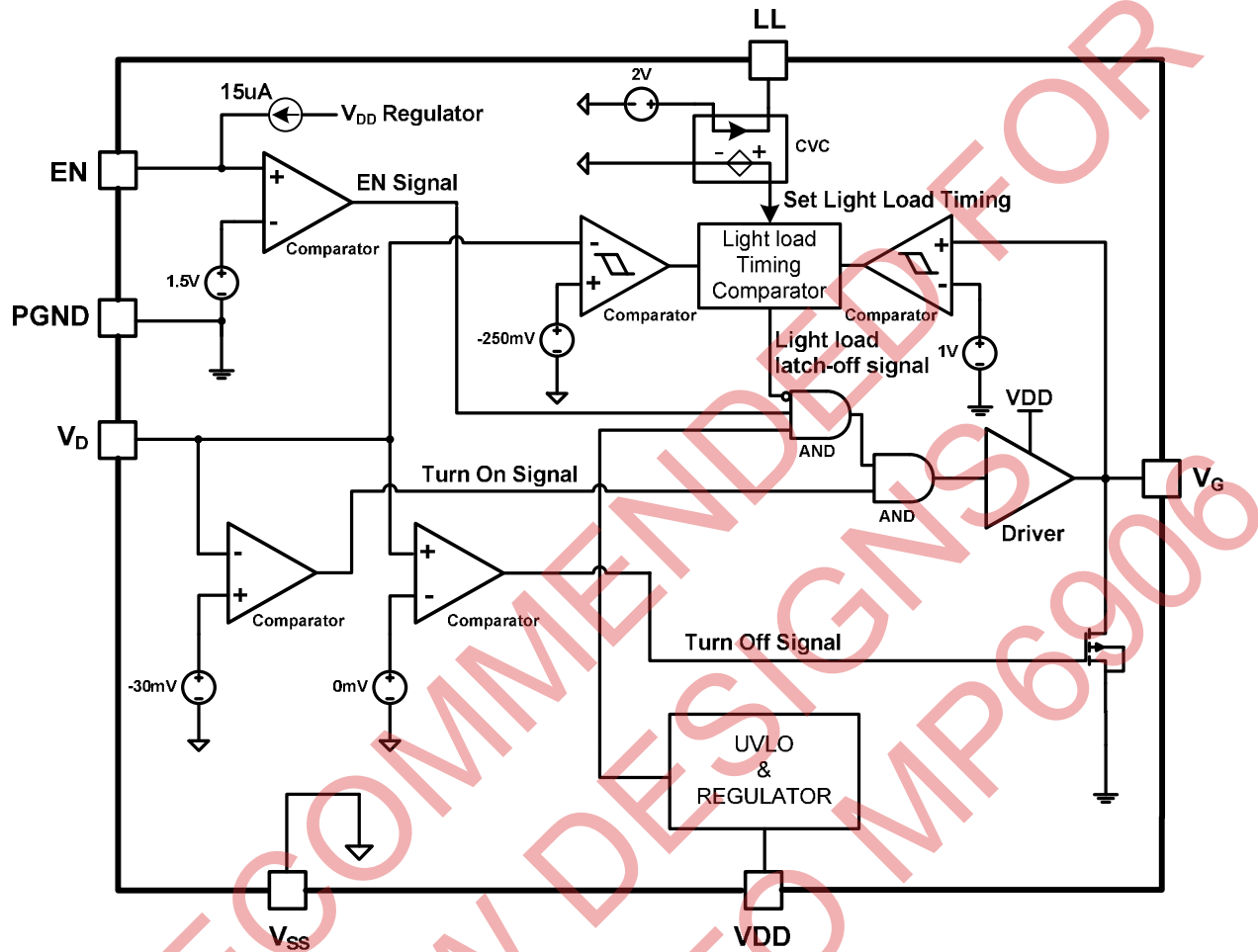


Figure 1: Functional Block Diagram

## OPERATION

The MP6905 operates in CCM, DCM and quasi-resonant flyback converters. The control circuitry controls the gate in forward mode and turns the gate off when the MOSFET current is low.

### Blanking

The control circuitry contains a blanking function. When it pulls the MOSFET on/off, it allows the on/off state to last for an extended period of time. The turn-on blanking time is  $\sim 1.6\mu\text{s}$ , which determines the minimum on time. During the turn-on blanking period, the turn-off threshold is blanked.

### VD Clamp

$V_D$  can reach up to 180V, which requires a high-voltage JFET at the input. To avoid excessive currents if  $V_G$  goes below  $-0.7\text{V}$ , a small resistor is recommended between  $V_D$  and the drain of the external MOSFET.

### Under-Voltage Lockout (UVLO)

If  $V_{DD}$  is below the UVLO threshold, the part enters sleep mode, and  $V_G$  is pulled down by a  $10\text{k}\Omega$  resistor.

### Enable

If EN is pulled low, the part enters shutdown mode, consuming  $<100\mu\text{A}$  shutdown current.

### Thermal Shutdown (TSD)

If the junction temperature of the chip exceeds  $170^\circ\text{C}$ , the  $V_G$  is pulled low and the part stops switching. The part returns to normal functioning after the junction temperature drops to  $120^\circ\text{C}$ .

### Turn-On Phase

When the switch current flows through the body diode of the MOSFET, it carries a negative  $V_{DS}$  ( $V_D - V_{SS}$ ) across ( $<-500\text{mV}$ ). The  $V_{DS}$  is much lower than the turn-on threshold of the control circuitry ( $-30\text{mV}$ ). This turns the MOSFET on after a  $200\text{ns}$  turn-on delay (see Figure 2).

When the turn-on threshold ( $-30\text{mV}$ ) is triggered, a blanking time (minimum on time) is added. This causes the turn-off threshold to be blanked. The blanking time helps avoid an error trigger on the

turn-off threshold caused by turn-on ringing from the synchronous MOSFET.

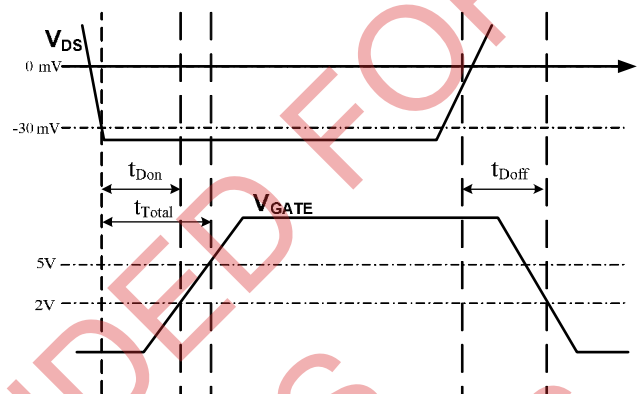


Figure 2: Turn-On and Turn-Off delay

### Conducting Phase

When the synchronous MOSFET is turned on,  $V_{DS}$  rises (according to its on resistance). If  $V_{DS}$  rises above the turn-on threshold ( $-30\text{mV}$ ), the control circuitry stops pulling the gate driver up. This pulls the gate driver down by internal pull-down resistance ( $10\text{k}\Omega$ ) to increase the on resistance, easing the rise of  $V_{DS}$ .  $V_{DS}$  is adjusted to around  $-30\text{mV}$  even if the current through the MOSFET is small. This function lowers the driver voltage when the synchronous MOSFET is turned off to cause a fast turn-off speed (which is active during turn-on blanking time). Even with a small duty, the gate driver can be turned off.

### Turn-off Phase

If  $V_{DS}$  rises and triggers the turn-off threshold ( $0\text{mV}$ ), the gate voltage is pulled low by the control circuitry after about  $20\text{ns}$  turn-off delay (see Figure 2). As with the turn-on phase, a  $200\text{ns}$  blanking time is added when the synchronous MOSFET is turned off to avoid an error trigger.

Figure 3 shows synchronous rectification operation in a heavy-load condition. Due to the high current, the gate driver initially is saturated. After  $V_{DS}$  rises above  $-30\text{mV}$ , the gate driver voltage decreases to adjust the  $V_{DS}$  (typically to  $-30\text{mV}$ ).

Figure 4 shows synchronous rectification operation in a light-load condition. Due to the low current, the gate-driver voltage never saturates but decreases when the synchronous MOSFET turns on, adjusting the  $V_{DS}$ .

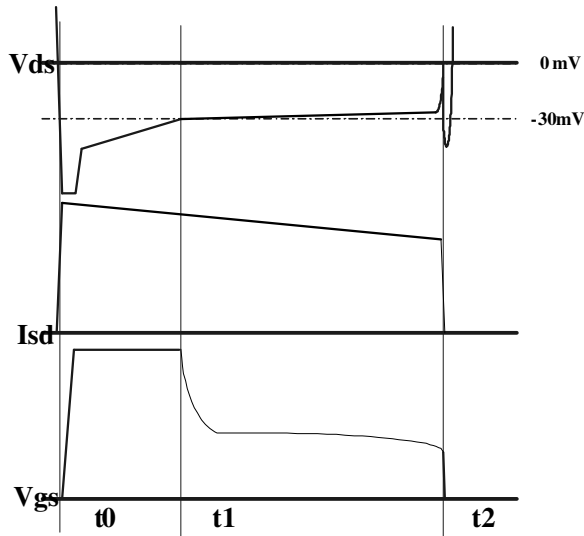


Figure 3: Synchronous Rectification Operation at Heavy Load

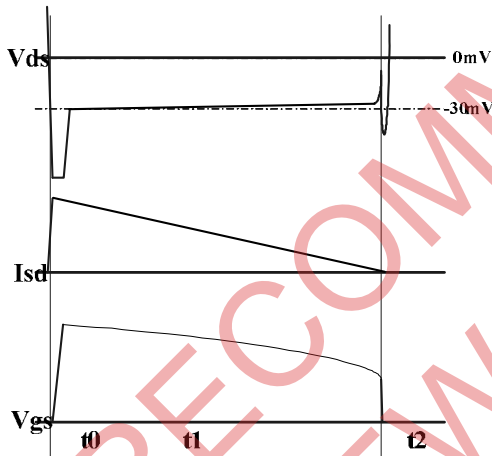


Figure 4: Synchronous Rectification Operation at Light Load

**Light-Load Latch-Off Function**

The MP6905 gate driver is latched. This reduces power loss in light-load conditions to improve efficiency. The light-load-enter pulse width  $T_{LL}$  is set by the resistor connected to LL. When the synchronous MOSFET conducting period is lower than  $T_{LL}$  for longer than the light-load-enter delay ( $T_{LL-Delay}$ ), MP6905 enters light-load mode and latches off the gate driver. The synchronous MOSFET conducting period begins when the gate driver turns on until  $V_{GS}$  drops to the light-load mode, enter-pulse width threshold ( $V_{LL-GS}$ ). During light-load mode, MP6905 monitors the synchronous MOSFET conducting period by sensing  $V_{DS}$  (when  $V_{DS}$  exceeds the light-load

mode exit-pulse width threshold  $V_{LL-DS}$ ). If it is longer than  $T_{LL}+T_{LL-H}$  ( $T_{LL-H}$  is light-load-enter pulse width hysteresis), the light-load mode finishes and the gate driver is unlatched to restart the synchronous rectification.

**SR MOSFET Selection**

To achieve higher efficiency, a MOSFET with a small  $R_{DS(ON)}$  is preferred. Although a  $Q_g$  is larger with a smaller  $R_{DS(ON)}$ , it lowers the turn-on/off speed and leads to greater power loss, including driver power loss. The MP6904 adjusts the  $V_{DS}$  to  $\sim -30mV$  during the driving period when the switching current is low.

A MOSFET with low  $R_{DS(ON)}$  is not recommended as the gate driver is pulled low when  $V_{DS} = -I_{SD} \times R_{DS(ON)}$  exceeds  $-50mV$ . This means the MOSFET's  $R_{DS(ON)}$  doesn't contribute to conduction loss ( $P_{CON} = -V_{DS} \times I_{SD} \approx I_{SD} \times 30mV$ ).

Figure 5 shows the typical waveform of a QR flyback: Assume a 50% duty cycle where  $I_{OUT}$  is the output current.

To efficiently utilize the MOSFET's  $R_{DS(ON)}$ , the MOSFET should be turned on at least 50% of the SR conduction period:

$$V_{ds} = -I_c \times R_{on} = -2 \cdot I_{OUT} \times R_{on} \leq -V_{fwd}$$

Where  $V_{DS}$  is the drain-source voltage, and  $V_{fwd}$  is the forward voltage threshold ( $\sim 30mV$ ).

The MOSFET's  $R_{DS(ON)}$  should be no lower than  $\sim 15/I_{OUT}$  (m $\Omega$ ).

For example, for 5A applications, the MOSFET  $R_{DS(ON)}$  should be no lower than 3m $\Omega$ .

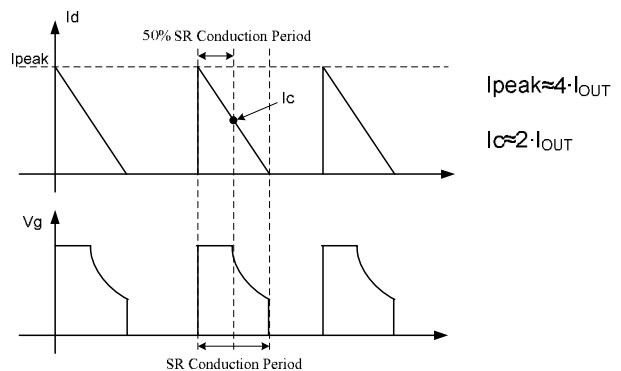
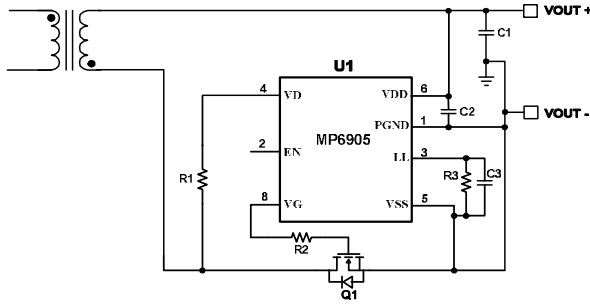
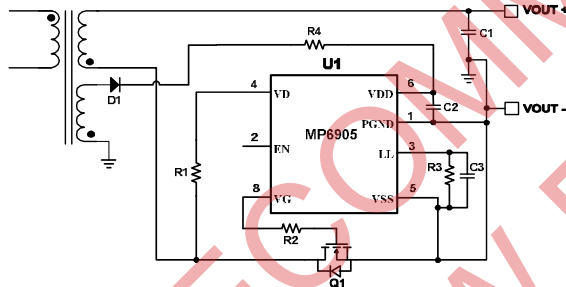
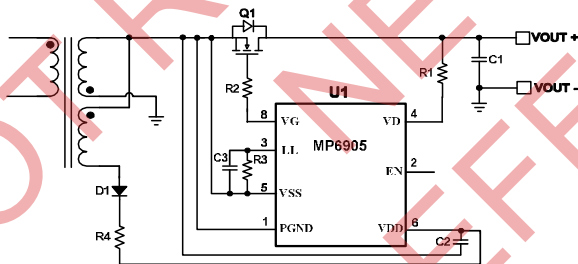


Figure 5: Synchronous Rectification typical Waveforms in QR Flyback

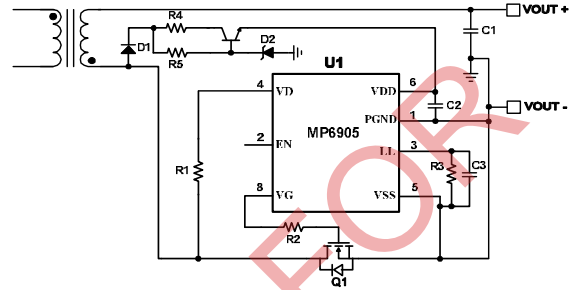
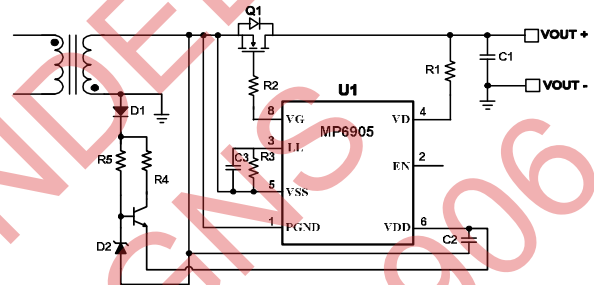
**Typical System Implementations**

**Figure 6: IC Supply derived directly from Output Voltage**

Typical system implementation for the IC supply (derived from output voltage) is available in low-side rectification (see Figure 6). The output voltage should be in the  $V_{DD}$  range of 8V to 24V.

If output voltage is out of the  $V_{DD}$  range (or high-side rectification is used), use an auxiliary winding from the power transformer for the IC supply ( see Figures 7 and 8).


**Figure 7: IC Supply Derived from Auxiliary Winding in Low-Side Rectification**

**Figure 8: IC Supply Derived from Auxiliary Winding in High-Side Rectification**

An additional non-auxiliary winding solution for the IC supply uses an external LDO circuit from the secondary transformer winding (see Figures 9 and 10). However, slightly higher power loss will occur, which dissipates on the LDO circuit, particularly when secondary-winding voltage is high.


**Figure 9: IC Supply Derived from Secondary Winding through External LDO in Low-Side Rectification**

**Figure 10: IC Supply Derived from Secondary Winding through External LDO in High-Side Rectification**

LAYOUT GUIDELINES

Sensing for  $V_D/V_{SS}$

The sensing connection ( $V_D/V_{SS}$ ) should be closed off to the MOSFET (drain/source). Make the sensing loop as small as possible and place the VD resistor close to the VD. Keep the IC out of the power loop to make sure the sensing loop and power loop won't interrupt each other (see Figure 11).

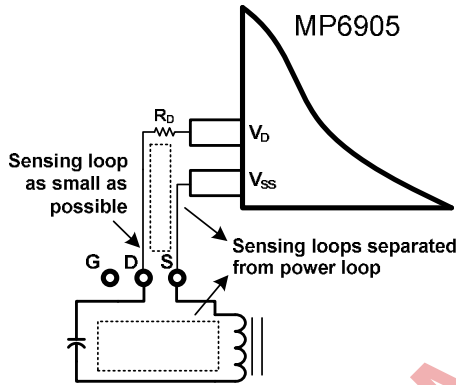


Figure 11: Voltage Sensing for  $V_D/V_{SS}$  on MP6905

Sensing for  $V_D/V_{SS}$

A decoupling ceramic capacitor (no smaller than 1uF) from  $V_{DD}$  to PGND should be close to the IC for adequate filtering.

Gate-Driver Loop

To minimize the parasitic inductance, the gate-driver loop should be as small as possible. Keep the driver signal far away from the VD sensing trace on the layout.

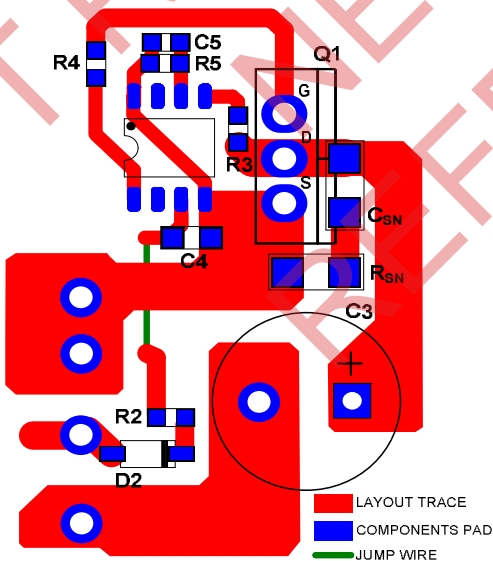


Figure 12: TO220 Package SR FET

Figure 12 shows a layout example of a single layer with a through-hole transformer and TO220 package SR FET (see the application circuit on page 1).  $R_{SN}$  and  $C_{SN}$  provide the RC snubber network for the SR FET.

The sensing loop ( $V_D/V_{SS}$  to the SR FET) is minimized and separates from the power loop. The  $V_{DD}$  decoupling capacitor ( $C4$ ) is placed beside the  $V_{DD}$ .

Figure 13 shows a layout example of a single layer with a PowerPAK/SO8 package SR FET, which also has a minimized sensing loop and power loop that won't interrupt each other.

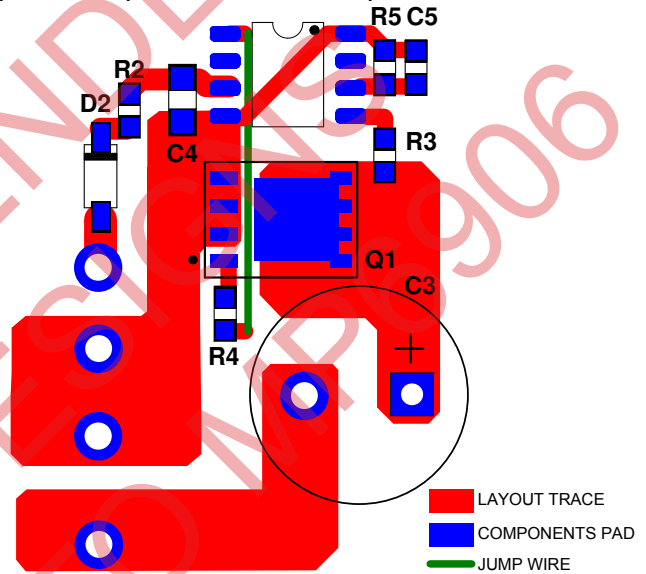


Figure 13: PowerPAK/SO8 Package SR FET

TYPICAL APPLICATION CIRCUIT

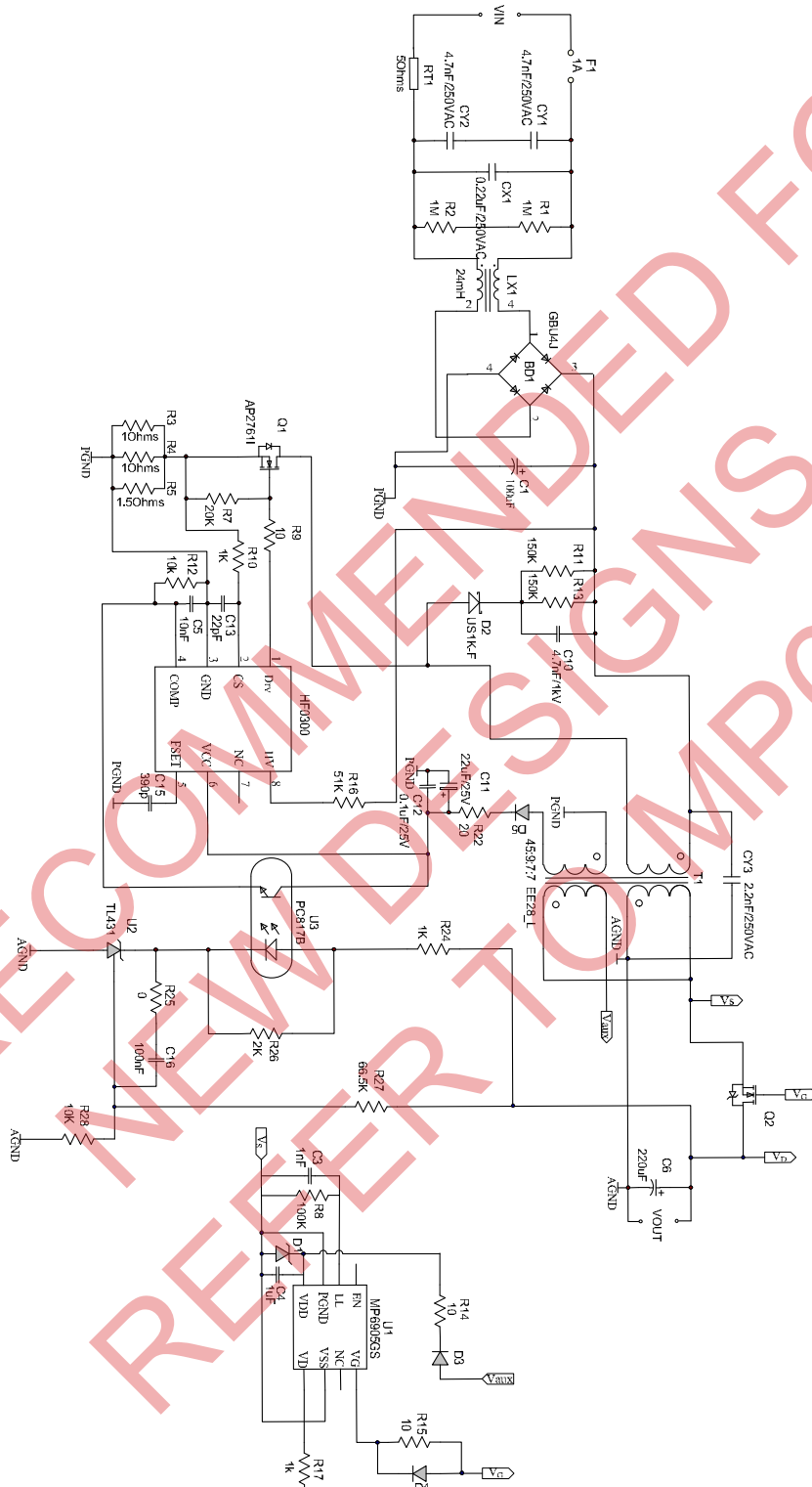
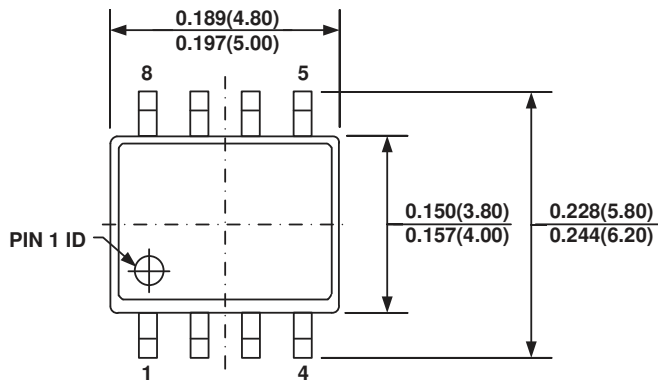
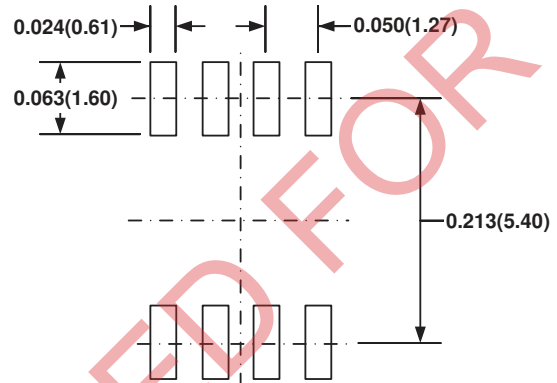


Figure 14:MP6905 for Secondary Synchronous Controller in 90W Flyback Application

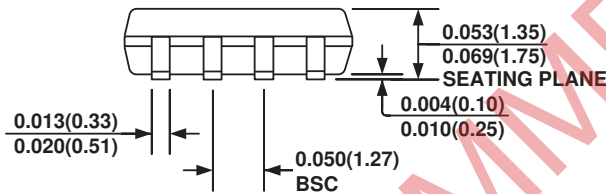
SOIC8



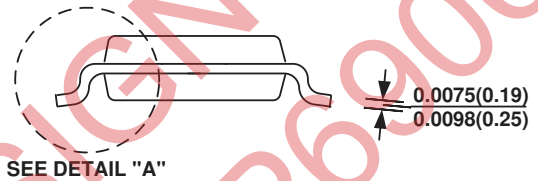
TOP VIEW



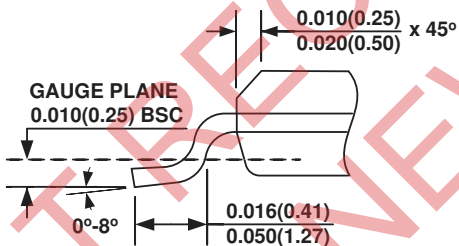
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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