

# Three Phase Inverter Automotive Power MOSFET Module

## NXV08V110DB1

### Features

- Three-Phase Inverter Bridge for Variable Speed Motor Drive
- RC Snubber for Low EMI
- Current Sensing and Temperature Sensing
- Electrically Isolated DBC Substrate for Low Thermal Resistance
- Compact Design for Low Total Module Resistance
- Module Serialization for Full Traceability
- AEC Qualified – AQC324
- PPAP Capable
- This Device is Pb-free, RoHS and UL94-V0 Compliant

### Applications

- 24 V and 48 V Motor Control
- DC-DC Converter

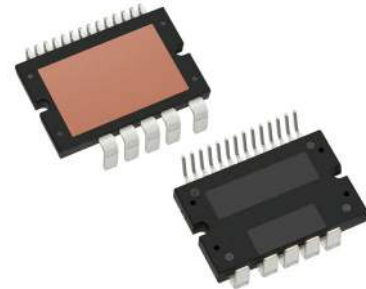
### Benefits

- Enable Design of Small, Efficient and Reliable System for Reduced Vehicle Fuel Consumption and CO<sub>2</sub> Emission
- Simplified Vehicle Assembly
- Enable Low Thermal Resistance to Junction-to-Heat Sink by Direct Mounting via Thermal Interface Material between Module Case and Heat Sink



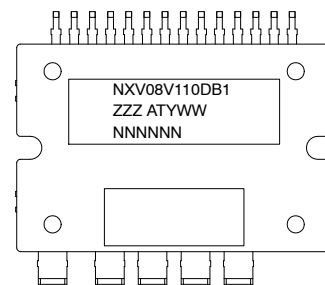
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CASE MODCD

### MARKING DIAGRAM



NXV08V110DB1 = Specific Device Code  
ZZZ = Lot ID  
AT = Assembly & Test Location  
Y = Year  
WW = Work Week  
NNN = Serial Number

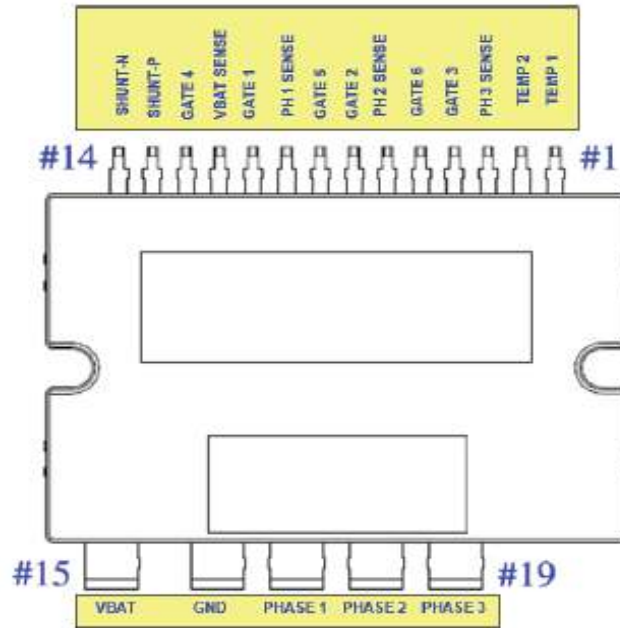
### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# NXV08V110DB1

## PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Package	Pb-Free and RoHS Compliant	Operating Temperature Range	Packing Method
NXV08V110DB1	APM19-CBC	yes	-40 ~ 125°C	Tube



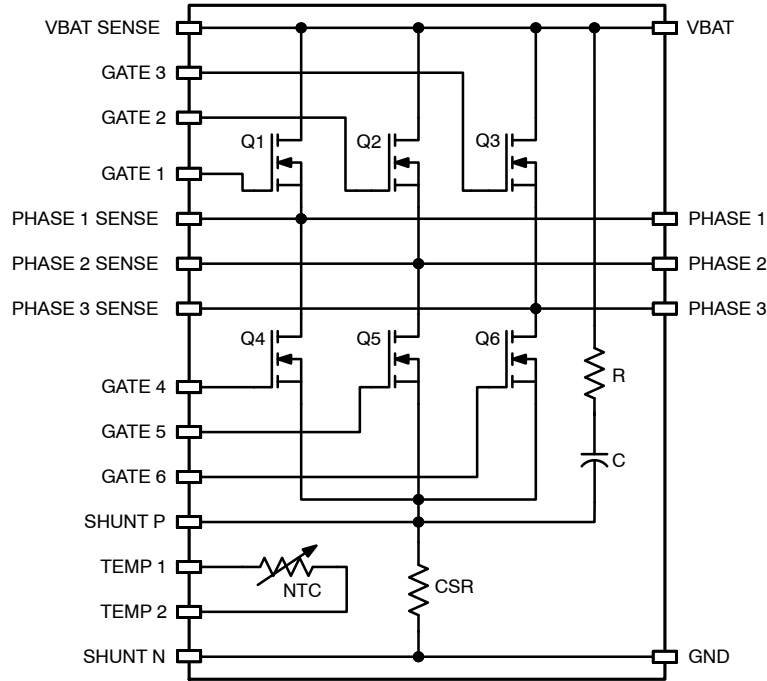
**Figure 1. Pin Configuration**

## PIN DESCRIPTION

Pin Number	Pin Name	Pin Description
1	TEMP 1	NTC Thermistor Terminal 1
2	TEMP 2	NTC Thermistor Terminal 2
3	PHASE 3 SENSE	Source of Q3 and Drain of Q6
4	GATE 3	Gate of Q3, high side Phase 3 MOSFET
5	GATE 6	Gate of Q6, low side Phase 3 MOSFET
6	PHASE 2 SENSE	Source of Q2 and Drain of Q5
7	GATE 2	Gate of Q2, high side Phase 2 MOSFET
8	GATE 5	Gate of Q5, low side Phase 2 MOSFET
9	PHASE 1 SENSE	Source of Q1 and Drain of Q4
10	GATE 1	Gate of Q2, high side Phase 1 MOSFET
11	VBAT SENSE	Sense pin for battery voltage and Drain of high side MOSFETs
12	GATE 4	Gate of Q4, low side Phase 1 MOSFET
13	SHUNT P	Positive CSR sense pin and source connection for low side MOSFETs
14	SHUNT N	Negative CSR sense pin and sense pin for battery return
15	VBAT	Battery voltage power lead
16	GND	Battery return power lead
17	PHASE 1	Phase 1 power lead
18	PHASE 2	Phase 2 power lead
19	PHASE 3	Phase 3 power lead

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## Schematic Diagram



**Figure 2. Schematic**

### Flammability Information

All materials present in the power module meet UL flammability rating class 94V-0.

### Compliance to RoHS Directives

The power module is 100% lead free and RoHS compliant 2000/53/C directive.

### Solder

Solder used is a lead free SnAgCu alloy.

Base of the leads, at the interface with the package body should not be exposed to more than 200°C during mounting on the PCB, this to prevent the remelt of the solder joints.

### ABSOLUTE MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Max.	Unit
VDS(Q1-Q6)	Drain to Source Voltage	80	V
VGS(Q1-Q6)	Gate to Source Voltage	$\pm 20$	V
EAS(Q1-Q6)	Single Pulse Avalanche Energy (Note 2)	324	mJ
$T_J$	Maximum Junction Temperature	175	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	125	$^\circ\text{C}$
$T_{lead}$	Temperature at the base of the leads at the interface with the package body during PCB mounting	200	$^\circ\text{C}$
$V_{ISO}$	Isolation Voltage (60Hz, Sinusoidal, AC 1minute, Connection Pins to heat sink plate)	2500	Vrms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Defined by design, not subject to production testing.

2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.08\text{ mH}$ ,  $I_{AS} = 90\text{ A}$ ,  $V_{DD} = 80\text{ V}$  during inductor charging and  $V_{DD} = 0\text{ V}$  during time in avalanche.

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## Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 3)	-	-	0.9	K/W

3. Test method compliant with MIL-STD-883-1012.1, case temperature measured below the package at the chip center. Cosmetic oxidation and discolor on the DBC surface is allowed.

## Module Specific Characteristics

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	BVDSS	80			V
Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	$V_{GS(th)}$	2		4	V
Gate-to-Source Leakage Current	$V_{GS} = \pm 20 V, V_{DS} = 0 V$	$I_{GSS}$	-100		+100	nA
Drain-to-Source Leakage Current	$V_{DS} = 80 V, V_{GS} = 0 V$	$I_{DSS}$			2	$\mu A$
Source-to-Drain Diode Voltage	$I_S = 80 A, V_{GS} = 0 V$	VSD			1.25	V
Q1 Inverter High Side MOSFETs (See Note 4)	$I_D = 80 A, V_{GS} = 10 V$ (Note 4)	RDS(ON)Q1		1.3	1.7	m $\Omega$
Q2 Inverter High Side MOSFETs (See Note 4)		RDS(ON)Q2		1.4	1.8	m $\Omega$
Q3 Inverter High Side MOSFETs (See Note 4)		RDS(ON)Q3		1.5	1.9	m $\Omega$
Q4 Inverter Low Side MOSFETs (See Note 4)		RDS(ON)Q4		1.6	1.9	m $\Omega$
Q5 Inverter Low Side MOSFETs (See Note 4)		RDS(ON)Q5		1.7	2.1	m $\Omega$
Q6 Inverter Low Side MOSFETs (See Note 4)		RDS(ON)Q6		2.0	2.4	m $\Omega$
VBAT to PHASE 1	$I_D = 80 A, V_{GS} = 10 V$	RDS(ON)MQ1		2.2	2.6	m $\Omega$
VBAT to PHASE 2		RDS(ON)MQ2		2.3	2.6	m $\Omega$
VBAT to PHASE 3		RDS(ON)MQ3		2.4	2.6	m $\Omega$
PHASE1 to GND		RDS(ON)MQ4		2.4	3.0	m $\Omega$
PHASE2 to GND		RDS(ON)MQ5		2.6	3.0	m $\Omega$
PHASE3 to GND		RDS(ON)MQ6		2.9	3.2	m $\Omega$
Total loop resistance B+ $\geq$ Phase $\geq$ GND	$V_{GS} = 10 V, I_D = 80 A$			4.9	7.3	m $\Omega$

4. All MOSFETs have same size and on resistance. However, the different values listed due to the different access points available inside the module for on resistance measurement. Q1 has the shortest measurement path in the layout, in this reason, on resistance of Q1 can be used for simple power loss calculation.

## Components

Symbol	Spec	Quantity	Size
RESISTOR	1.0 $\Omega$	1	142 $\times$ 55 mil
CAPACITOR	100 V, 0.022 $\mu F$	1	79 $\times$ 49 mil
CURRENT SENSING RESISTOR	0.5 m $\Omega$	1	250 $\times$ 120 mil
NTC	NCP18XH103F0SRB, 10 k $\Omega$	1	63 $\times$ 32 mil

## Electrical Characteristics

( $T_J = 25^\circ C$  unless otherwise noted, Reference typical characteristics of FDBL86363-F085, TOLL)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz$	-	10000	-	pF
$C_{oss}$	Output Capacitance		-	1540	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	70	-	pF
$R_g$	Gate Resistance	$f = 1 MHz$	-	2.8	-	$\Omega$
$Q_{g(ToT)}$	Total Gate Charge at 10 V	$V_{GS} = 0$ to 10 V	-	130	169	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2 V	-	18	27	nC
$Q_{gs}$	Gate-to-Source Gate Charge	$V_{DD} = 40 V, I_D = 80 A$	-	47	-	nC
$Q_{gd}$	Gate-to-Drain "Miller" Charge		-	24	-	nC

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## ELECTRICAL CHARACTERISTICS (continued)

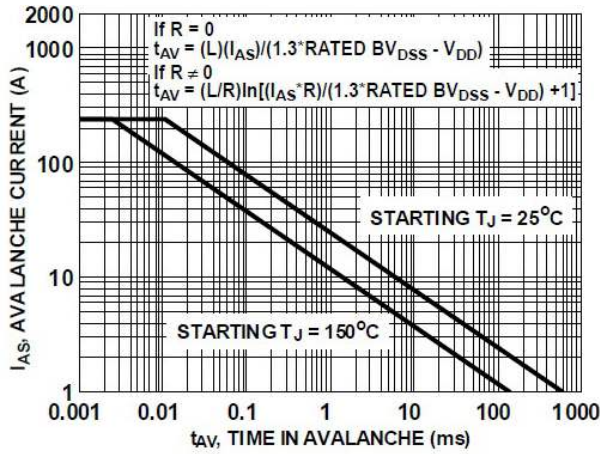
( $T_J = 25^\circ\text{C}$  unless otherwise noted, Reference typical characteristics of FDBL86363–F085, TOLL)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>SWITCHING CHARACTERISTICS</b>						
$t_{on}$	Turn-On Time	$V_{DD} = 40\text{ V}, I_D = 80\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$	–	–	133	ns
$t_{d(on)}$	Turn-On Delay		–	39	–	ns
$t_r$	Rise Time		–	63	–	ns
$t_{d(off)}$	Turn-Off Delay		–	61	–	ns
$t_f$	Fall Time		–	33	–	ns
$t_{off}$	Turn-Off Time		–	–	140	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

(Graphs are generated using the die assembled in discrete package for reference purposes only. Datasheet of FDBL86363-F085 is available in the web)



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515.

Figure 3. Unclamped Inductive Switching Capability

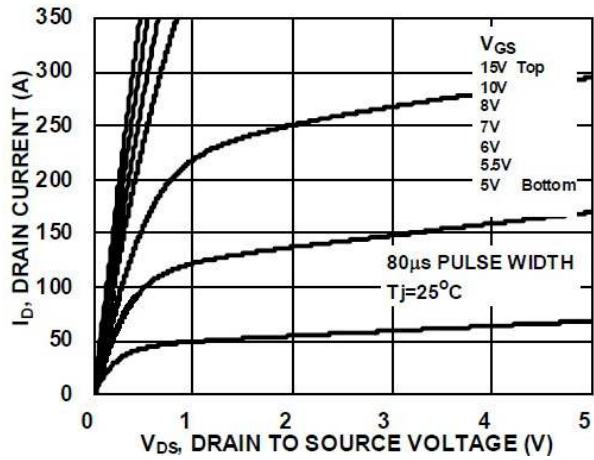


Figure 4. Saturation Characteristics

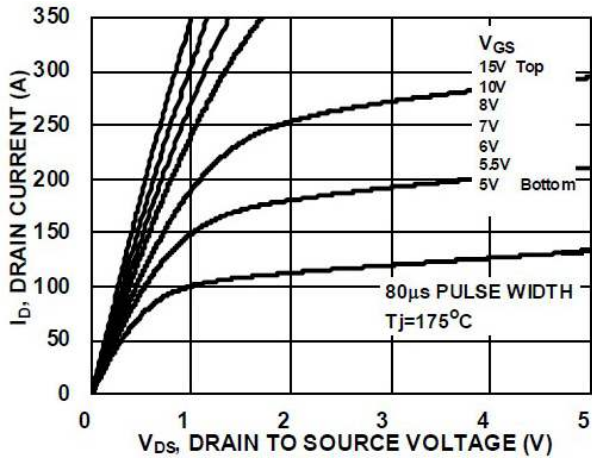


Figure 5. Saturation Characteristics

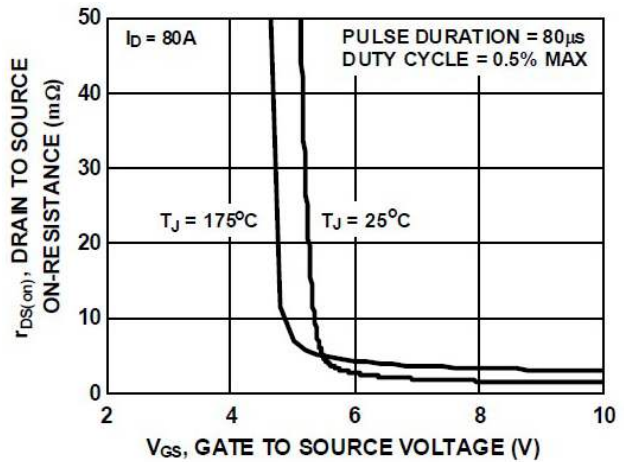


Figure 6.  $R_{DS(on)}$  vs. Gate Voltage

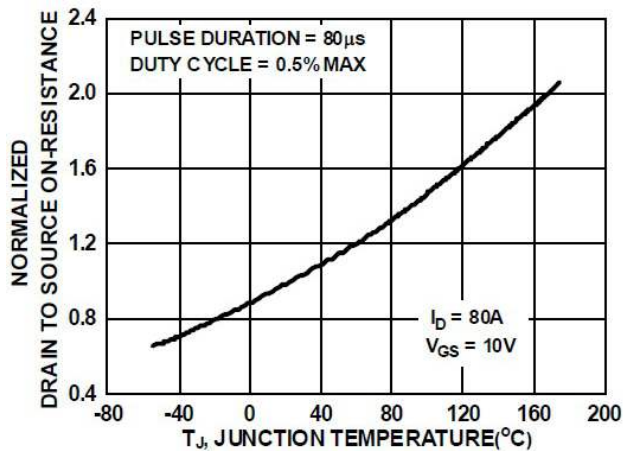


Figure 7. Normalized  $R_{DS(on)}$  vs. Junction Temperature

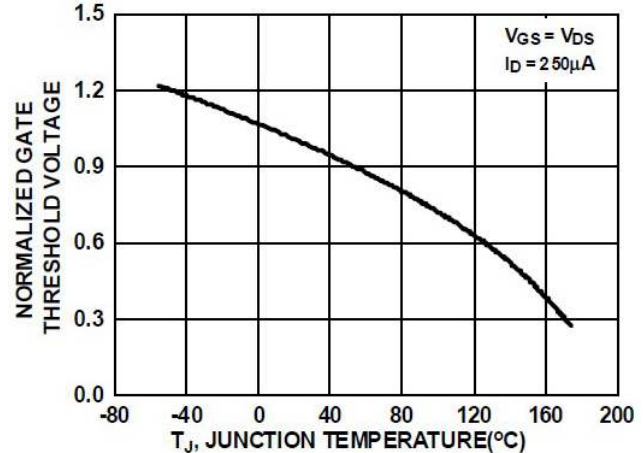


Figure 8. Normalized Gate Threshold Voltage vs. Temperature

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## TYPICAL CHARACTERISTICS (continued)

(Graphs are generated using the die assembled in discrete package for reference purposes only. Datasheet of FDBL86363-F085 is available in the web)

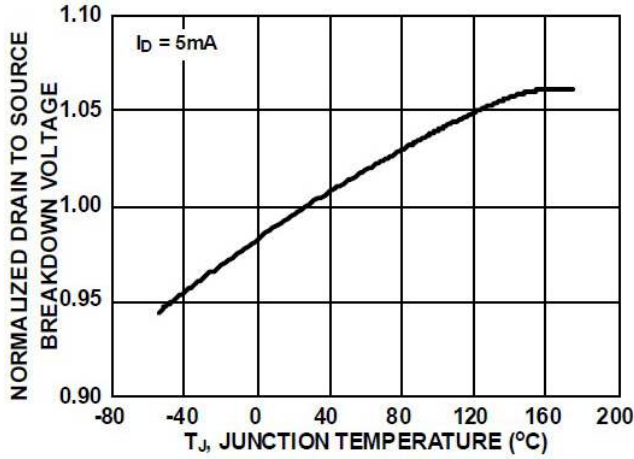


Figure 9. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

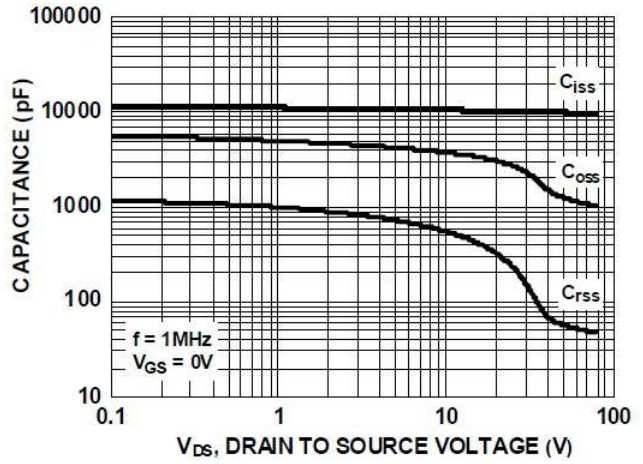


Figure 10. Capacitance vs. Drain to Source Voltage

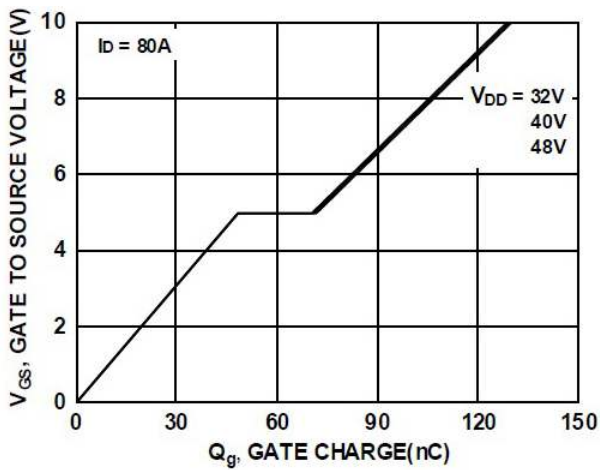
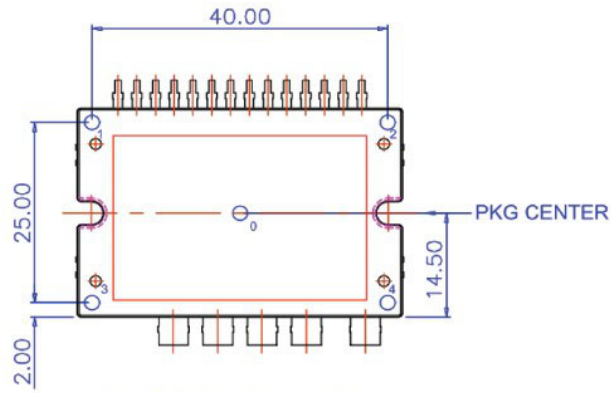


Figure 11. Gate Charge vs. Gate to Source Voltage

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FLATNESS: MAX. 150um

-. MEASURING AT INDICATING POINTS  
1, 2, 3, AND 4 (BASED ON "0")

**Figure 12. Flatness Measurement Position**

## MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Device Flatness	Refer to the package dimensions	0	-	150	um
Mounting Torque	Mounting screw: M3, recommended 0.7 N•m	0.4	-	0.8	N•m
Weight		-	20	-	g



# MECHANICAL CASE OUTLINE

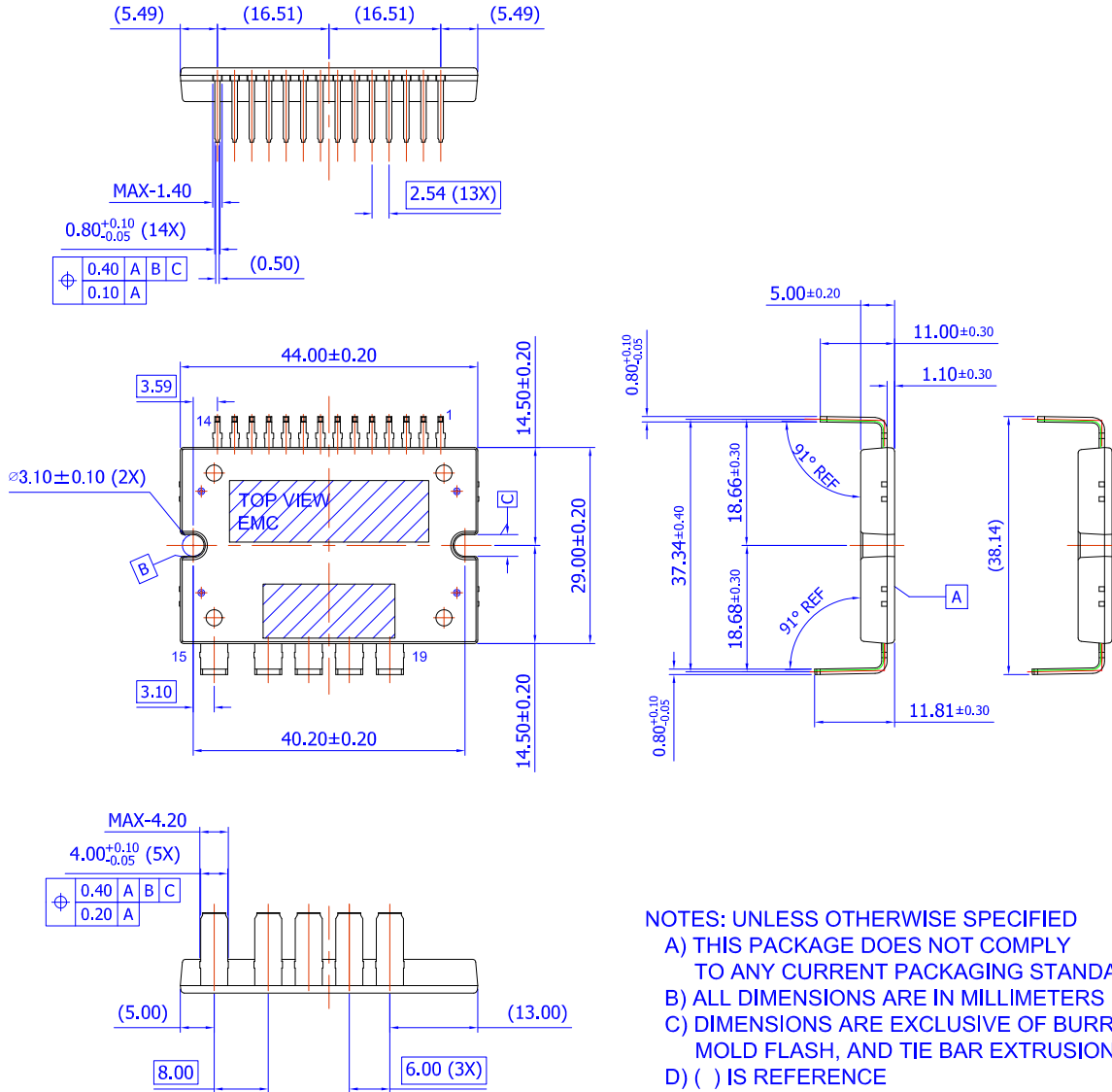
## PACKAGE DIMENSIONS

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### 19LD, APM, PDD STD (APM19-CBC) CASE MODCD ISSUE 0

DATE 30 NOV 2016



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