# NST3906DXV6T1, NST3906DXV6T5

# Dual General Purpose Transistor

The NST3906DXV6T1 device is a spin- off of our popular SOT-23/SOT-323 three-leaded device. It is designed for general purpose amplifier applications and is housed in the SOT- 563 six-leaded surface mount package. By putting two discrete devices in one package, this device is ideal for low-power surface mount applications where board space is at a premium.

- $h_{FE}$, 100-300
- Low $V_{CE(sat)}$, ≤ 0.4 V
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Lead-Free Solder Plating

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector- Emitter Voltage | $V_{CEO}$ | -40 | Vdc |
| Collector- Base Voltage | $V_{CBO}$ | -40 | Vdc |
| Emitter- Base Voltage | $V_{EBO}$ | -5.0 | Vdc |
| Collector Current - Continuous | $I_C$ | -200 | mAdc |
| Electrostatic Discharge | ESD | HBM>16000, MM>2000 | V |

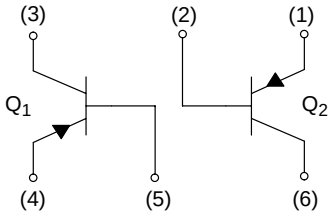
**THERMAL CHARACTERISTICS**

| Characteristic (One Junction Heated) | Symbol | Max | Unit |
|---|---|---|---|
| Total Device Dissipation $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 357 (Note 1)<br>2.9 (Note 1) | mW<br>mW/°C |
| Thermal Resistance Junction-to-Ambient | $R_{\theta JA}$ | 350 (Note 1) | °C/W |
| **Characteristic (Both Junctions Heated)** | **Symbol** | **Max** | **Unit** |
| Total Device Dissipation $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 500 (Note 1)<br>4.0 (Note 1) | mW<br>mW/°C |
| Thermal Resistance Junction-to-Ambient | $R_{\theta JA}$ | 250 (Note 1) | °C/W |
| Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | - 55 to +150 | °C |

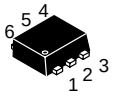
1. FR-4 @ Minimum Pad

ON Semiconductor®

http://onsemi.com




NST3906DXV6T1




**SOT-563**
**CASE 463A**
**PLASTIC**

**MARKING DIAGRAM**


A2 = Specific Device Code
D = Date Code

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NST3906DXV6T1 | SOT-563 | 4 mm pitch 4000/Tape & Reel |
| NST3906DXV6T5 | SOT-563 | 2 mm pitch 8000/Tape & Reel |

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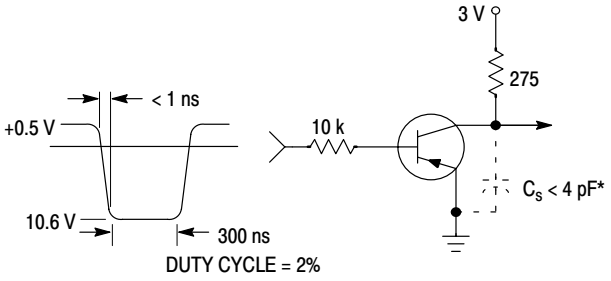
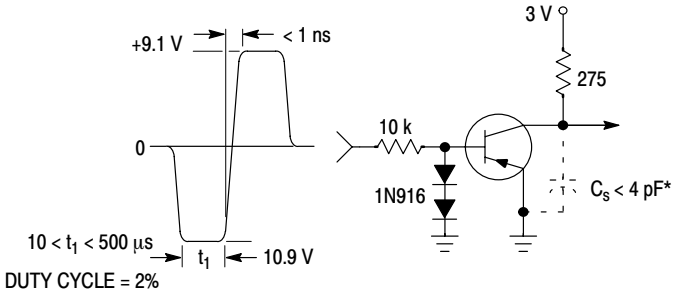
**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | |
| Collector - Emitter Breakdown Voltage (Note 2) | $V_{(BR)CEO}$ | -40 | - | Vdc |
| Collector - Base Breakdown Voltage | $V_{(BR)CBO}$ | -40 | - | Vdc |
| Emitter - Base Breakdown Voltage | $V_{(BR)EBO}$ | -5.0 | - | Vdc |
| Base Cutoff Current | $I_{BL}$ | - | -50 | nAdc |
| Collector Cutoff Current | $I_{CEX}$ | - | -50 | nAdc |
| **ON CHARACTERISTICS** (Note 2) | | | | |
| DC Current Gain<br>($I_C$ = -0.1 mAdc, $V_{CE}$ = -1.0 Vdc)<br>($I_C$ = -1.0 mAdc, $V_{CE}$ = -1.0 Vdc)<br>($I_C$ = -10 mAdc, $V_{CE}$ = -1.0 Vdc)<br>($I_C$ = -50 mAdc, $V_{CE}$ = -1.0 Vdc)<br>($I_C$ = -100 mAdc, $V_{CE}$ = -1.0 Vdc) | $h_{FE}$ | <br>60<br>80<br>100<br>60<br>30 | <br>-<br>-<br>300<br>-<br>- | - |
| Collector - Emitter Saturation Voltage<br>($I_C$ = -10 mAdc, $I_B$ = -1.0 mAdc)<br>($I_C$ = -50 mAdc, $I_B$ = -5.0 mAdc) | $V_{CE(sat)}$ | <br>-<br>- | <br>-0.25<br>-0.4 | Vdc |
| Base - Emitter Saturation Voltage<br>($I_C$ = -10 mAdc, $I_B$ = -1.0 mAdc)<br>($I_C$ = -50 mAdc, $I_B$ = -5.0 mAdc) | $V_{BE(sat)}$ | <br>-0.65<br>- | <br>-0.85<br>-0.95 | Vdc |
| **SMALL- SIGNAL CHARACTERISTICS** | | | | |
| Current - Gain - Bandwidth Product | $f_T$ | 250 | - | MHz |
| Output Capacitance | $C_{obo}$ | - | 4.5 | pF |
| Input Capacitance | $C_{ibo}$ | - | 10.0 | pF |
| Input Impedance<br>($V_{CE}$ = -10 Vdc, $I_C$ = -1.0 mAdc, f = 1.0 kHz) | $h_{ie}$ | 2.0 | 12 | k Ω |
| Voltage Feedback Ratio<br>($V_{CE}$ = -10 Vdc, $I_C$ = -1.0 mAdc, f = 1.0 kHz) | $h_{re}$ | 0.1 | 10 | X $10^{-4}$ |
| Small - Signal Current Gain<br>($V_{CE}$ = -10 Vdc, $I_C$ = -1.0 mAdc, f = 1.0 kHz) | $h_{fe}$ | 100 | 400 | - |
| Output Admittance<br>($V_{CE}$ = -10 Vdc, $I_C$ = -1.0 mAdc, f = 1.0 kHz) | $h_{oe}$ | 3.0 | 60 | μmhos |
| Noise Figure<br>($V_{CE}$ = -5.0 Vdc, $I_C$ = -100 μAdc, $R_S$ = 1.0 k Ω, f = 1.0 kHz) | NF | - | 4.0 | dB |
| **SWITCHING CHARACTERISTICS** | | | | |
| Delay Time | ($V_{CC}$ = -3.0 Vdc, $V_{BE}$ = 0.5 Vdc) | $t_d$ | - | 35 | ns |
| Rise Time | ($I_C$ = -10 mAdc, $I_{B1}$ = -1.0 mAdc) | $t_r$ | - | 35 | |
| Storage Time | ($V_{CC}$ = -3.0 Vdc, $I_C$ = -10 mAdc) | $t_s$ | - | 225 | ns |
| Fall Time | ($I_{B1}$ = $I_{B2}$ = -1.0 mAdc) | $t_f$ | - | 75 | |

2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.




* Total shunt capacitance of test jig and connectors

**Figure 1. Delay and Rise Time Equivalent Test Circuit**

**Figure 2. Storage and Fall Time Equivalent Test Circuit**

## TYPICAL TRANSIENT CHARACTERISTICS

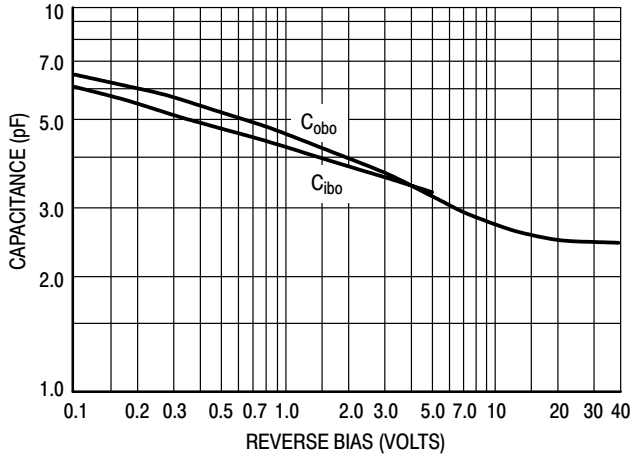



**Figure 3. Capacitance**

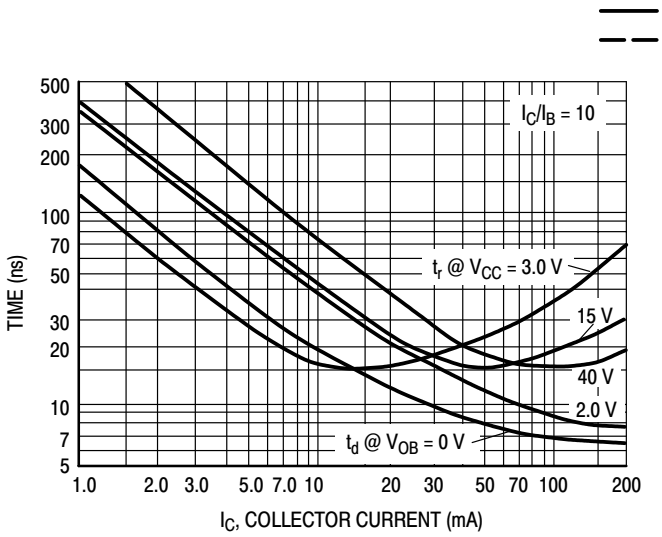



**Figure 4. Turn - On Time**

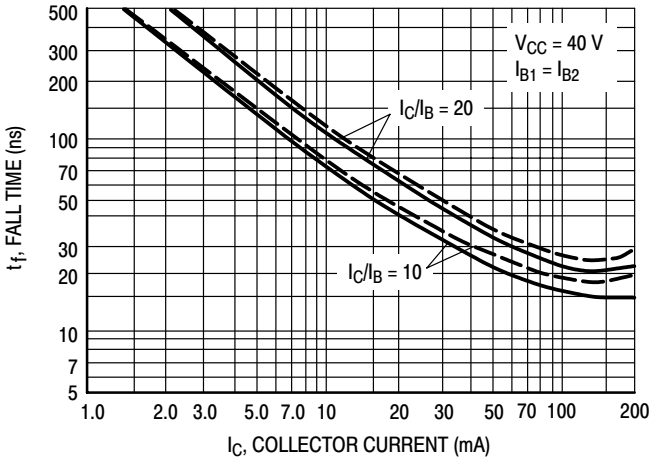



**Figure 5. Fall Time**

## TYPICAL AUDIO SMALL-SIGNAL CHARACTERISTICS
## NOISE FIGURE VARIATIONS

($V_{CE}$ = -5.0 Vdc, $T_A$ = 25°C, Bandwidth = 1.0 Hz)

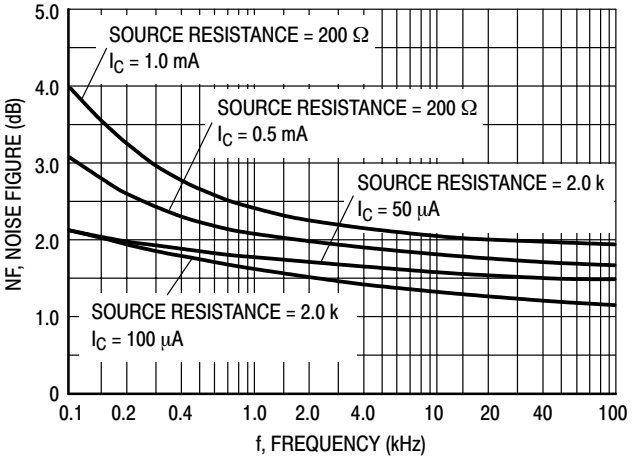



**Figure 6.**

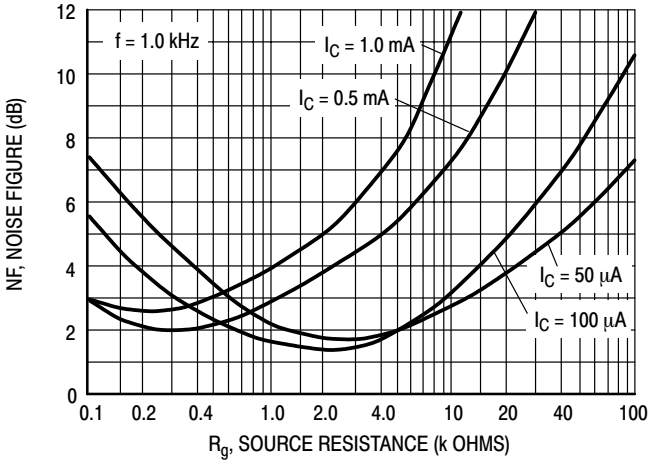



**Figure 7.**

## h PARAMETERS

($V_{CE}$ = -10 Vdc, f = 1.0 kHz, $T_A$ = 25°C)

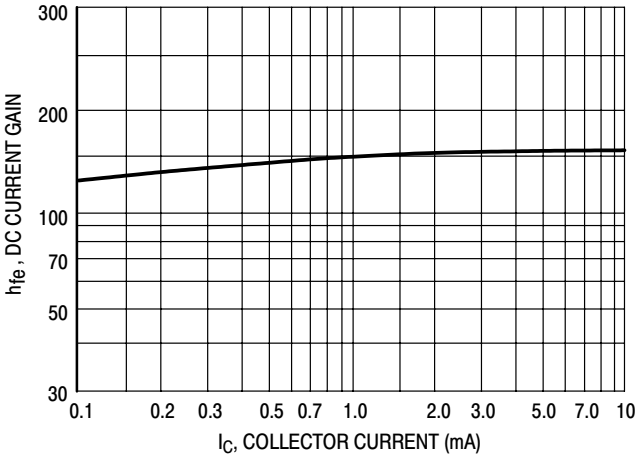



**Figure 8. Current Gain**

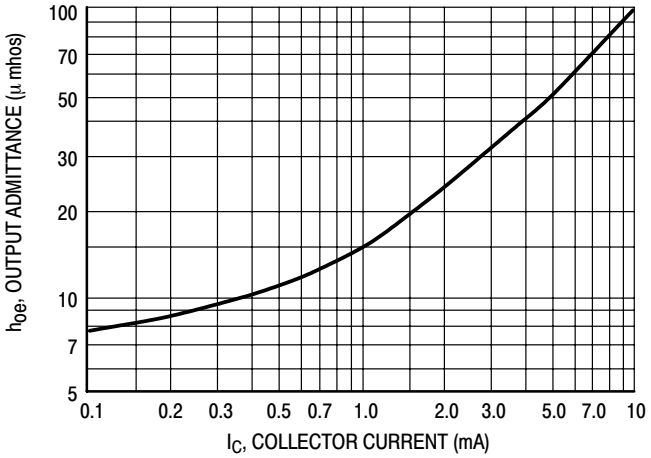



**Figure 9. Output Admittance**

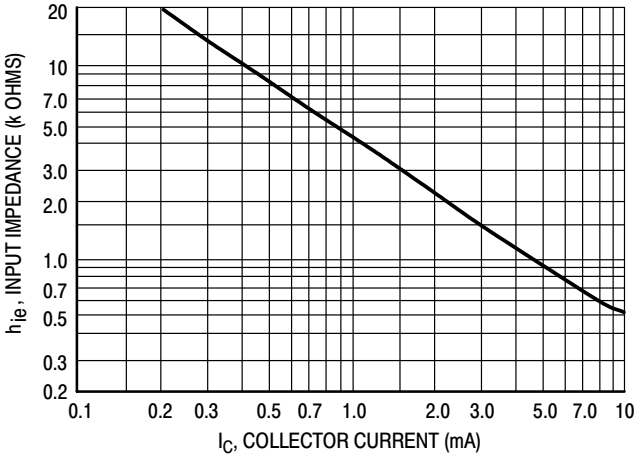



**Figure 10. Input Impedance**

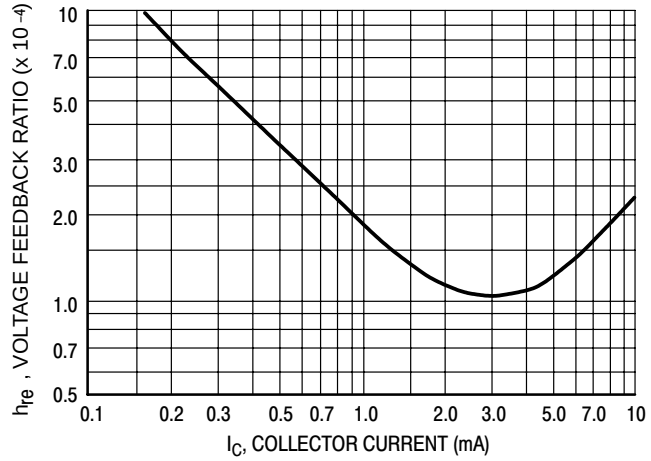



**Figure 11. Voltage Feedback Ratio**

## TYPICAL STATIC CHARACTERISTICS

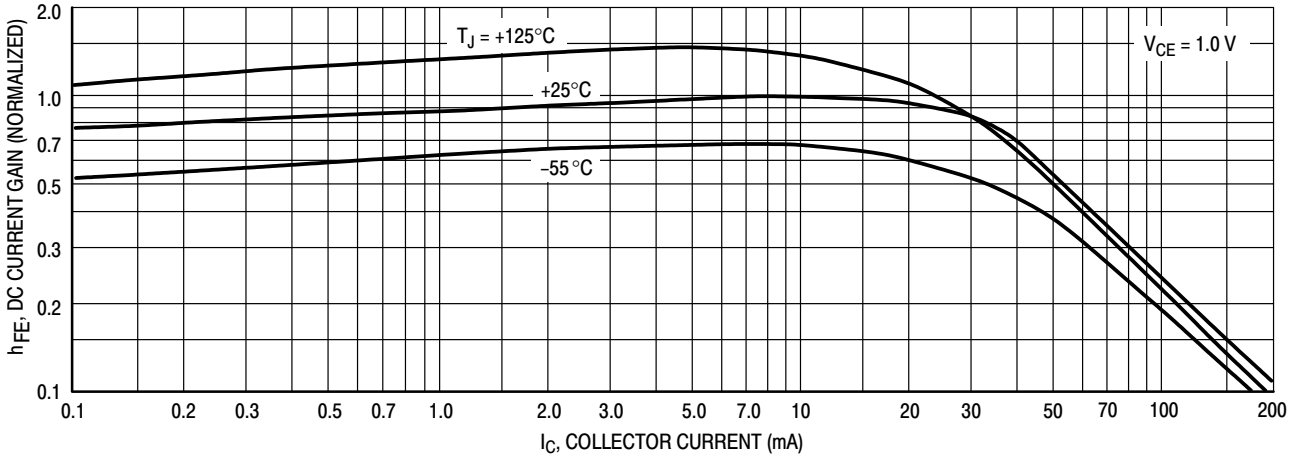



**Figure 12. DC Current Gain**

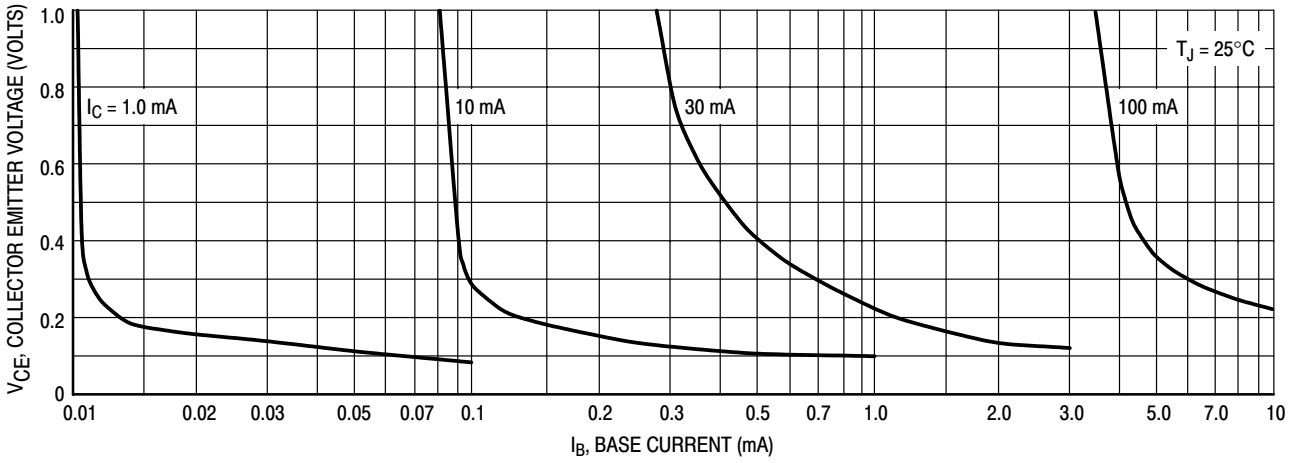



**Figure 13. Collector Saturation Region**

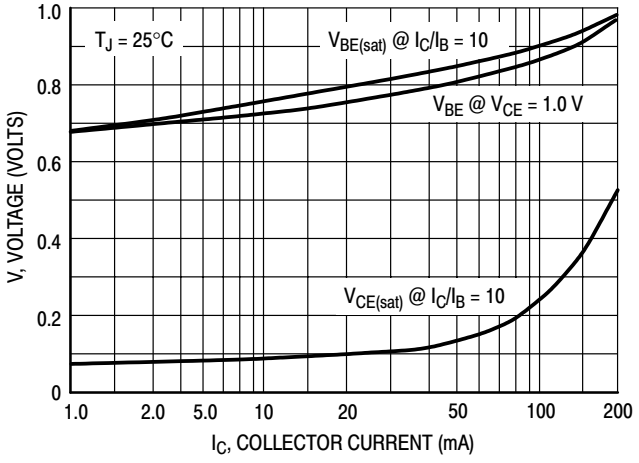



**Figure 14. “ON” Voltages**

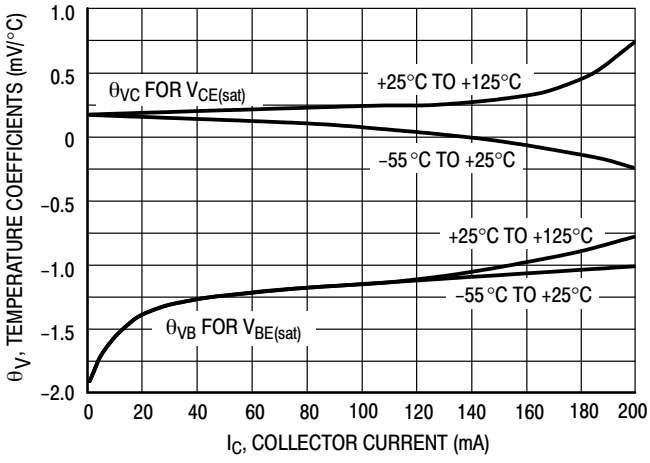
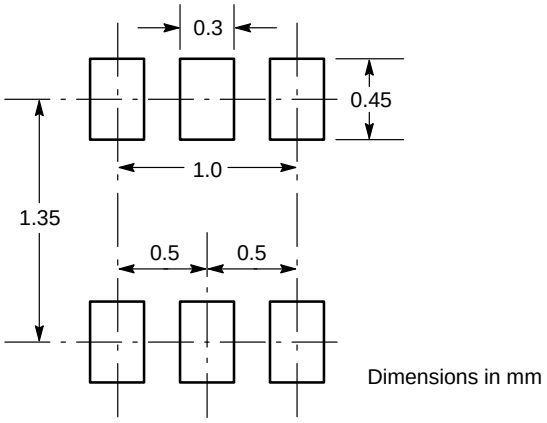



**Figure 15. Temperature Coefficients**

# INFORMATION FOR USING THE SOT-563 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




**SOT-563**

## SOT-563 POWER DISSIPATION

The power dissipation of the SOT-563 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT-563 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150°C - 25°C}{833°C/W} = 150 \text{ milliwatts}$$

The 833°C/W for the SOT-563 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-563 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

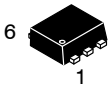
Thermal Clad is a registered trademark of the Bergquist Company.

### SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

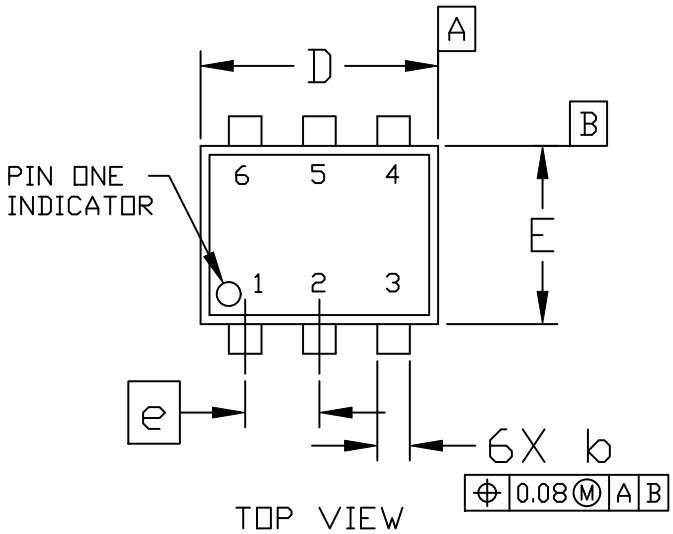



**SCALE 4:1**

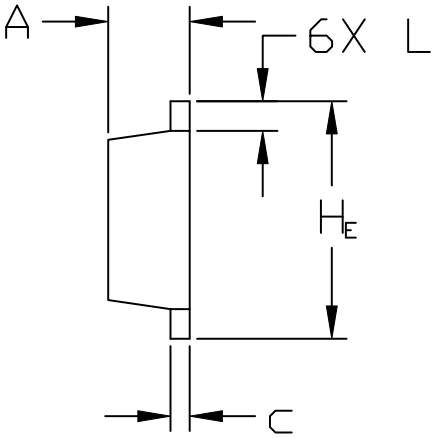
**SOT−563, 6 LEAD**
CASE 463A
ISSUE H

DATE 26 JAN 2021

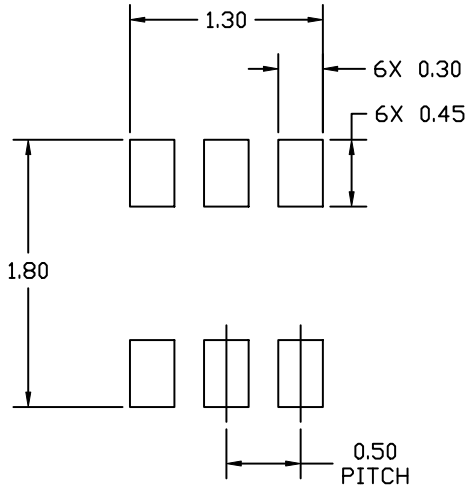
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.




TOP VIEW




SIDE VIEW




RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.50 | 0.55 | 0.60 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.08 | 0.13 | 0.18 |
| D | 1.50 | 1.60 | 1.70 |
| E | 1.10 | 1.20 | 1.30 |
| e | 0.50 BSC | | |
| L | 0.10 | 0.20 | 0.30 |
| $H_E$ | 1.50 | 1.60 | 1.70 |



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**SOT−563, 6 LEAD**
CASE 463A
ISSUE H

DATE 26 JAN 2021

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

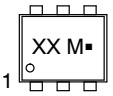
STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

**GENERIC**
**MARKING DIAGRAM***




XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|---|---|---|---|
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| **DESCRIPTION:** | **SOT−563, 6 LEAD** | | **PAGE 2 OF 2** |

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